

Towards a High-Precision 4D Tracking System at IHEP

Qi Yan（严琪）

Institute of High Energy Physics, Chinese Academy of Sciences

On behalf of PAIRS Collaboration

The 3rd International Workshop on Physics at High Baryon Density, Dalian, Nov 9, 2026

PAIRS COLLABORATION

Precision and Advanced semiconductor detectors with Integrated high-performance Readout and Systems

Zhengze Chang, Jiaolong Chen, Siyu Chen, Yuxin Cui, Mingzheng Ding, Jie Du, Chengdong Fu, Chenxi Fu, Yongshuai Ge, Dizhou Guo, Kun Hu, Yuqiang Hu, Wentao Jia, Hui Jiang, Xiaoping Jing, Dazhang Li, Gang Li, Xiaoting Li, Ziyao Li, Baiqi Liu, Boxuan Liu, Lei Liu, Zeyu Liu, Shoudong Luo, Cai Meng, Xiaohui Qian, Rui Qu, Haoyu Shi, Xin Shi, Xueyan Shi, Jiajian Teoh, Chuanye Wang, Congcong Wang, Kaining Wang, Wenjing Wang, Yiwei Wang, Zhenyu Wu, Gaobo Xu, Xiongbo Yan, Junling Yang, Jingbo Ye, Yunkai Yue, Xiyuan Zhang, Yihan Zhang, Zhentao Zhang, Zhihang Zhang, Mei Zhao, Xuhang Zhao, Zhanhong Zhao, Jiaqi Zhou, Junjian Zhou, Ningchuang Zhou, **Qi Yan***

(PAIRS Collaboration)

Institute of High Energy Physics, Chinese Academy of Sciences*

Institute of Microelectronics, Chinese Academy of Sciences

Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences

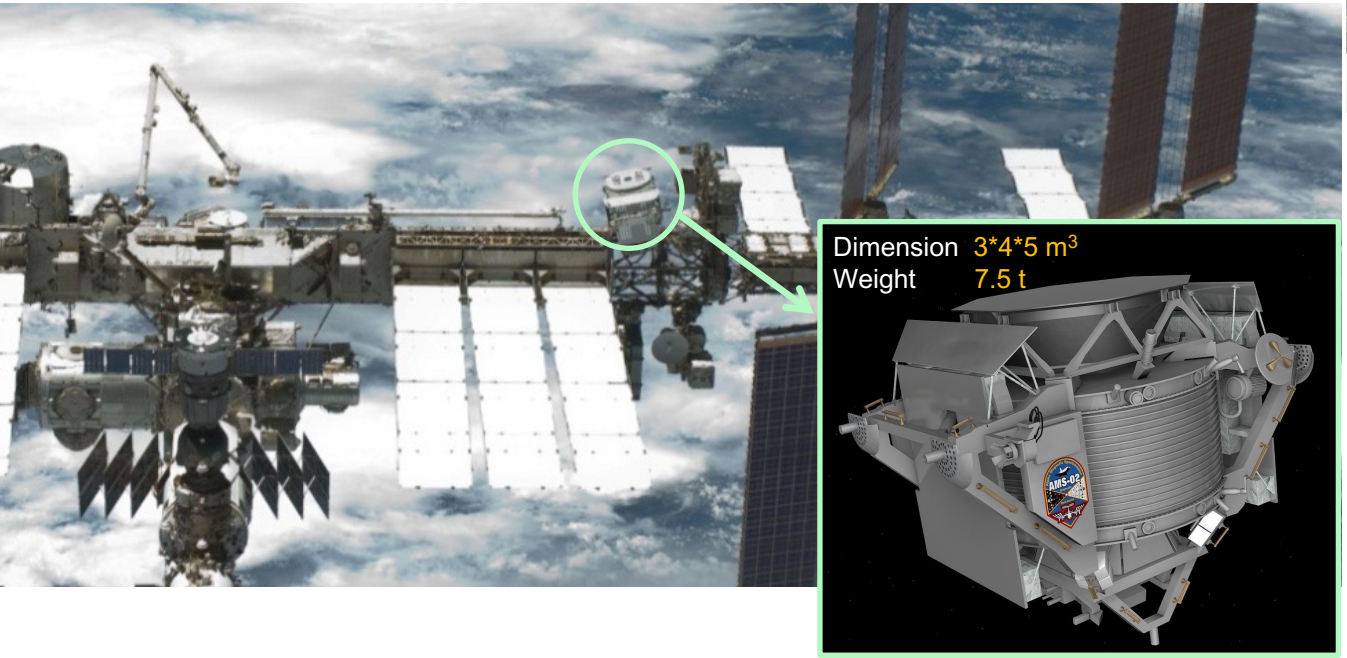
Technical Institute of Physics and Chemistry, Chinese Academy of Sciences

Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences

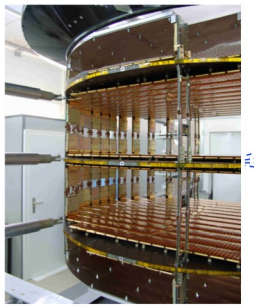
Shandong University

Personal Background

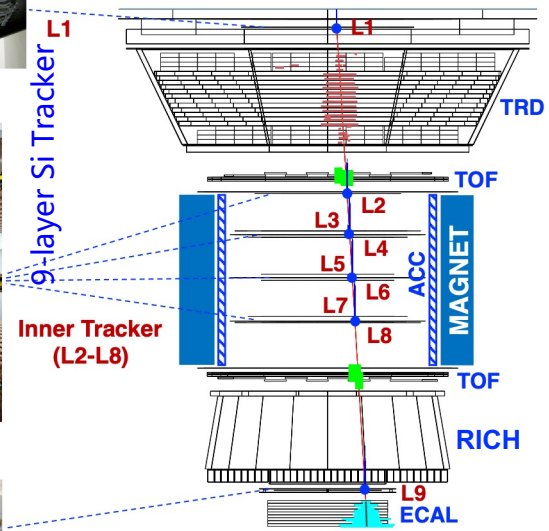
Joined IHEP in April 2024 after ten years of work at MIT. Previously focused on the Alpha Magnetic Spectrometer (AMS) experiment aboard the International Space Station, including the development of key technologies for its Silicon Tracker. Now leads silicon tracker R&D, driven by the CEPC detector program.

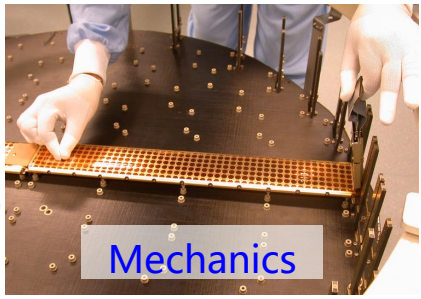






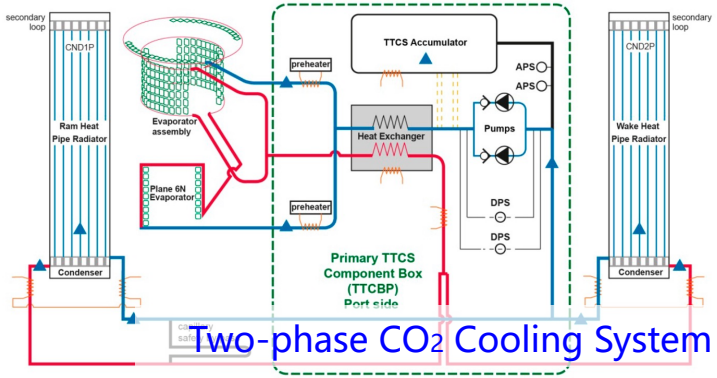








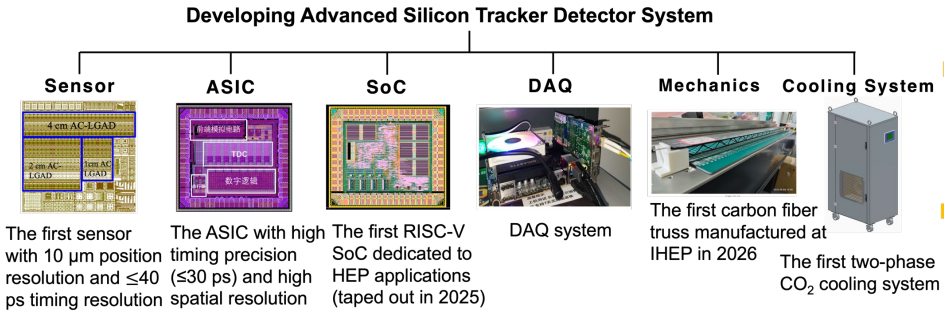
The Alpha Magnetic Spectrometer (AMS) is a unique precision magnetic particle spectrometer in space, comparable to most sophisticated detectors at ground-based accelerators. AMS measures charged cosmic-ray particles and antiparticles to study dark matter, antimatter and the origin of cosmic rays, and searches for other new physics.



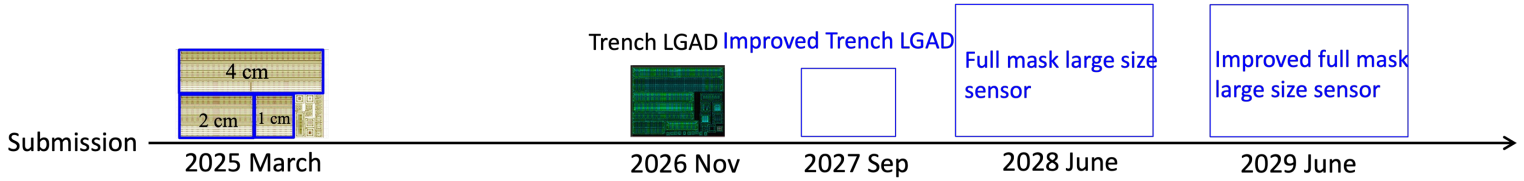
Advanced Semiconductor Detector R&D

Semiconductor Detector R&D

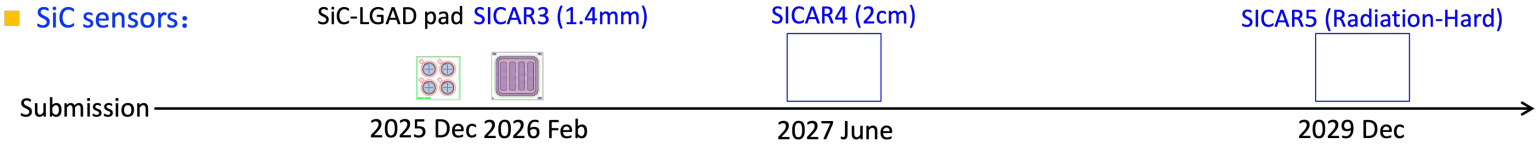
- Our group's core members are from the CEPC Silicon Tracker team (~40 people)
- Develop semiconductor detectors with picosecond timing and micrometer position resolution (4D) for next-generation particle spectrometers. Establish a complete technology chain for high-performance tracking detectors, spanning novel sensors, dedicated readout electronics, system integration and engineering demonstrators.



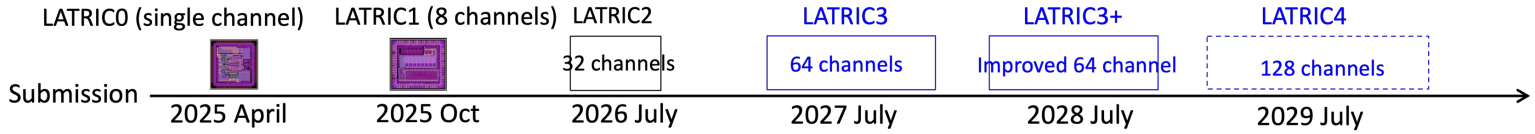
- LGAD sensors are evolving toward improved process, larger size, higher performance, and lower power consumption:



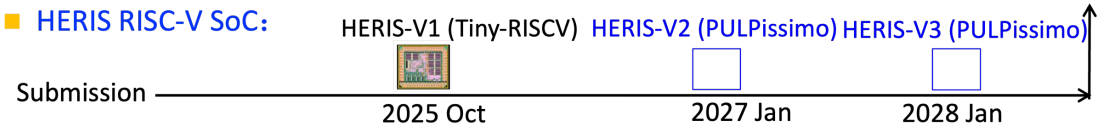
- SiC sensors:



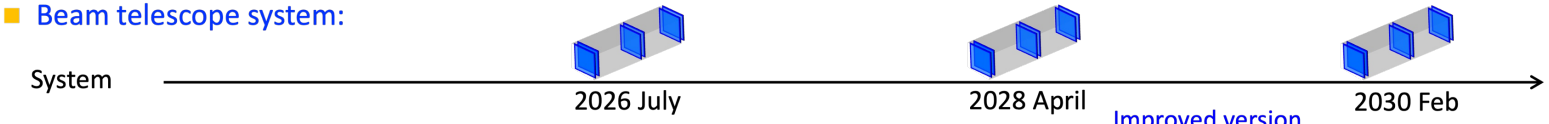
- LGAD readout ASIC, LATRIC, is being developed towards multi-channels:



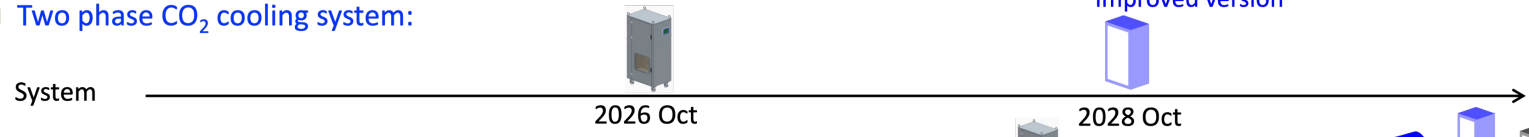
- HERIS RISC-V SoC:



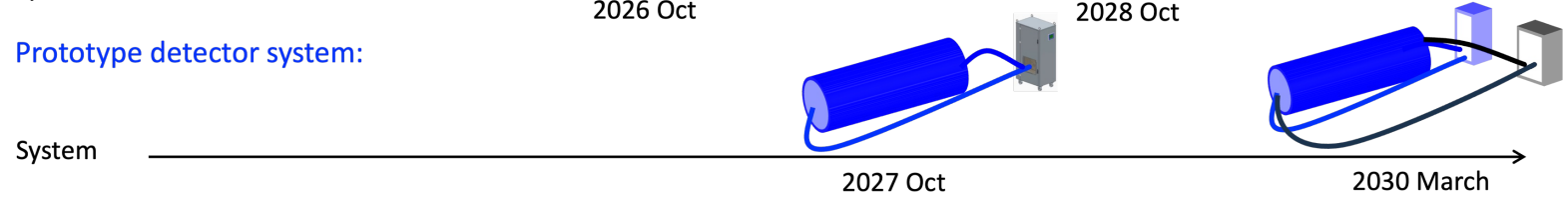
- Beam telescope system:



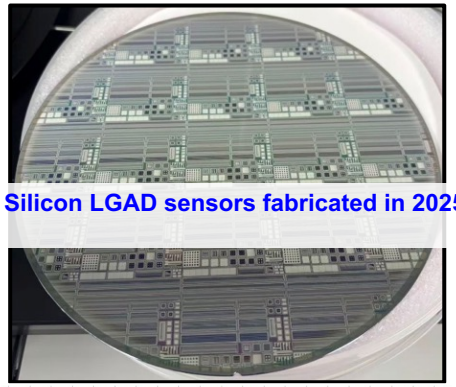
- Two phase CO_2 cooling system:



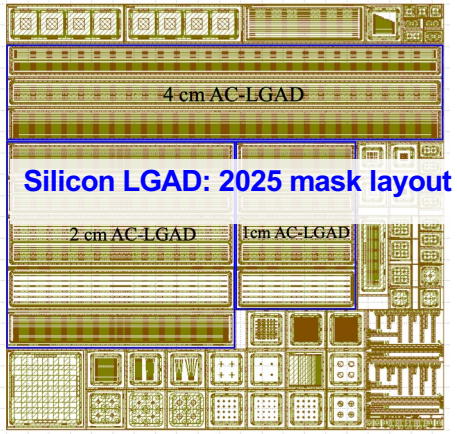
- Prototype detector system:



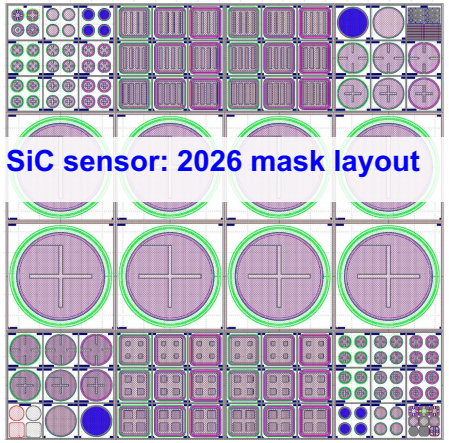
Sensor and ASIC Development



Silicon LGAD sensors fabricated in 2025



Silicon LGAD: 2025 mask layout



SiC sensor: 2026 mask layout

Semiconductor sensors:

- **Silicon:** develop the world's first large-area silicon sensor combining timing resolution <40 ps with <10 μm position resolution.
- **SiC:** develop 4H-SiC sensors with ~30 ps timing for operating at high temperatures and under intense radiation.

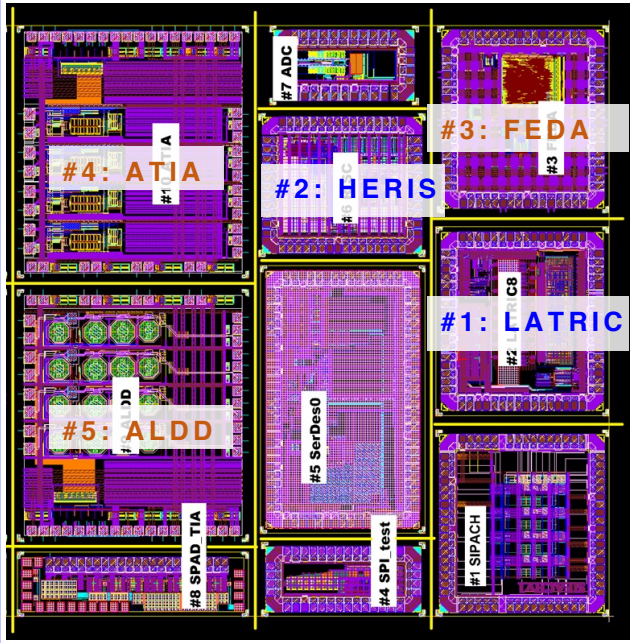
Dedicated semiconductor detector readout ASICs:

- **LATRIC:** high timing precision (≤30 ps), readout compatible with 10 μm position resolution, low power and high integration.
- **HERIS:** China's first radiation-hard RISC-V system-on-chip for particle physics applications.

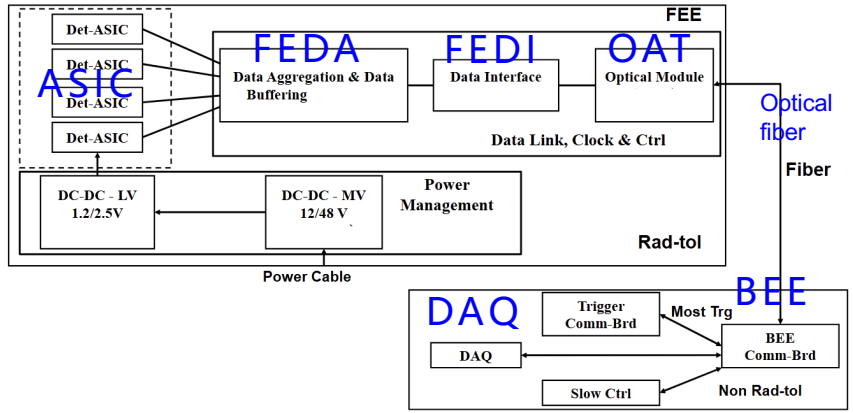
Other high-speed data transmission ASICs:

- **FEDA:** 10.24 Gb/s data aggregator
- **FEDI:** data interface chip
- **ATIA:** optical data receiver
- **ALDD:** laser diode driver

Joint R&D by IHEP, CCNU, NPU and partners, with applications beyond semiconductor detectors



ASIC tape-out layouts



Proposed detector readout architecture

Silicon Sensors with Precise Timing and Position Resolution

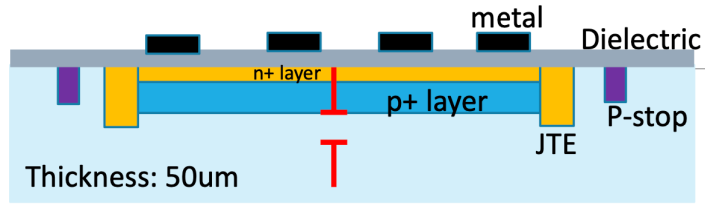
Developing the first large-area, engineering-grade silicon sensor with <10 μm position and 40 ps timing resolution

⇨ AC-coupled LGAD (AC-LGAD) sensors target large areas (≥2 cm × 2 cm), excellent position and timing resolution, and lower power. The latest tape-out was submitted in 2025.

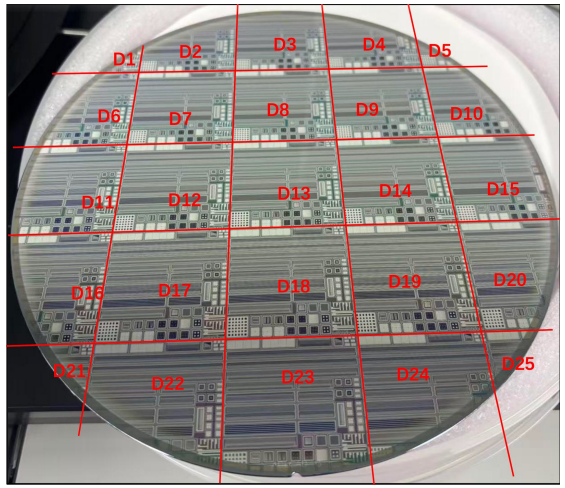
- **Pixels:** pitches of 55, 100, 150, and 200 μm
- **Strips:** lengths of 1, 2, and 4 cm

  pitches of 100, 200 and 500 μm
- **Electrode widths:** 25, 50, and 100 μm
- Tune doping to improve timing and position precision
- Optimize sensor structures, including epitaxial thickness, to reduce parasitic capacitance and readout power

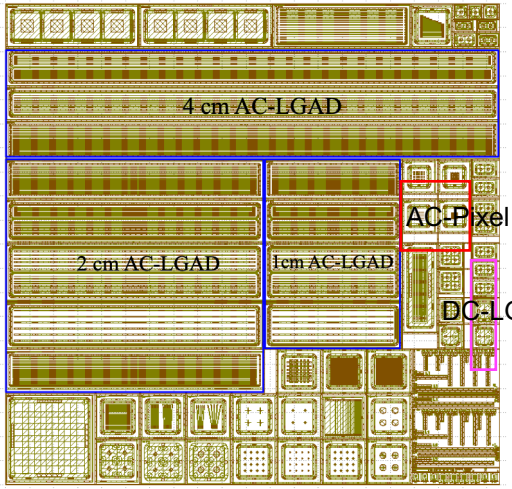
AC-LGAD structure



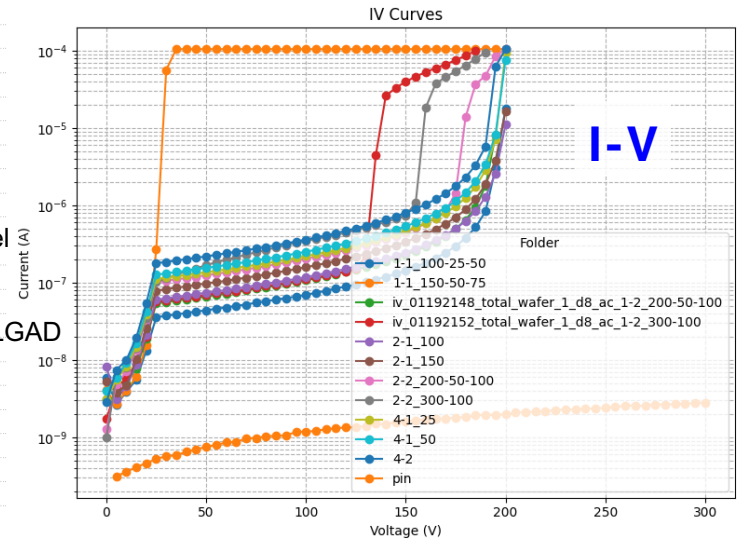
See details in Mei Zhao's talk

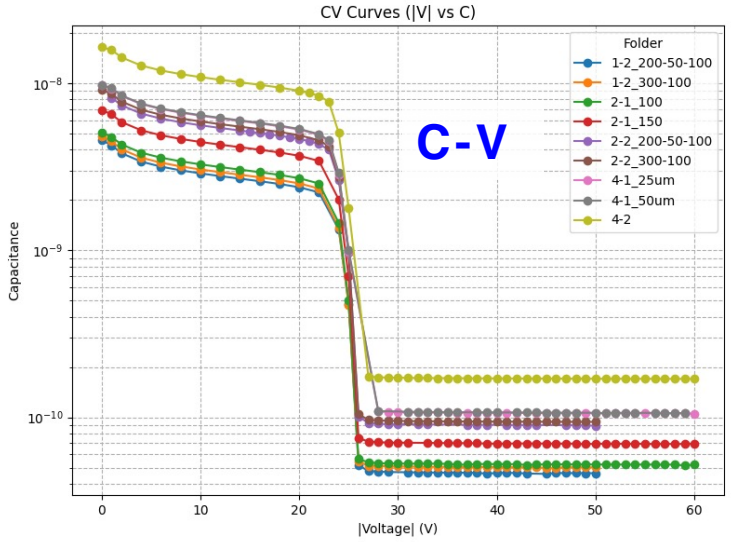


Latest silicon AC-LGAD wafer



Sensor mask layout

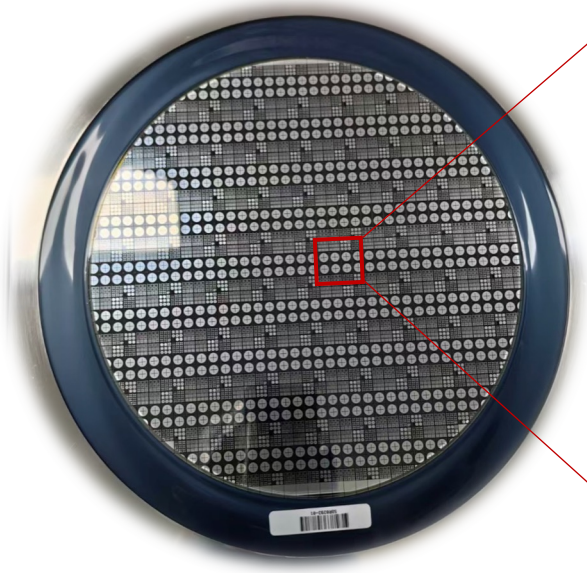




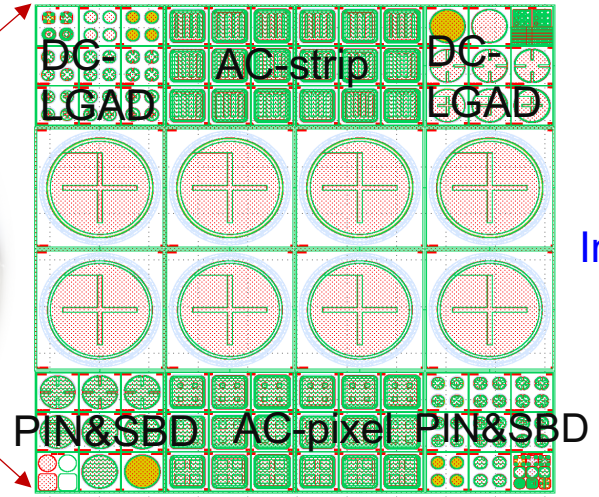
Silcon Carbide (SiC) Sensors

⇨ Wide-bandgap SiC offers a high breakdown field, high thermal conductivity and stability, low noise and excellent radiation tolerance, making it suitable for harsh environments. After three iterations of device structures and processes, the team completed the latest tape-out of implanted SiC sensors in May 2026:

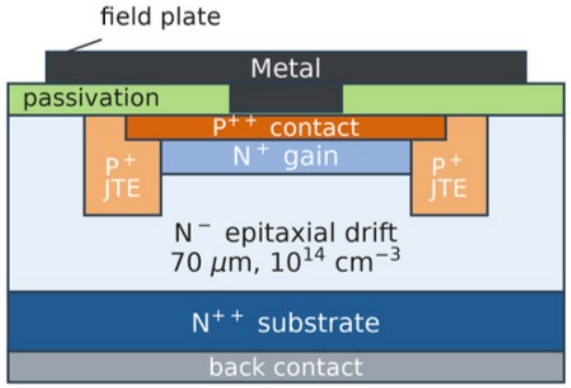
- **PIN diodes:** active size 1.4 mm / 0.5 mm
- **Schottky barrier diodes (SBD):** active size 0.5 mm
- **Low-gain avalanche diodes (LGAD):** active size 1.4 mm / 0.5 mm
- **AC-coupled LGAD (AC-LGAD):** pixels / strips



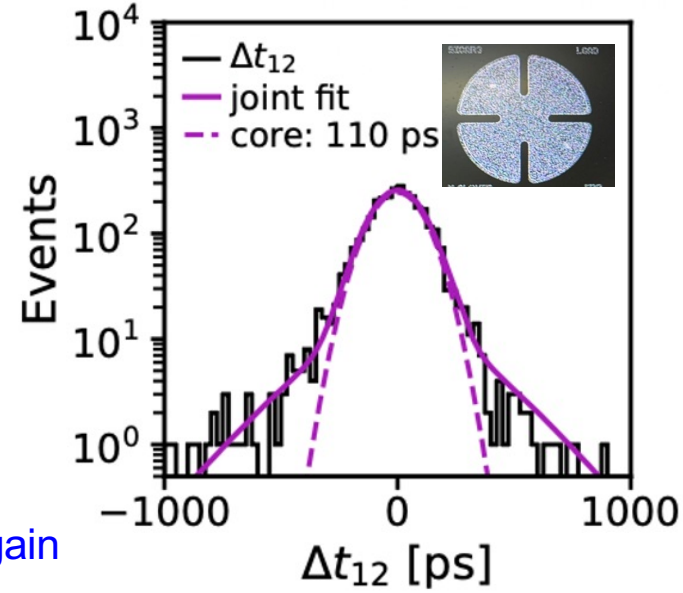
Latest tape-out SiC wafer
(8-inch MOSFET)



SiC sensor mask layout



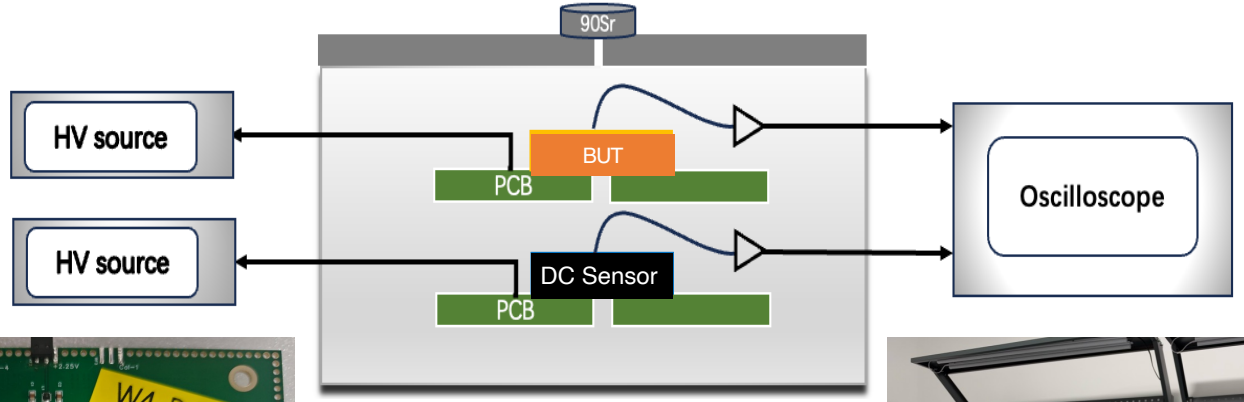
Implanted DC-SiC structure with gain

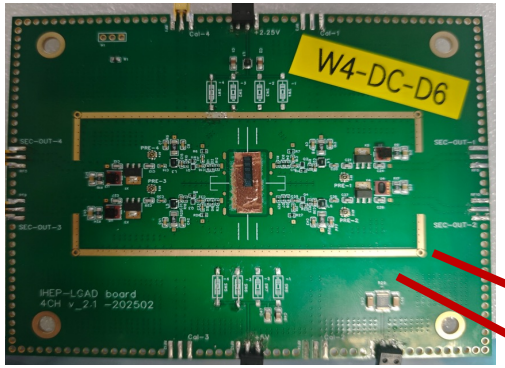


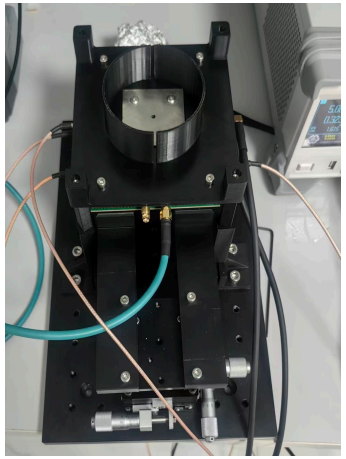
77 ps timing resolution in ^{90}Sr β tests

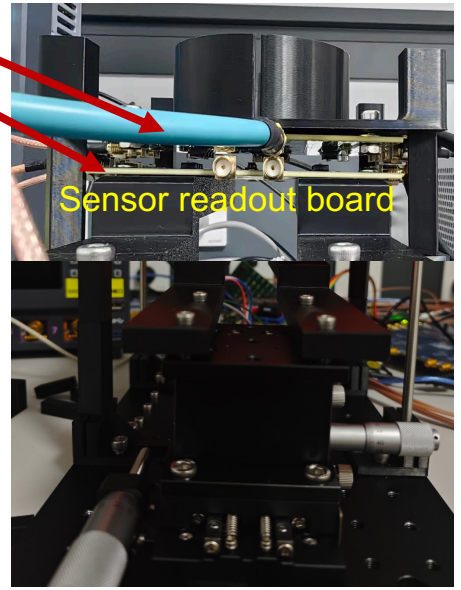
By optimization of substrates/epitaxy and fabrication processes, we aims to achieve stable, engineering-ready, large-area SiC sensors with precise timing and position measurement, within a silicon-led R&D program spanning multiple materials.

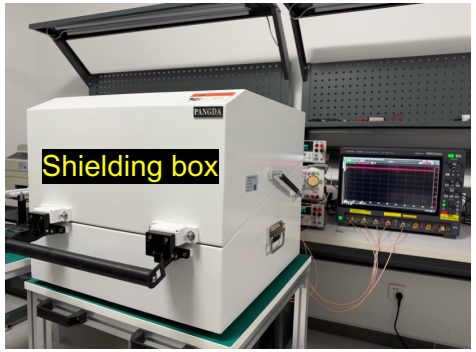
Silicon Sensors Timing: ^{90}Sr β Tests

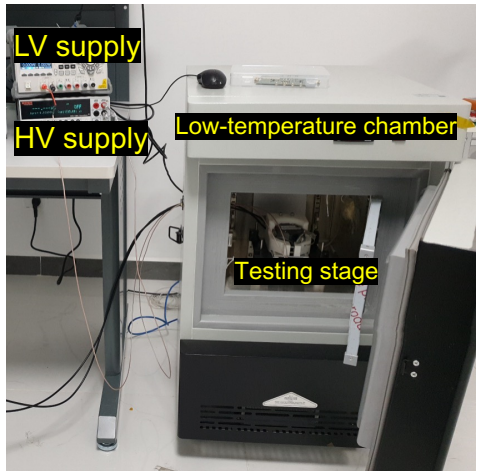


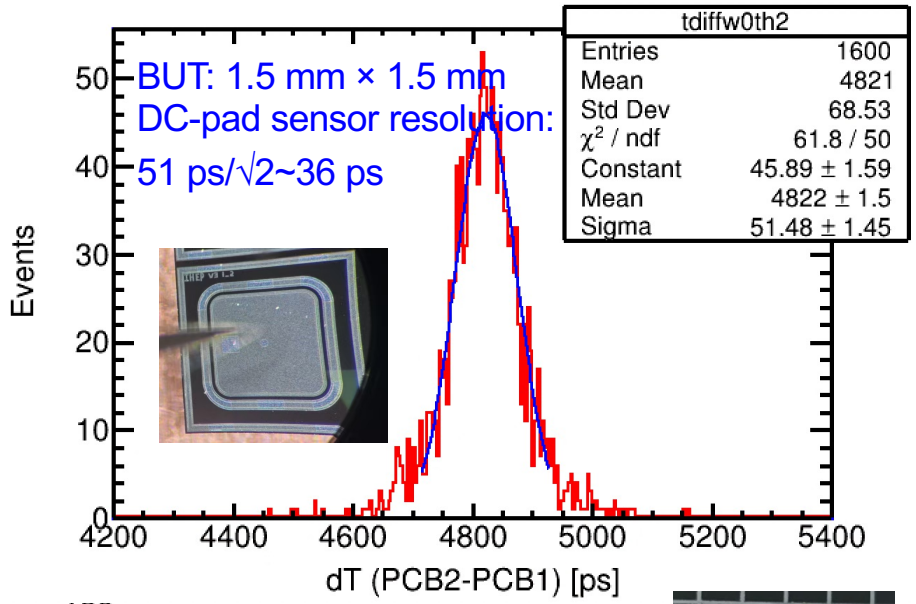


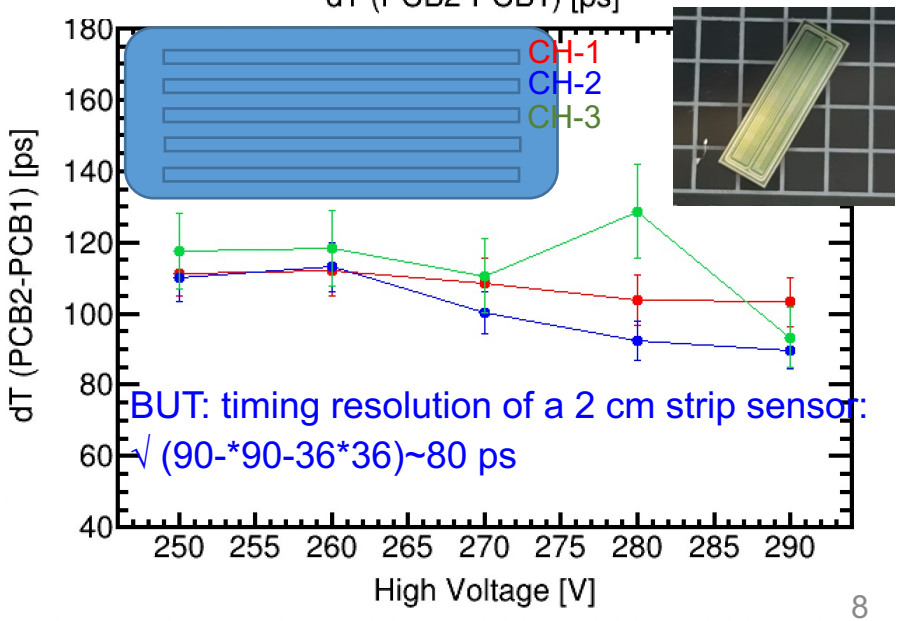




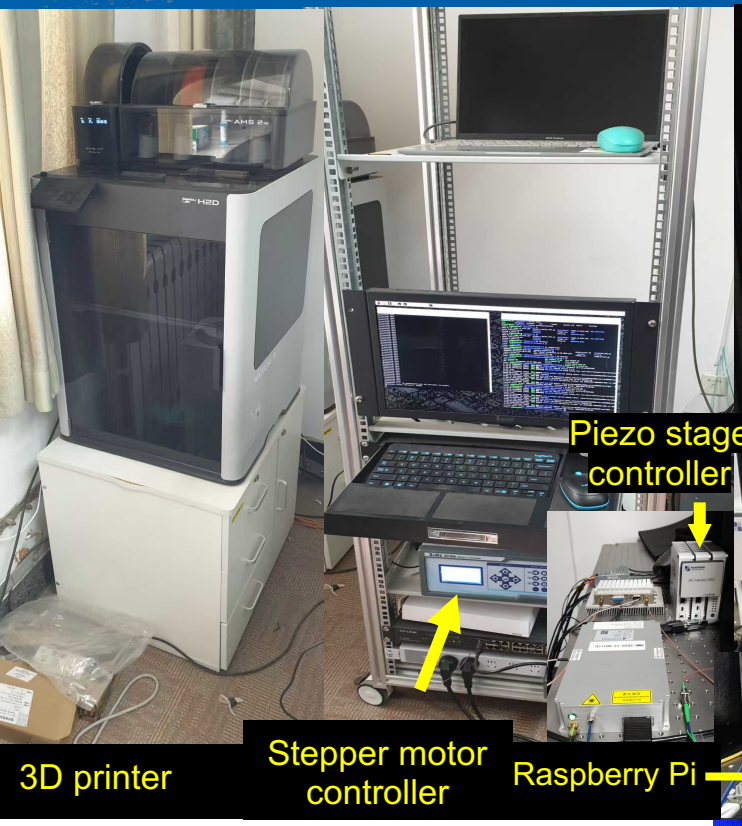


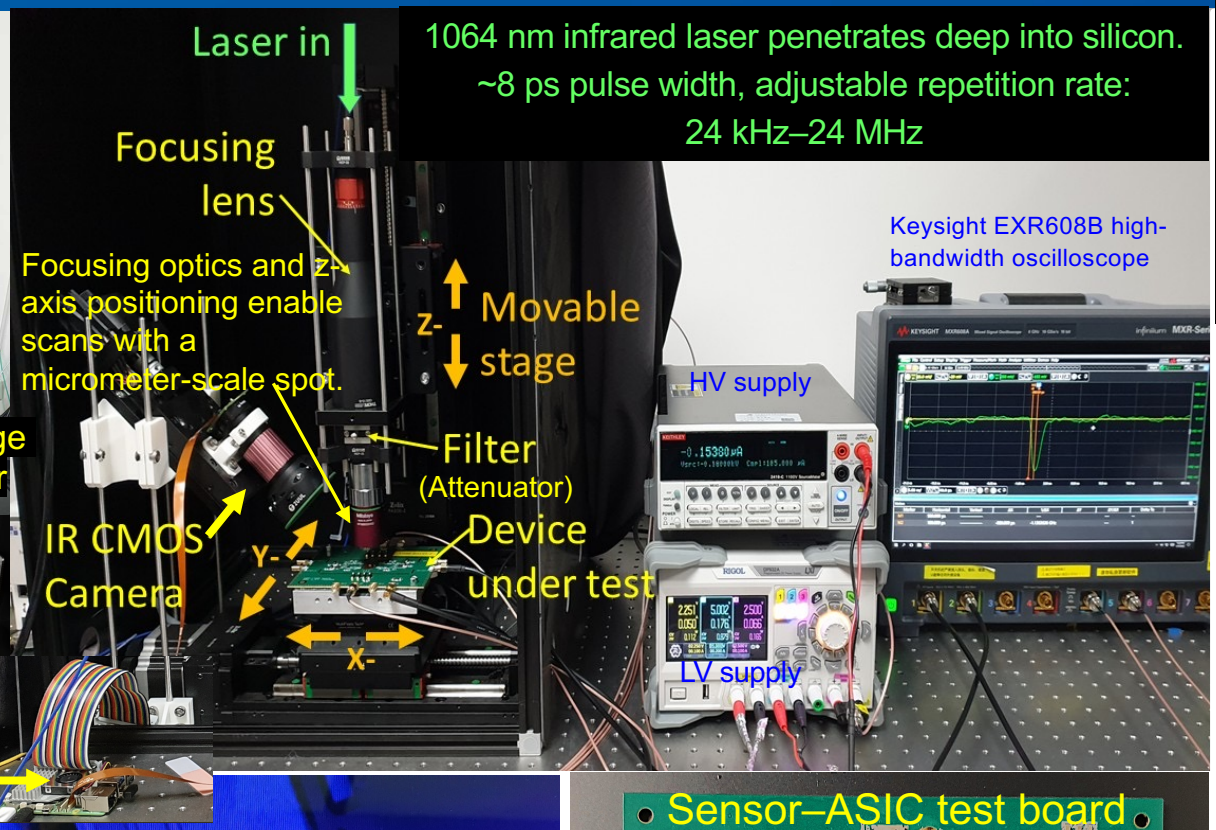






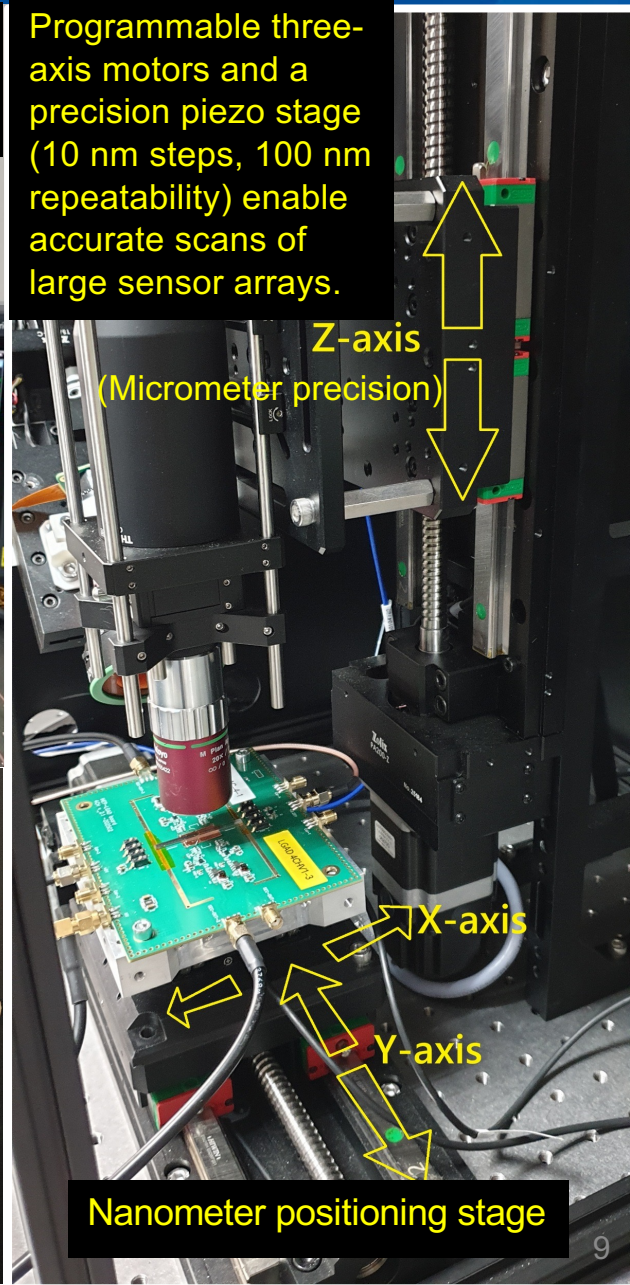
Precision Infrared Laser Test System

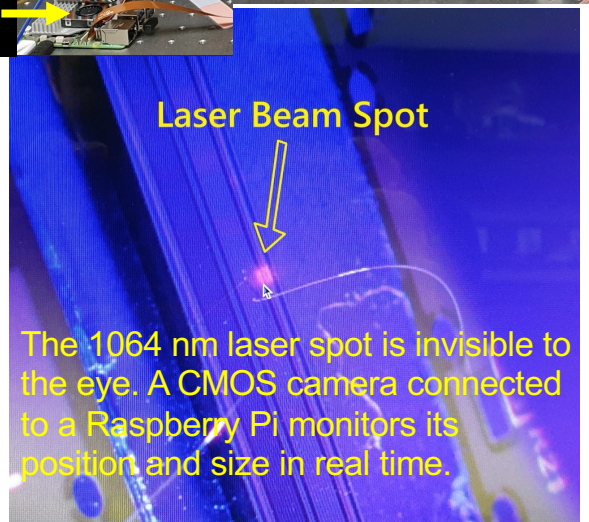


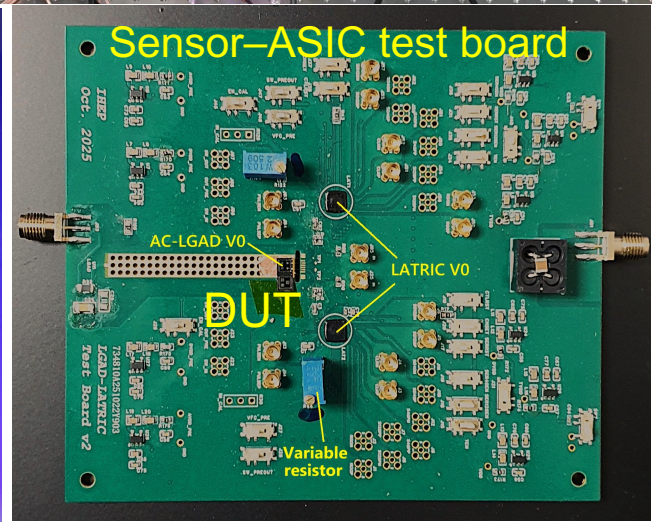


1064 nm infrared laser penetrates deep into silicon. ~8 ps pulse width, adjustable repetition rate: 24 kHz–24 MHz

Programmable three-axis motors and a precision piezo stage (10 nm steps, 100 nm repeatability) enable accurate scans of large sensor arrays.



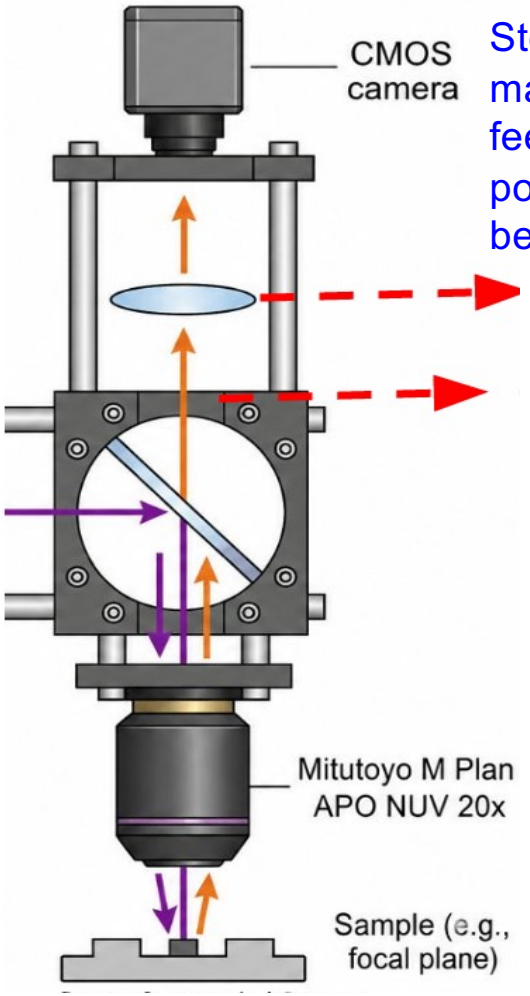




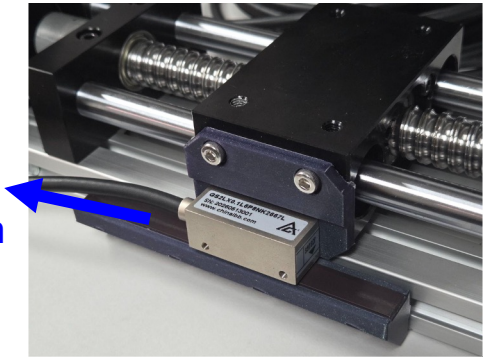
- **Precision picosecond infrared laser TCT system for testing sensors and readout ASICs**

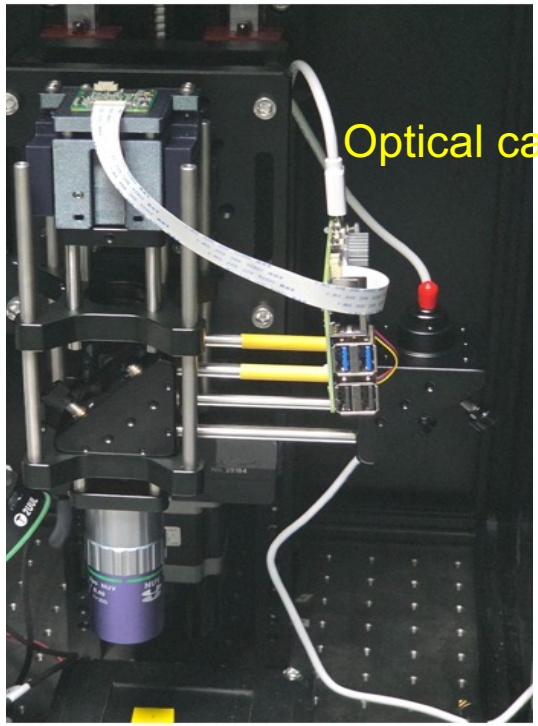
Two-Photon Laser Test System for Wide-bandgap Sensors:

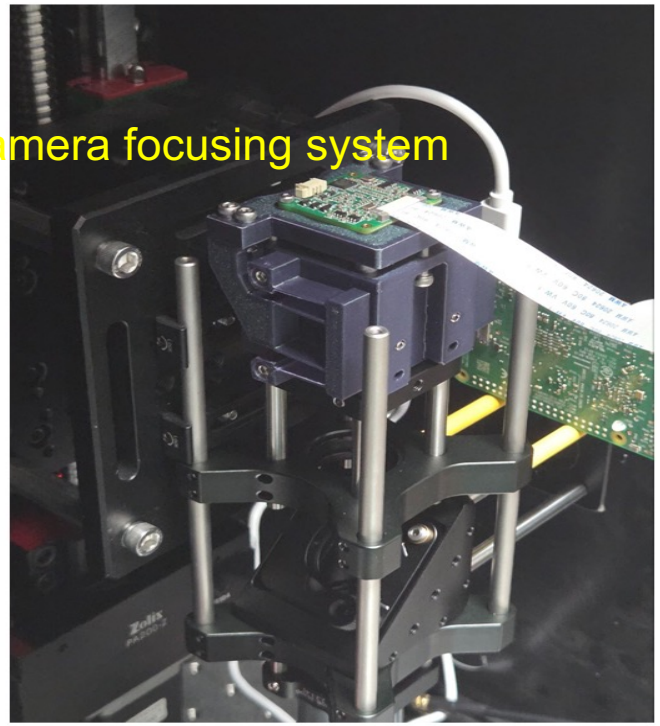
Alongside infrared testing for silicon detectors, we developed a precision two-photon laser test platform for wide-bandgap sensors. Si and SiC detectors share an automated test hardware/software framework, infrastructure, front-end readout electronics and system integration.



Stepper motors with magnetic encoder feedback provide positioning precision better than 0.1 μm

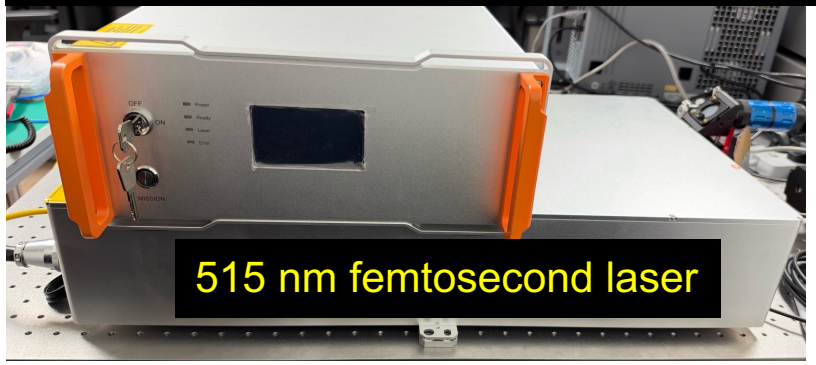


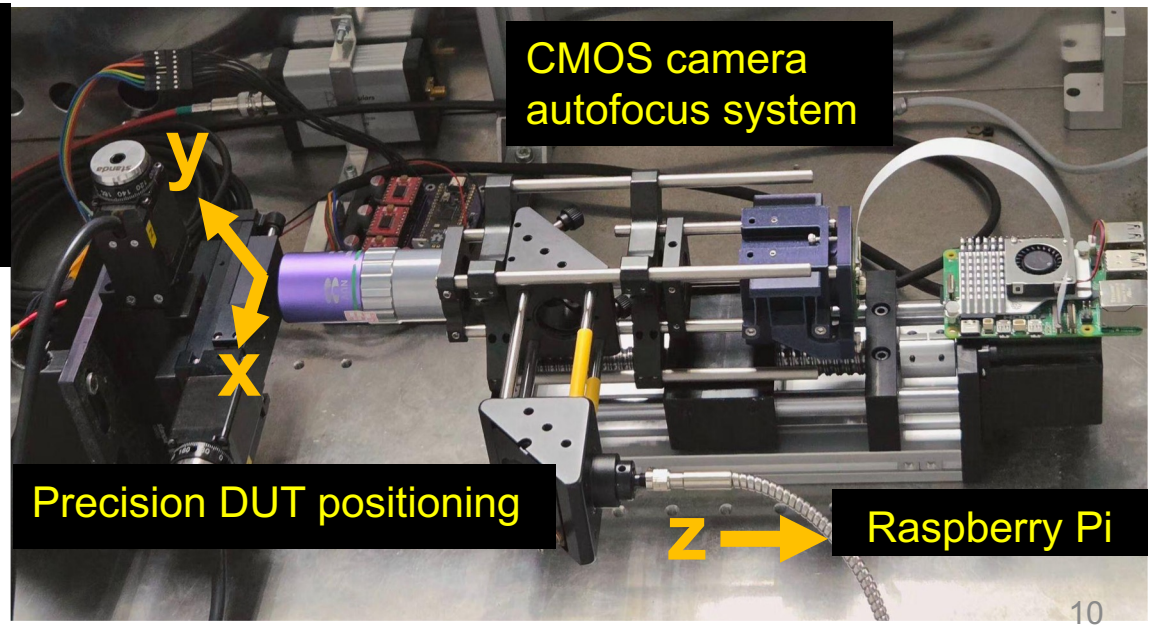




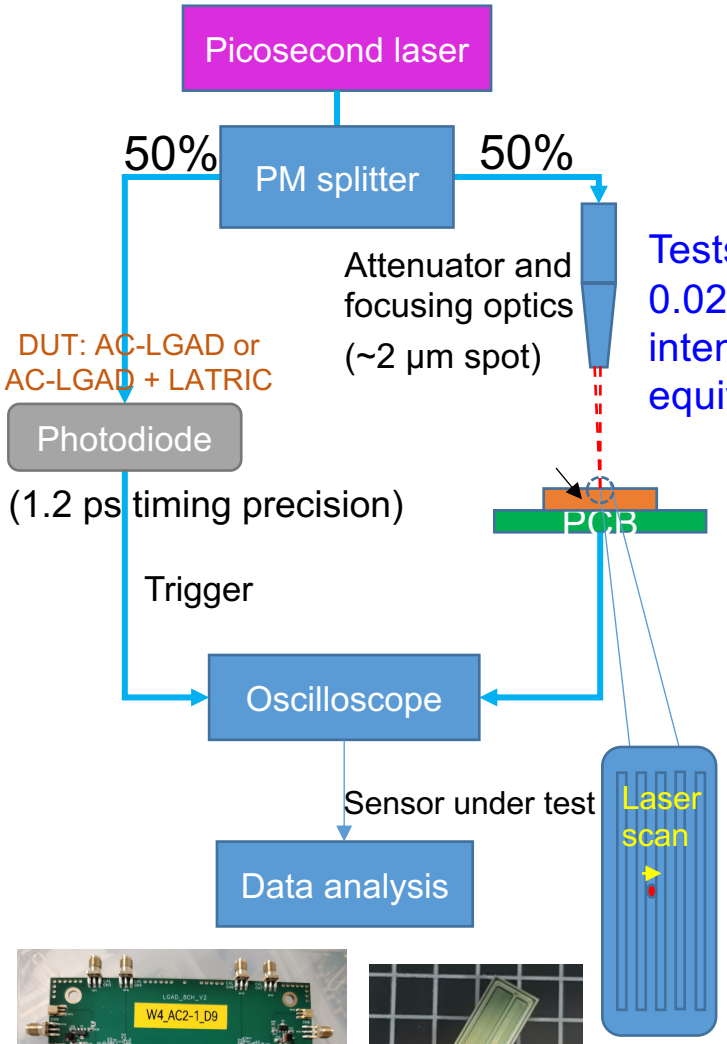
Upgrade to a 515 nm femtosecond (<200 fs) laser system for wide-bandgap semiconductor characterization:

- Two-photon excitation penetrates up to 60 μm to emulate MIP ionization in SiC

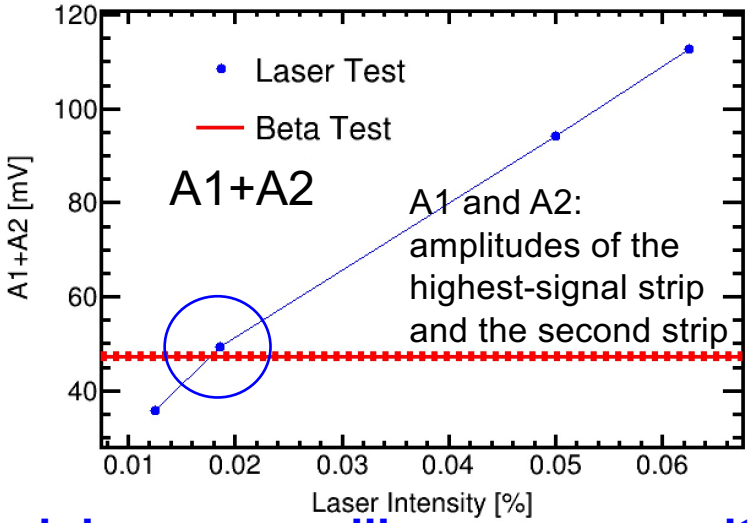


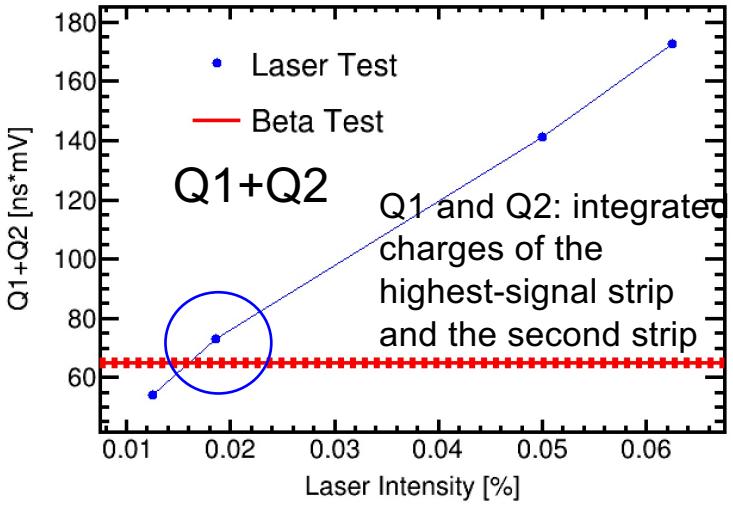


MIP-Equivalent Laser Tests: Strip Sensors



Tests show that 0.02% laser intensity is MIP-equivalent



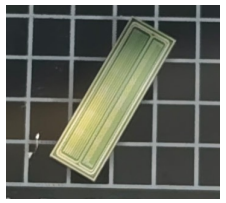


R&D goal: large-area silicon sensors with 40 ps timing and 10 μm position resolution

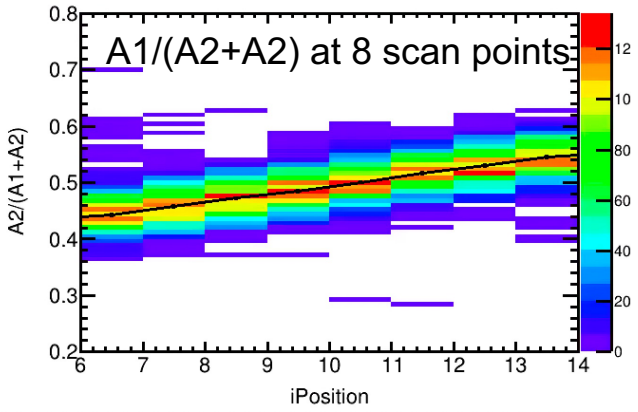
The latest 2026 silicon LGAD sensor with 2 cm strips and 100 μm pitch achieves 8 μm position precision and 60 ps timing at MIP-equivalent laser intensity (0.02%).

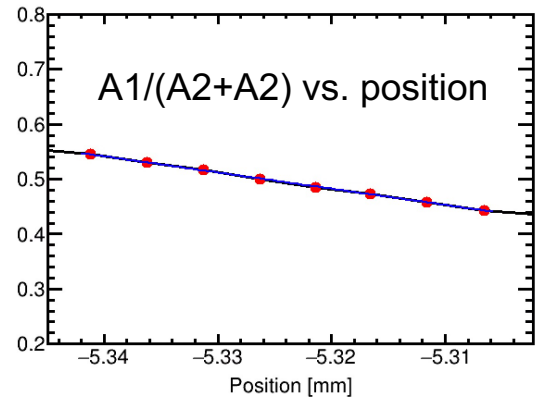
See details in Mei Zhao's talk

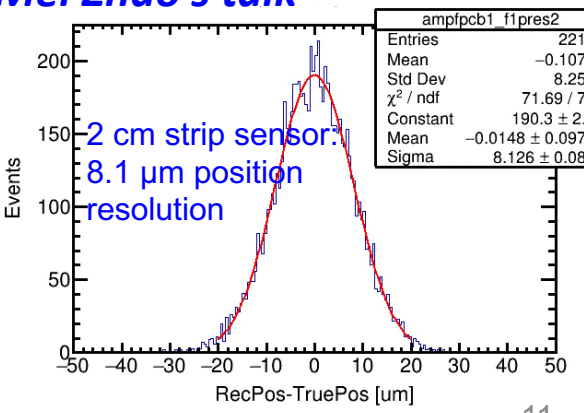




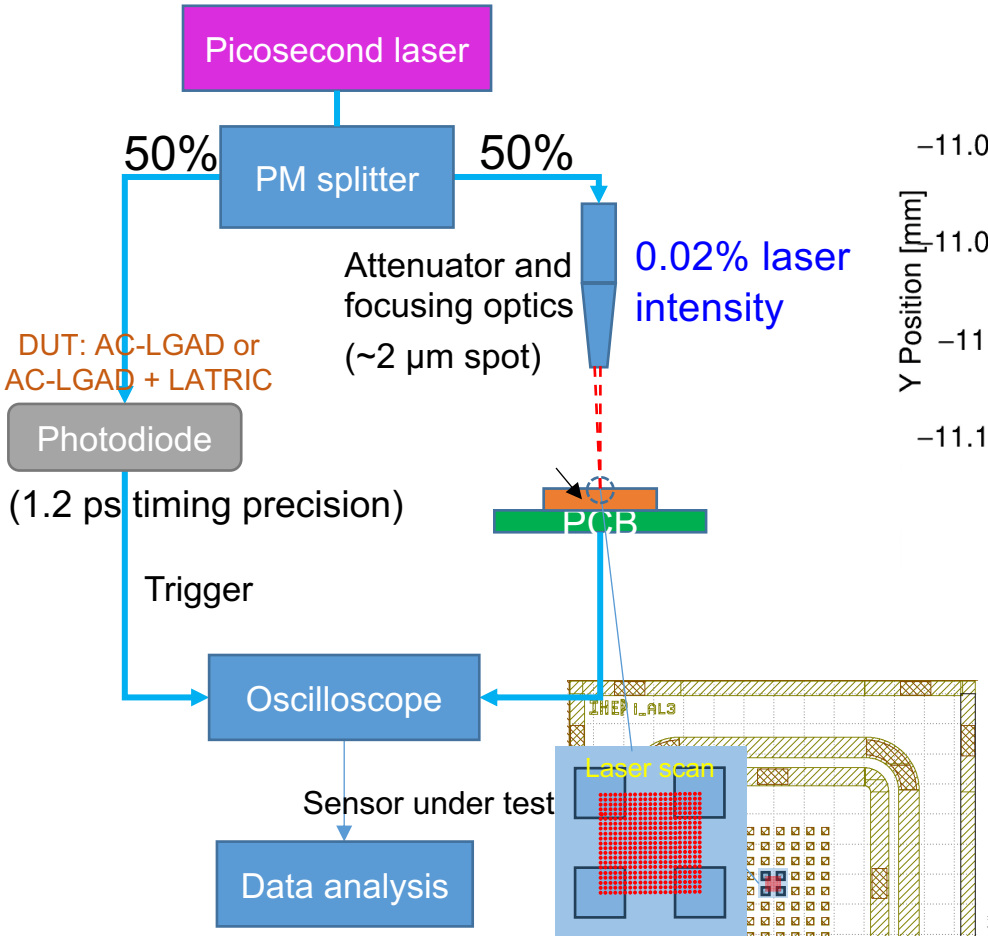
2 cm strip sensor

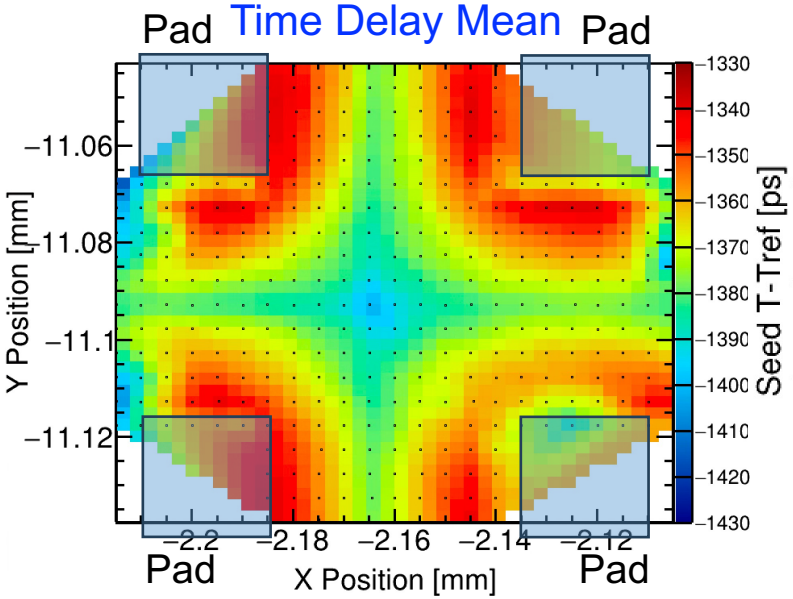


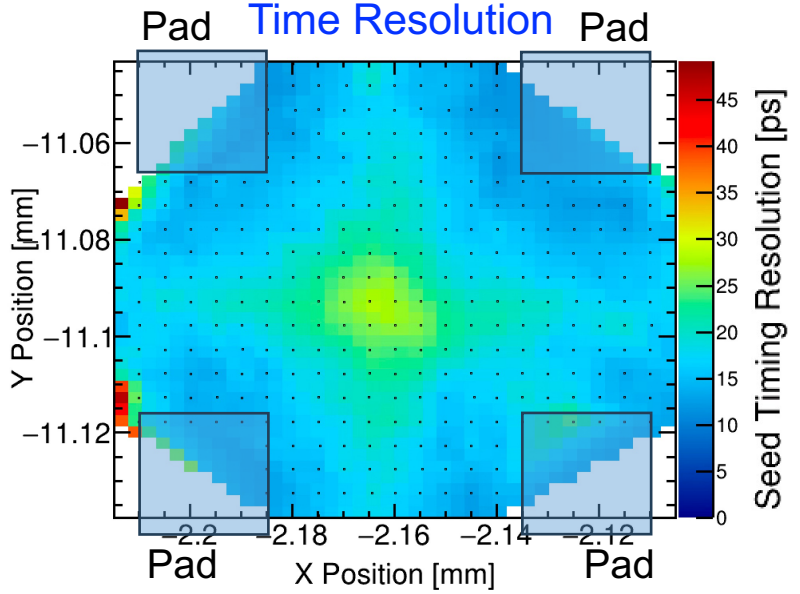




MIP-Equivalent Laser Tests: Pixel Sensors

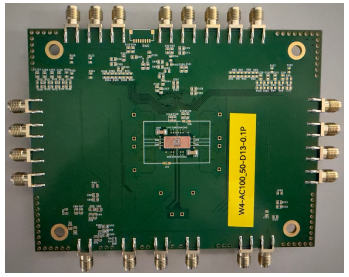


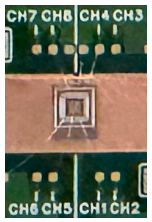




The latest 2026 silicon LGAD sensor with 100 μm pixels and 50 μm readout pads achieves 3 μm position precision and ~20 ps timing at MIP-equivalent laser intensity (0.02%).

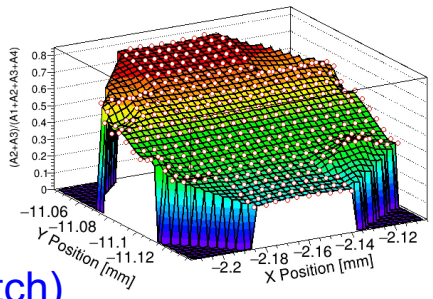
See details in Mei Zhao's talk

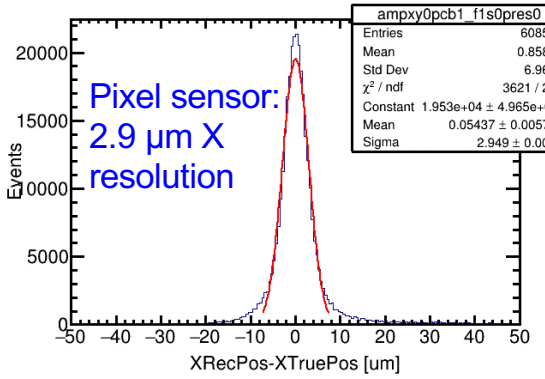


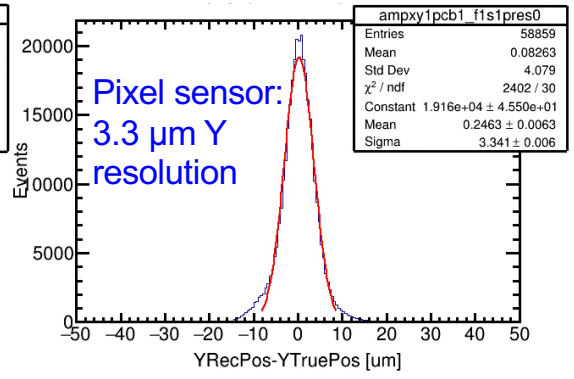


Pixel sensor (100 μm pitch)

(A2+A3)/(A1+A2+A3+A3) VS Laser Position





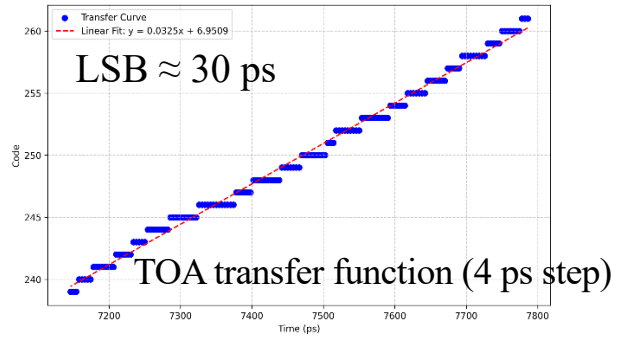


Readout ASIC (LATRIC) Development

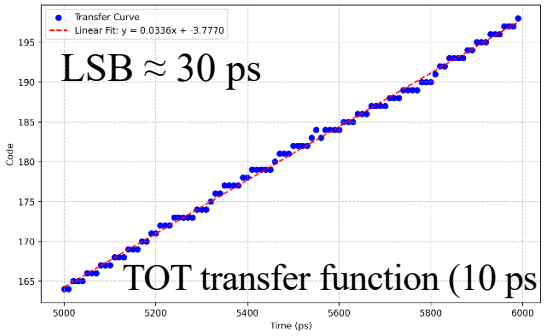
◘ LATRIC readout ASIC targets ≤30 ps timing, readout compatible with 10 μm position resolution, low power and high integration (100 μm channel pitch, ≥64 channels):

⇨ The first single-channel prototype, LATRIC0, completed design and tape-out submission in April 2025.

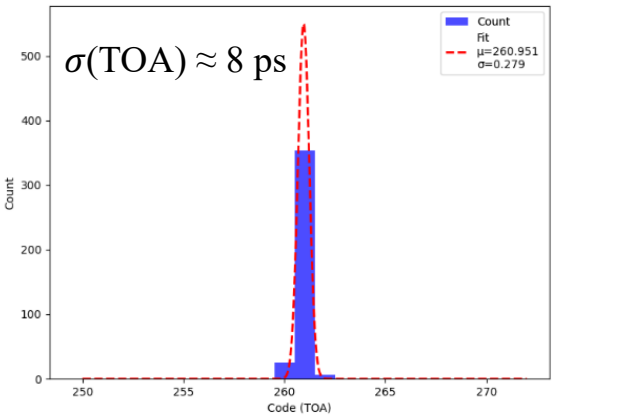
- The ASIC integrates an analog preamplifier, discriminator, time-to-digital converter (TDC) and readout serializer.
- Measured timing LSB ~30 ps. TDC current at 1.2 V: 0.1 mA at 0.5 million triggers/s, 0.3 mA at 1 million triggers/s, and 0.5 mA at 2 million triggers/s, meeting design requirements.

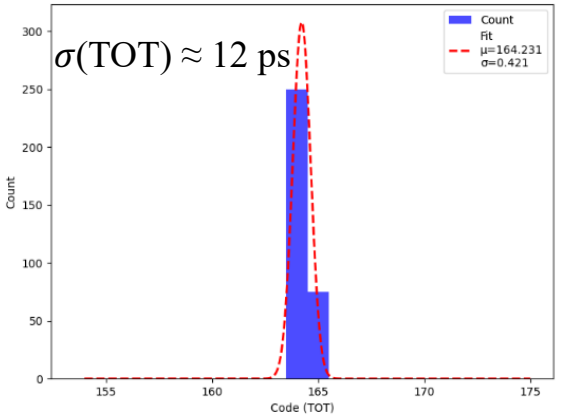


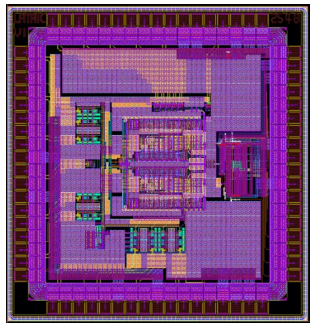
TOA transfer function (4 ps step)



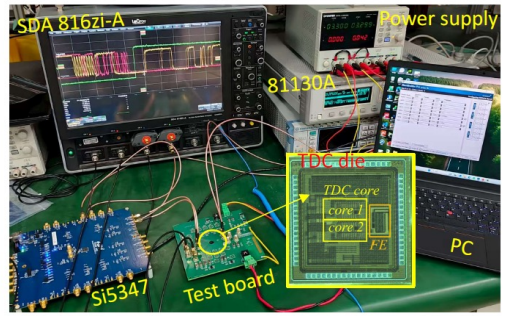
TOT transfer function (10 ps step)



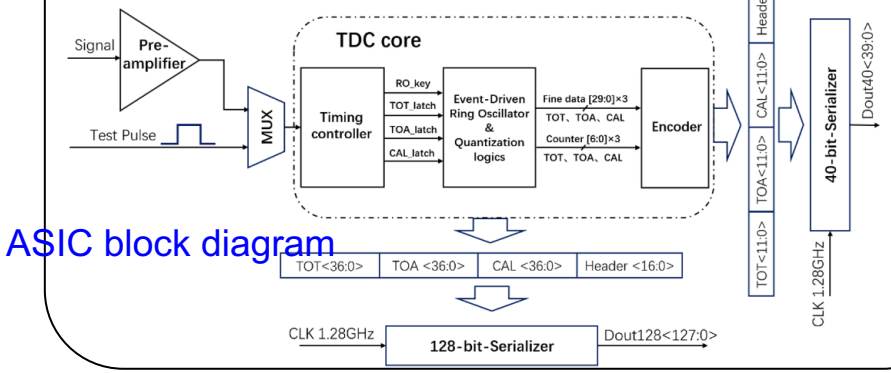




LATRIC0 chip layout



ASIC test setup

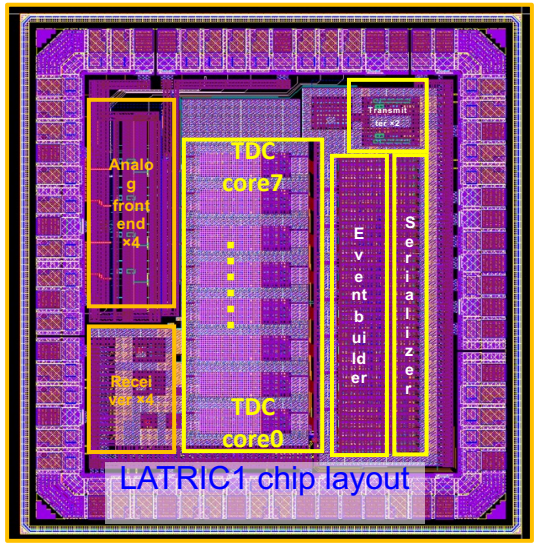


ASIC block diagram

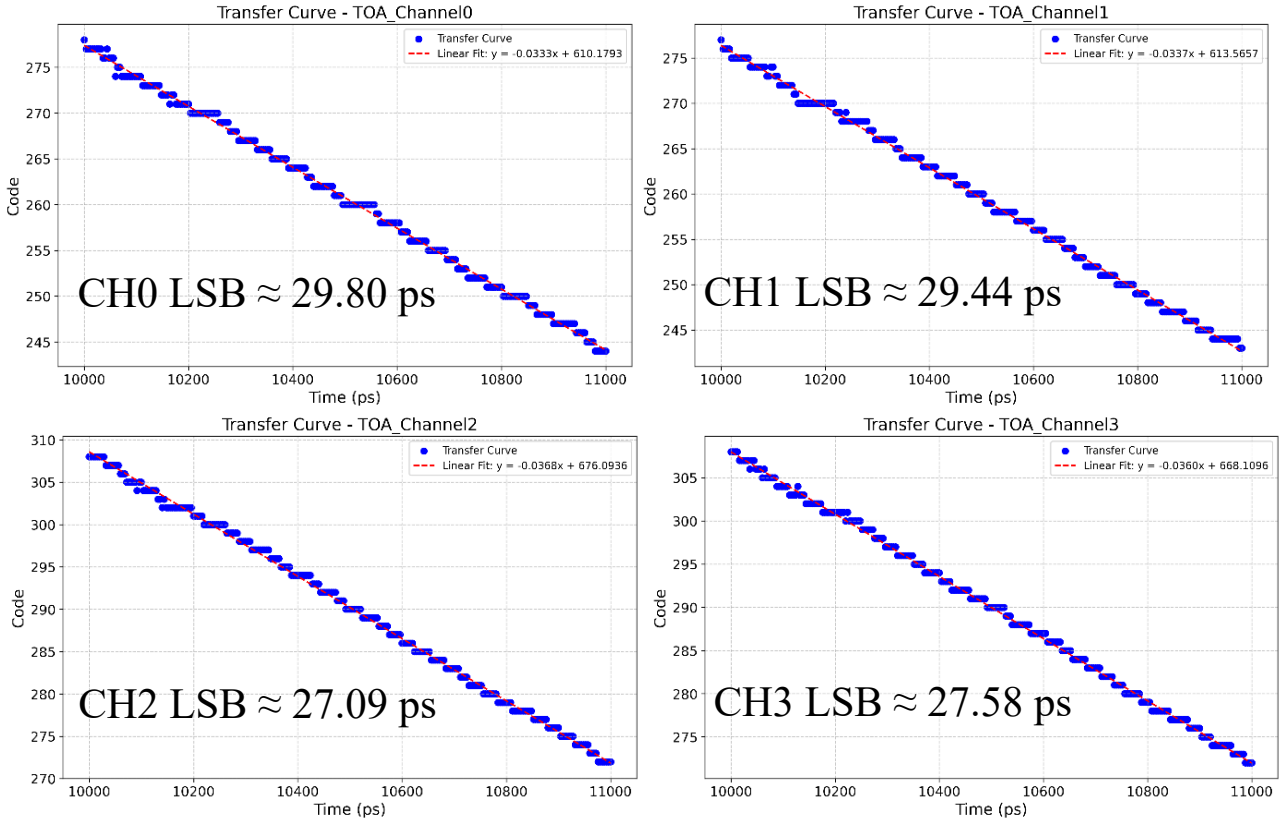
LATRIC1: Design and Measurement Results

⇨ The second version LATRIC1 has 8 channels. Design and tape-out submission were completed in October 2025.

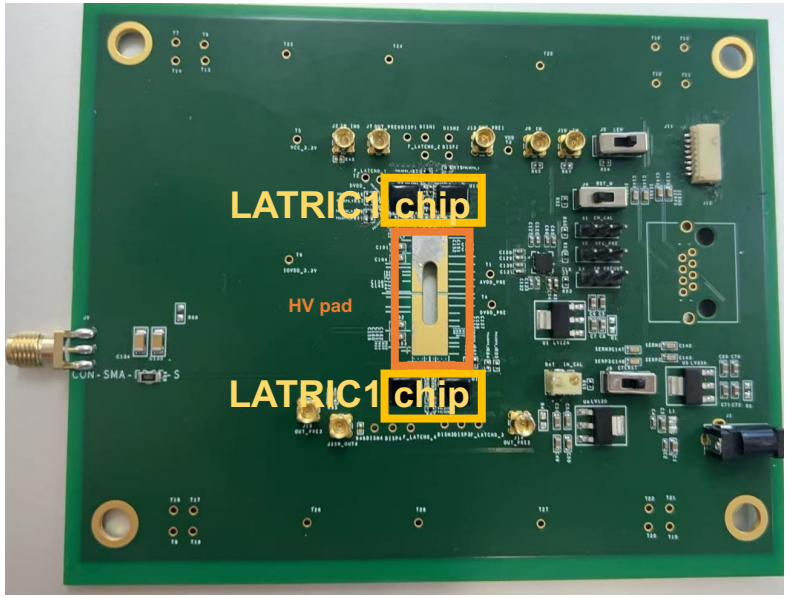
- Four channels integrate analog front ends and TDCs. Four more connect TDCs to differential pulse receivers. Channel pitch: 100 μm.
- Improvements include a higher-gain analog front end for better SNR, refined encoder logic, an event builder and timestamps.



LATRIC1 chip layout



Measured LATRIC1 timing LSBs, chips received in March 2026



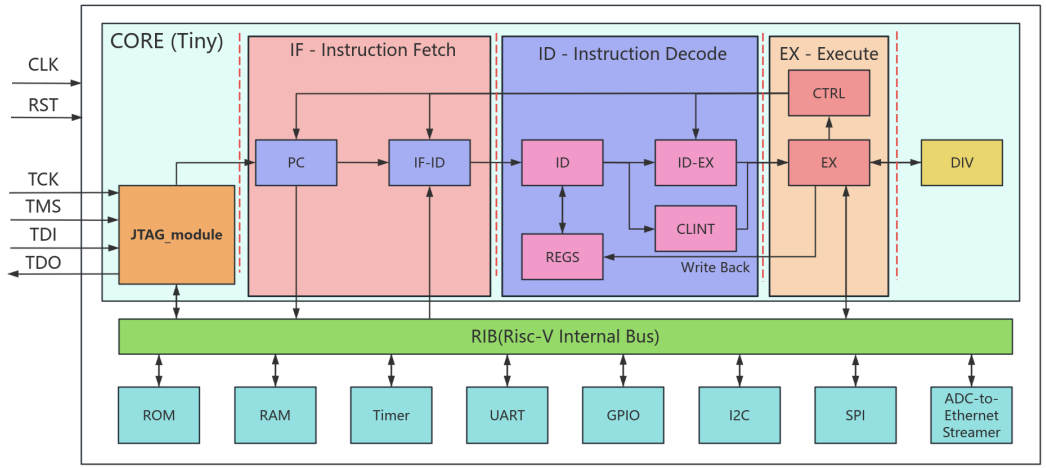
LATRIC1–sensor test board

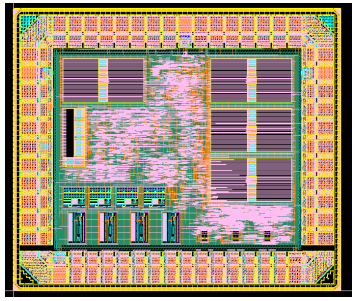
HERIS: A RISC-V System-on-Chip

HERIS: a radiation-hard RISC-V SoC dedicated to particle physics

⇨ Fixed hardware logic in conventional ASICs limits flexibility, configurability and intelligence. Programmable front-end SoCs integrate a CPU, memory, buses and peripherals to enable active sensing and adaptive control. Development of HERIS-V1, based on Tiny RiscV and targeting China's first radiation-hard RISC-V SoC for particle physics, began in early 2025. The team completed RTL development, FPGA prototyping and digital backend integration, followed by a 55 nm CMOS tape-out in October 2025. Future integration with LATRIC will combine precision measurement with on-chip intelligent processing.

- Core (Tiny RiscV)
  - RV32IM instruction set
  - 3-stage pipeline
  - CoreMark/MHz = 2.4
- JTAG interface
  - OpenOCD support
  - GDB debugging and boot support
- Peripherals
  - 4 KB ROM, 32 KB RAM
  - I²C, UART and SPI support
  - Integrated ADC data acquisition with UDP transmission





- 55 nm process
- Clock frequency: 50 MHz
- Die size: 1.020 × 1.196 mm
- Supply voltage: 1.2 V

HERIS-V1 Functional Tests

- Power-on, OpenOCD connection and ROM execution verified

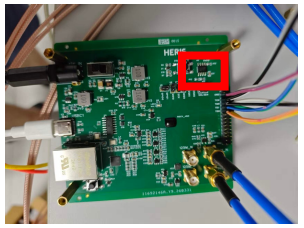
```
PS E:\fpga\Tools\xpack-openocd-0.12.0-6\bin> .\openocd.exe -f .\tinyriscv_JTAG_HS2.cfg
xPack Open On-Chip Debugger 0.12.0+dev-01850-geb6f2745b-dirty (2025-02-07-10:08)
Licensed under GNU GPL v2
For bug reports, read
        http://openocd.org/doc/doxygen/bugs.html
Info : clock speed 1000 kHz
Info : JTAG tap: riscv.cpu tap/device found: 0x1e200a6f (mfg: 0x537 (Wuhan Xun Zhan Electronic Technology), part: 0xe200
, ver: 0x1)
Info : datacount=3 progbufsize=1
Info : Examined RISC-V core; found 2 harts
Info :  hart 0: XLEN=32, misa=0x0
Info : [riscv.cpu] Examination succeed
Info : [riscv.cpu] starting gdb server on 3333
Info : Listening on port 3333 for gdb connections
Info : Listening on port 6666 for tcl connections
```

串口调试助手 + TCP/UDP

端口名：COM5
波特率：115200
数据位：8
校验位：None
停止位：1
RI DSR CTS DTR RTS

```
--- RISC-V Bootloader Started ---
Initializing SD card on SPI channel 1...
SD_INIT: Failed on CMD0
!!! FATAL: SD Card initialization failed. Halting. !!!
Target RAM size: 14336 bytes. Need to read 28 blocks from SD card.
Starting to copy data from SD:@0x0 to RAM:@0x10000000...
```

- Onboard EEPROM operates via I²C



```
int main() {
    uart_init();
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);

    uint16_t test_addr = 0x1234;
    uint8_t test_data  = 0xAC;

    eeprom_write_byte(test_addr, test_data);
    uint8_t read_back = eeprom_read_byte(test_addr);
```

```
== I2C Master Final Test Program ===
[I2C] Write: Addr=0x1234 Data=0xAC
  > Config Check: Slave=0x53, Addr=0x1234, Data=0xAC
[I2C] Read: Addr=0x1234
```

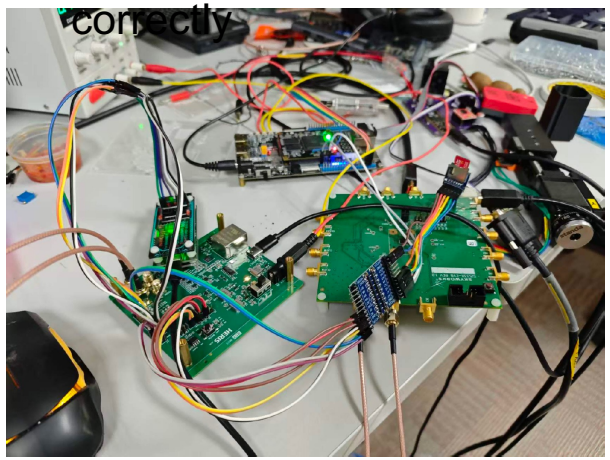
```
int main() {
    uart_init();
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);

    uint16_t test_addr3 = 0x0123;
    uint8_t read_back3 = eeprom_read_byte(test_addr3);
    uint16_t test_addr2 = 0x1234;
    uint8_t read_back2 = eeprom_read_byte(test_addr2);

    xprintf("[I2C] Verification: Read1 0x%02X, Read2 0x%02X\n", read_back3, read_back2);
```

```
=== I2C Mater Final Test Program ===
[I2C] Read: Addr=0x0123
[I2C] Read: Addr=0x1234
[I2C] Verification: Read1 0xFF, Read2 0xAC
```

- ROM, SD card and SPI operate correctly

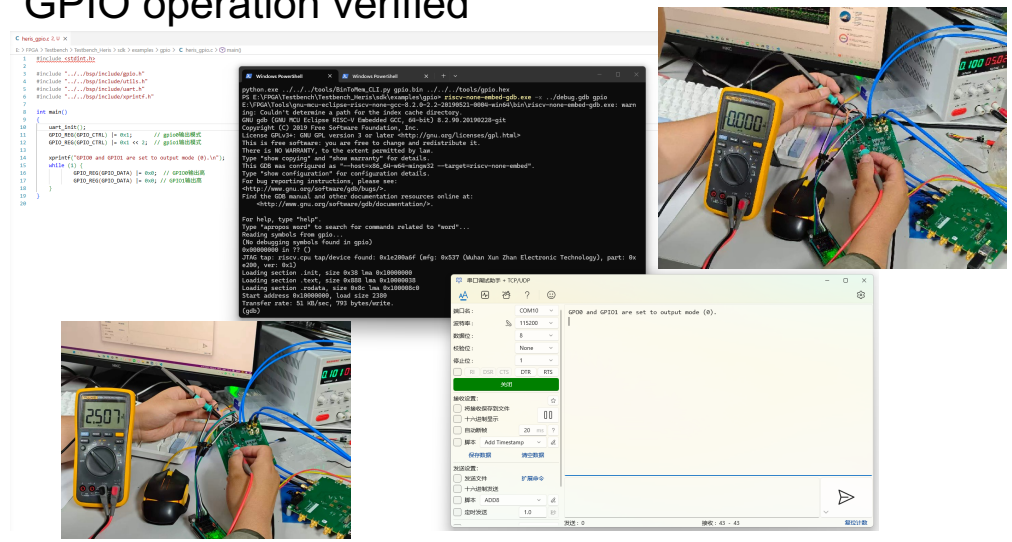


串口调试助手 + TCP/UDP

端口名：COM11
波特率：115200
数据位：8
校验位：None
停止位：1
RI DSR CTS DTR RTS
关闭
接收设置：
将接收保存到文件
十六进制显示
自动断帧 20 ms
脚本 Add Timestamp
保存数据 清空数据

```
--- RISC-V Bootloader Started ---
Initializing SD card on SPI channel 1...
SD Card on SPI CH-1 initialized successfully.
SD Card initialized successfully.
Target RAM size: 14336 bytes. Need to read 28 blocks from SD card.
Starting to copy data from SD:@0x0 to RAM:@0x10000000...
.......
Data copy complete.
Bootloader finished. Jumping to application at 0x10000000...
hello world
```

- GPIO operation verified



HERIS-V1 Performance

Test conditions

CoreMark Benchmark Statistics

Test Configuration

Item	Value
CPU Architecture	RV32IM Softcore
Benchmark	CoreMark
Iterations	100
Compiler	GCC 8.2.0
Optimization	`-O2 -funroll-loops -finline-functions`
Memory Mode	STATIC
Assumed Timer Clock	50 MHz

HERIS-V1 benchmark

CoreMark Results Summary

Run	Total Ticks	Time (s)	CoreMark	CoreMark/MHz
1	47,140,681	0.943	106.07	2.121
2	57,254,527	1.145	87.33	1.747
3	57,254,216	1.145	87.33	1.747
4	57,254,809	1.145	87.32	1.746
5	57,254,522	1.145	87.33	1.747
6	57,254,148	1.145	87.33	1.747
7	57,255,302	1.145	87.31	1.746
8	57,256,313	1.145	87.30	1.746
9	57,253,503	1.145	87.33	1.747
10	36,131,525	0.723	138.38	2.768
11	57,254,188	1.145	87.33	1.747
12	57,254,522	1.145	87.33	1.747
13	57,254,203	1.145	87.33	1.747

FPGA benchmark

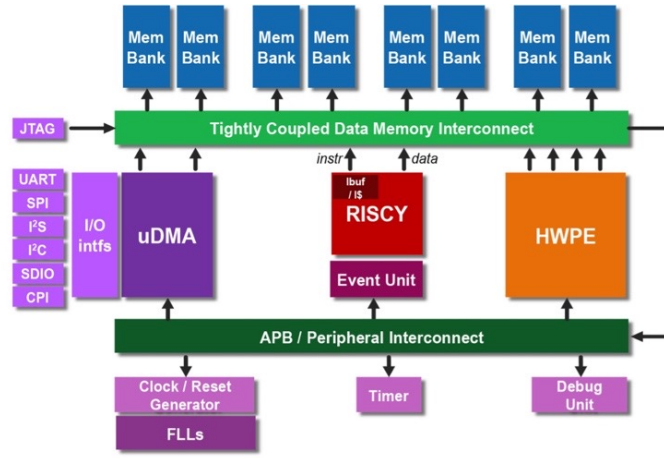
#	Total Ticks	CoreMark	CoreMark/MHz
1	264,551,913	18.90	0.378
2	25,685,150	194.66	3.893
3	55,131,135	90.69	1.814
4	29,876,551	167.35	3.347
5	57,253,579	87.33	1.747
6	57,243,713	87.35	1.747
7	29,906,285	167.19	3.344
8	57,254,426	87.33	1.747
9	41,493,461	120.50	2.410
10	46,612,237	107.27	2.145
11	54,497,797	91.75	1.835
12	48,237,510	103.65	2.073
13	28,275,053	176.83	3.537
14	57,253,726	87.35	1.747
15	13,635,777	366.68	7.334
16	25,475,668	196.27	3.925
17	57,253,893	87.35	1.747
18	57,253,672	87.36	1.747
19	57,253,673	87.36	1.747
20	26,854,754	186.19	3.724
21	57,250,967	87.40	1.748

Clock: 50 MHz
Maximum: 150 MHz

Performance comparison:

- ARM Cortex-M0/M0+: ~0.9–1.0
- PicoRV32 (minimal RISC-V): ~0.5–0.8
- HERIS-V1: 1.75 (consistent ASIC and FPGA benchmarks)
- VexRiscv / Hummingbird E203: ~1.5–2.2
- ARM Cortex-M3 / M4: ~3.3–3.4

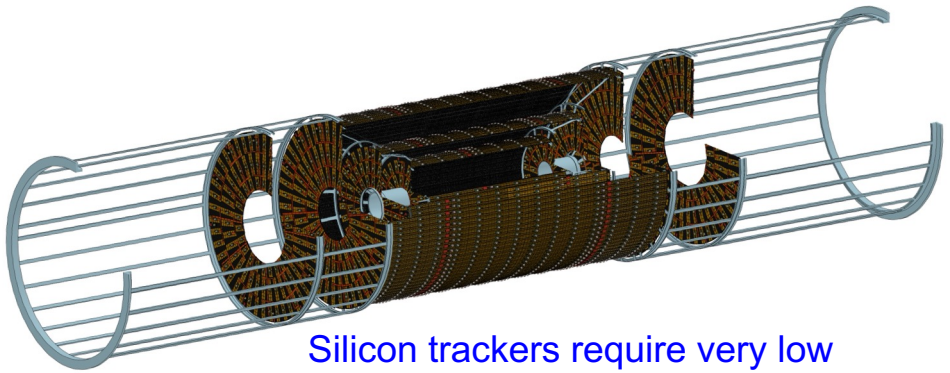
⇨ HERIS-V2 uses the PULPissimo SoC platform with RISCY/Ibex cores. Multilevel radiation hardening combines logic-level triple modular redundancy (TMR), memory-level error-correcting codes (ECC), and system-level software recovery. Design completion and tape-out submission are planned for January 2027.



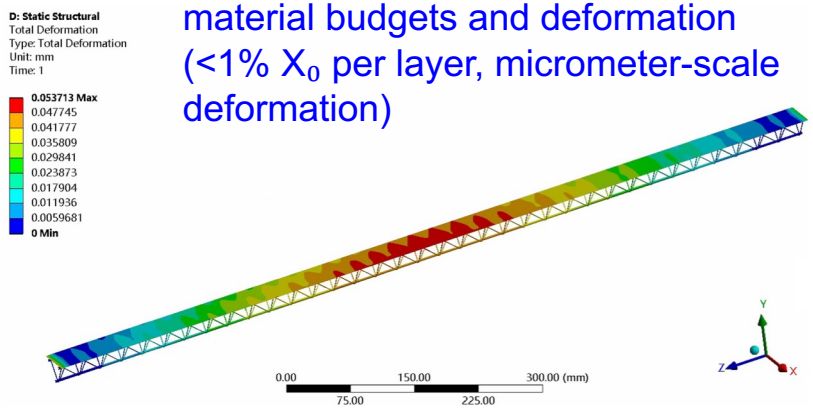
Detector Mechanics and Prototyping

Semiconductor Detector Mechanics Laboratory

⇨ Multiple scattering and mechanical deformation directly affect tracking precision, while detector heat must be removed efficiently. This requires low-mass, stiff, thermally conductive carbon-fiber structures integrated with cooling. To address the lack of a systematic domestic capability, the team established a mechanics laboratory. It develops carbon-fiber structural design and manufacturing for silicon tracker prototypes, enabling engineering applications of lightweight composites in semiconductor detectors.



Silicon trackers require very low material budgets and deformation (<1% X_0 per layer, micrometer-scale deformation)

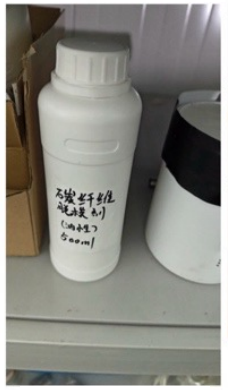




M55J prepreg



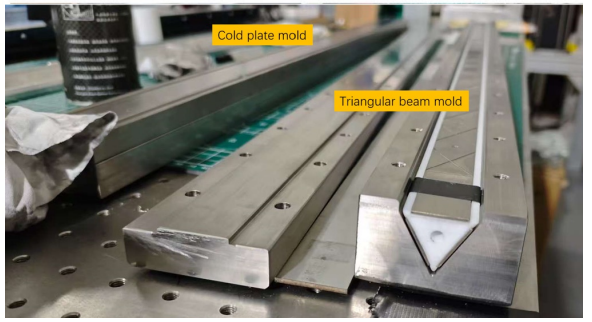
M55J carbon fiber



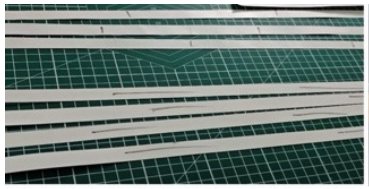
Resin and release agent



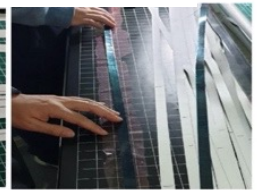
Oven



Custom hot-press molds



Prepreg cutting strips



Prepreg lay-up



Release-agent coating

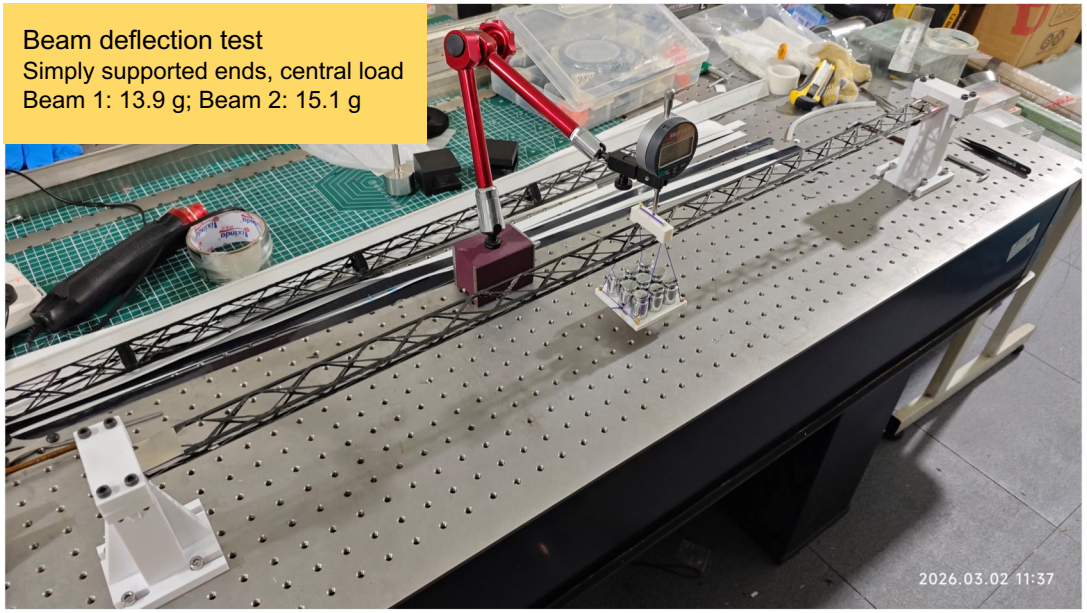


Molded samples

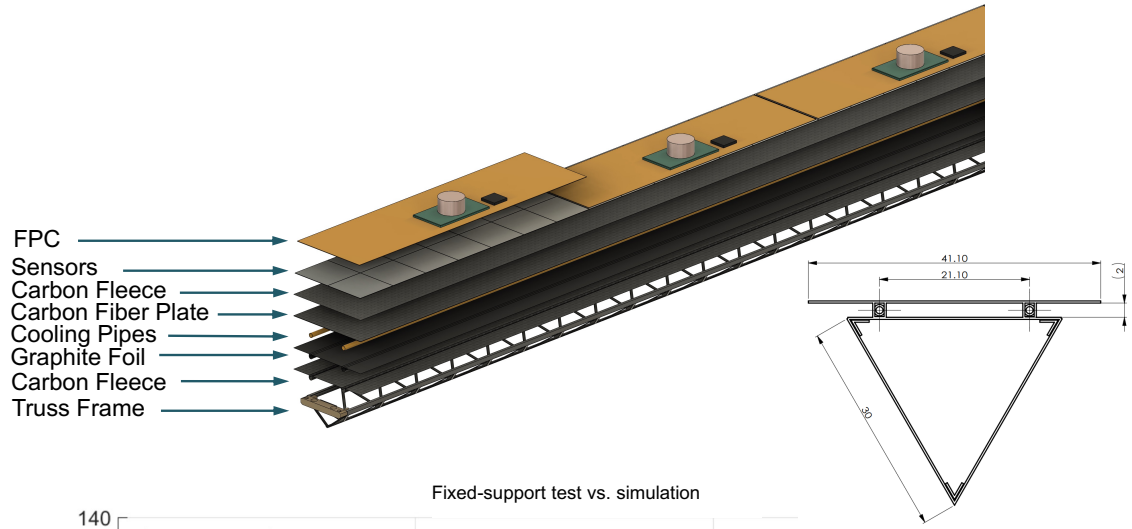
Engineering samples designed and fabricated by the team in 2026

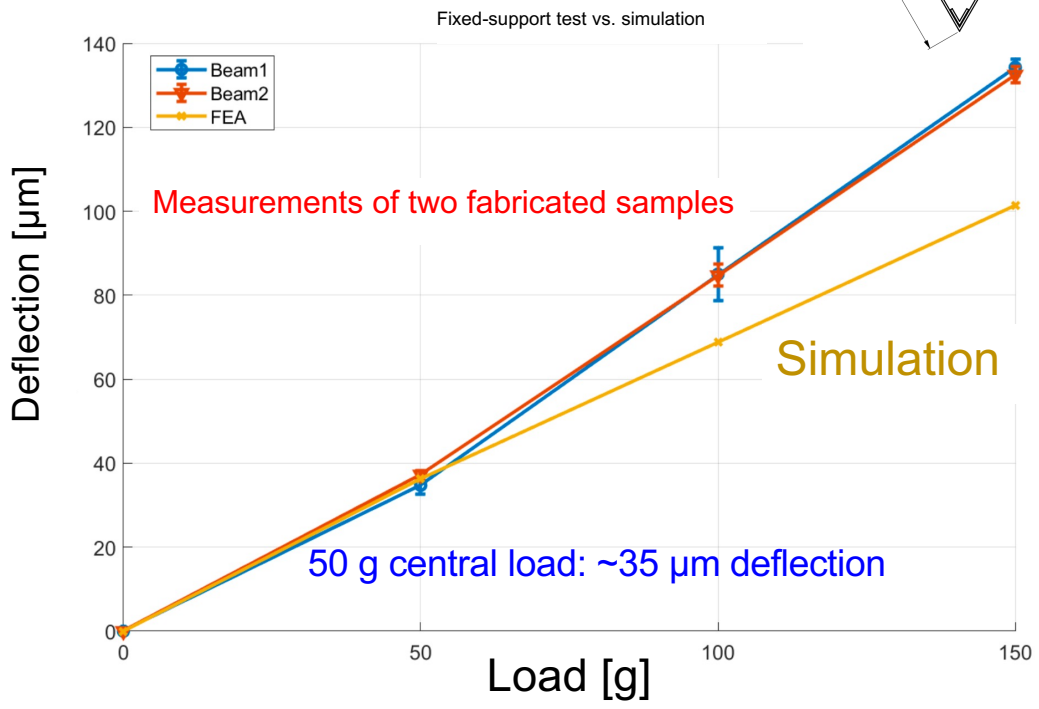
Carbon-Fiber Structures: Design and Validation

⇨ Modeling and simulation guide strucutre optimization. Mold and process studies cover high-strength prepreg lay-up, filament winding and integrated hot-press curing. Key challenges include high modulus, thermal-expansion matching across materials, flatness and demolding. Mechanical and optical measurements characterize performance, building capabilities from design and process development through validation.

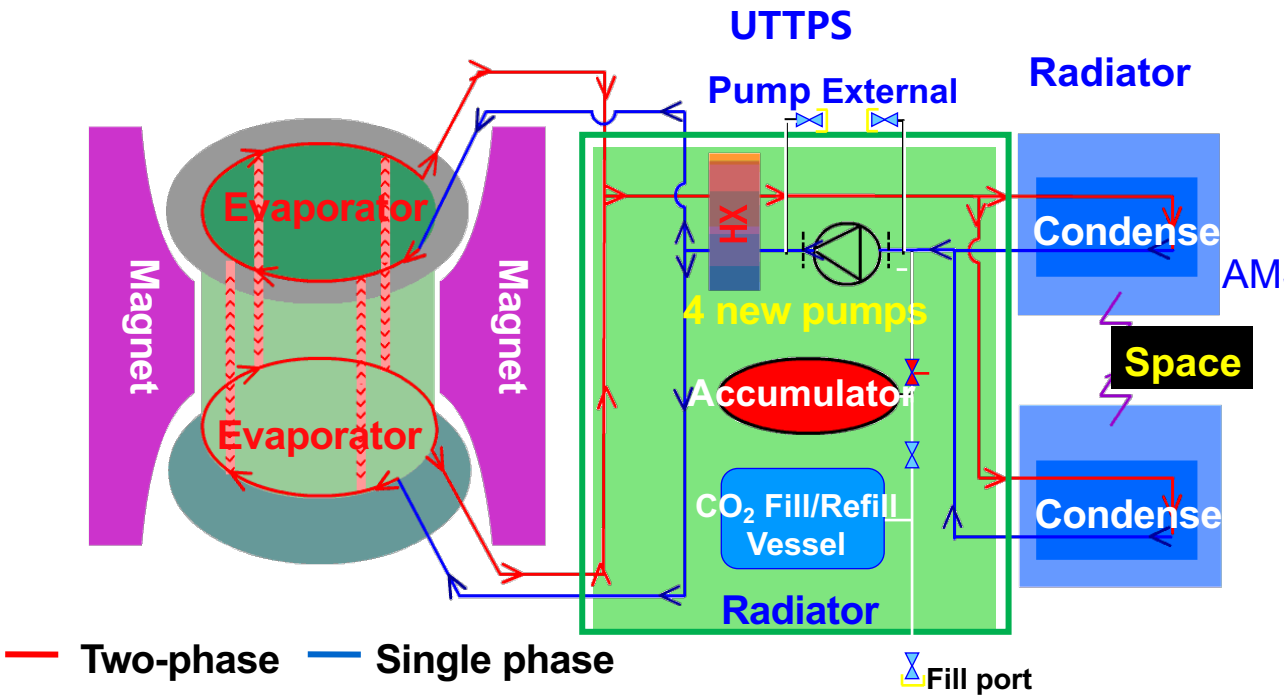


Load–deflection test of a custom 1 m carbon-fiber structure (15 g)

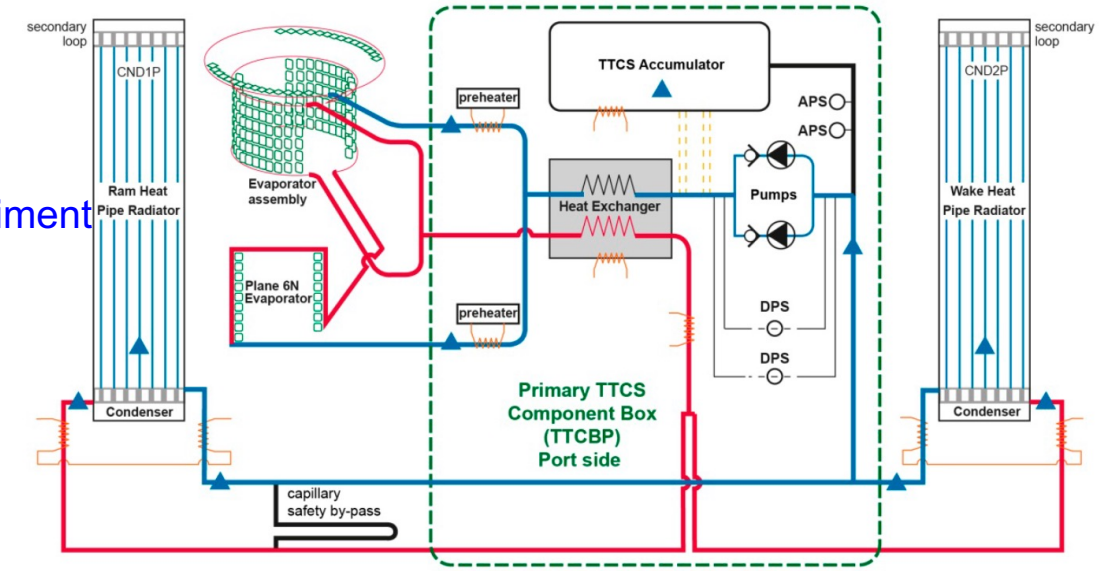




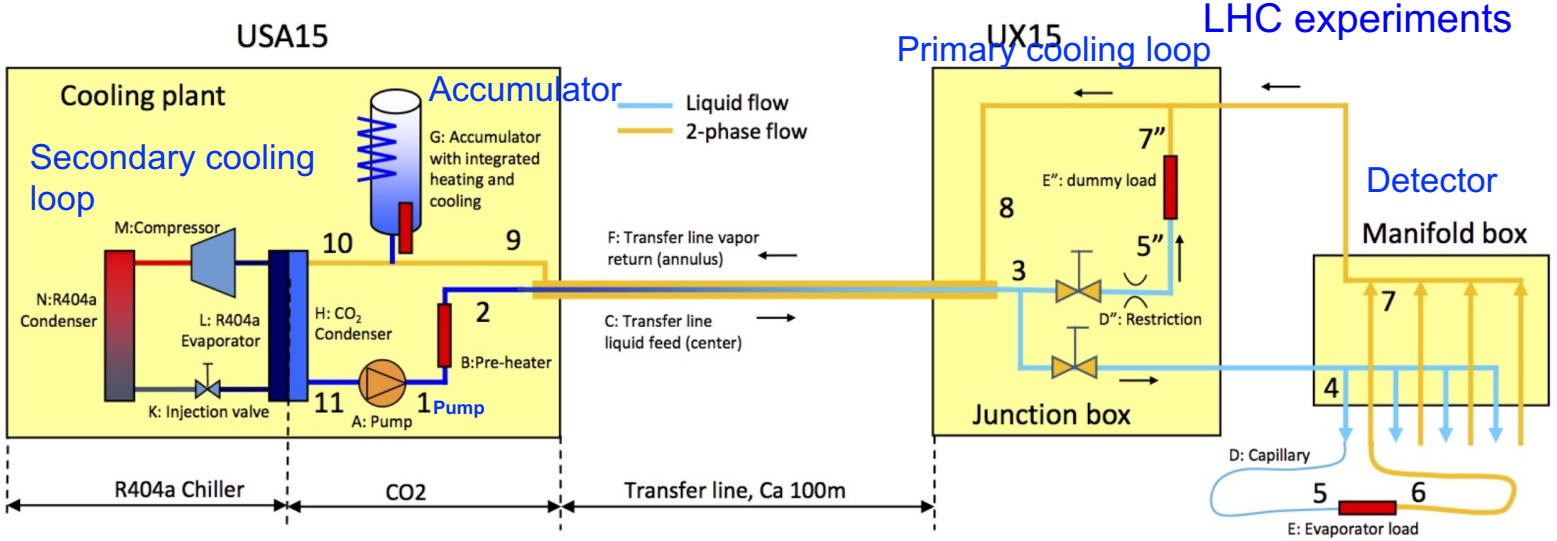
Two-Phase CO_2 Cooling for Tracking Detectors



AMS experiment



LHC experiments

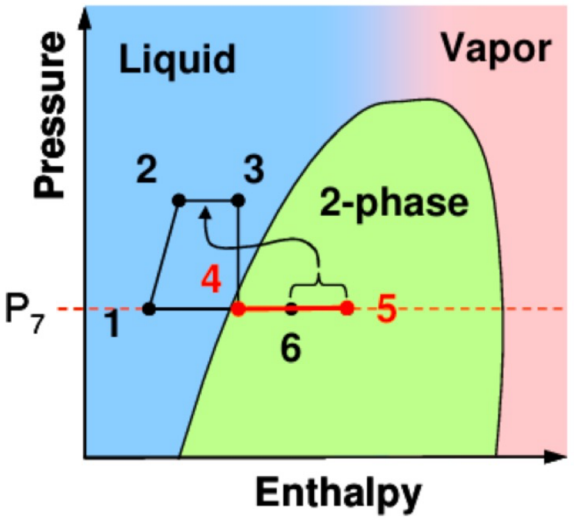


Two-phase CO_2 cooling is a key technology for semiconductor trackers. Beyond particle physics, it can also supports space payloads, electronics cooling, and heat removal from high-power-density systems.

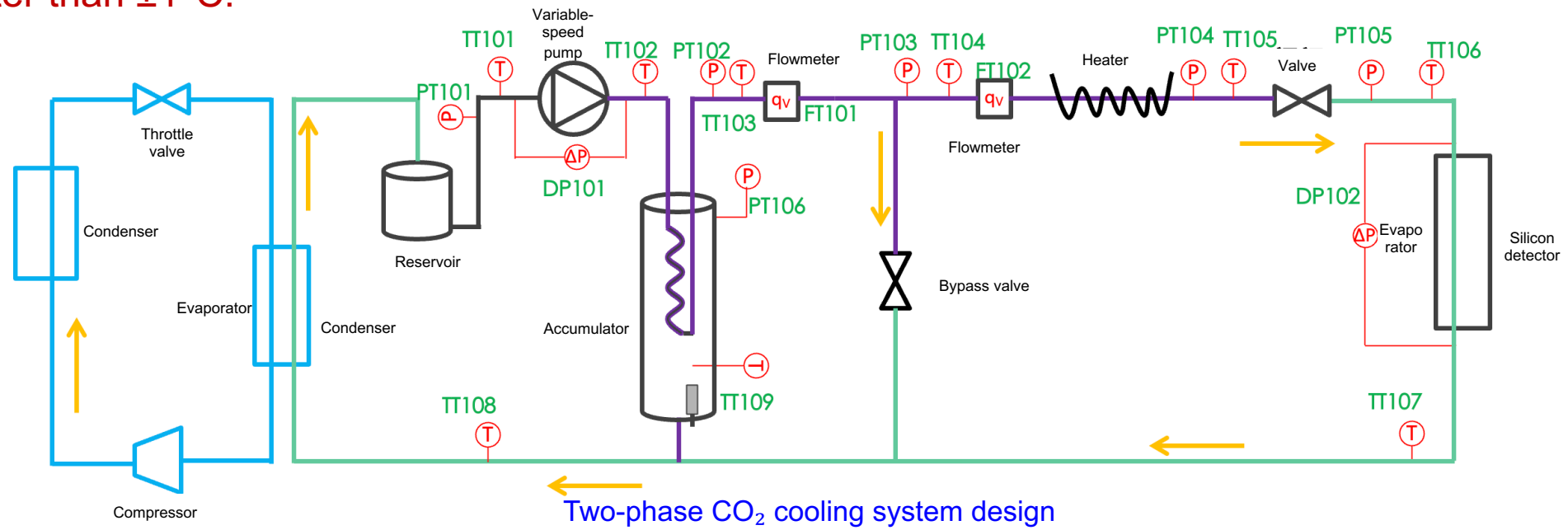
Two-Phase CO_2 Cooling System Development

Two-phase CO_2 cooling system

⇨ Low-temperature operation improves semiconductor detector SNR, making CO_2 an ideal coolant. With TIPC, we are developing a complete prototype for high-power tracking detectors. The compact, portable system provides ~1.2 kW cooling (upgradable to >2 kW), an adjustable temperature range of −40°C to 20°C, and temperature control better than ±1°C.



CO_2 pressure–enthalpy diagram

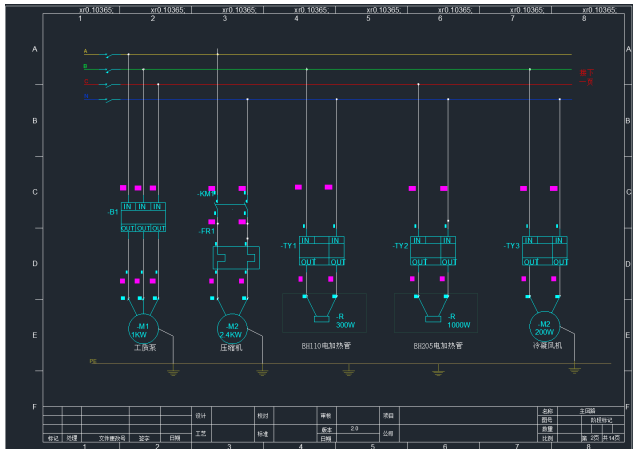
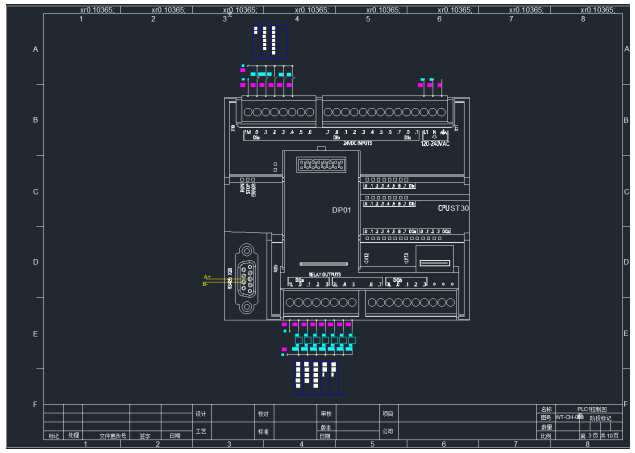
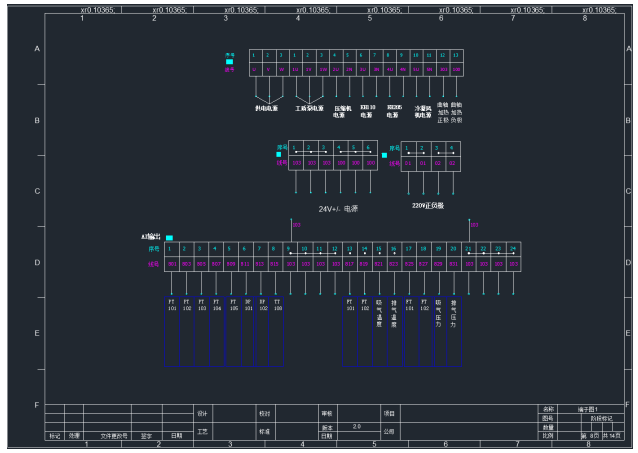
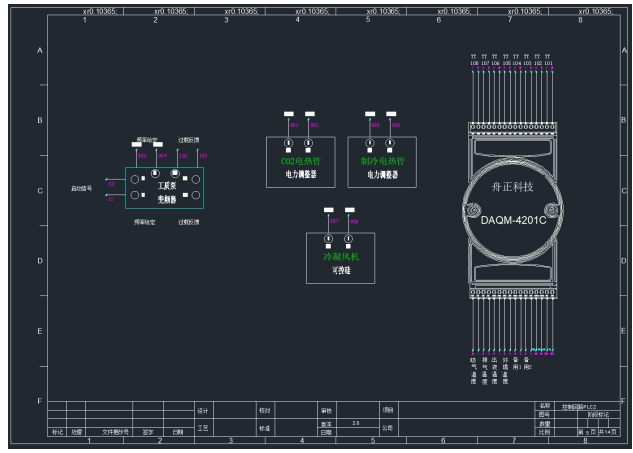


Two-phase CO_2 cooling system design

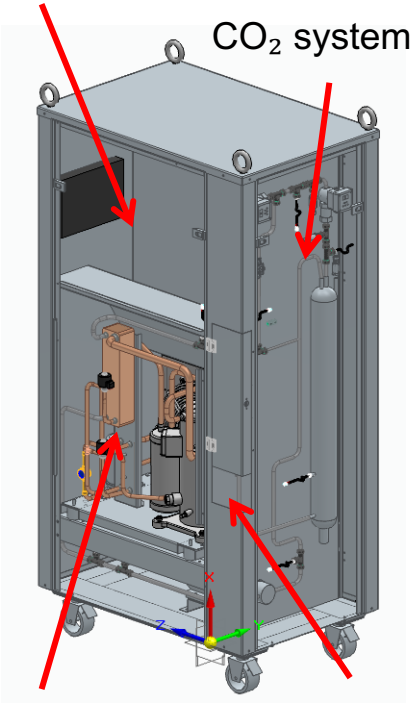
Instrumentation: 9 temperature, 7 pressure and 2 differential-pressure sensors, 2 flowmeters and 2 level sensors

This designed system can integrate with different thermal loads and experimental configurations. Its compact layout weighs about 100 kg and supports scaling to larger cooling systems.

➢ Electrical System Design

Control cabinet location



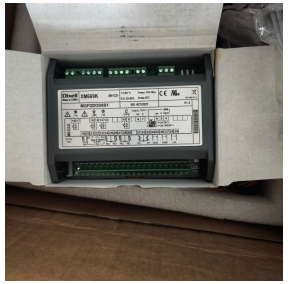
➢ Hardware components



Compressor



Plate heat exchanger



Expansion-valve driver



R404A filter



R404A sight glass



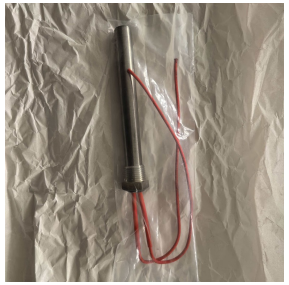
Oil separator



Vapor-injection valve driver



Temperature sensor



Heater rod



Pressure sensor



CO_2 filter



Differential-pressure sensor

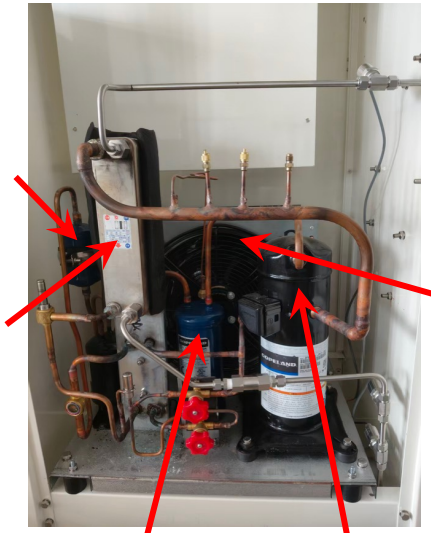


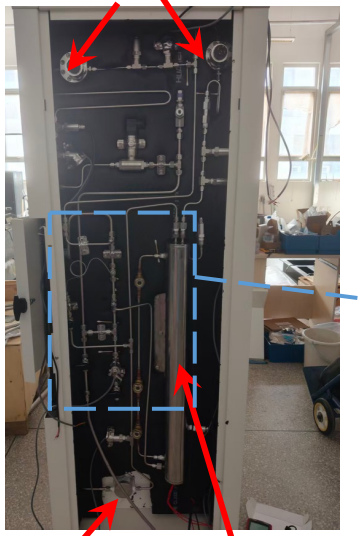
Flowmeter

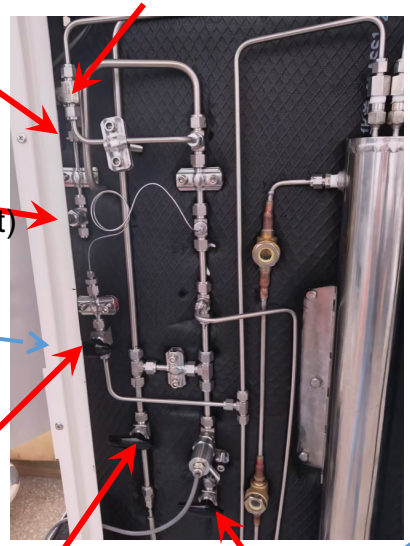


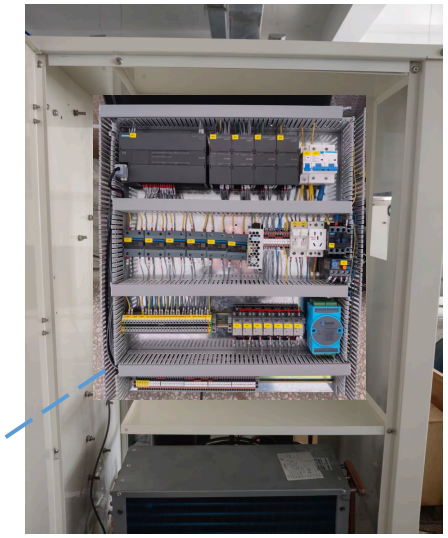
CO_2 sight glass

➢ Two-Phase CO_2 Cooling System Assembly









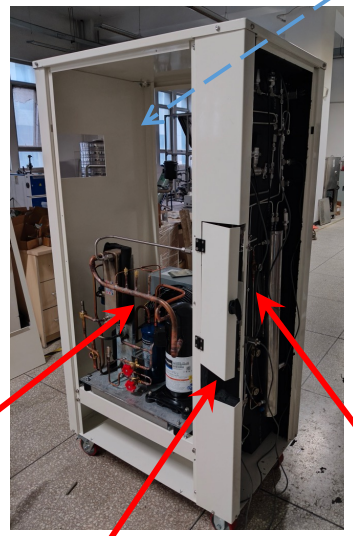
Two-phase CO_2 system assembly

Silicon detector thermal-load test system

Commissioning

Full CO_2 cooling system integration is underway. Operation and commissioning are planned for November 2026.





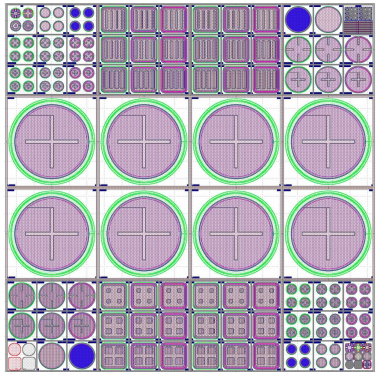


Core R&D: Sensors and ASICs

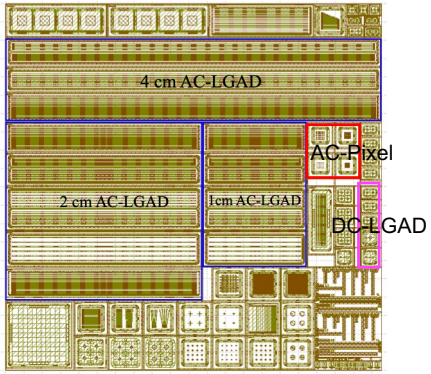
Sensor and ASIC Development

- A silicon-led semiconductor detector with coordinated development across multiple materials
- Cover the full R&D chain: processes, design, testing, analysis and system integration

SiC sensors

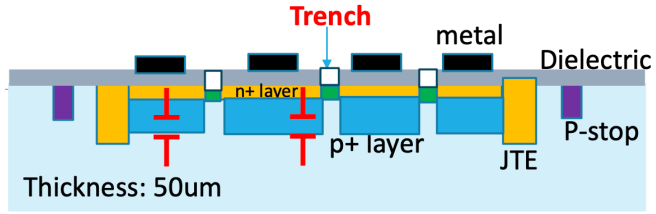


Silicon LGAD sensors



Larger sensors, higher performance and lower power

- The next sensor tape-out will reduce capacitance to meet large-area, high-precision and low-power requirements.



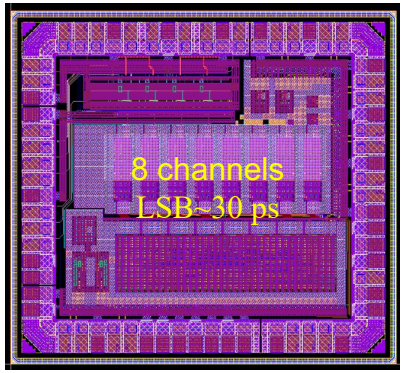
Trench isolation structure

$$C = \varepsilon_0 * \varepsilon_r * A \downarrow / d$$

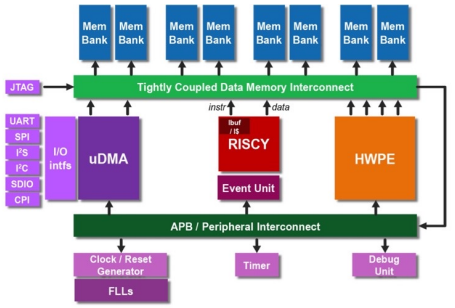
Precision LATRIC readout ASICs

- Design of the 32-channel LATRIC2 is being planned. The high-performance radiation-hard RISC-V SoC HERIS-V2 targets design completion and tape-out submission by January 2027.

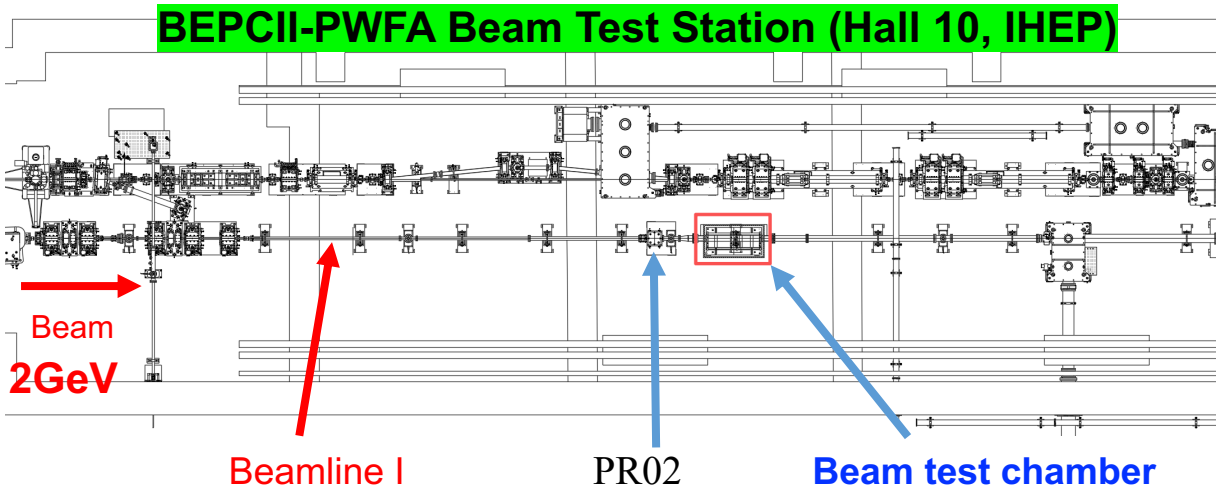
LATRIC1

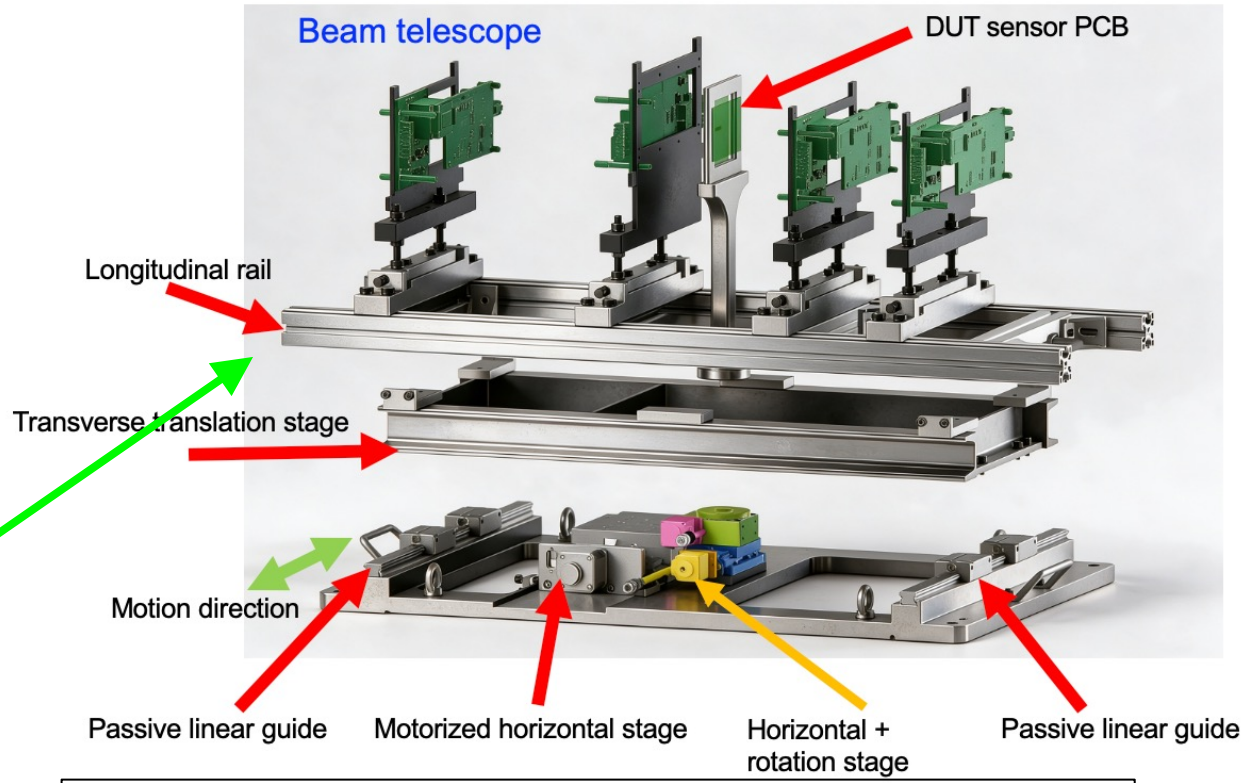


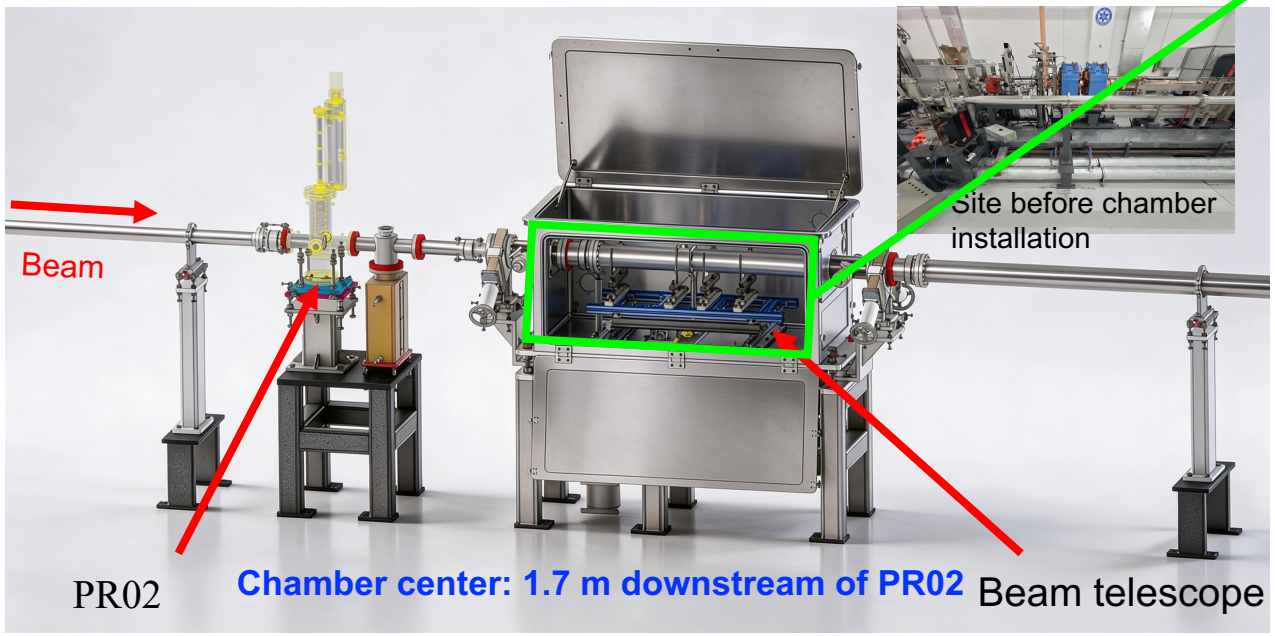
HERIS-V2 SoC core architecture



Construction of BEPCII-PWFA Beam Test Station (BII-PBTS)







With no suitable domestic high-energy beam test station available, the team is now leading the development of BEPCII-PWFA BT station (IHEP)

- Beam energy: 2 GeV
- Beam test chamber: operation planned in January 2027
- Full beam tests of sensor/ASIC telescope system are planned for January–February 2027 at the new BII-PBTS station.

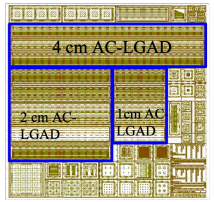
Summary

- Engineering prototypes drive the development of the first 4D tracking detectors, spanning advanced sensors, dedicated readout electronics, mechanics, cooling, and system integration, to advance semiconductor detector technologies.

- Together, our efforts aim to establish a comprehensive development pathway, strengthen engineering capabilities, and build the expertise needed for China's next-generation particle-physics detectors.

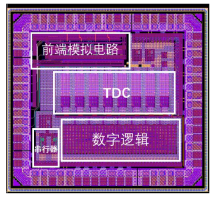
Developing Advanced Silicon Tracker Detector System

Sensor



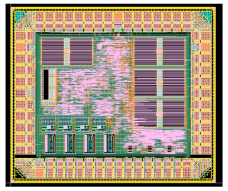
The first sensor with 10 μm position resolution and ≤40 ps timing resolution

ASIC



The ASIC with high timing precision (≤30 ps) and high spatial resolution

SoC



The first RISC-V SoC dedicated to HEP applications (taped out in 2025)

DAQ



DAQ system

Mechanics



The first carbon fiber truss manufactured at IHEP in 2026

Cooling System



The first two-phase CO_2 cooling system

- Semiconductor detector development requires specialized expertise and sustained commitment. We welcome interested institutions to join us in advancing semiconductor detector technologies.

- We also welcome opportunities to support the heavy-ion physics community and others by contributing to the development of advanced sensors, electronics (including readout ASICs), mechanical structures, cooling systems, and system integration.

Thank you!

PAIRS COLLABORATION

Precision and Advanced semiconductor detectors with Integrated high-performance Readout and Systems

Zhengze Chang, Jiaolong Chen, Siyu Chen, Yuxin Cui, Mingzheng Ding, Jie Du, Chengdong Fu, Chenxi Fu, Yongshuai Ge, Dizhou Guo, Kun Hu, Yuqiang Hu, Wentao Jia, Hui Jiang, Xiaoping Jing, Dazhang Li, Gang Li, Xiaoting Li, Ziyao Li, Baiqi Liu, Boxuan Liu, Lei Liu, Zeyu Liu, Shoudong Luo, Cai Meng, Xiaohui Qian, Rui Qu, Haoyu Shi, Xin Shi, Xueyan Shi, Jiajian Teoh, Chuanye Wang, Congcong Wang, Kaining Wang, Wenjing Wang, Yiwei Wang, Zhenyu Wu, Gaobo Xu, Xiongbo Yan, Junling Yang, Jingbo Ye, Yunkai Yue, Xiyuan Zhang, Yihan Zhang, Zhentao Zhang, Zhihang Zhang, Mei Zhao, Xuhang Zhao, Zhanhong Zhao, Jiaqi Zhou, Junjian Zhou, Ningchuang Zhou, **Qi Yan***

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