Development of a MAPS Based Inner Tracker for STCF

Lailin Xu
University of Science and Technology of China
On behalf of the STCF ITKM group (USTC, CCNU, SDU, NPU, AUST)

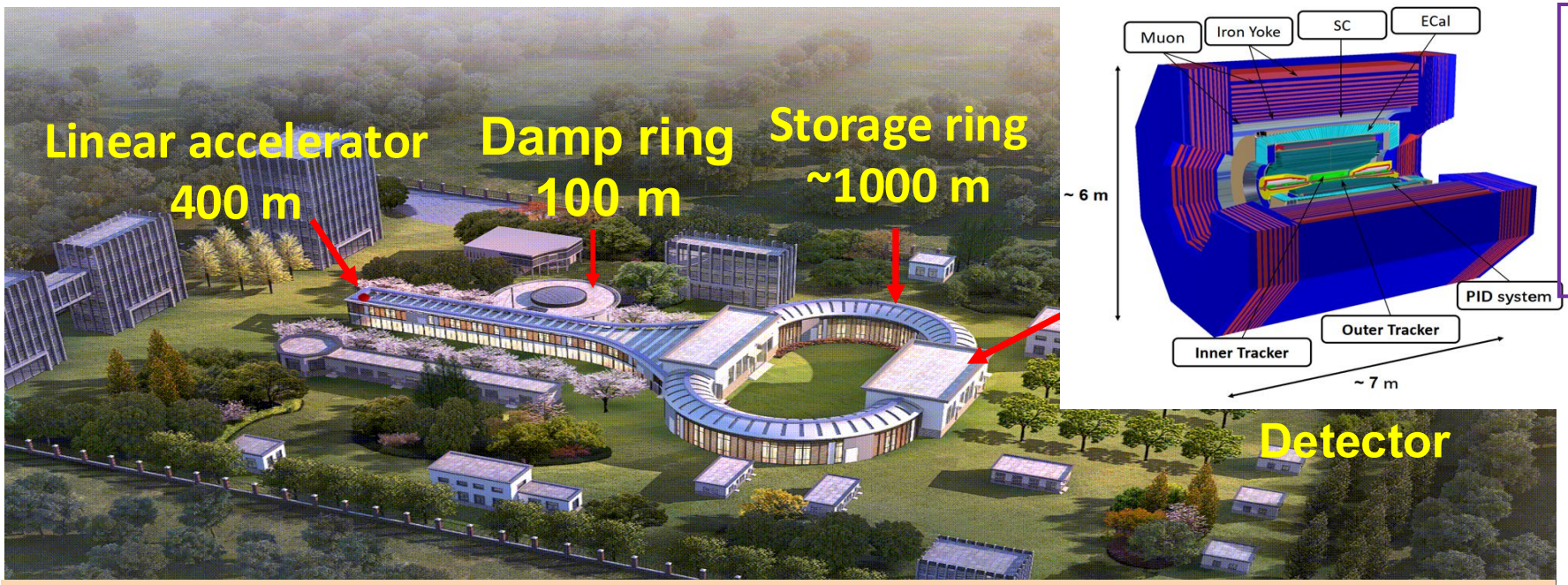
Mini-Workshop on AC-LGAD and Its Applications
Nov 9-11, 2026, Dalian

超级陶粲装置
Super Tau-Charm Facility

Outline

- Introduction to STCF and the inner tracker
- CharTPix protypes R&D
  - Simulations
  - CharTPix_180A: small protypes with high-resistivity epi wafers
  - CharTPix_130: super-pixel readout
  - CharTPix_180B: depleted MAPS with modified process
- Summary

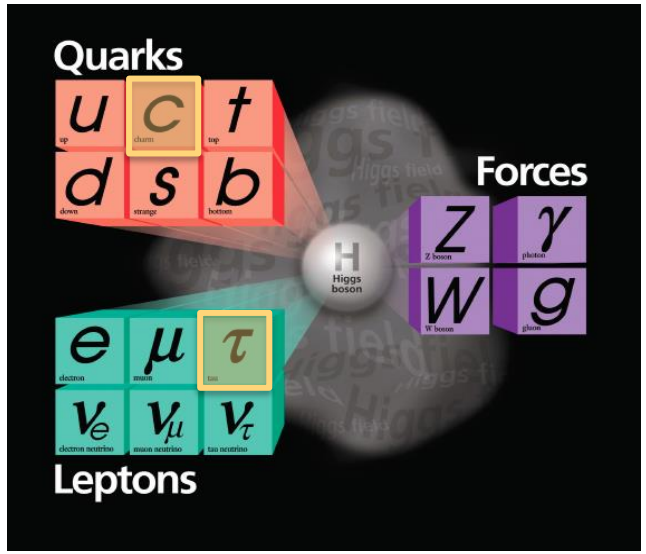
Super Tau Charm Facility (STCF)



Detector

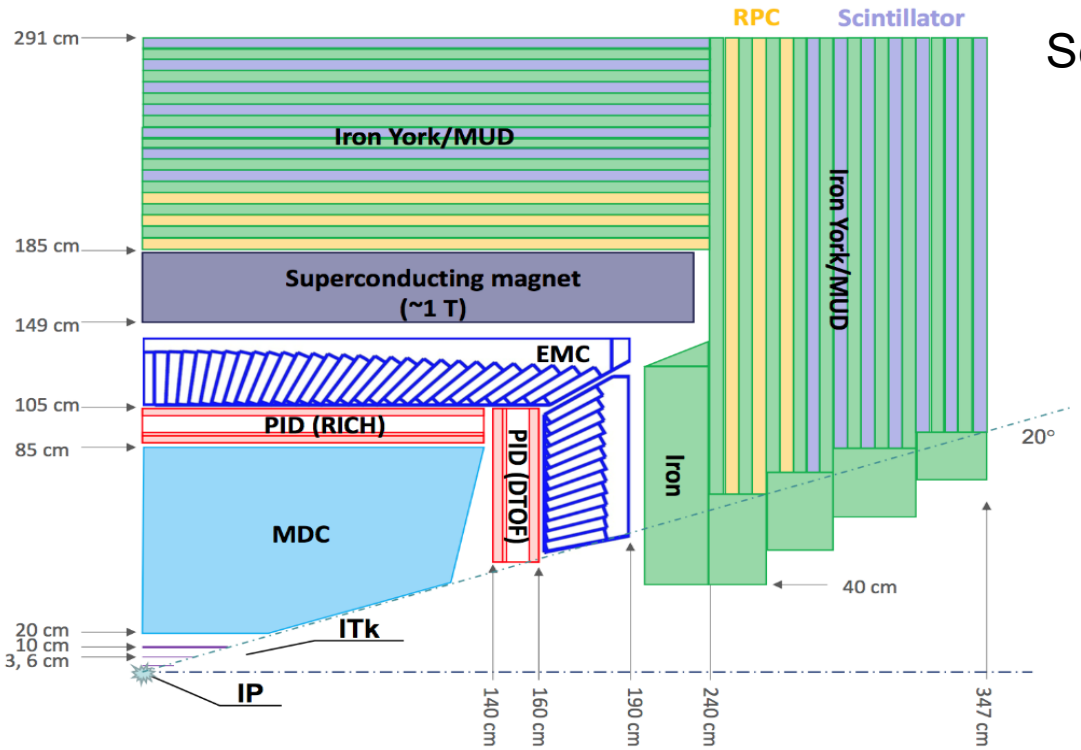
A next-generation high-luminosity e^+e^- collider operating in the $\tau - charm$ energy region

- Energy range: E_{cm} = 2-7 GeV
- Peak luminosity >0.5×10^{35} cm^{-2} s^{-1} at 4 GeV
- Potential for an upgrade to increase lumi. and realize polarized beam



- 1 ab^{-1} data expected per year
- Generate an unprecedentedly large number of τ leptons, particles made of c quarks
- Important playground for study of QCD, exotic hadrons, flavor and search for new physics

Conceptual design of the STCF detector



Solid angle coverage: 93%·4π (polar angle: 20°~160°)

Inner tracker(ITK)
- <0.35%X_0/layer
- σ_{xy}<100 μm

Main drift chamber(MDC)
- σ_{xy} < 130 μm
- σ_p/p~ 0.5% @ 1GeV
- dE/dx ~ 6%

FRONTIERS OF PHYSICS

REPORT
Volume 19 / Issue 1 / 14701 / 2024

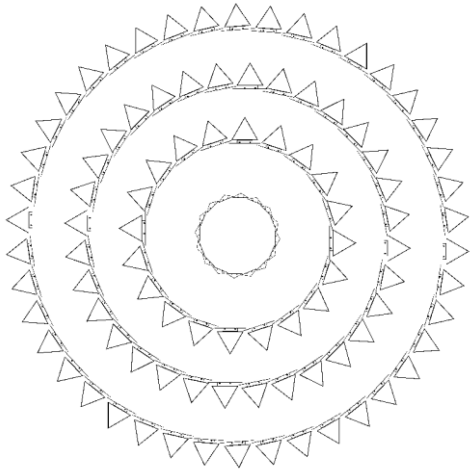
STCF conceptual design report (Volume 1): Physics & detector

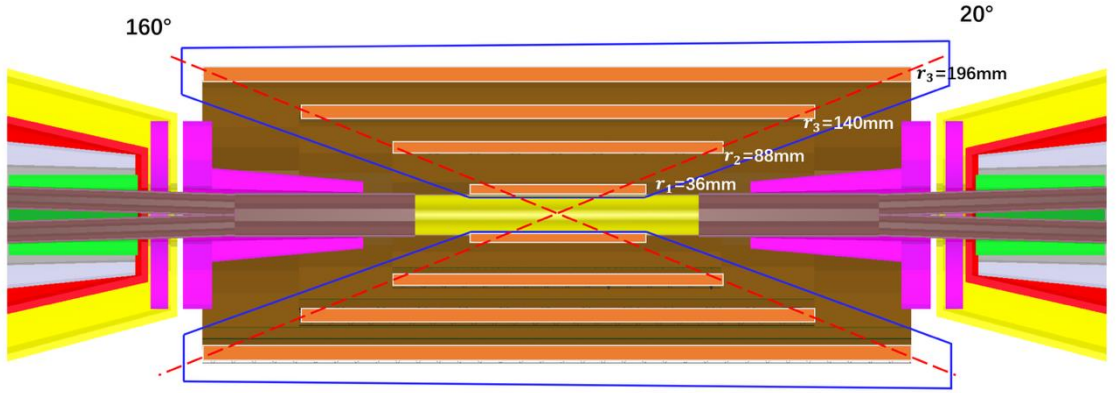
Front. Phys. 19, 14701 (2024)

Process	Physics Interest	Optimized Sub-detector	Requirements
$\tau \to K_s\pi\nu_\tau$,	CPV in τ sector,		acceptance: 93% of 4π; trk. effi.:
$J/\psi \to \Lambda\bar{\Lambda}$,	CPV in hyperon sector,	Tracker	> 99% at p_T > 0.3 GeV/c; > 90% at p_T = 0.1 GeV/c
$D_{(s)}$ tag	Charm physics		σ_p/p = 0.5%, $\sigma_{\gamma\phi}$ = 130 μm at 1 GeV/c

Conceptual design of the MAPS tracker

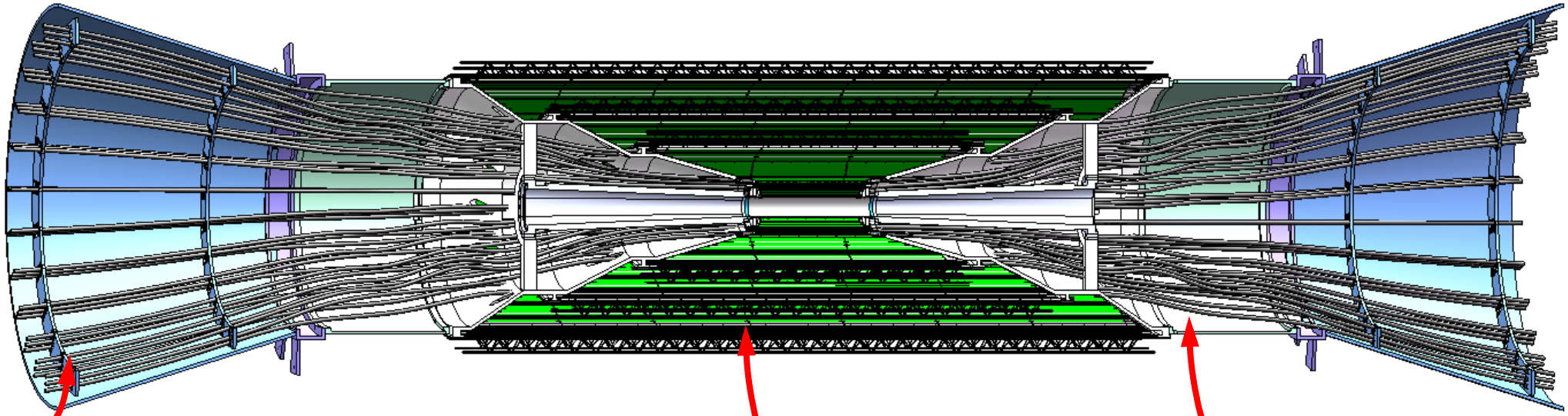
- To meet the physics requirements of the STCF Inner Tracker:
  - Tracking efficiency: >99% @ $p_T > 0.3\ GeV$; >90% @ $p_T > 0.1\ GeV$
- Low material budget is essential
- A preliminary design of the MAPS based Inner Tracker (ITKM)
  - Four layers of silicon pixel detectors
  - Acceptance: polar angle of 20º~160º
- Total area: 2.5m^2

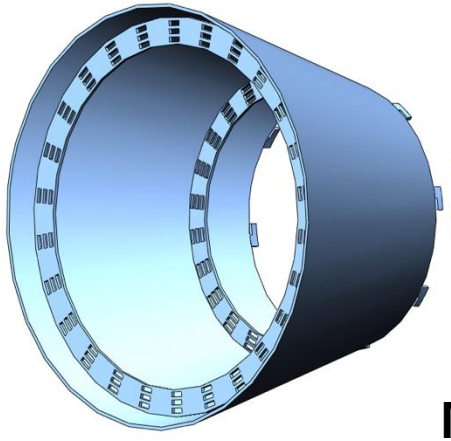


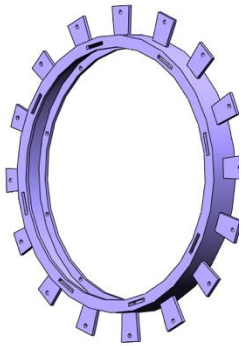


Layer	Radii (mm)	Length (mm)	Stave No.	Area (cm^2)
1	36	250	12	576
2	88	510	15	3000
3	140	800	24	7488
4	196	1100	32	13824

Mechanical design of STCF ITKM

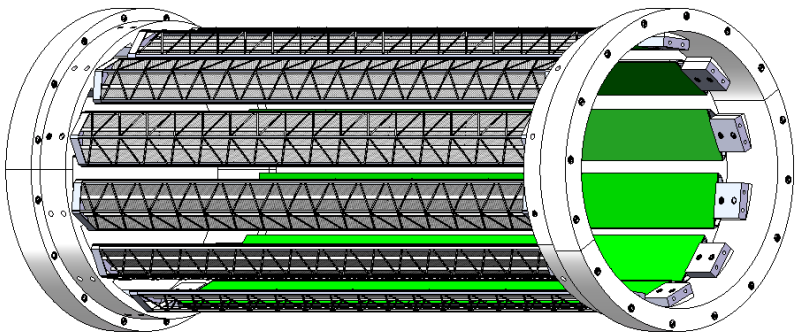






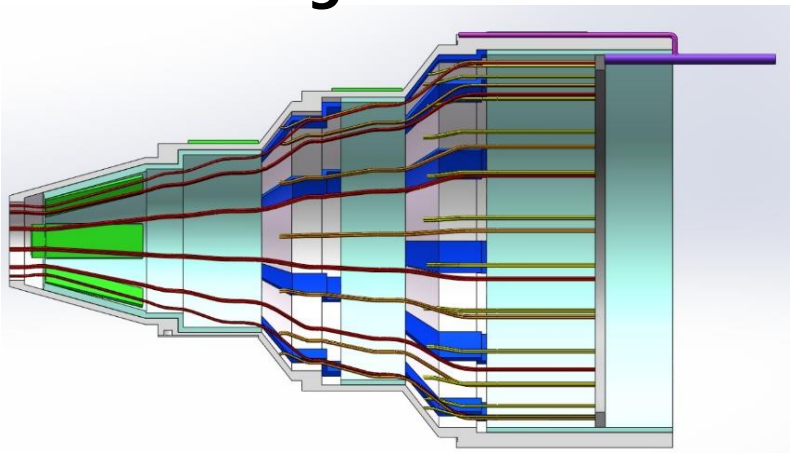
Service support

MDC connection



Inner stave

Water cooling

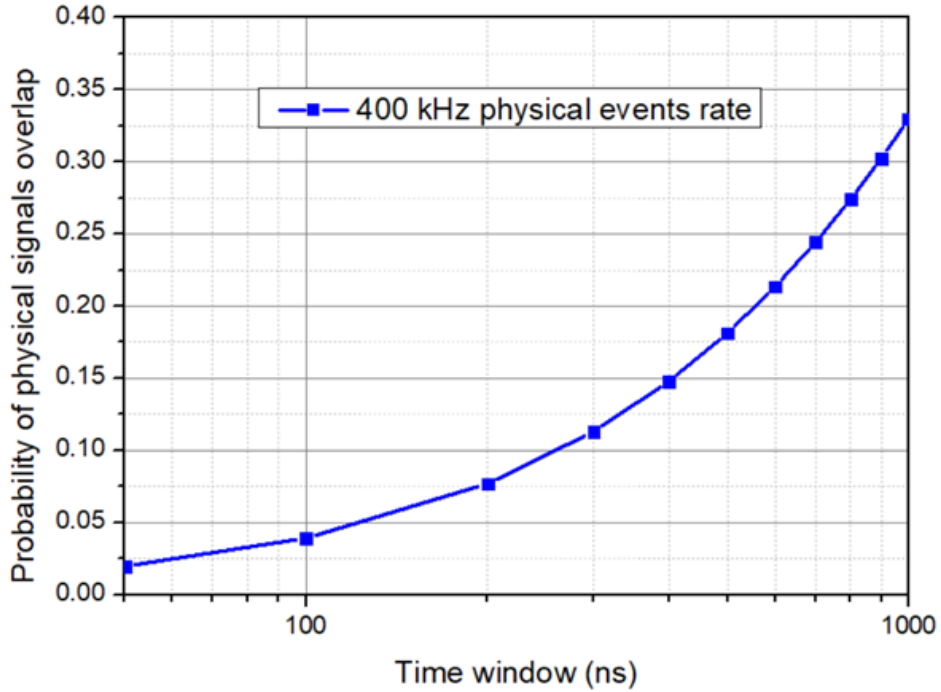


MAPS design targets

- Requirements on the STCF MAPS
  - Power consumption: $\leq 100mW/cm^2$ (targeting $50mW/cm^2$)
  - Material budget per layer: $\leq 0.35\%\ X_0$
  - Spatial resolution: $\leq 30\mu m$
  - Time resolution: $\leq 20\mathrm{ns}$ (to deal with the pileup issue at high luminosity)
  - Hit rate capability: $\geq 1\mathrm{MHz}/cm^2$
  - TID >1 Mrad/year, NIEL >1×10^{11} 1MeV n_{eq}/cm^2/year
  - Time-over-threshold (TOT) measurement:
    - Time-walk correction
    - Correction of multi-coulomb scattering in track finding

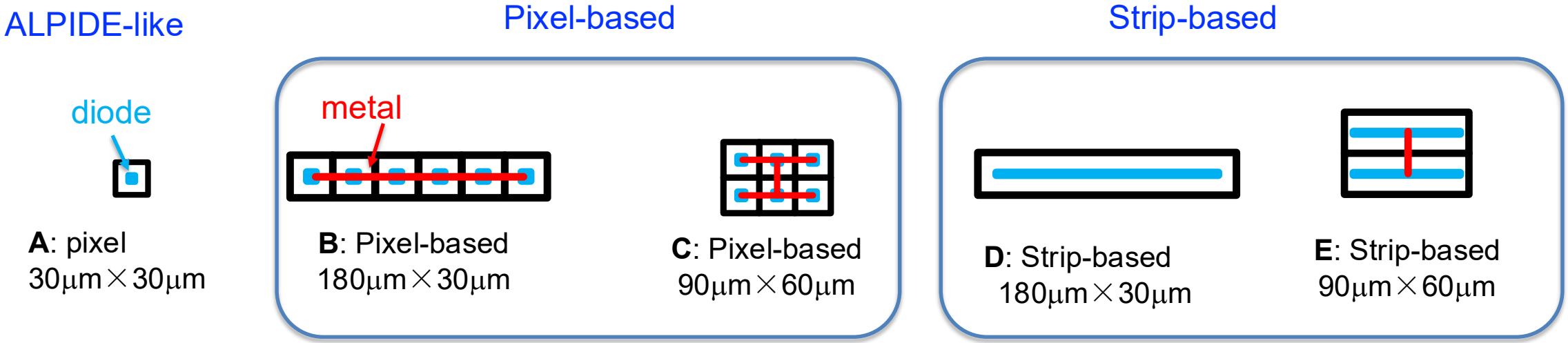
No existing MAPS could satisfy the STCF requirements! → dedicated R&D needed

Probability of pileup(with an event rate of 400 kHz @ J/ψ, bunch crossing of 4ns):
- 4% within 100ns
- 8% within 200ns



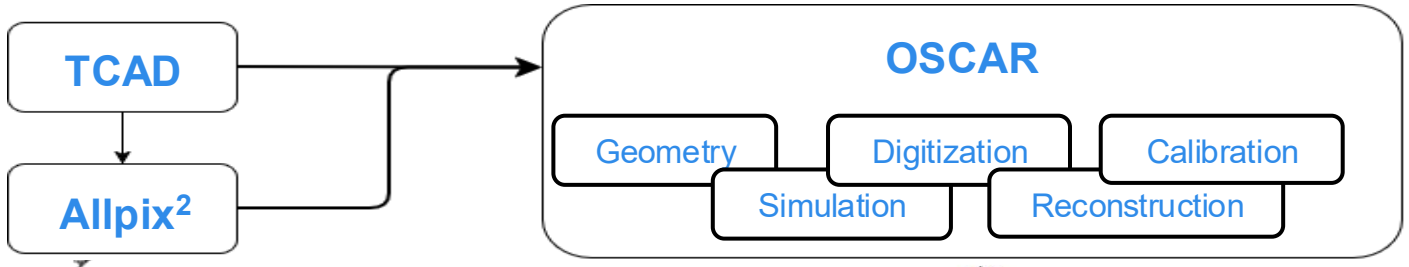
CharTPix sensor concept

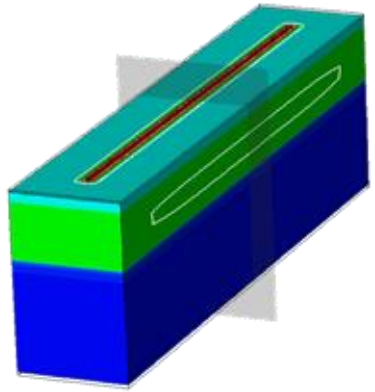
- Pixel size considerations
  - Higher priority on the power consumption than the spatial resolution → larger pixel size to reduce the power consumption density
  - Three different designs
    - Pixel-based: analog connected small pixels ($1\times6 \rightarrow 1, 2\times3 \rightarrow 1$) using metal lines
    - Strip-based: extended diode size in one direction
    - Superpixel based: digital connected small pixels



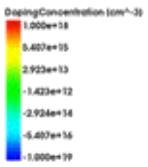
STCF ITKM simulation

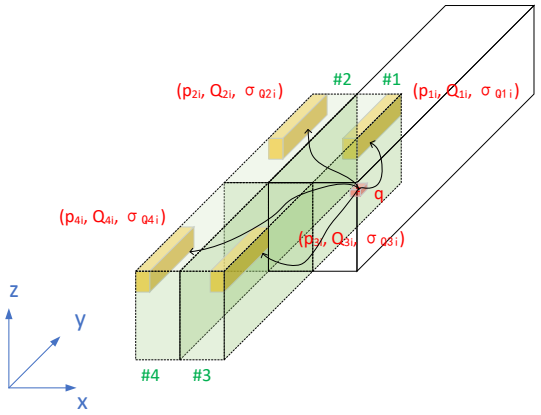
- TCAD+Allpix2: Sensor modelling for process and geometry optimization
  - Baseline sensor plan: 170 μm×30 μm sensor with HR epitaxial layer
- Simulation workflow in the Offline software framework for STCF (OSCAR):
  - Two simulation methods: Propagation-level full sim; LUT-based fast sim
  - Digitization: Time & Charge (ToA & ToT)

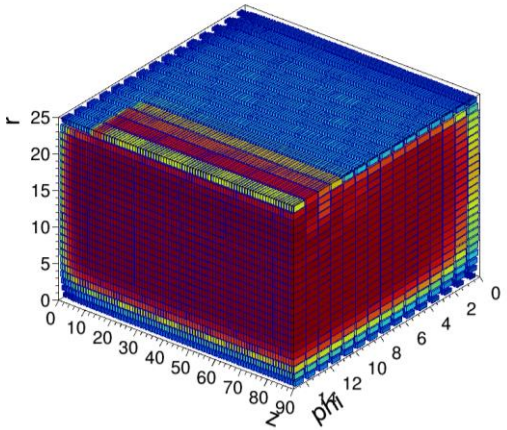




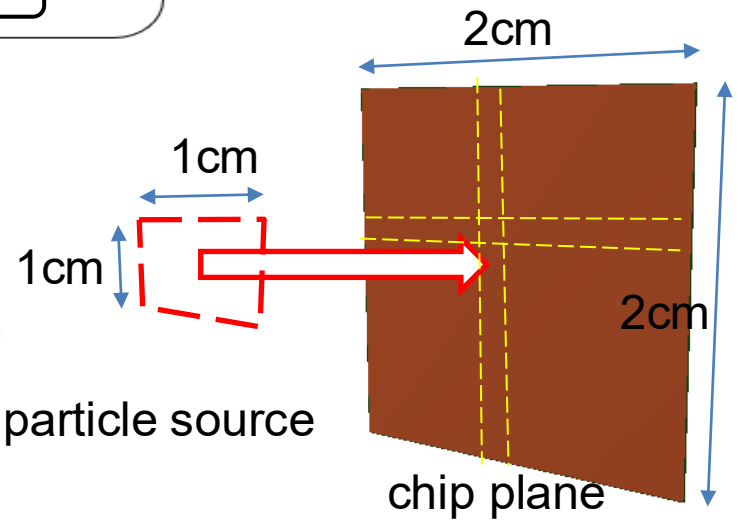
Baseline sensor design







Digitization with look-up tables

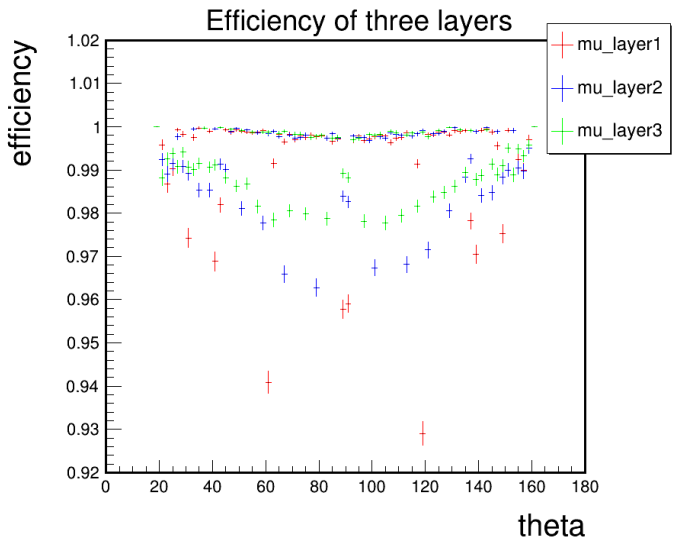


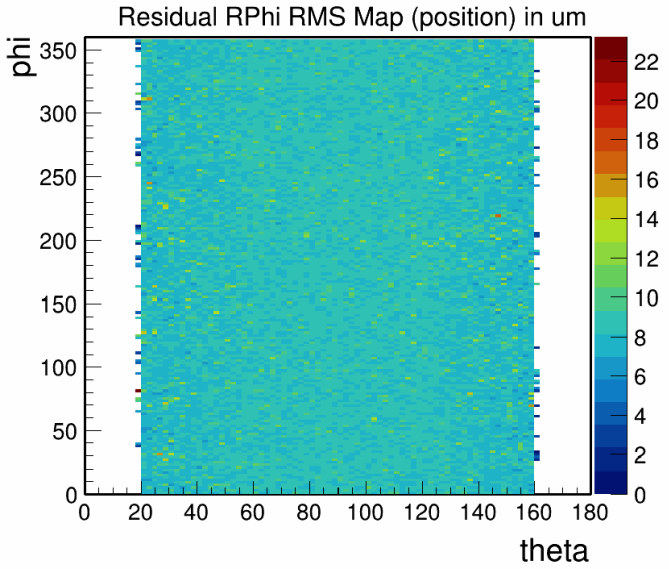
STCF ITKM simulation

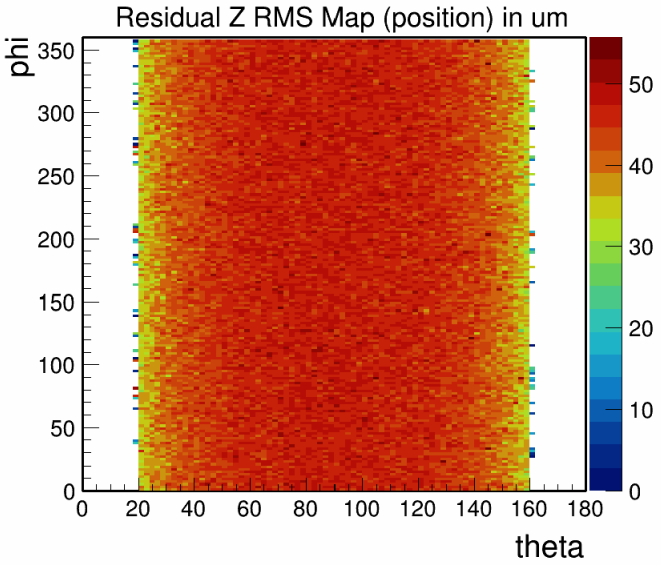
- Pixel type:
  - CharTPix_180A, 170μm×30μm, strip-based
- Simulation settings:
  - 1GeV μ^-, θ range 20°-160°
  - Pixel threshold: 300e

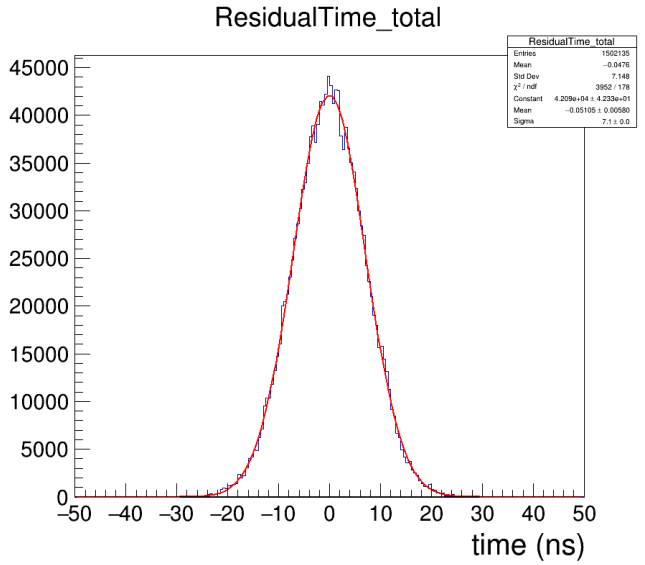
✓ Average detection efficiency 99.2%
✓ Position resolution: $\sigma_z = 33.5\mu m$, $\sigma_{rphi} = 6.8\mu m$
✓ Time resolution (sensor only) 7.1ns

A MAPS based Inner Tracker can meet the physics requirements of STCF







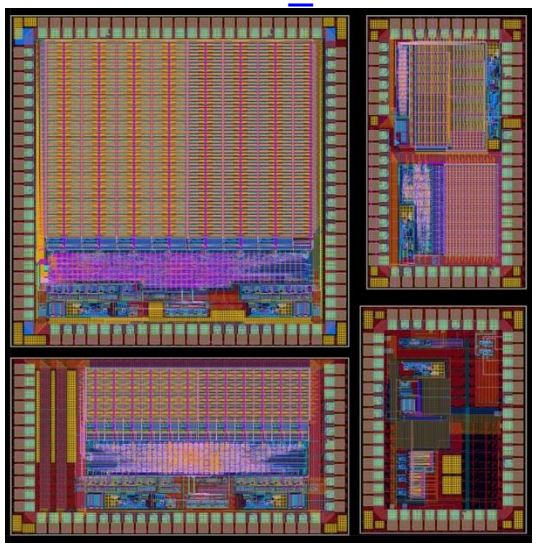


CharTPix protypes

180nm process

- Low res substrate + high res (>$1\mathrm{k}\Omega \cdot \mathrm{cm}$) EPI (standard process)

CharTPix_180A



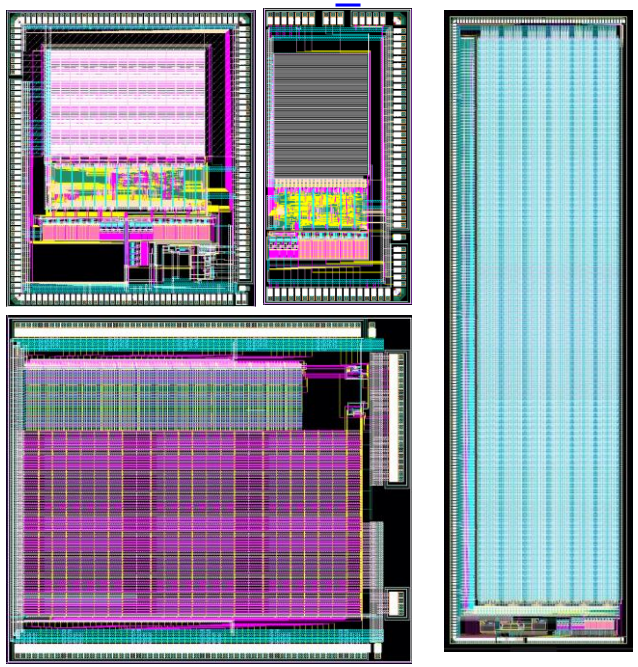
Submitted in March 2024
Chip returned in Dec 2024

2nd version returned Sept 2026

130nm process

- High res substrate, no EPI

CharTPix_130

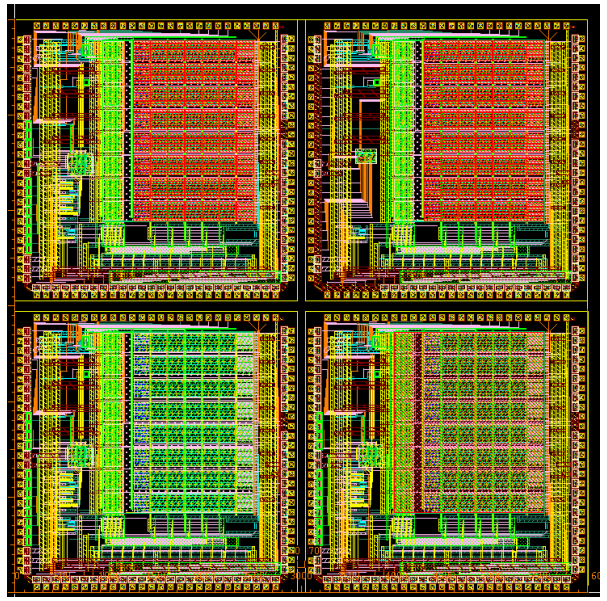


Submitted in September 2024
Chips returned in May 2025

180 nm process (Modified)

- High-resistivity EPI + N-blanket

CharTPix_180B

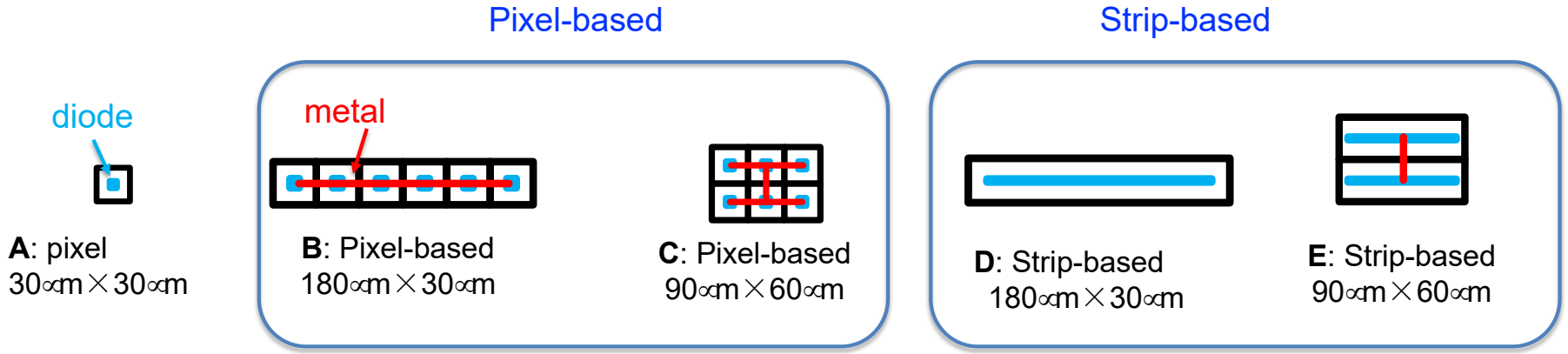


Chips returned in Oct. 2025

CharTPix_180A v1

Nucl. Instrum. Meth. A 1080 (2025) 170725

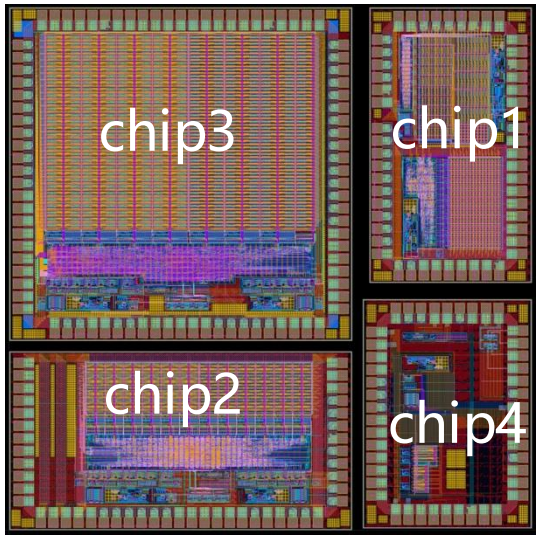
- To explore different sensor geometries & charge collection diodes



Four flavors of prototype chips:

- **Chip1**: Small pixel, no timing
- **Chip 2 & 3**: Enlarged pixel size, timing with ToA & ToT
- **Chip 4**: Analog readout for sensor performance comparison

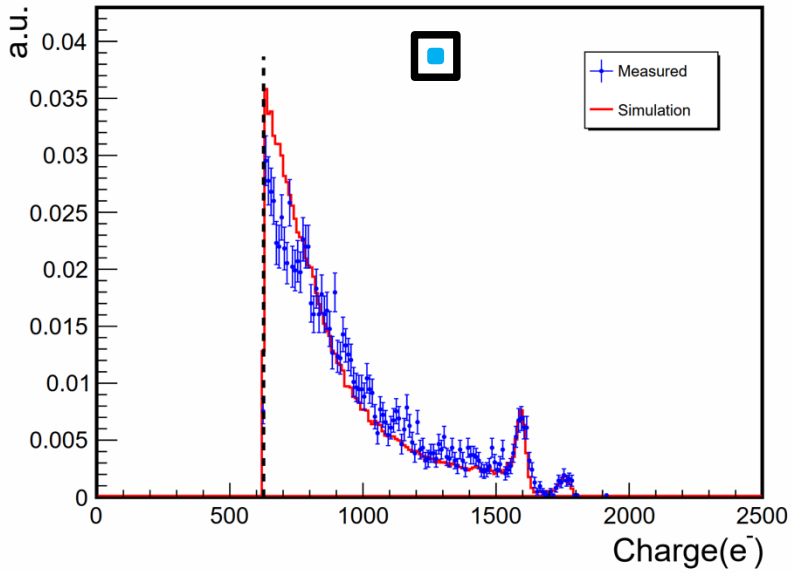
	Chip1	Chip2		Chip3		Chip4
Pixel size (μm×μm)	28.1x30.1	96.4x59.6		170.0x31.0		Mixed
Sensor	ALPIDE-like	Strip-based	Pixel-based	Strip-based	Pixel-based	Mixed
Pixel array	16x30	8x12	8x12	60x8	60x7	Mixed
Readout	Token	Token		Token		Analog readout
ToA & ToT	X	√		√		X

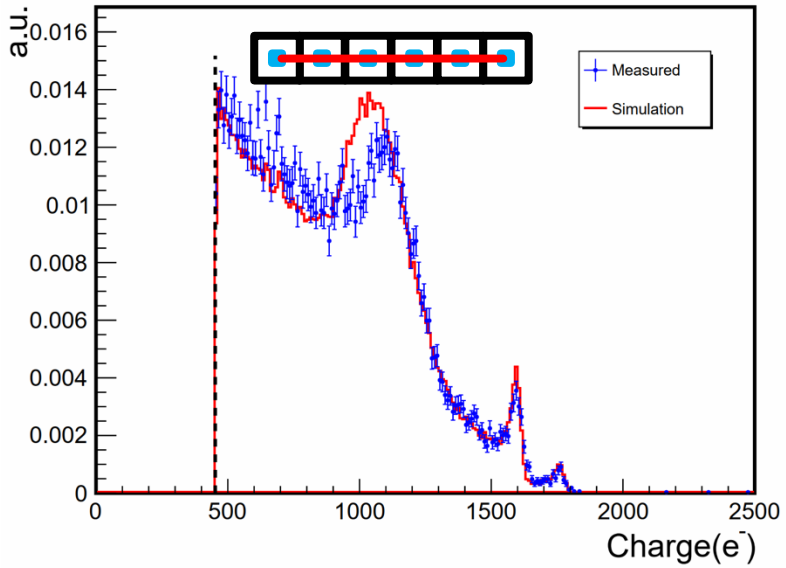


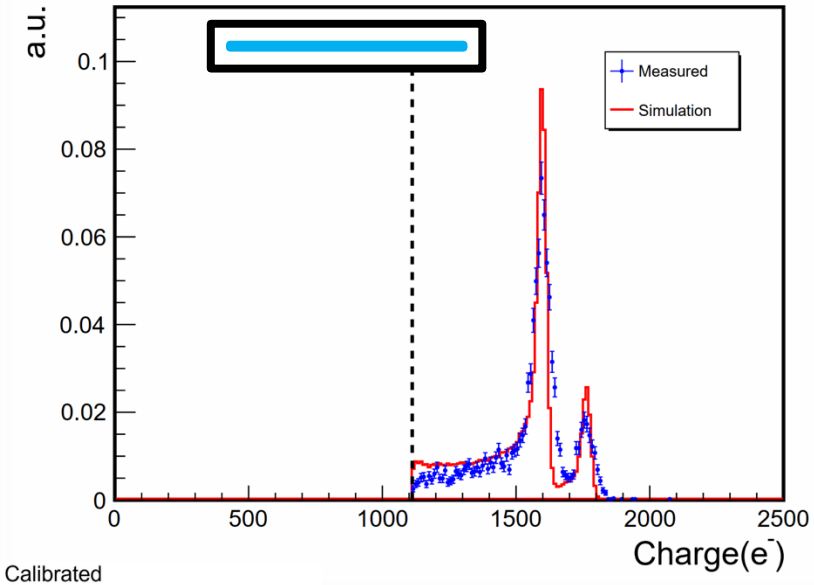
Total area: 5 mm×5 mm

CharTPix_180A v1 test results

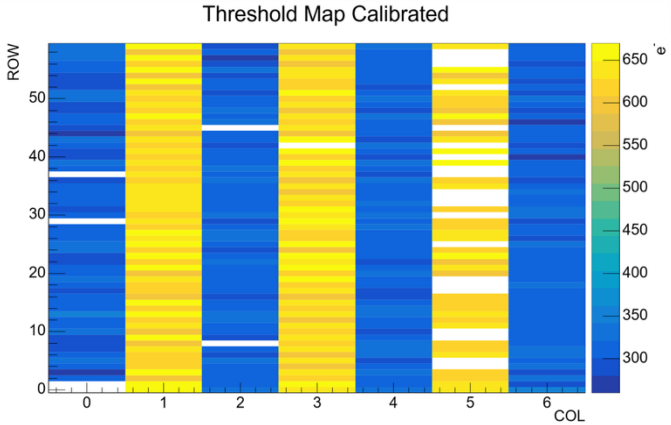
- 3T sensor tests using Fe-55 X-ray
  - The active-connect sensor with HR epi. layer features the best charge collection ability as expected







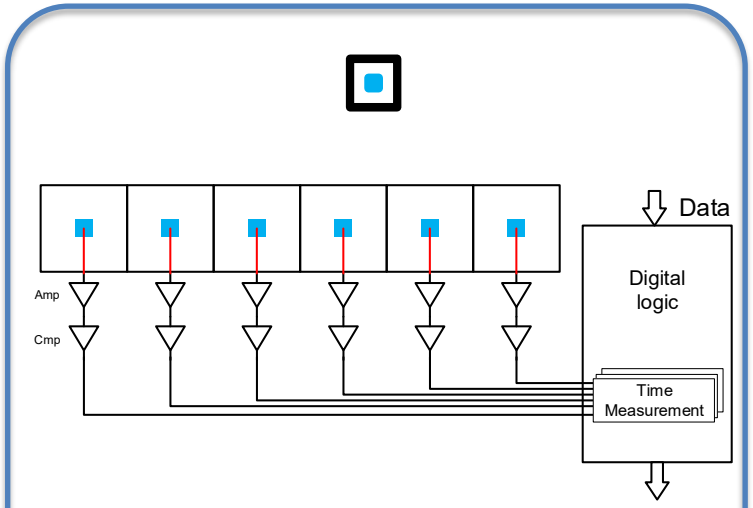
	Threshold(e^-)	Mismatch(e^-)	TN(e^-)
	311	13.9	15.6
	340	22.2	30.1



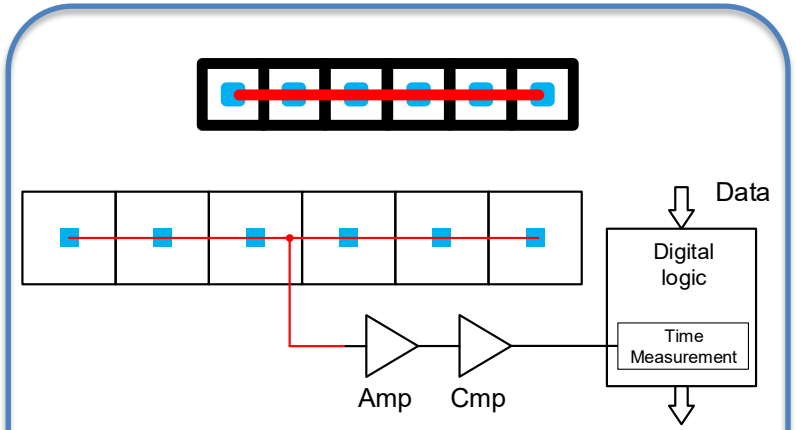
Observed cross-talks → could only read one pixel each time

The super-pixel architecture

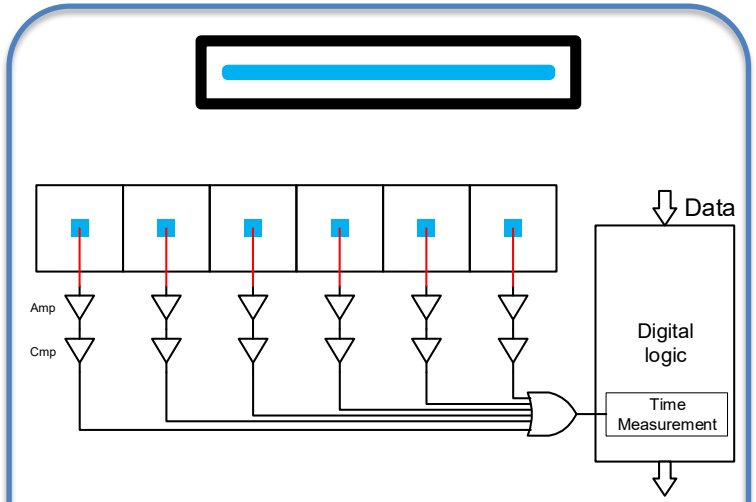
- Towards finer timing & higher spatial resolution with low power consumption



✓ Small collection diode
→ Good time performance
→ Good spatial resolution
✓ Multiple readout channels
→ High digital power



✓ Large collection diode
→ Low time performance
→ Low spatial resolution
✓ Fewer readout channels
→ Low digital power

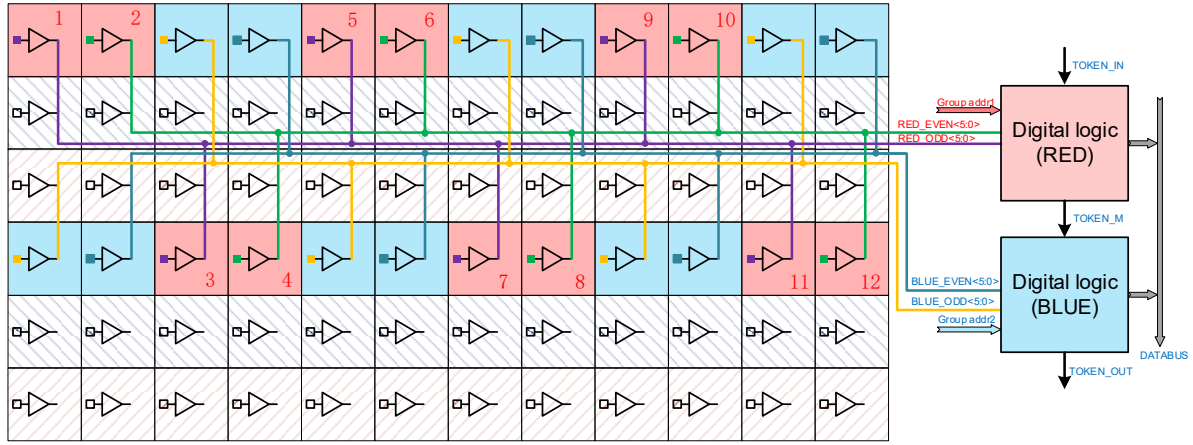


✓ Small collection diode
→ Good time performance
→ Good spatial resolution
✓ Fewer readout channels
→ Low digital power

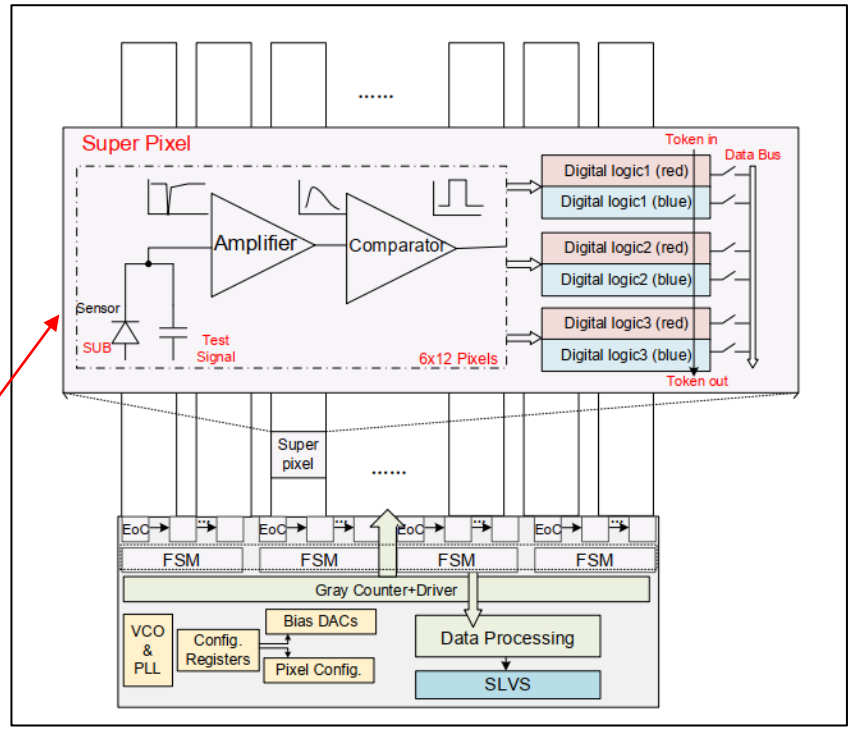
CharTPix_130

IEEE TNS, 2025, 72(3): 217-224

- Combining non-adjacent pixels: avoid ToT loss
- Super-pixel with 6×12 pixel array
  - 6 sets of digital readout logic
  - When cluster size < 3X4, no ToT loss occurs





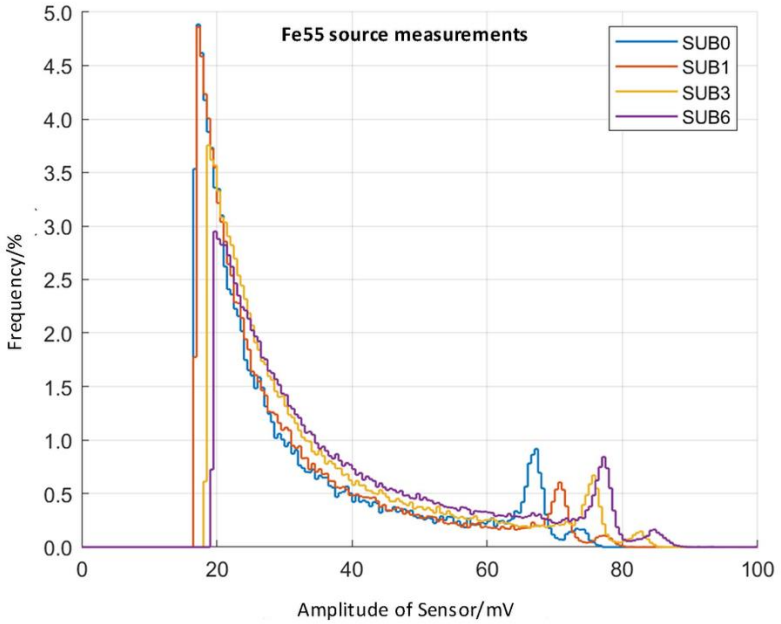


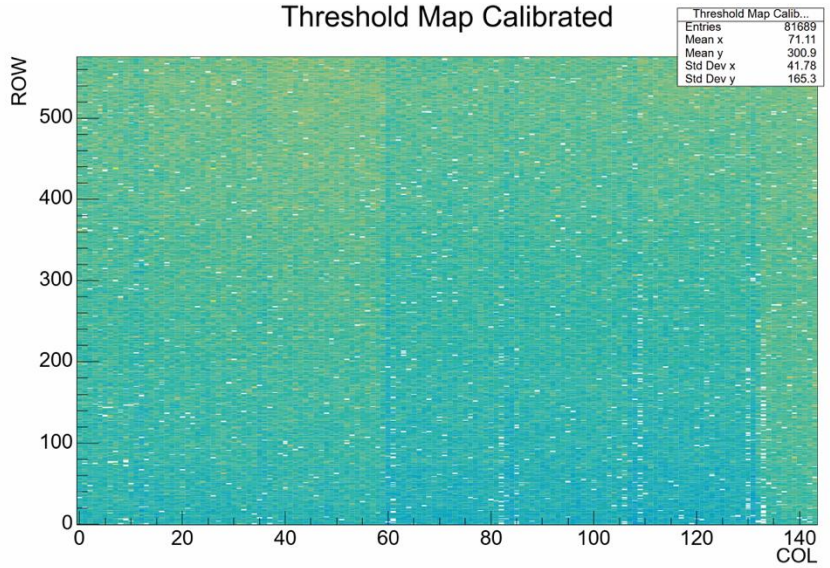
Process	ChartPix 130 nm
Chip Size	**6.1 mm×22.0 mm**
Array	576(row)×144(col)
Pixel Size	33.2 μm×33.2 μm
Power	44.5 mW
Power/pixel	150 nA/pix
ToA	13-bit (5-bit Fine+8-bit coarse)
ToT	8-bit

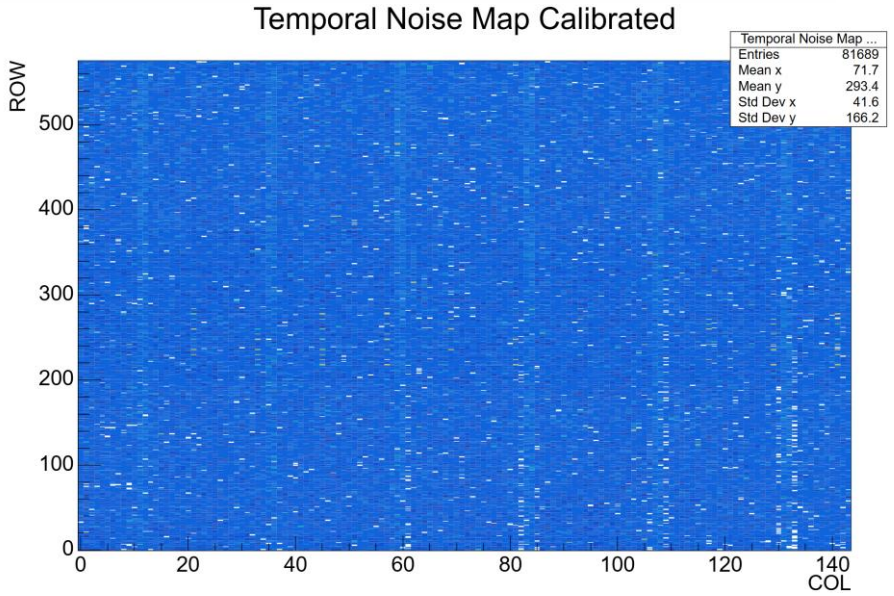
2 ns bin size (500 MHz VCO)

CharTPix_130

- 3T sensor tests using Fe-55 X-ray
  - Using a 16ch-ADC readout system



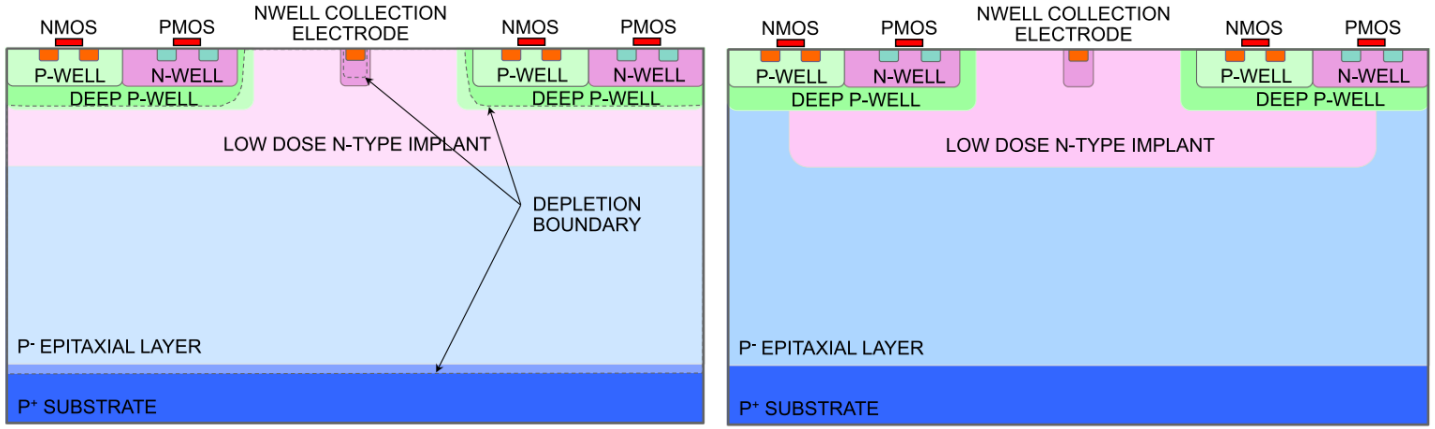




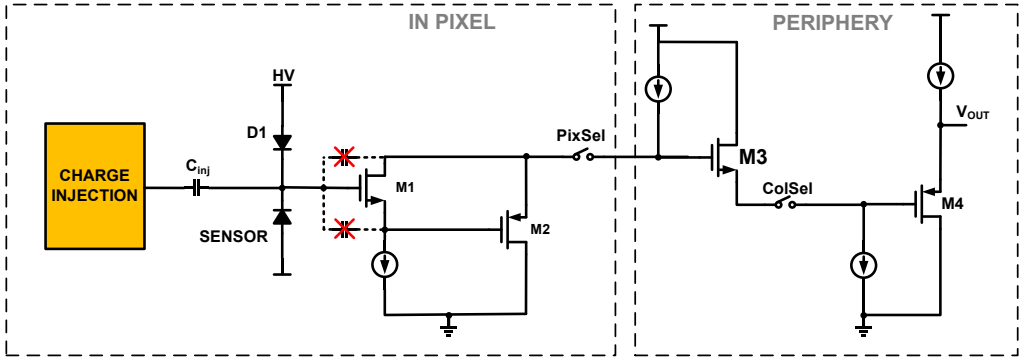
- CharTPix_130 MAPS with super-pixel readout
  - Threshold: 252.0e$^-$, Mismatch: 31.0e-
  - TN: 7.1e-, TN sigma: 2.3e- (@SUB = -4 V)

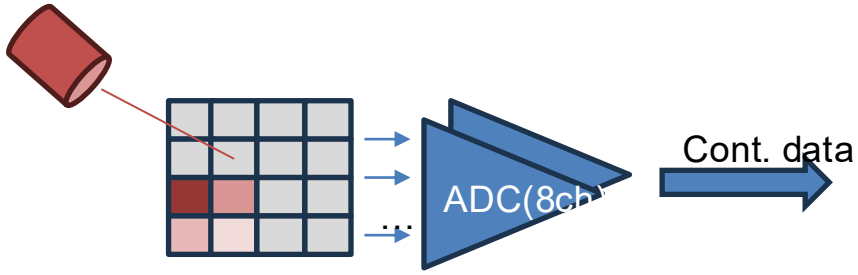
CharTPix_180B with modified process

- To improve the time resolution
- 180 nm CMOS with process modification
  - Low dose n-type implant
  - Low dose n-type implant with gap
- 3T sensor prototypes
  - Standard process, N-blanket, N-gap
  - Different sensor geometries
- Lab test with a 16ch ADC



MALTA2, IEEE TNS, Vol. 69, No. 6, 2022

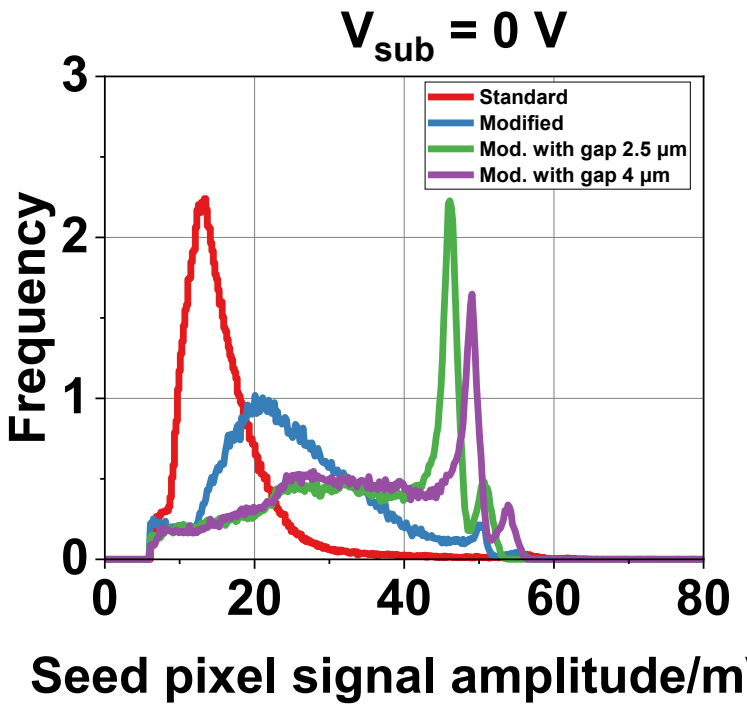


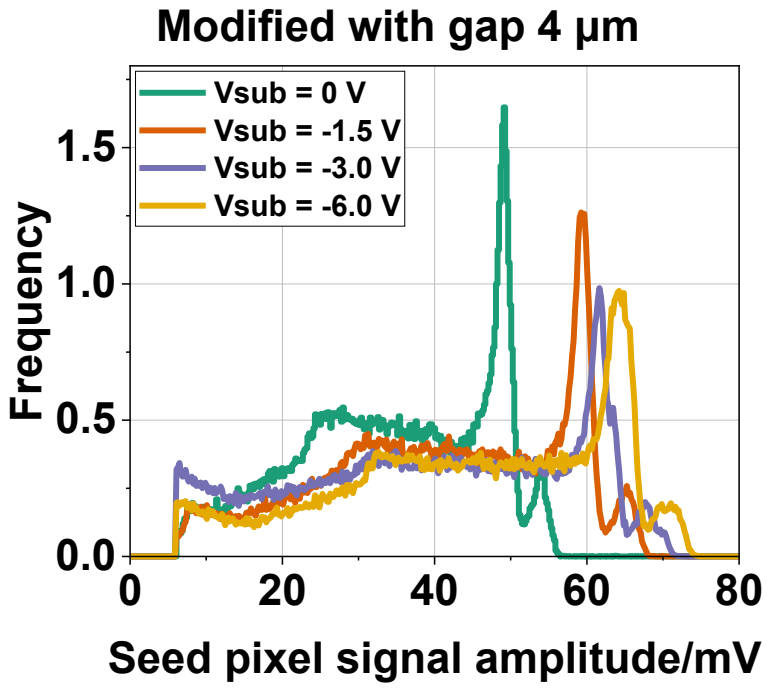


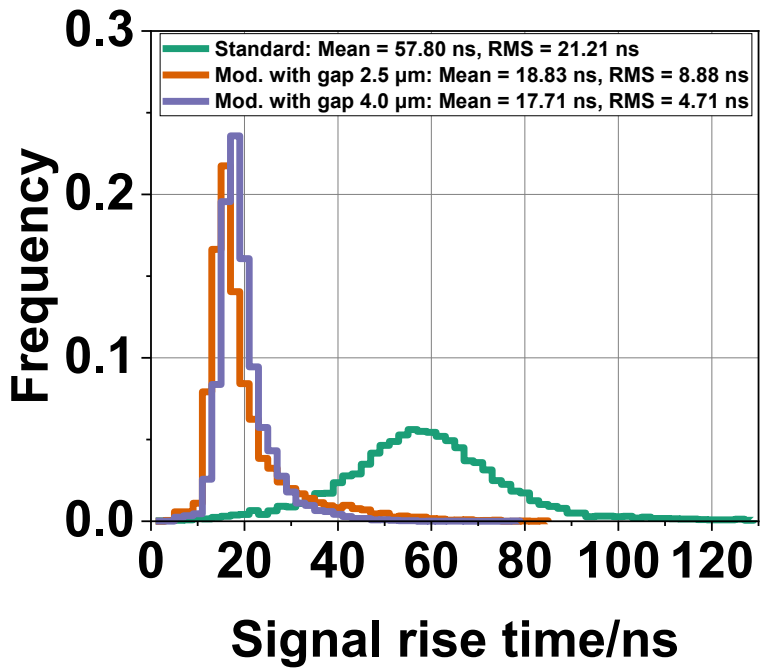
CharTPix_180B with modified process

- Fe-55 source test

Xinyu Bing, Pixel 2026



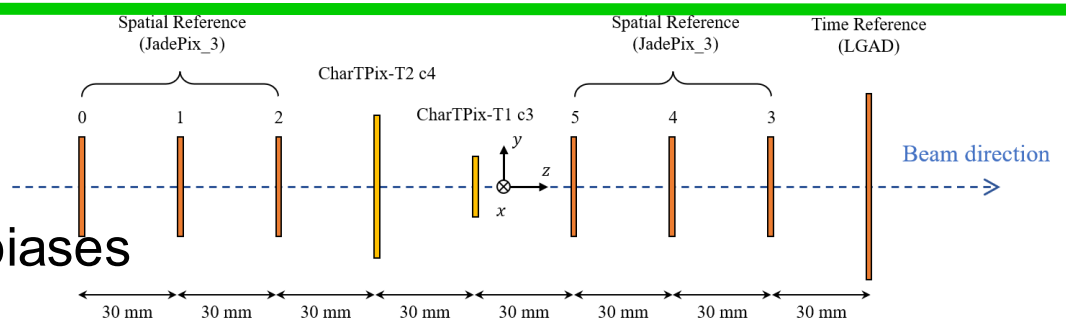




- ❖ Much improved performance (charge collection efficiency, signal rising time) with modified processes as expected
- ❖ Also validated the process modification

Beam tests

- Beam telescope with 6 JadePix-3 and 1 LGAD
- Carried out two beam tests at CERN PS
  - 1st beam test: Performance under different substrate biases
  - 2nd beam test: Performance after irradiation

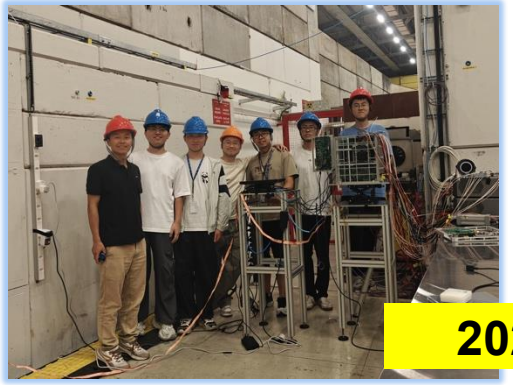








2025.10

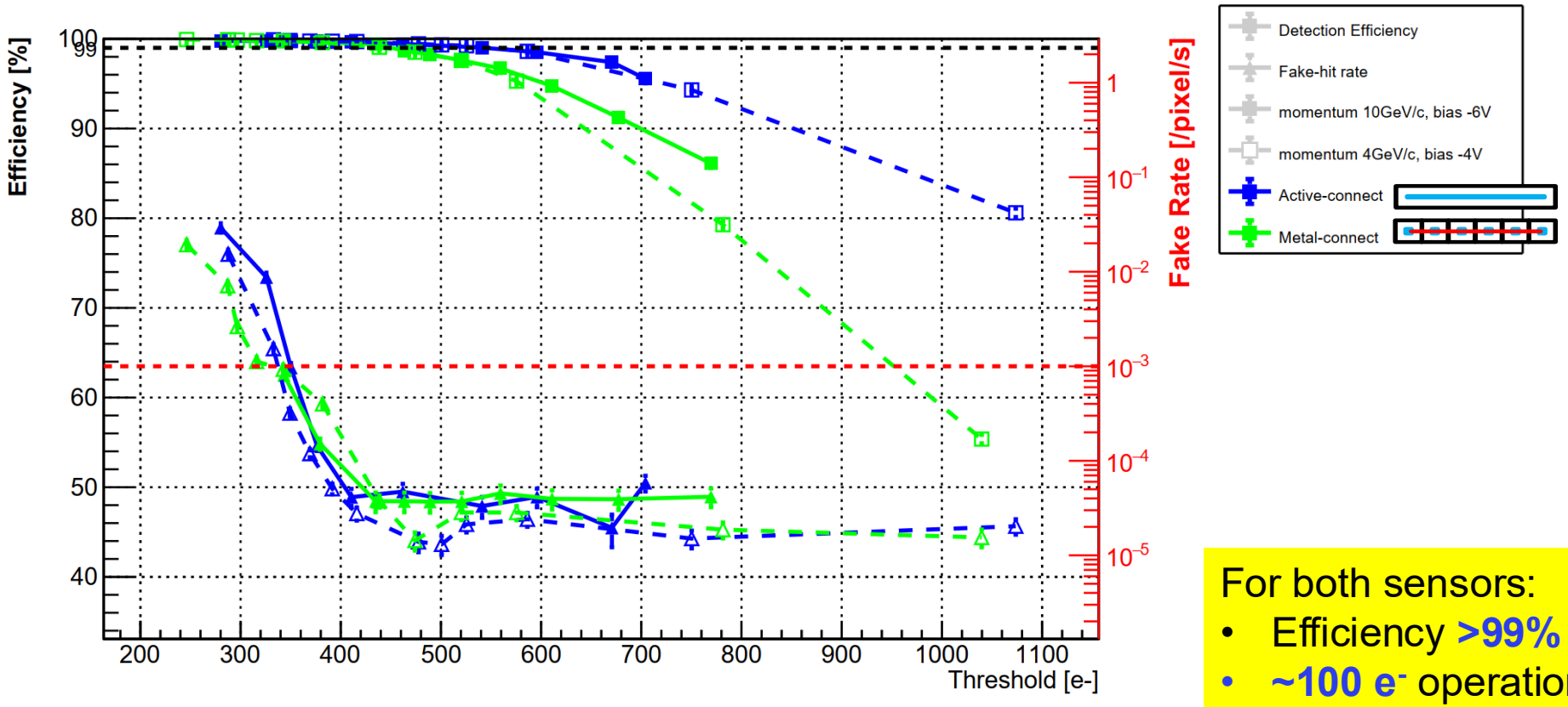


2026.06

CharTPix_180A v1

- Detection efficiency measurements

arXiv:2610.27595

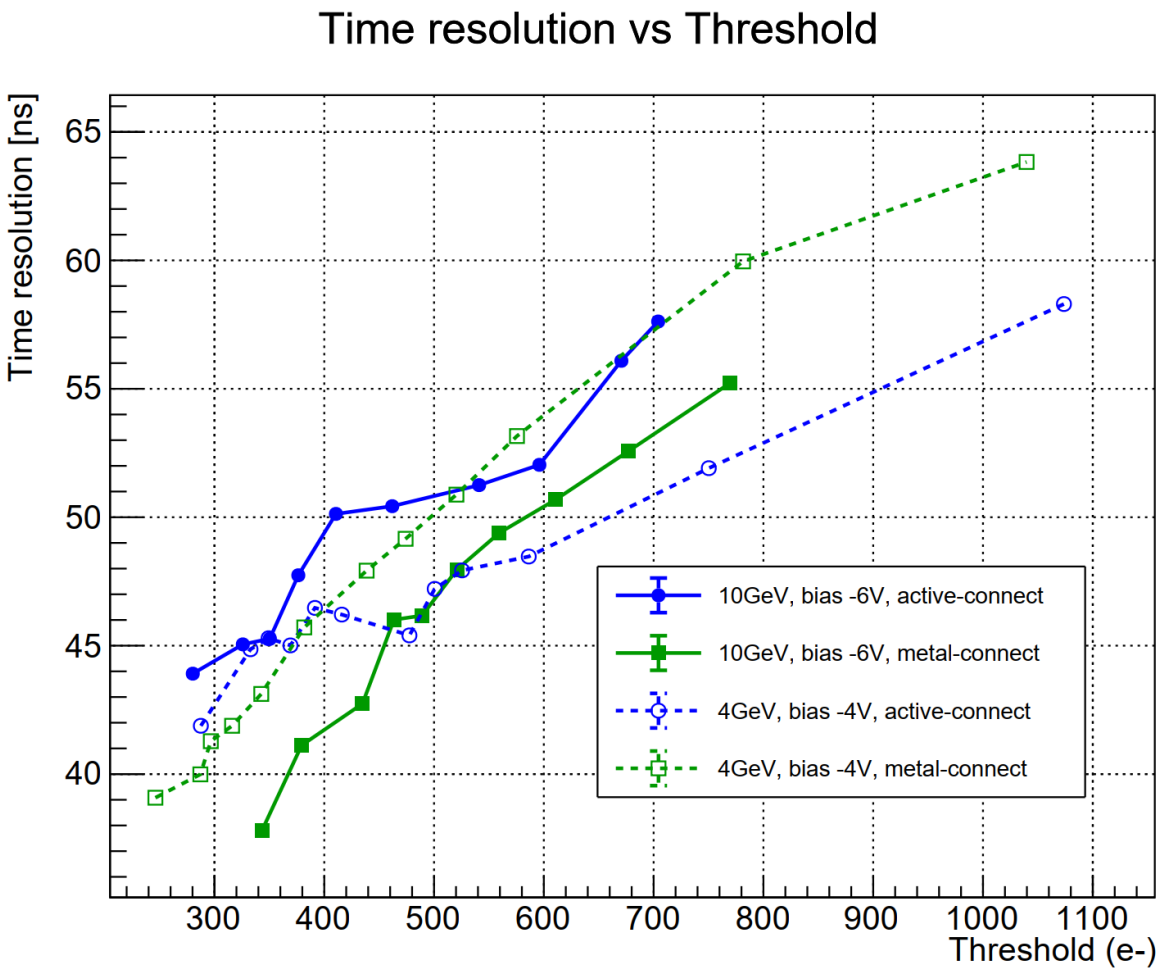


For both sensors:

- Efficiency **>99% below ~500 e⁻**
- **~100 e⁻** operational margin
- Best time resolution of **~40 ns** reached (before time-walk calibration)

CharTPix_180A v1

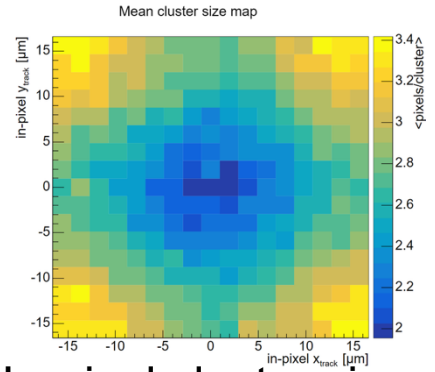
- Timing resolution



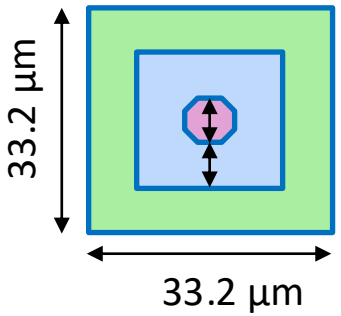
~ 40 ns time resolution is achieved **without** time-walk correction

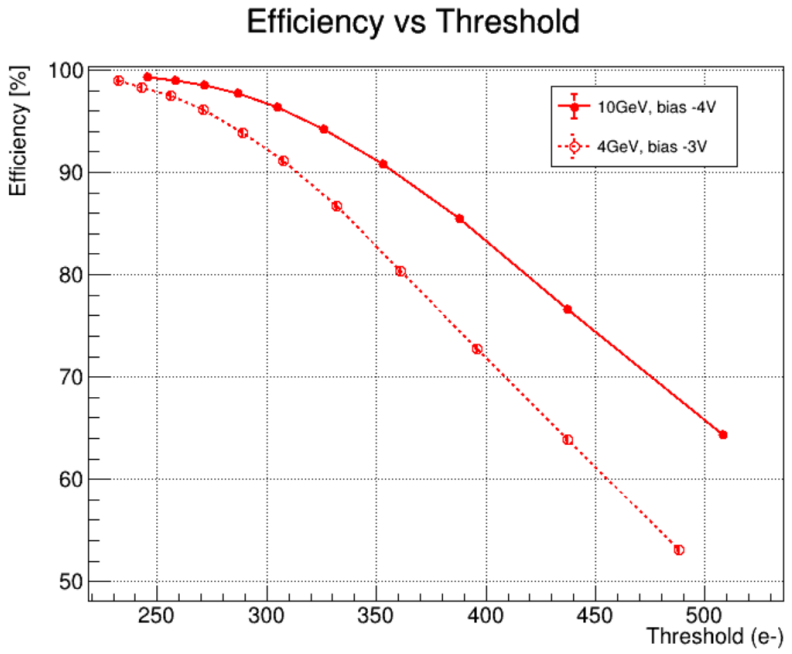
CharTPix_130

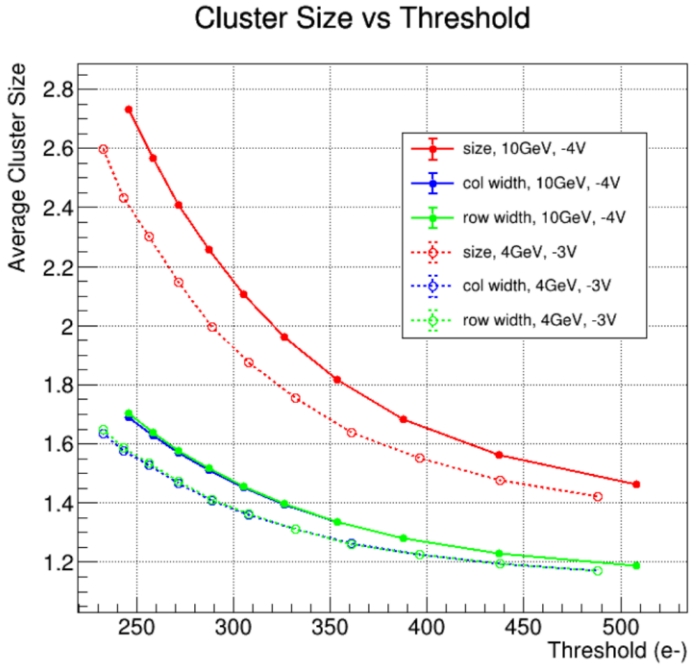
- Detection efficiency improves as substrate bias increases
- Efficiency drops rapidly beyond 300e$^-$, limited by the process
- Best resolution of **5 µm** is reached with charge-weighted centering

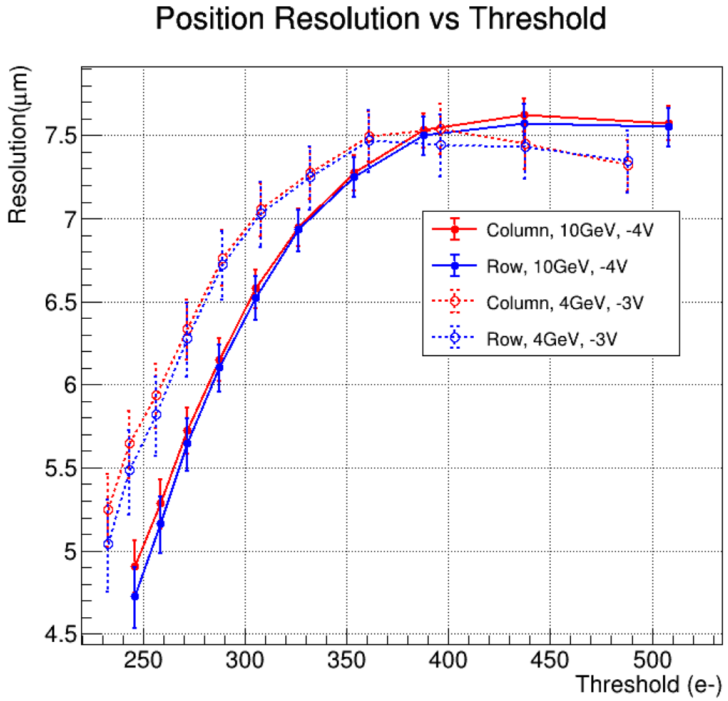


In-pixel cluster size



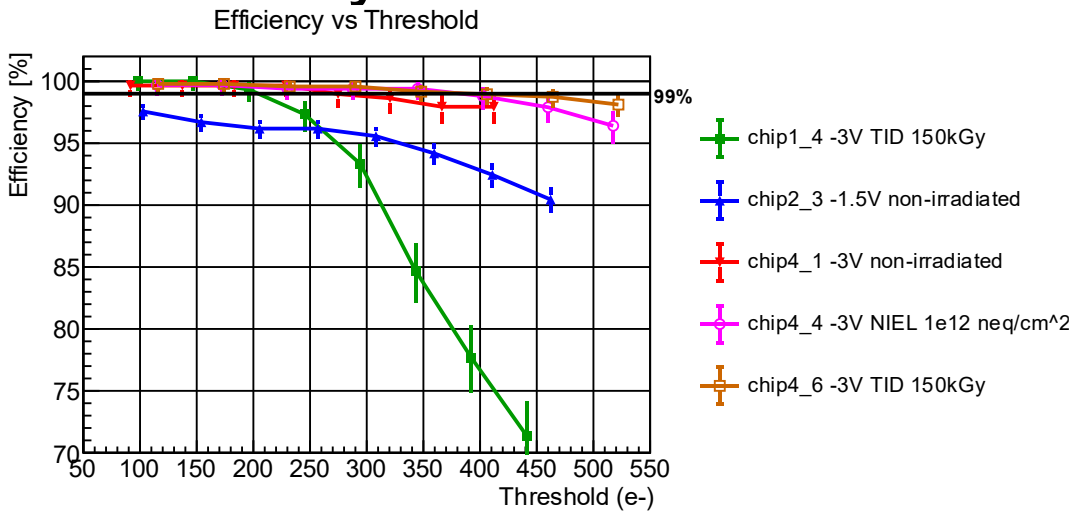


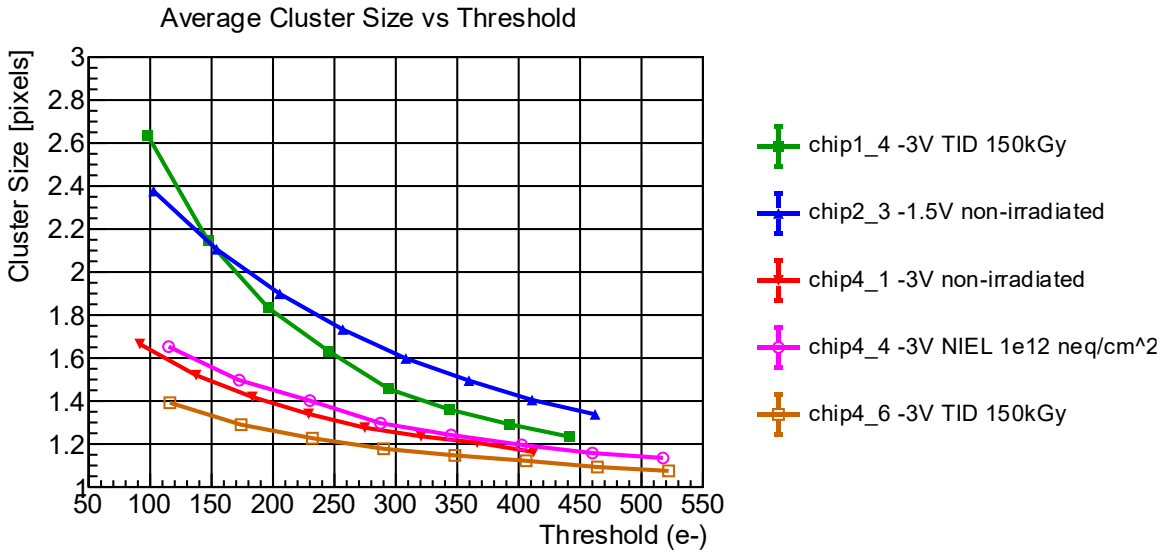




CharTPix_180B 3T sensors

- Preliminary results





Efficiency

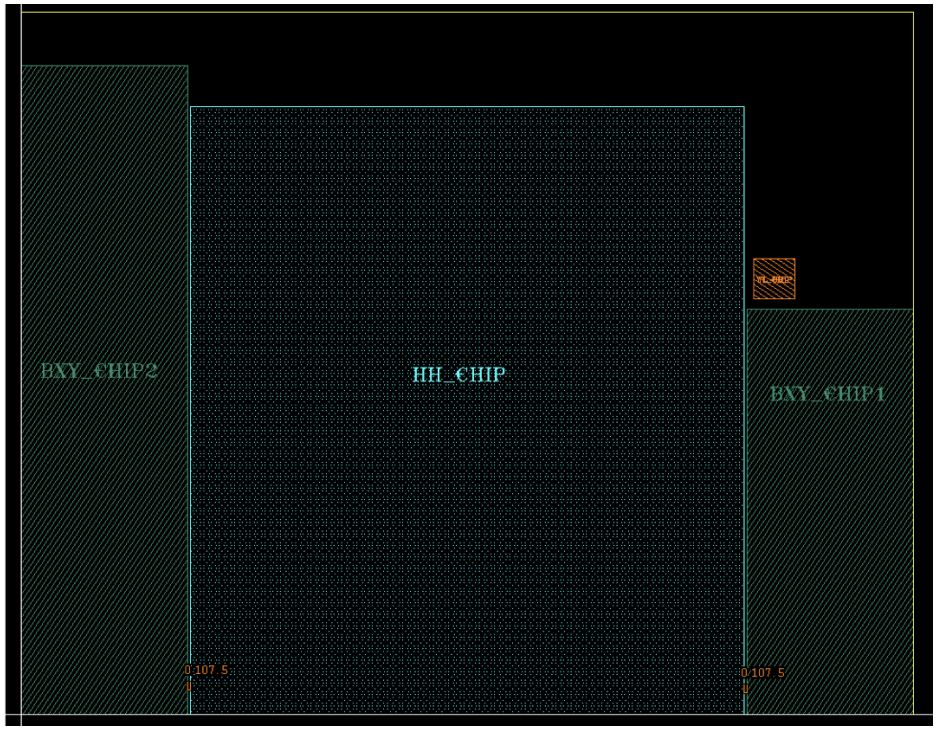
- ❖ Efficiency of standard process drops rapidly after 200 e^- THR
- ❖ Efficiency of N-gap remains above 99% before ~400 e^-

Average cluster size

- ❖ Roughly see the trend: Standard > Modified > Modified with gap
- ❖ Less charge sharing of modified with gap process

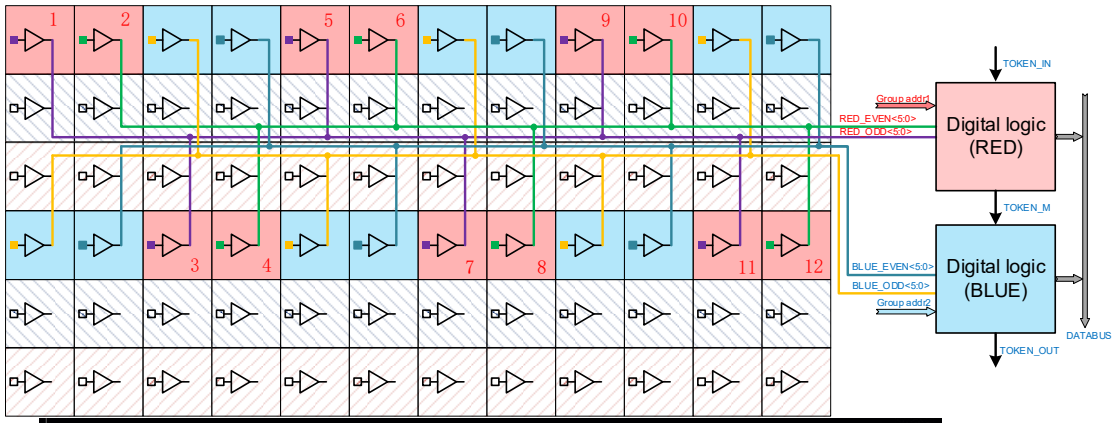
CharTPix: outlook

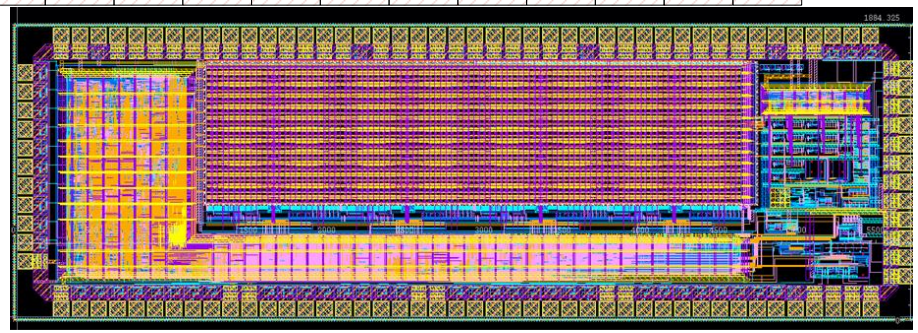
- 2nd submission with the 180nm modified process scheduled in Nov 2026
- Engineering run (2.6cm×3.3cm) with multiple MAPS chips
  - Full-size chip with super-pixel readout (migrated from the CharTPix_130 design)
  - New prototypes with asynchronous readout



CharTPix Super-pixel MAPS

- The super-pixel design can achieve multi-goals in one go: good spatial resolution, timing resolution and low power consumption
  - Already verified with the 130nm design prototypes (high-resistivity substrate wafers)
- Design migrated to the standard 180nm process (chips received in Sept)
  - To be tested soon

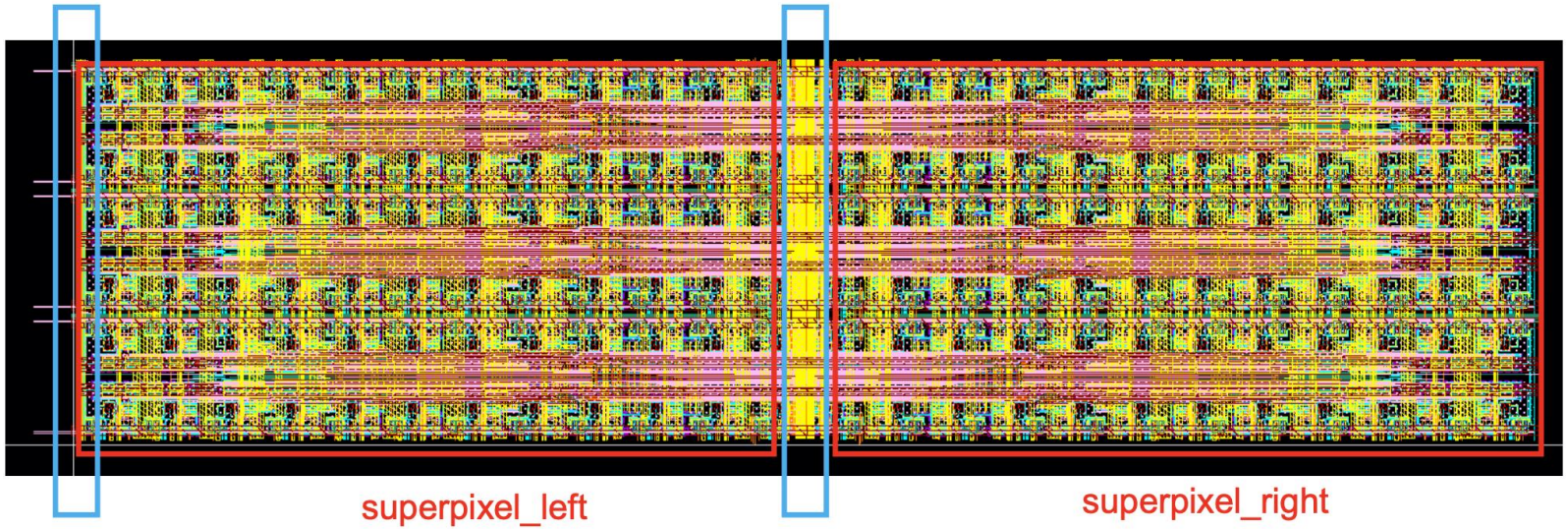




Process	CharTPix_130	ChartPix_180A
Pitch (μm)	33.2×33.2	35.6×35.6
Threshold (e^-)	153.6	153.0
ENC (e^-)	5.1	5.4
MISMATCH (e^-)	5.8	4.7
σ_{Jitter} (ns)	1.2 (400 e^-)	1.1 (400 e^-)
σ_{ele} (ns)	1.54 (400 e^-)	1.43 (400 e^-)
Power consumption (analog) (mW/cm^2)	16.3	17.0
Power consumption (CLK) (mW/cm^2, gray)	11.0	16.3

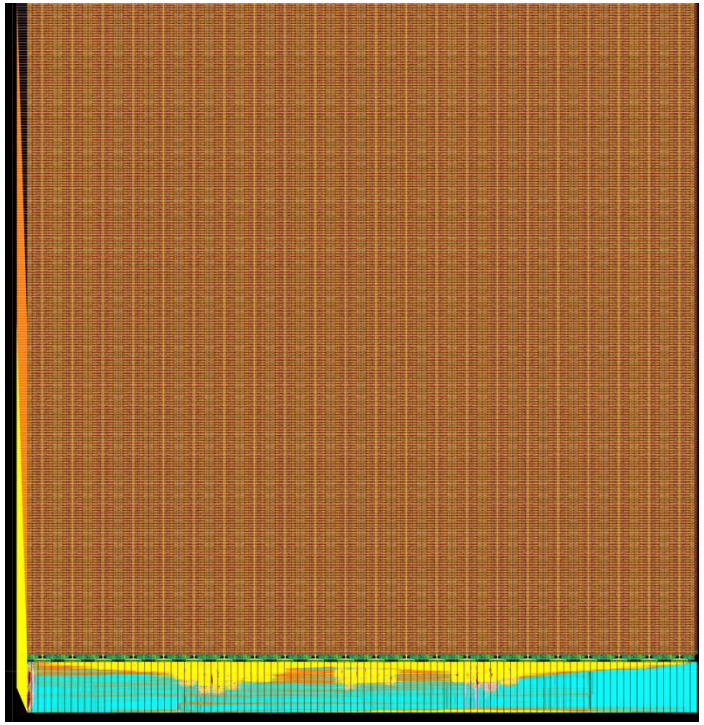
CharTPix_180B Super-pixel MAPS

- Also being migrated to the modified 180nm process
- Full-size chip: 2.00 cm × 2.01 cm
  - Pixel array: 528×504 pixels, 44×84 superpixels
  - Pitch size enlarged to 38 μm × 39 μm



Super pixels: 6 rows × 12 columns, with each pixel of 38 μm × 39 μm

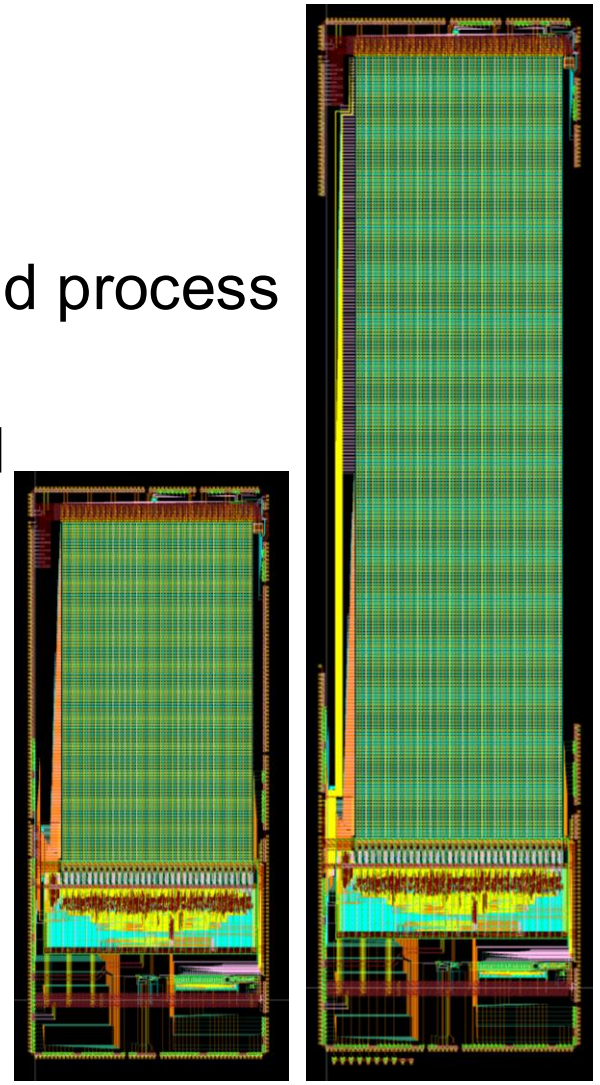
2cm × 2cm, 528 cols × 504 rows



CharTPix_180B Asynchronous MAPS

- Our previous CharTPix prototypes are all based on synchronous readout architecture
  - In pixel TOA, TOT (LE, FE)
  - Column drain readout to the with token priority chains
  - Achieved ~50ns timing resolution with the standard 180nm process
- Sensor intrinsic timing resolution should be ~1 ns with the modified process
- To achieve the 10 ns hit timing resolution target of STCF, with $\leq 50\ \mathrm{mW/cm^2}$ power consumption, a new readout design in needed
- CharTPix_180B asynchronous readout prototypes
  - Features a new in-pixel analog circuit with flipped voltage follower
  - Pixel groups: 4 × 4 pixels with a pitch of 37.5 μm × 38.0 μm
  - TOA: Fast OR (only the seeding pixel), EoC Ping-pong TDC
  - TOT:
    - In-pixel TOT, with AERD readout
    - Column drain among pixel groups

Chip1: 1.45 cm × 0.61 cm
Chip2: 2.45 cm × 0.61 cm



Chip1 Chip2

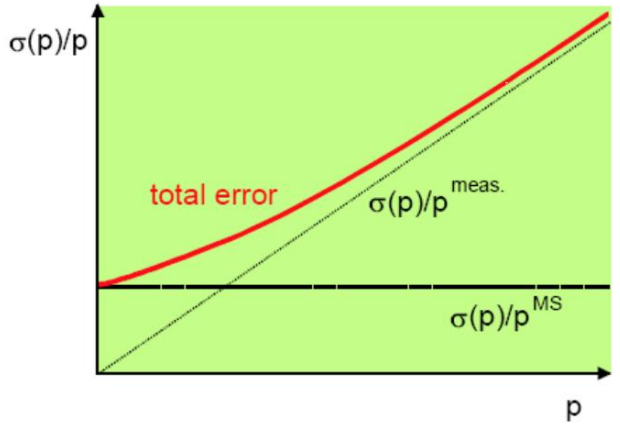
Summary

- Super Tau-Charm Facility: a next generation e^+e^- collider operating in 2-7 GeV
- MAPS became a promising technology for its inner tracker
  - Material budget ~0.3% X_0/layer, rate capability >1 MHz/cm^2
- Extensive development efforts towards the ITKM specifications
  - Full simulation of the tracking system
  - Various chip designs with different technologies
- Characterization of CharTPix prototypes showed promising results
  - Power consumption <50 mW/cm^2
  - Time resolution ~40 ns
  - Efficiency > 99% and FHR < 10-3/pixel/s
  - Position resolution <5 μm
- Future R&D
  - Fully depleted MAPS, full-size chip, asynchronous readout …

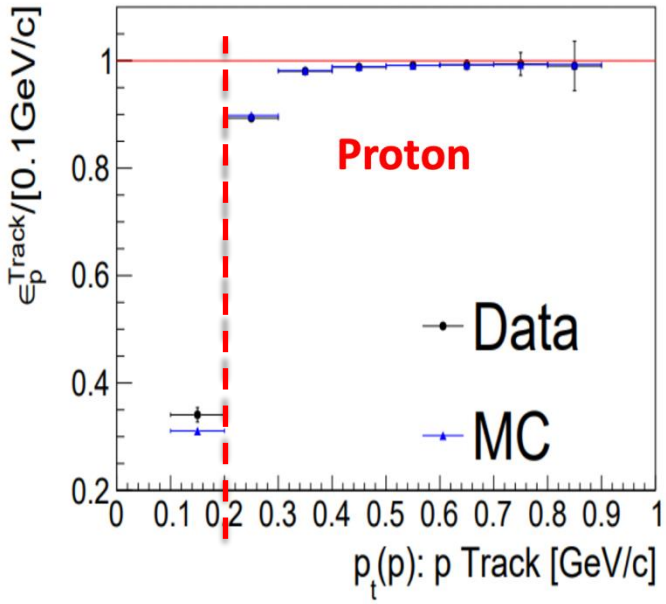
Backup

Detector considerations

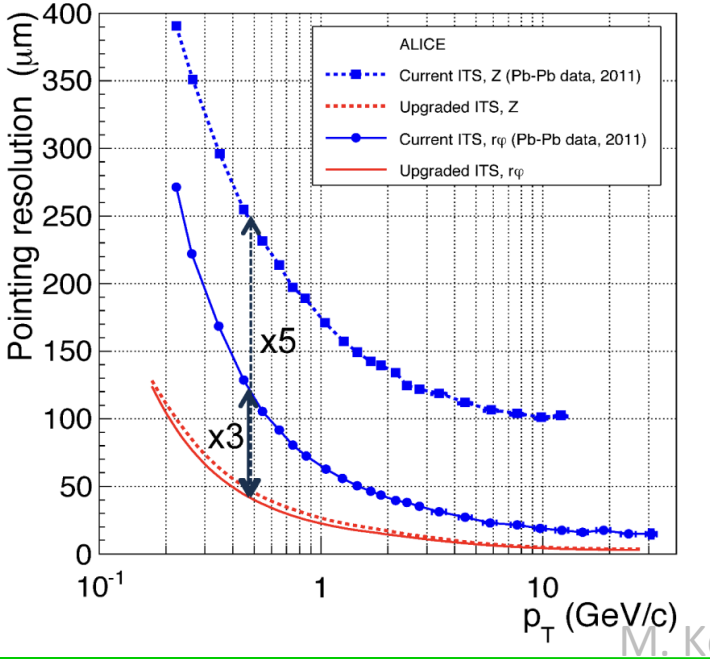
- Tracking challenges at low p_T
  - Momentum resolution: Multiple Coulomb scattering
  - Track reconstruction efficiency
- Low material budget is essential

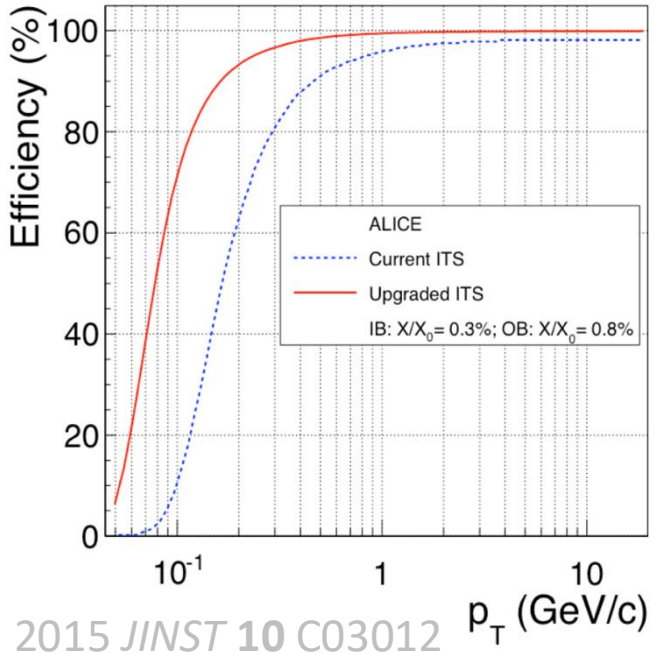


BESIII tracking efficiency



ALICE ITS2 Upgrade Tracking Performance :
1.14%X_0 → 0.3%X_0 (inner layers)



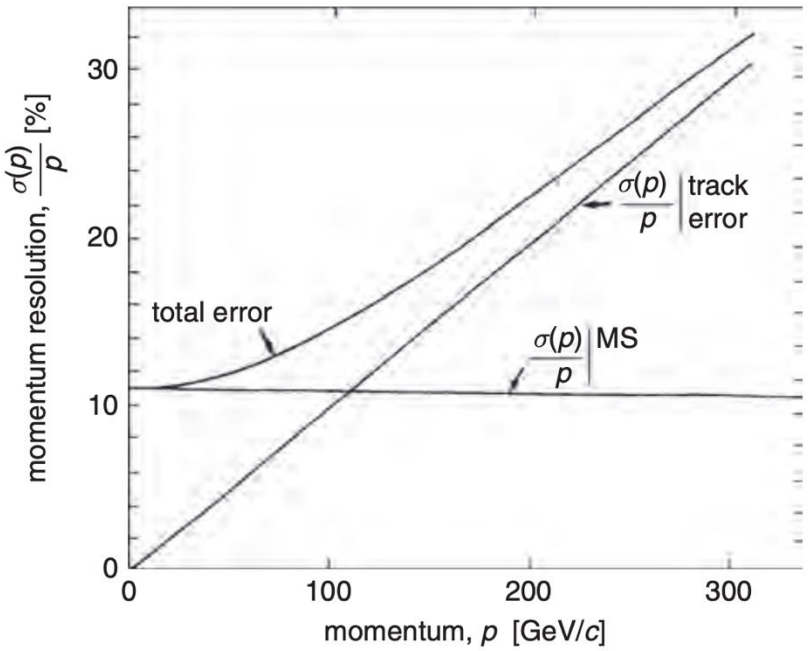


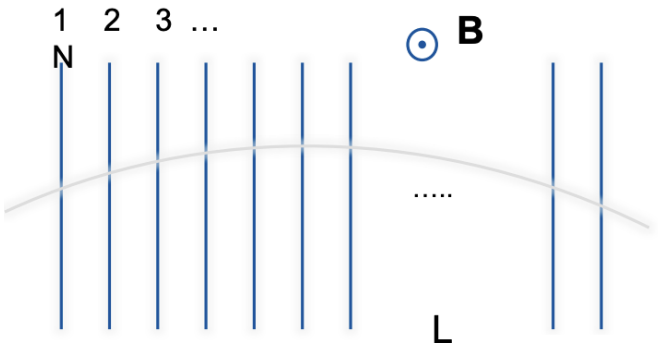
M. Keil 2015 *JINST* **10** C03012

Tracking

Particle Detectors, C. Grupen, B. Schwartz

- Momentum resolution





$$\frac{\sigma(p)}{p_{\mathrm{T}}} = \frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{track error}} \oplus \frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{MS}}$$

$$\frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{track error}} \approx \frac{\sigma_{r\phi}[m]p_{\mathrm{T}}[\mathrm{GeV}]}{0.3B[T](L[m])^2}\sqrt{\frac{720}{N+4}}$$

Position resolution: O(10μm) on hybrid and down to O(1-3μm) on MAPS

$$\frac{\sigma(p)}{p_{\mathrm{T}}}\Big|^{\text{MS}} \approx \frac{0.0542}{\beta B[T]L[m]}\sqrt{\frac{X_{\mathrm{tot}}}{X_0}}$$

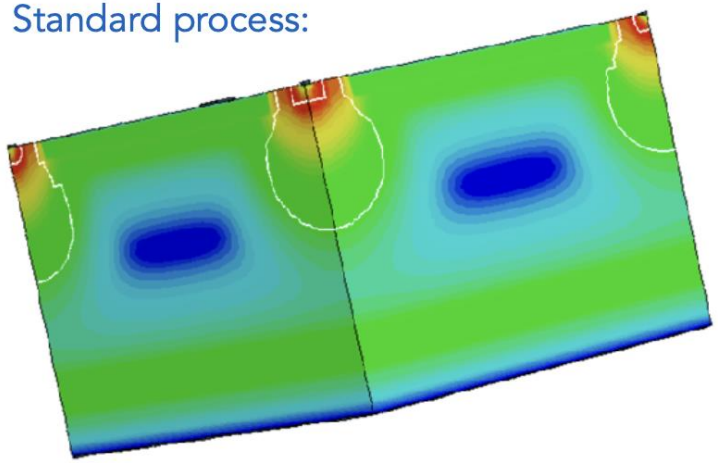
Multiple scattering: Thin detectors on light carbon fiber supports

X_{tot}/X_0: Total material budget

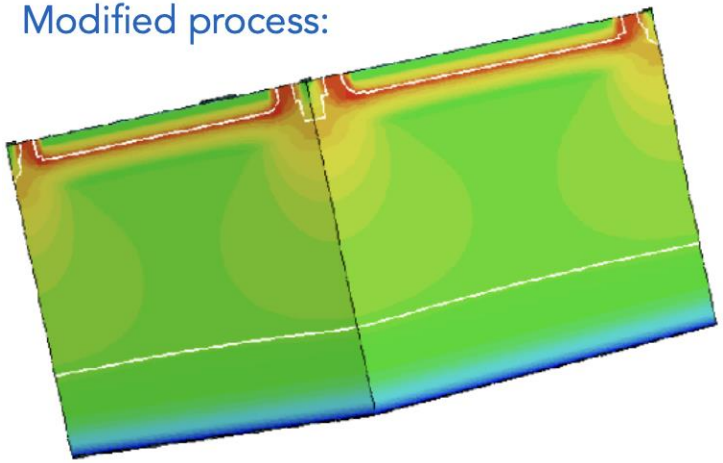
Process modification: simulation

Magdalena Munker

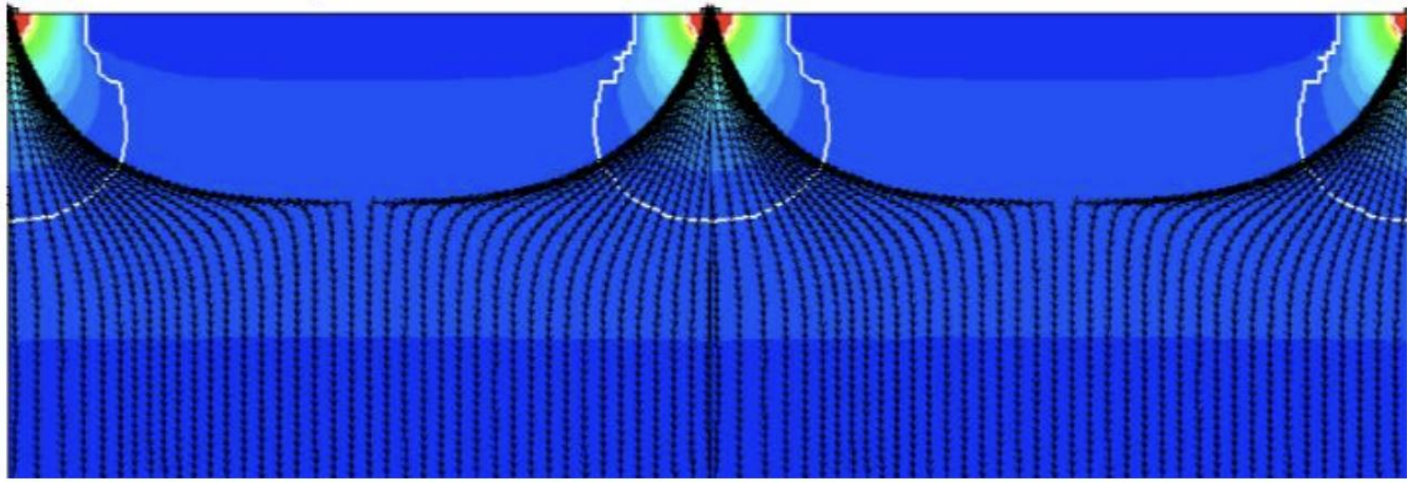
Standard process:



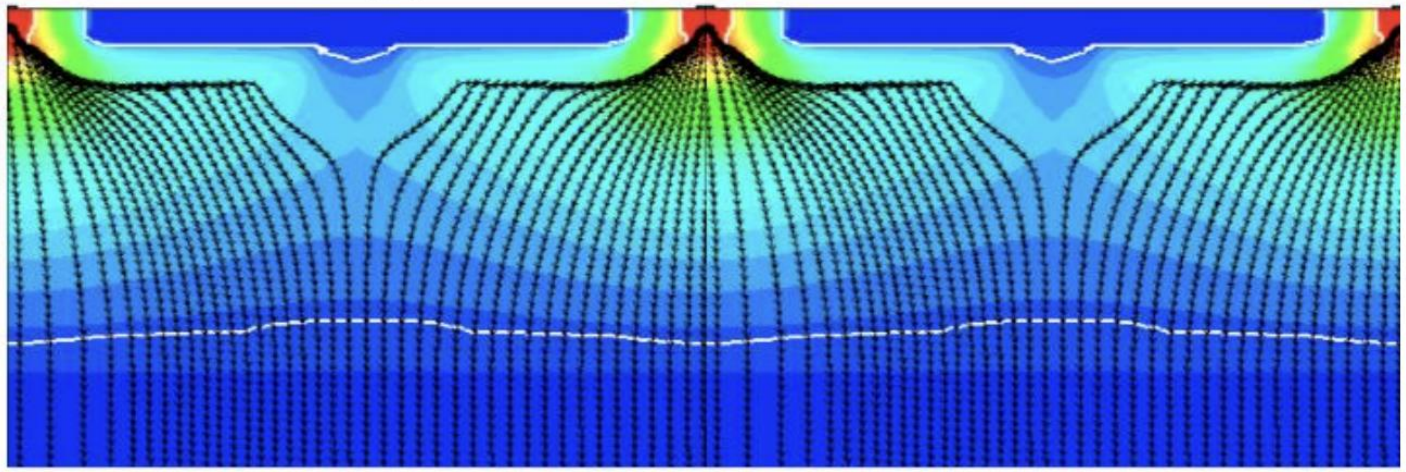
Modified process:



Standard – ALPIDE like sensor



Modified with gap sensor



Expected tracking performance for STCF

Front. Phys. 19, 14701 (2024)

