Progress of readout electronics for particle physics experiments：high precision, speed, and density

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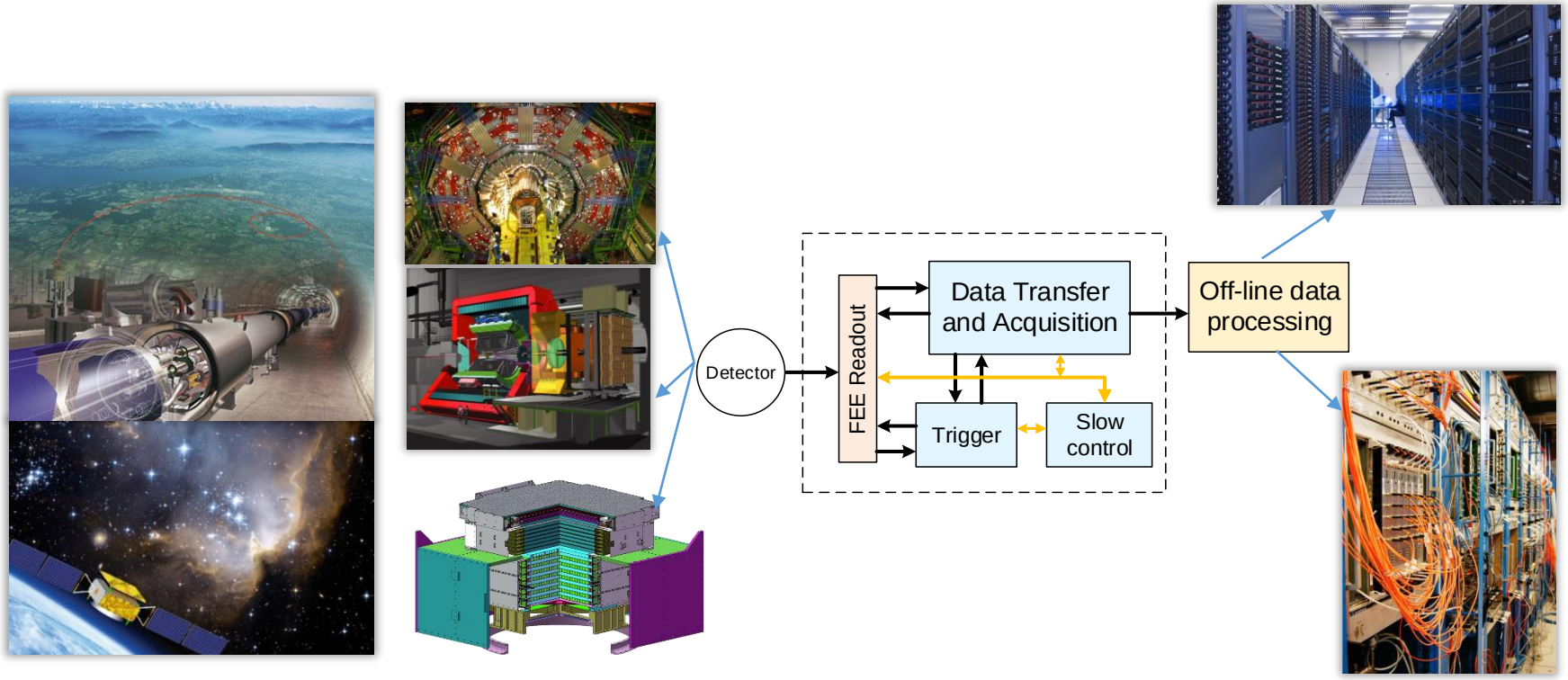
2026.11

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

MODERN PHYSICS DEPARTMENT

Readout electronics in particle physics experiments

- In large-scale particle physics experiment facilities, electronics are key parts.



- The information obtained from the detectors (sensors) has to be manipulated, processed, and transferred by the electronics before being used by the computer farms.

Tasks of readout electronics

❖ New challenges appear for electronics with the development of particle physics experiments:

- ■ Electronics from other fields can not meet the requirements
- ■ Necessary to study key techniques

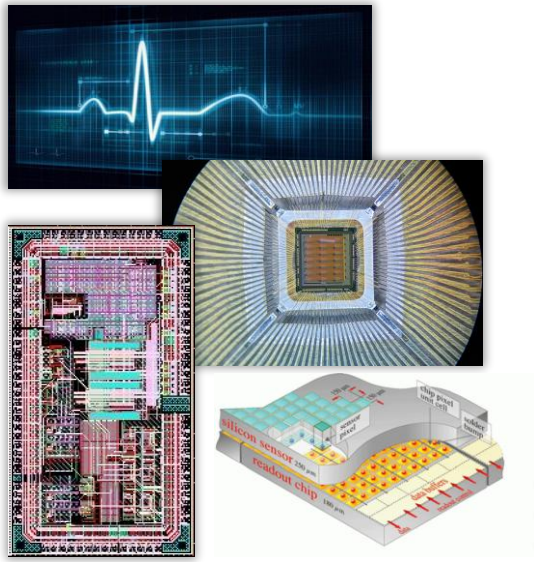
◇ Faster signal processing
  - ◇ ns → sub-ns

◇ Higher measurement accuracy
  - ◇ ps Time、sub-fC Charge

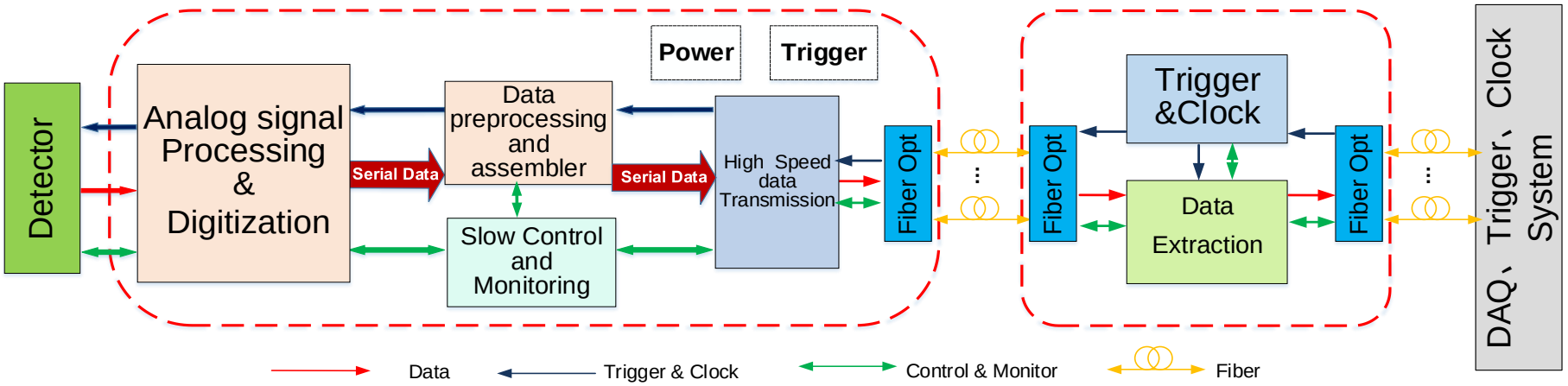
◇ Larger number of channels
  - ◇ Tens of thousands -> millions or more channels

◇ High-speed real-time data processing and transmission

◇ Higher Speed
◇ Higher Accuracy
◇ Higher Integration
◇ Low Power
◇ Radiation Tolerance



Readout electronics system



- Data Link: Analog → Digital →Preprocessing → Reformat →Extraction
- Time stamp Link: Clock System → Synchronized Clock → Clock Distribution
- Trigger Link: Multi-Level Trigger →Trigger Information Dec & Check

  →Trigger Signal Distribution
- Control Link: Control Information Dec & Check → Control Signal Distribution

Outline

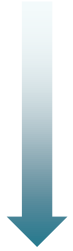
- Precision front-end measurement
  - High-precision **charge** measurement
  - High-precision **time** measurement
  - High-speed waveform digitization
  - Silicon pixel detector (**position** measurement) readout
- Data aggregation and transmission
  - High-speed interface circuits
  - Data aggregation
  - Optical signal transceiver

Outline

- Precision front-end measurement
  - High-precision charge measurement
  - High-precision time measurement
  - High-speed waveform digitization
  - Silicon pixel detector readout
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  - High-speed interface circuits
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High-precision charge measurement

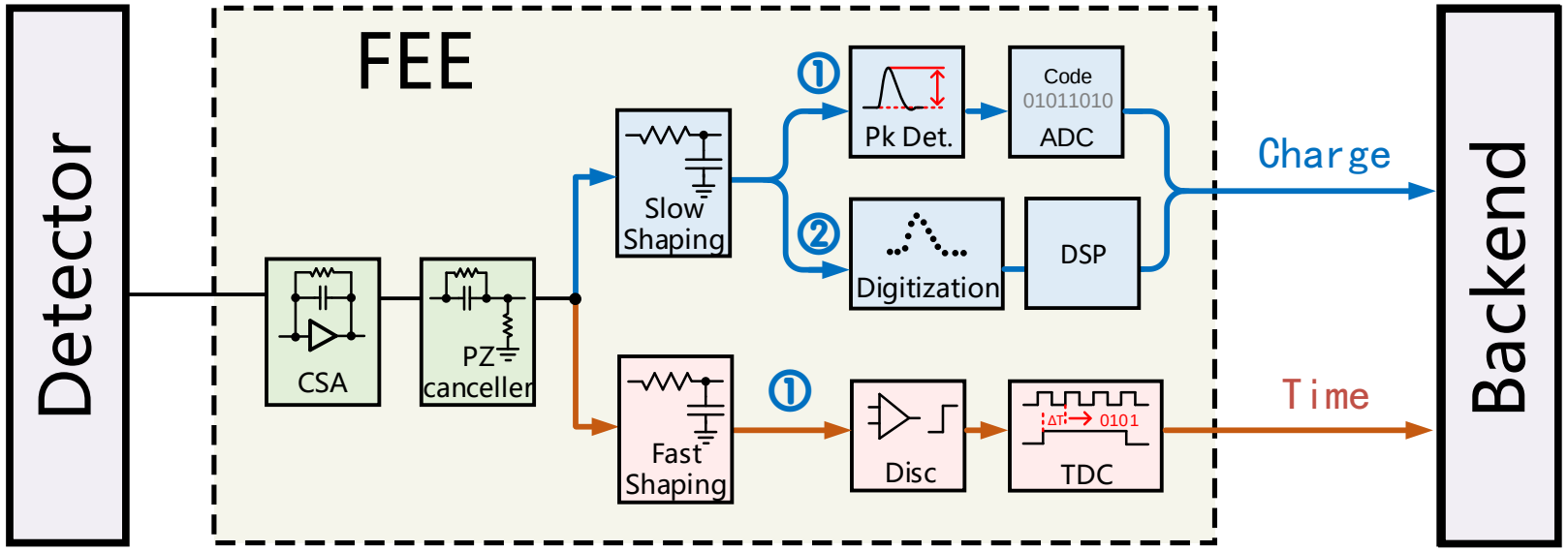
- Readout ASIC techniques for MPGD (Micro Pattern Gas Detector) and silicon-strip
  - ◇ Features: low noise, high integration
  - ◇ Classification:
    - Full analog readout → charge
    - On-chip discrimination → charge, time
    - Semi-digitization → charge, time
    - Fully digitization → charge, time
      - Amplify and shape to measure charge; amplify and discriminate to measure time
      - Waveform digitization after amplification and shaping



More functions
Higher integration, lower power
Higher rates...

- Cosmic-ray experiment readout
  - ◇ Large dynamic range
  - ◇ Time + charge measurement
  - ...

High-precision charge measurement ASIC



Typical ASIC chips

Name	Chn. No.	Tech. Type	Shaping Time (ns)	Noise	Range	Power mW/ch	Hit Rate	Time Precision	Application	Detector Type	Unit	Process
CASAGEM	17	Analog Output CSA+Shaper	20 to 80	173.2 e +16.52 e/pF @ 80 ns	Up to 1 pC	11	-	-	nTPC	GEM	Tsinghua	350 nm
CATIA	1	Analog Output TIA	none	1.8 fC @ 7.2 pC 18 fC @ 72 pC	Up to 72 pC	-	-	30 ps @1.8 pC	CMS ECAL barrel	APD	Université Paris-Saclay, France	130 nm
-	2	Analog Output CSA+Shaper	90 to 250	278.2 e +26 e/pF	15 fC	8.7	344 kHz @ 8fC	4 ns @ corrected	CBM experiment at FAIR center, Germany	silicon microstrip	AGH University of Science and Technology, Poland	180 nm
FEAM	8	Analog Output CSA+Shaper	80 to 1000	4000 e @100 pF Cin	1 pC	6.6	10 kHz	3 ns @14 fC	CEE MWDC	MWDC	IMP	-
-	16	Analog Output CSA+Shaper	25 to 250	17,000e @10 pC Range @100 pF Cin @120 ns τpeak	Up to 10 pC	8.6	200 kHz	-	CSNS Back-n	MPGD	USTC	180 nm
-	12	Analog Output CSA+Shaper	350 to 1430	59 e @0 pF Cin	0.6 fC; 2 fC	1.25	-	-	-	-	NPU	-
XAA1.2	128	Disc. On-chip CSA+Shaper +Discri. +Peak S&H	2000	935 e @ 30 pF Cin	5 fC	1	0.02	-	SuperAGILE X-ray imager onboard the AGILE satellite	silicon microstrip	INAF, Italy	800 nm
VATA241	64	Disc. On-chip CSA +Shaper +Discri.	190	1300 e +65 e/pF	72 fC	-	500 kHz	1 ns @ 72 fC	BrainPET scanner	APD	CIEMAT, Spain	-
SENSROC13	4	Disc. On-chip CSA+Shaper +Discri.	250	57 e +20 e/pF	15 fC	1.25	1 MHz	-	electronic personal dosimeter	Si-PIN	NPU	350 nm
-	8	Disc. On-chip Current conveyor +Discri.	-	592.4 e + 50.7 e/pF	50 fC	17.6	120 MHz	22.7ps +2.3ps/pF @ 15 fC	X-ray time-resolved	APD	UCAS	130 nm
RX64	64	Disc. On-chip CSA+Shaper +Discri.	500 to 1000	167 e @ 2.5 pF Cin	3.2 fC	2.5	200 kHz	-	digital X-ray imaging	silicon microstrip	Universita del Piemonte Orientale, Italy	800 nm
CBC3	254	Disc. On-chip CSA+Shaper +Discri.	25	200 e +100 e/pF	8 fC	1.65	1 MHz	-	CMS Tracker at the High Luminosity LHC	silicon microstrip	Imperial College London, UK	130 nm
-	4	Disc. On-chip CSA+Shaper +Discri. +Peak S&H	160 to 1000	3000 e @1 pC Range 30,000 e @10 pC Range	Up to 10 pC	-	20 kHz	-	-	plastic scintillator	IMP	-
VLAST SiReadout-S	16	Disc. On-chip CSA+CR-RC+MFB +S/H+Disc.	3.7–4.0 (Qin>0) 5.0–5.5 (Qin<0)	671+2.8 e^-/pF (Qin>0) 832+3.7 e^-/pF (Qin<0)	±220 fC	0.298 (Core)	—	— (Just disc. For trigger)	VLAST	Silicon Strip	IMP	180 nm

Typical ASIC chips

Name	Chn. No.	Tech. Type	Shaping Time (ns)	Noise	Range	Power mW/ch	Hit Rate	Time Precision	Application	Detector Type	Unit	Process
APV25	128	Semi-digital CSA+Shaper +SCA	50	270e+38e/pF	20 fC	2.7 @20 MSps	1 kHz @ full readout	< 1 ns @ 20 fC	CMS tracker	GEM、silicon microstrip	Imperial College, UK	250 nm
-	32	Semi-digital CSA+Shaper +Disc. +S&H +Wilkinson ADC	3000	2099 e +1.5 e/pF	300 fC	3.5	-	-	Onboard the International Space Station	APD	Waseda University, Japan	350 nm
AGET	64	Semi-digital CSA+Shaper +SCA	50 to 1000	900e @120 fC Range @30 pF Cin @230 ns τpeak	Up to 10 pC	10 @40 MSps	< 1 kHz	< 1 ns @ 20 fC	SPIRAL2 at GANIL in France RIKEN at Wako in Japan FAIR at Darmstadt in Germany etc.	GEM TPC	CEA Saclay, France	350 nm
TIGER	64	Fully digital CSA+Shaper +S&H +TAC +Wilkinson ADC	170	1500e+10e/pF	50 fC	12	60 kHz	30 ps @ TDC only	BESIII	GEM TPC	Politecnico di Torino, Italy	110 nm
SAMPA	32	Fully digital CSA+Shaper +SAR SCA +DSP	160 to 300	800e @67 fC Range @22 pF Cin @160 ns τpeak	Up to 500 fC	19 @20 MSps	50 kHz	-	ALICE TPC and MCH at LHC	GEM TPC、MWPC MCH	Escola Politécnica da Universidade de São Paulo, Brazil	130 nm
VMM3	64	Fully digital CSA+Shaper +S&H +TAC +SAR ADC	25 to 200	2280e @110 fC Range @100 pF Cin @25 ns τpeak	Up to 2 pC	15	1 MHz	< 1 ns	New Small Wheels Phase I upgrade project of the ATLAS	MPGD TPC	Brookhaven National Laboratory	130 nm
STS-XYTER2	128	Fully digital CSA+Shaper +Discri. +TDC +flash ADC	30	583 e +44 e/pF	15 fC	11	150 kHz	-	CBM experiment at FAIR center, Germany	silicon microstrip	AGH University of Science and Technology, Poland	180 nm
SECALROC3	4	Fully digital CSA+Shaper +S&H +SAR ADC +Disc. +TDC	200 to 800	1966 e +3.08 e/pF @ 1.68 μs τpeak	500 fC	35	4 MHz	< 125 ps @200 fC	ECAL	APD	NPU	180 nm
WASA	16	Fully digital CSA+Shaper +SAR ADC	160	569e+14.8e/pF	120 fC	4.94	-	-	CEPC experiment	MPGD TPC	Tsinghua	65 nm
-	64	Fully digital CSA+Shaper +SCA +Wilkinson ADC	70~1000	1100e @48 fC Range @20 pF Cin @70 ns τpeak	Up to 10 pC	20 @120 MSps	>75 kHz	< 1 ns @ 20 fC	STCF RICH PID	MPGD	USTC	180 nm
-	64	Fully digital CSA+Shaper + Disc. +SAR ADC	40	0.1 fC + 0.006 fC/pF	Up to 10pC	<5 mW	4 MHz	< 10 ns @ 2.5 fC Qin @ 35 pF Cin	STCF ITKW	MPGD	USTC	180 nm
-	8	Fully digital CSA+Shaper +Disc. +SAR ADC	180 to 900	-	Up to 10 pC	-	-	-	-	-	IMP	-

Analog readout

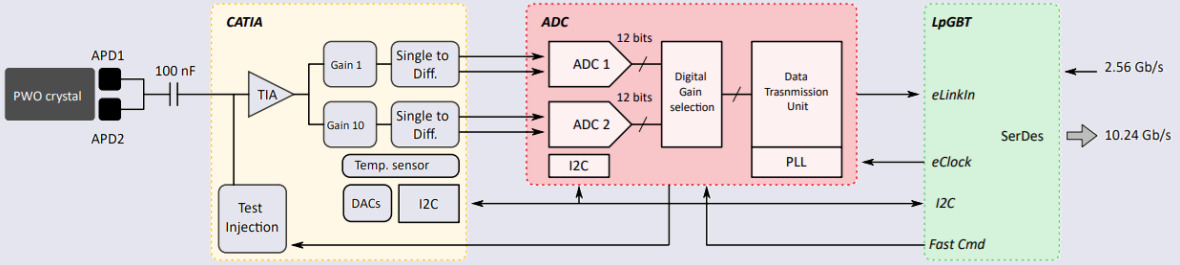
① CATIA

Channels: 128

Dynamic range: 20 fC

Noise: 270 e- + 38 e-/pF

Power: 2.7 mW/ch



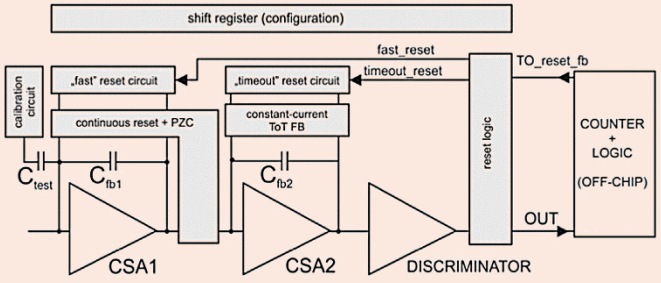
② AGH University of Science and Technology

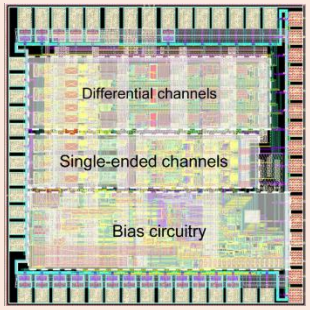
Channels: 2

Dynamic range: 15 fC

Noise: 278.2 e- + 26 e-/pF

Power: 8.7 mW/ch





On-chip discrimination

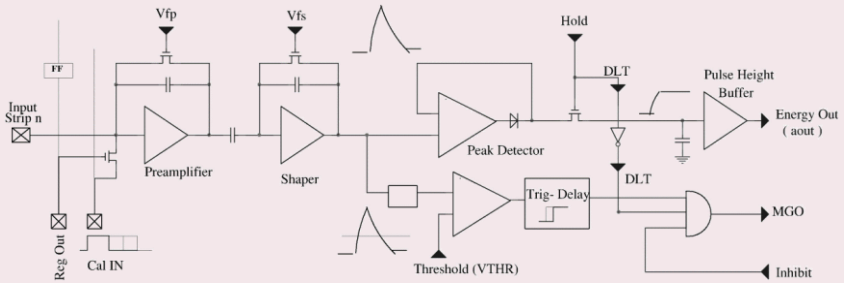
① XAA1.2

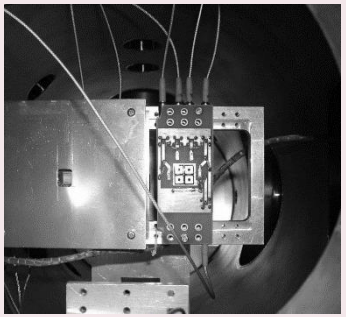
Channels: 128

Dynamic range: 5 fC

Noise: 935 e- @ 30 pF Cin

Power: 1 mW/ch





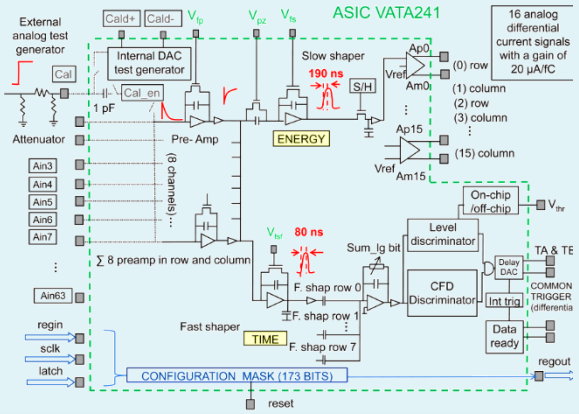
② VATA241

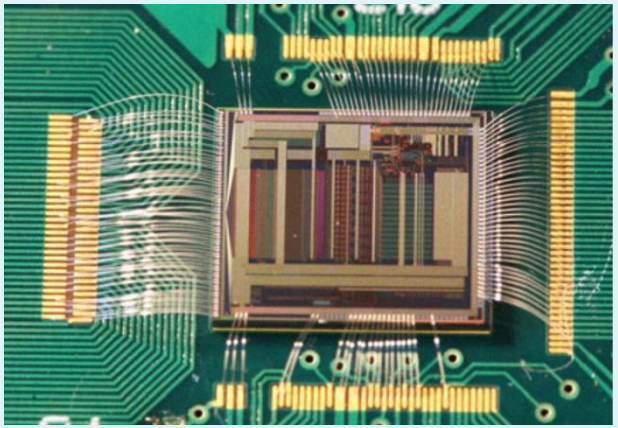
Channels: 128

Dynamic range: 15 fC

Noise: 583 e- + 44 e-/pF

Power: 8 mW/ch





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Semi-digitization

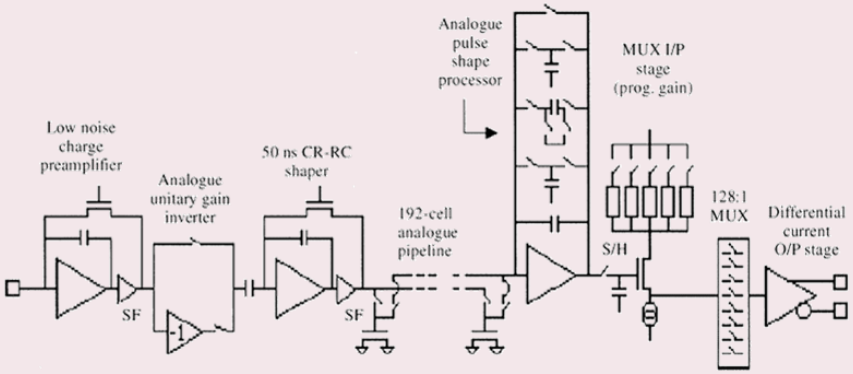
① APV25

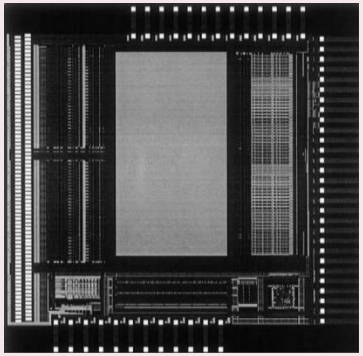
Channels: 128

Dynamic range: 20 fC

Noise: 270 e- + 38 e-/pF

Power: 2.7 mW/ch





② AGET

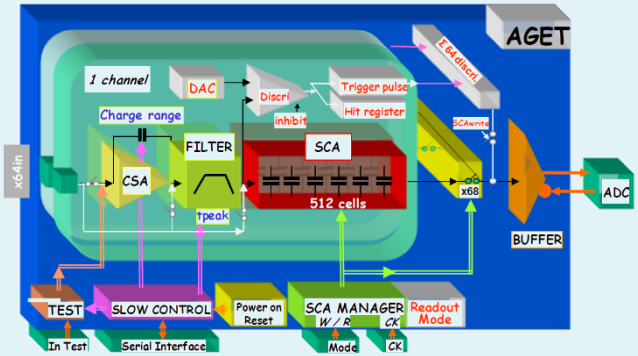
Channels: 64

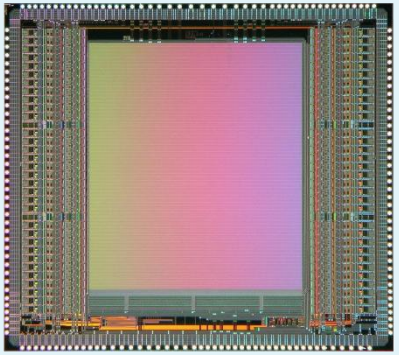
Dynamic range: Up to 10 pC

Noise: (435~34000) +(19~7.4) e-/pF

Power: 10 mW/ch

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Fully digitization

① VMM3

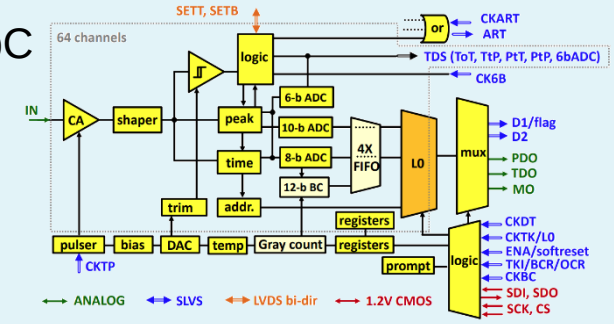
Channels: 64

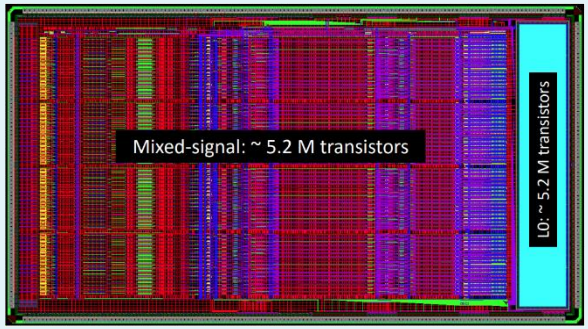
Dynamic range: Up to 2 pC

Noise: 2280 e-

@110 fC range
@100 pF Cin
@25 ns тpeak

Power: 15 mW/ch





② SAMPA

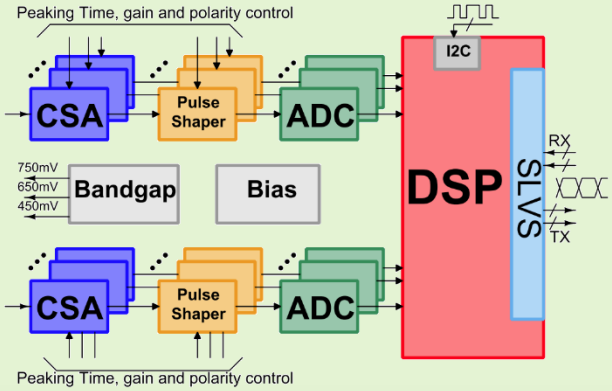
Channels: 32

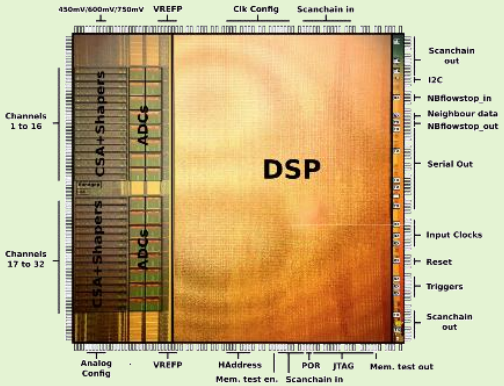
Dynamic range: 500 fC

Noise: < 1600 e-

@80 pF Cin

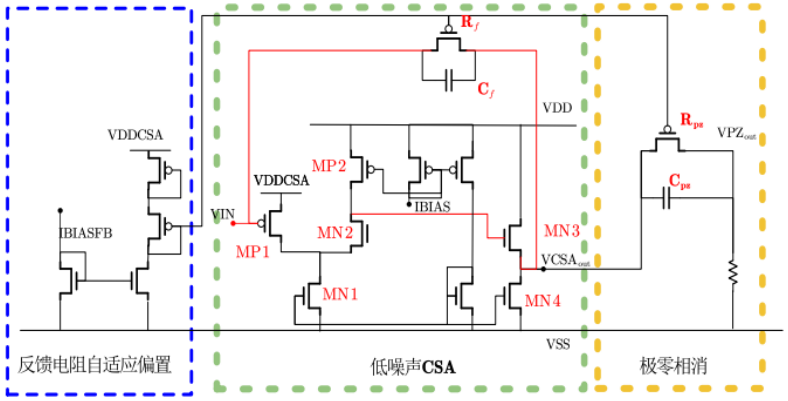
Power: 8 mW/ch

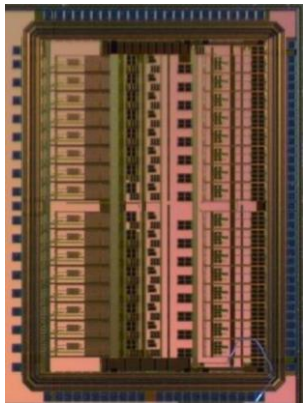


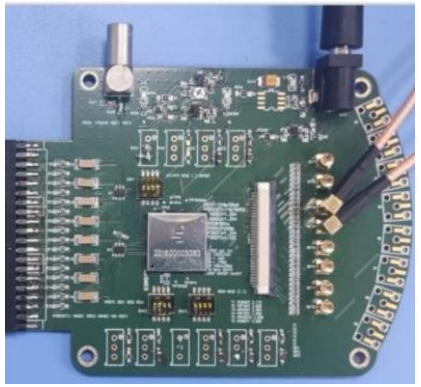


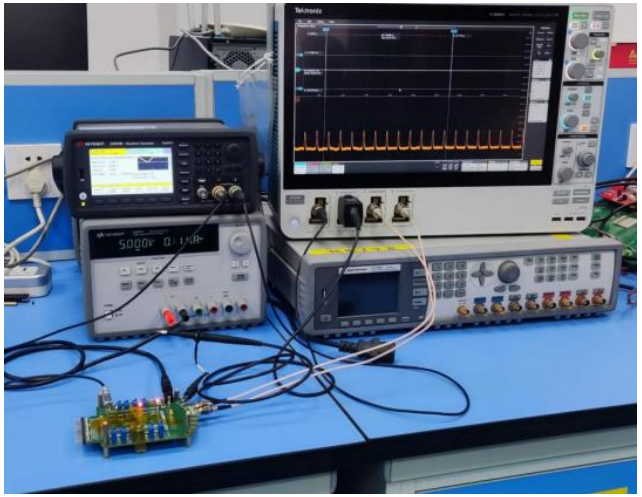
FEAT ASIC

- FEAT: Front-End ASIC for TPC
- CSA + pole-zero cancellation + shaping + driver





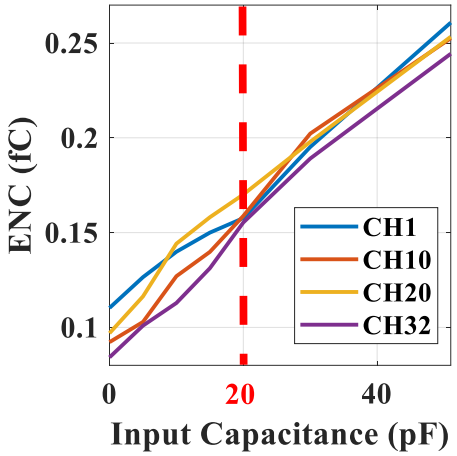




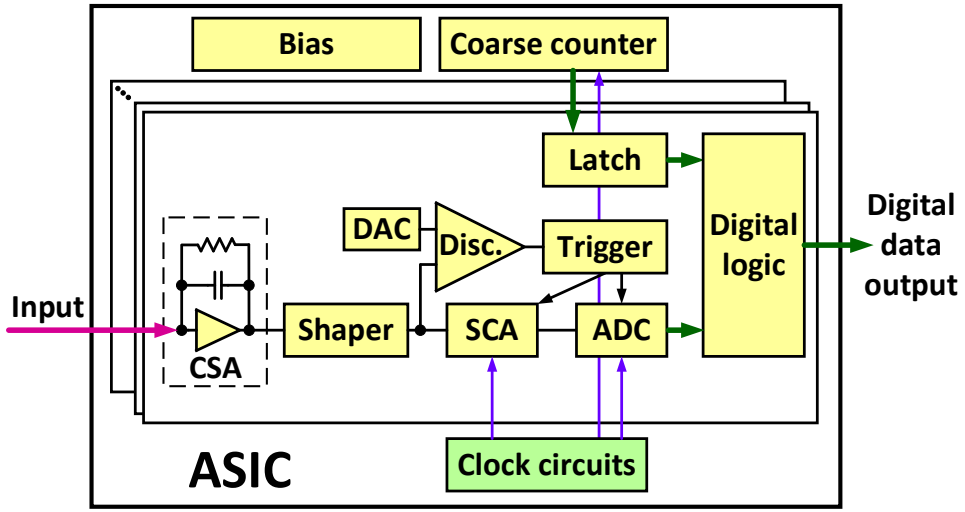
Parameter	Value
Channels	16
Gain	0.1mV/fC 1mV/fC 5mV/fC 10mV/fC
Peaking time	80ns/160ns
Noise	2974e-@20pF@800fC
Counting rate	1 MHz @60% range
Power	9.6mW/ch single-ended, 15mW/ch differential

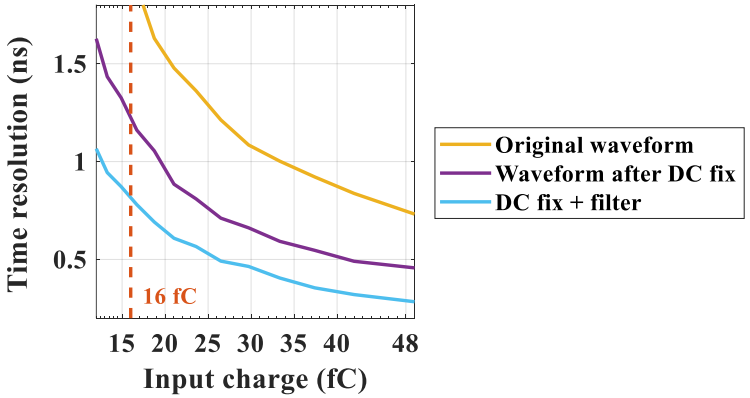
High density full digitization readout ASIC

- A 64-channel mixed-signal readout ASIC integrating front-end analog circuit and on-chip ADC has been developed.
- Fully digital output, the chip feeds data directly to an FPGA.
- Supports both self-trigger and external-trigger modes; waveform readout and time/charge readout.



ENC @ 70 ns @ 48 fC range





Timing precision @ 48 fC range @ 20 pF

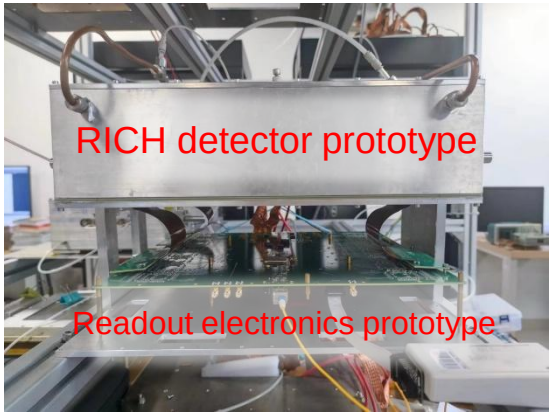
High density full digitization readout ASIC

- Based on the prototype ASIC, a readout module integrating 1024 channels has been designed.

Channels per chip	64 channels
Charge measurement range	48 fC, 240 fC, 2 pC, 10 pC (configurable)
Shaping time	70 ns, 200 ns, 400 ns, 1 μs (configurable)
ENC	0.1 fC + 0.004 fC/pF @ 70 ns @ 48 fC range
Timing precision	≤ 1 ns @ Q_{in} > 1/3 full scale @ 20 pF C_{in}
Event rate per channel	> 75 kHz



- Radioactive source (^{55}Fe) test was carried out with a prototype PIDB detector.



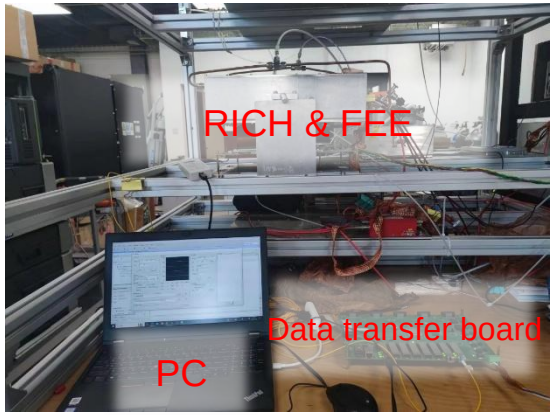
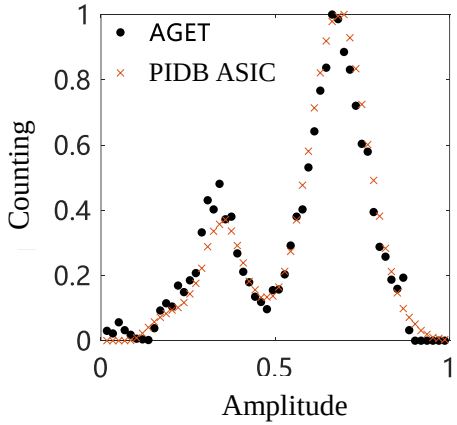


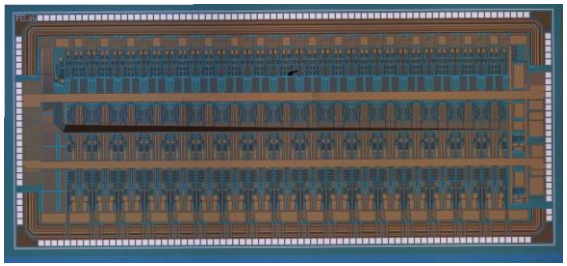
Photo of the test setup

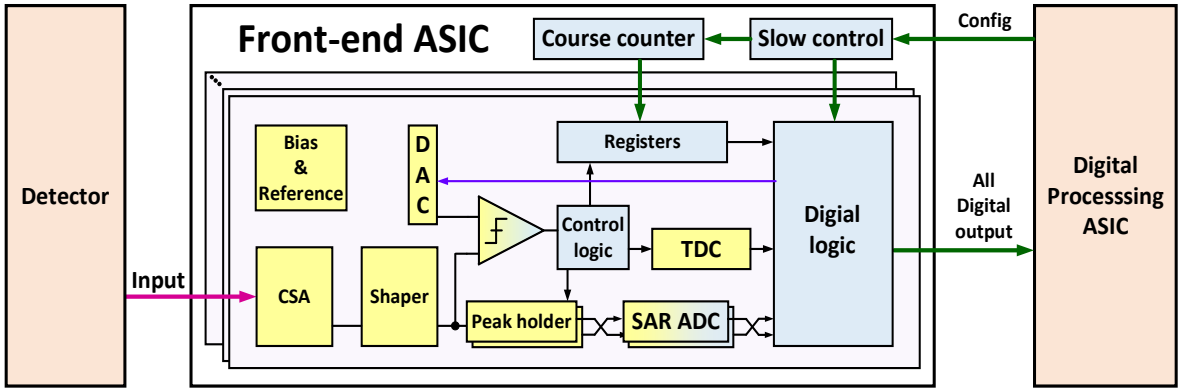


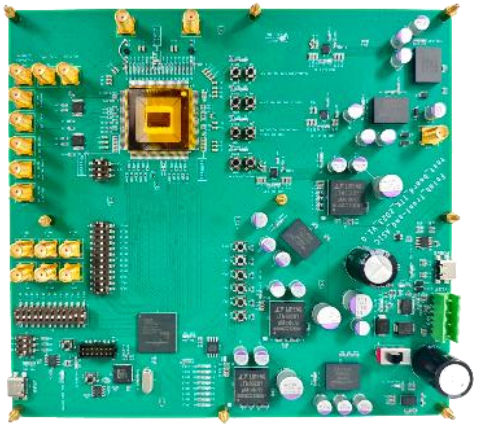
Measured ^{55}Fe energy spectrum

High hit rate full digitization readout ASIC

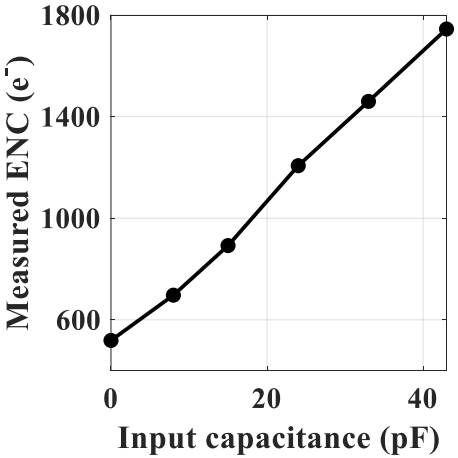
- A 32/64-channel high hit rate readout ASIC with fully digital output has been developed for the MPGD.
- Charge Sensitive Amplifier + Shaper for low-noise and high-gain amplification.
- Peak holder + Analog-to-Digital Converter (ADC) for charge measurement.
- Discriminator + Time-to-Digital Converter (TDC) for time measurement.
- **Event rate per channel: 4 MHz**



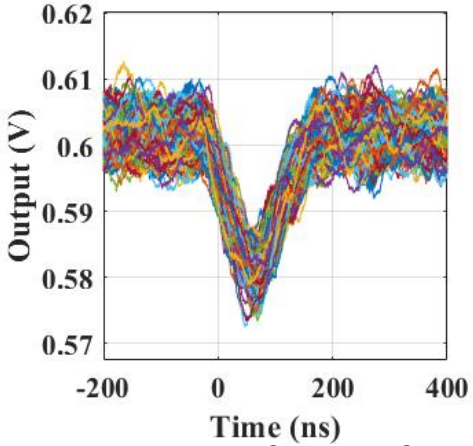




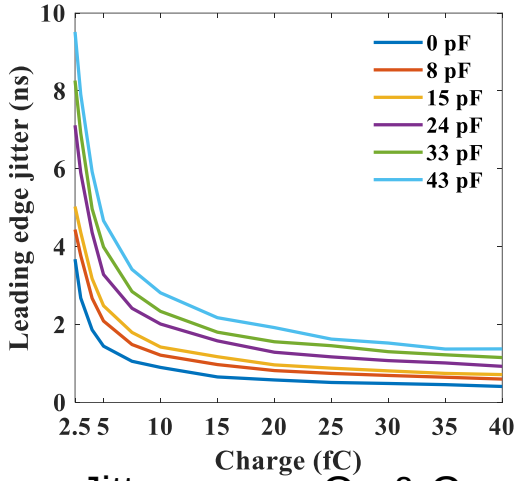
High hit rate full digitization readout ASIC



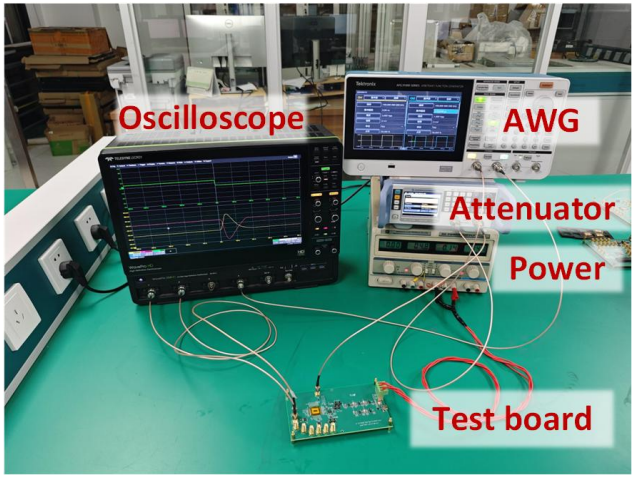
ENC versus Cin



1000 Outputs for 2.5 fC signal
@ 33 pF C_{in}@ 75 ns



Jitter versus Q_{in} & C_{in}
@ 75 ns charge collection time



Channels per chip	64
Charge measurement range	2.5 fC to 40 fC
Shaping time	40 ns
ENC	0.1 fC + 0.006 fC/pF
Charge resolution	< 1 fC @ 35 pF C_{in}
Timing precision	< 10 ns @ 2.5 fC Q_{in} @ 35 pF C_{in}
Event rate per channel	> 4 MHz
Power per channel	< 5 mW

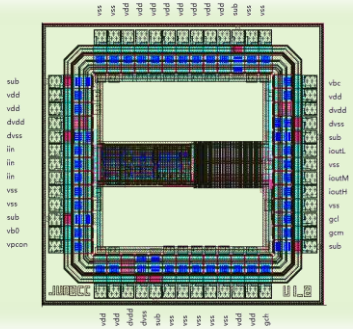
Charge measurement with a large dynamic range

① JUNOCC (IHEP, deployed)

Dynamic range (PMT gain 10^7): 1 – 4000 p.e.

Noise: 0.05 pe

Range: 3 V; input impedance: 1 Ω @ <10 MHz





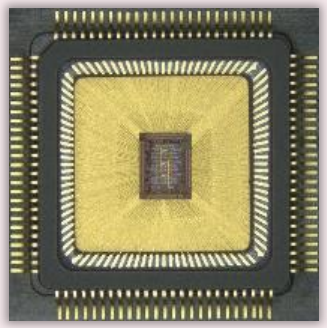
② PASC (USTC, deployed)

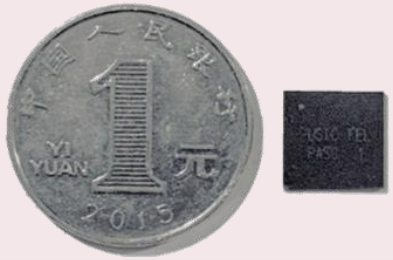
Dynamic range: 1–4000 p.e.

Charge accuracy: <10% @1 p.e.

Time resolution: <300 ps

Dead time: <600 ns





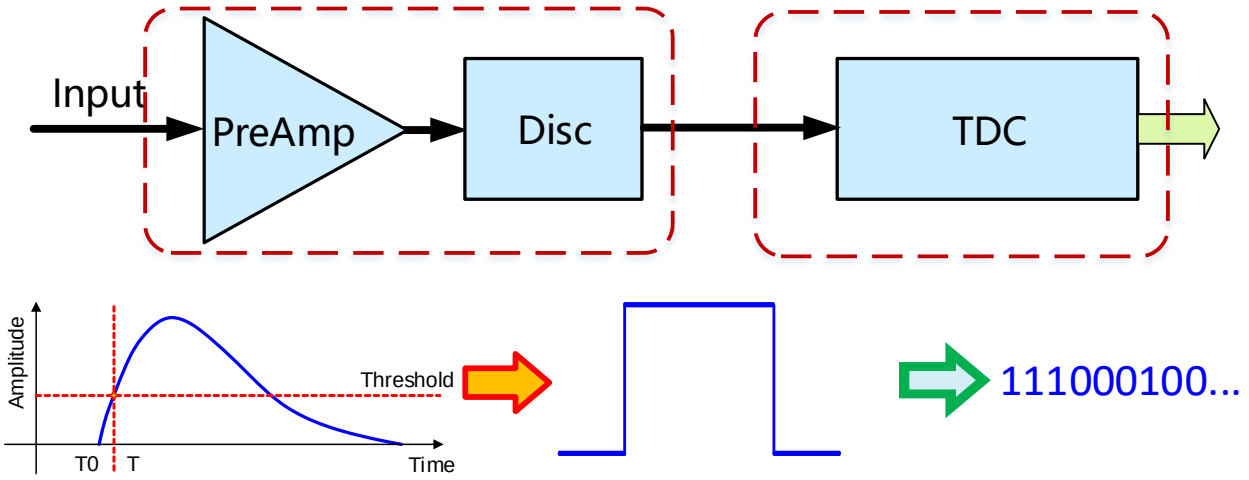


Outline

- Precision front-end measurement
  - High-precision charge measurement
  - High-precision time measurement
  - High-speed waveform digitization
  - Silicon pixel detector readout
- Data aggregation and transmission
  - High-speed interface circuits
  - Data aggregation
  - Optical signal transceiver

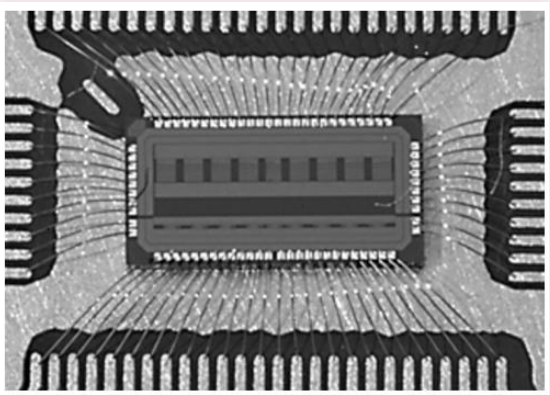
High-precision front-end time measurement

- Typical technical routes:



- Timing circuits
  - Discrete devices: high-speed discriminators
  - ASICs: NINO, PADI, ...
- Time digitization (TDC)
  - FPGA TDC
  - ASIC TDC

International discriminator ASICs — NINO, PADI, FastIC

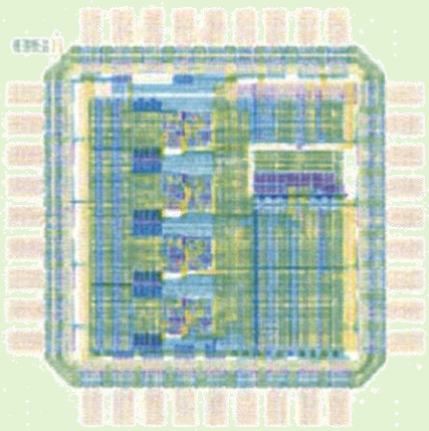


① NINO

Applications:

MRPC readout

250 nm CMOS, 8 channels



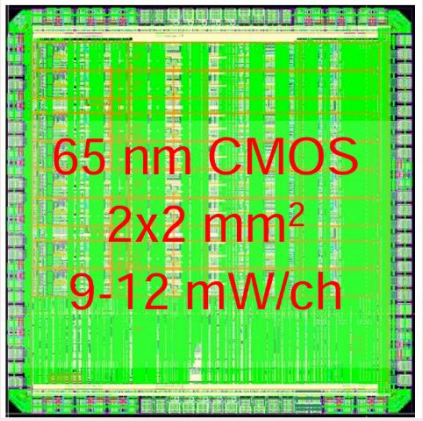
② PADI

Applications:

MRPC readout

Diamond detector readout

180 nm CMOS, 4 channels



③ FastIC

Applications:

PMT readout

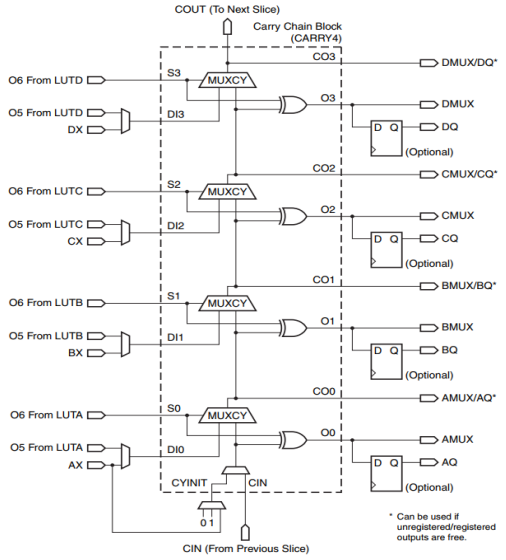
MCP readout

SiPM readout

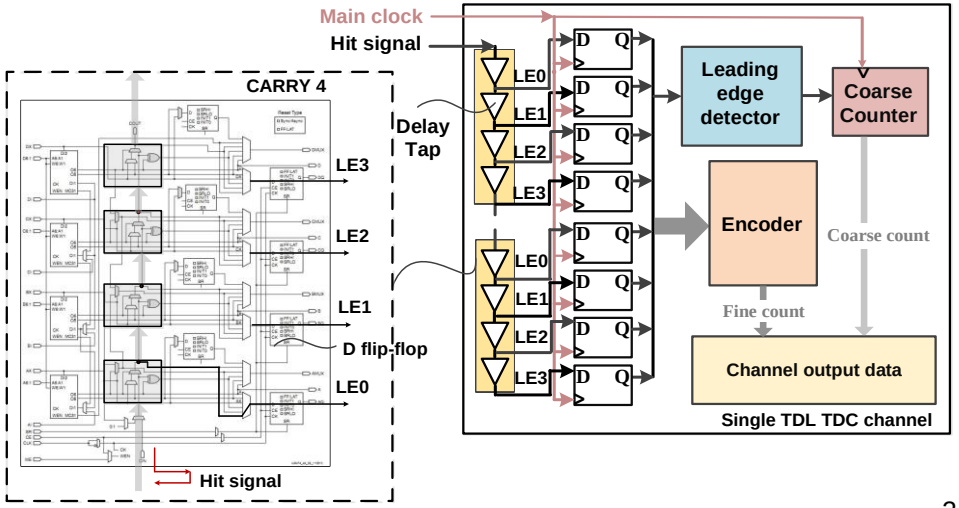
65 nm CMOS, 8 channels

FPGA TDC

- Delay lines built from dedicated FPGA carry chains
- Improved resolution
  - Advanced devices such as UltraScale
  - Averaging over multiple delay chains
  - Wave Union and similar techniques
- Achievable resolution
  - <5 ps RMS



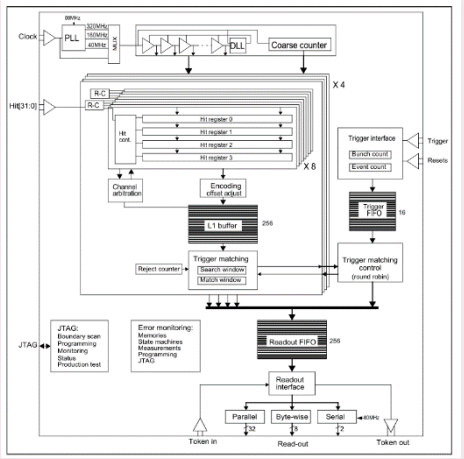
Carry chain

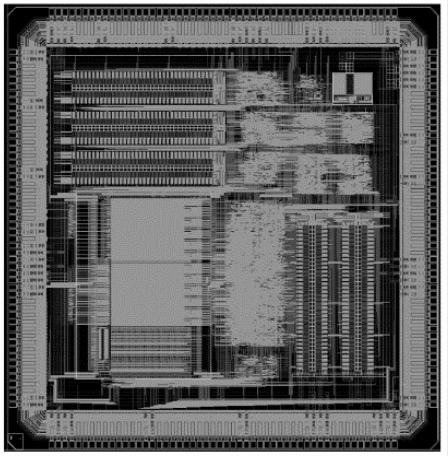


Typical TDC ASIC — HPTDC

ASIC specs

Architecture: delay line
Channels: 32
Process: 250 nm
LSB: 25/100 ps
Resolution: ~20 ps
Power: 450–1500 mW





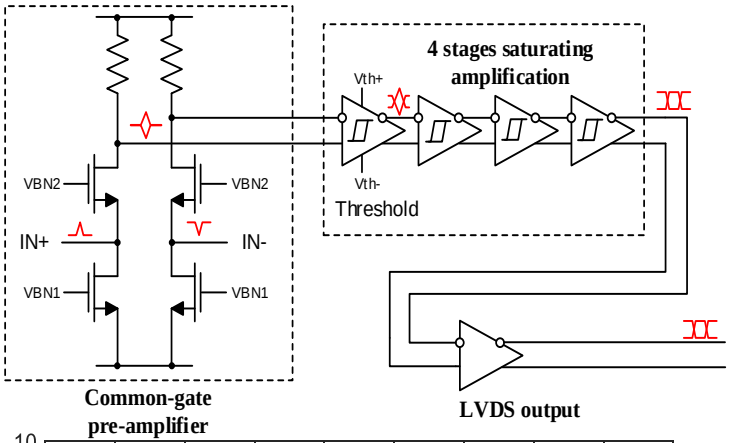
Applications

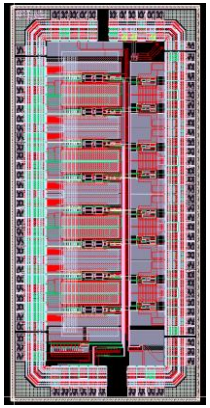
- ALICE
  - ✓ Used in the TOF TRM
  - ✓ 20 ps resolution
- BES III
  - ✓ Used in the TOF
  - ✓ 20 ps resolution
- HIRFL-CSR
- ATLAS
- HADES

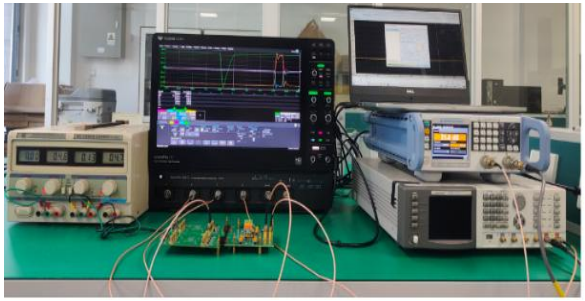


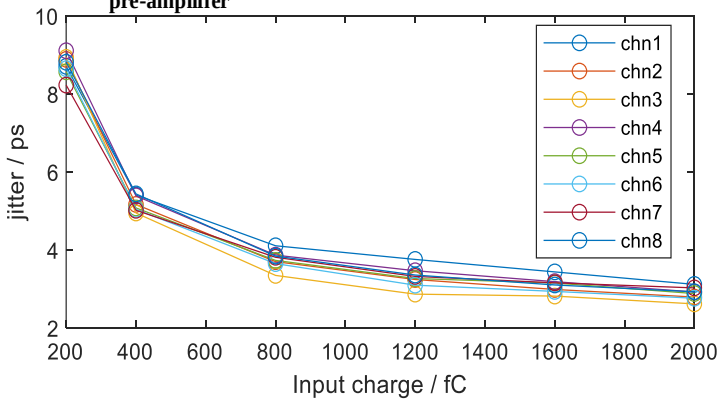
DISA ASIC

- Differential current(I) Saturation Amplifier （DISA）
- High-precision time measurement for MRPC detector
- High-speed amplification and discrimination ASIC
  - **The jitter is better than 10 ps**





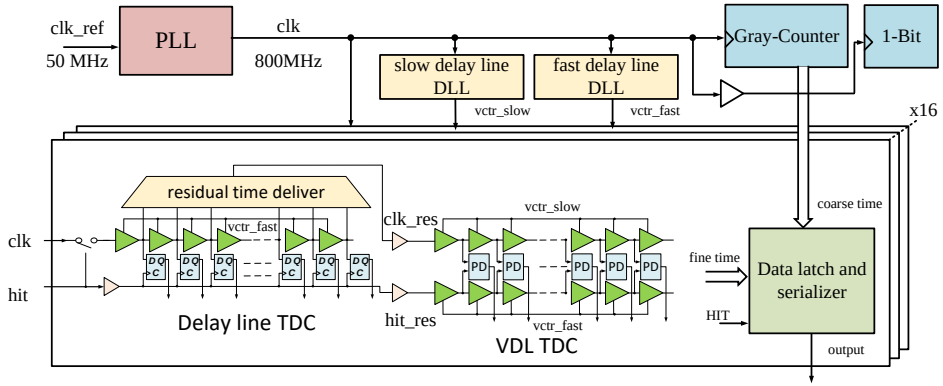




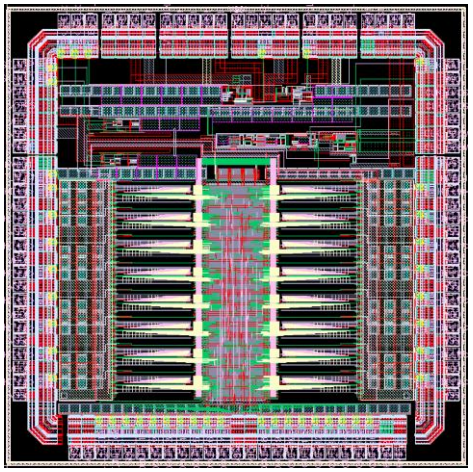
Parameter	Performance
CMOS process	180nm
Number of channels	8
Input impedance (Ω)	40~200
Jitter (ps, RMS)	<10
Power consumption (mW / chn)	<25

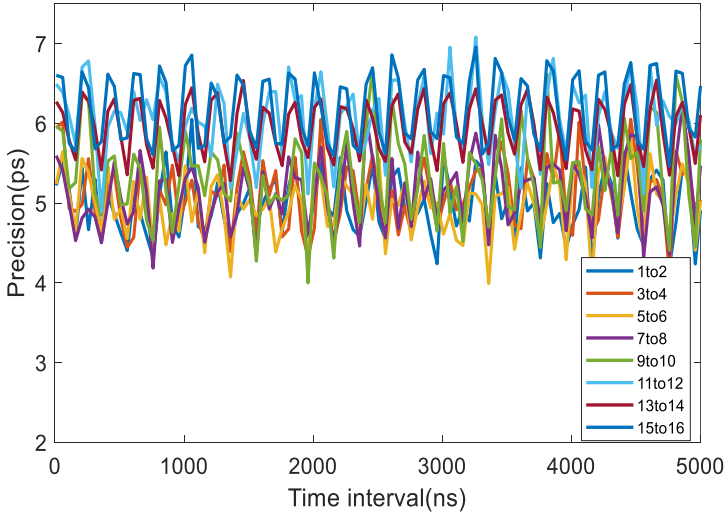
High-precision TDC ASIC

- Two-stage interpolation to achieve fine resolution
  - Delay Line + Vernier Line
- Time precision < 10 ps



Parameters	Performance
Chn. No.	16
Precision	<8 ps
Dynamic Range	5120 ns
Power/chn	<10 mW

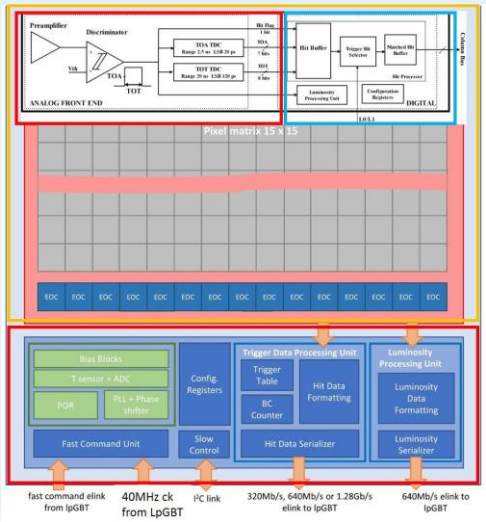


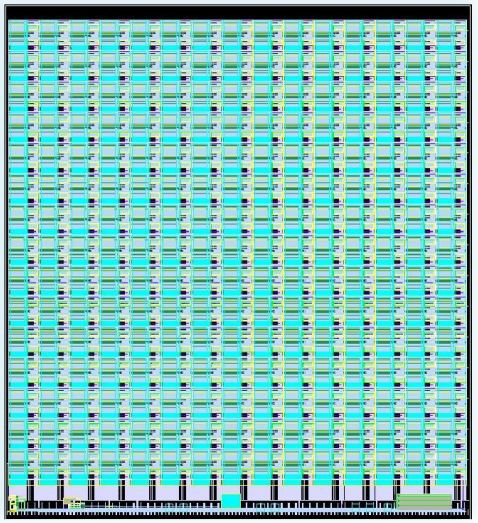


LGAD (Low-Gain Avalanche Detector) readout ASIC

ALTIROC

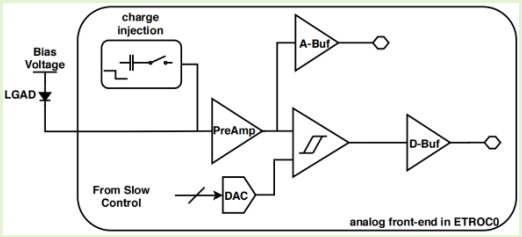
LGAD readout for the ATLAS experiment
Function: Amp. + Disc. + TDC
Process: 130 nm
Channels: 5×5 (V1), 15×15 (V2)
LSB: ~20 ps (TOA)
Resolution: ~20 ps @ 10 fC (TOA)
Size: 20 mm × 22 mm (V2)

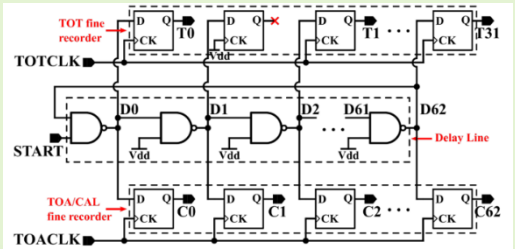


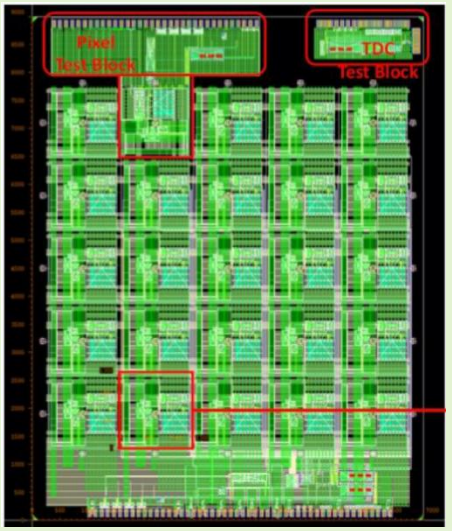


ETROC (Fermilab)

LGAD readout for the CMS experiment
Function: Amp. + Disc. + TDC
PA：Cascode + Source Follower
Process: 65 nm
TDC：Delay chain TDC(15 ps LSB)
Jitter：~20 ps @ 10 fC



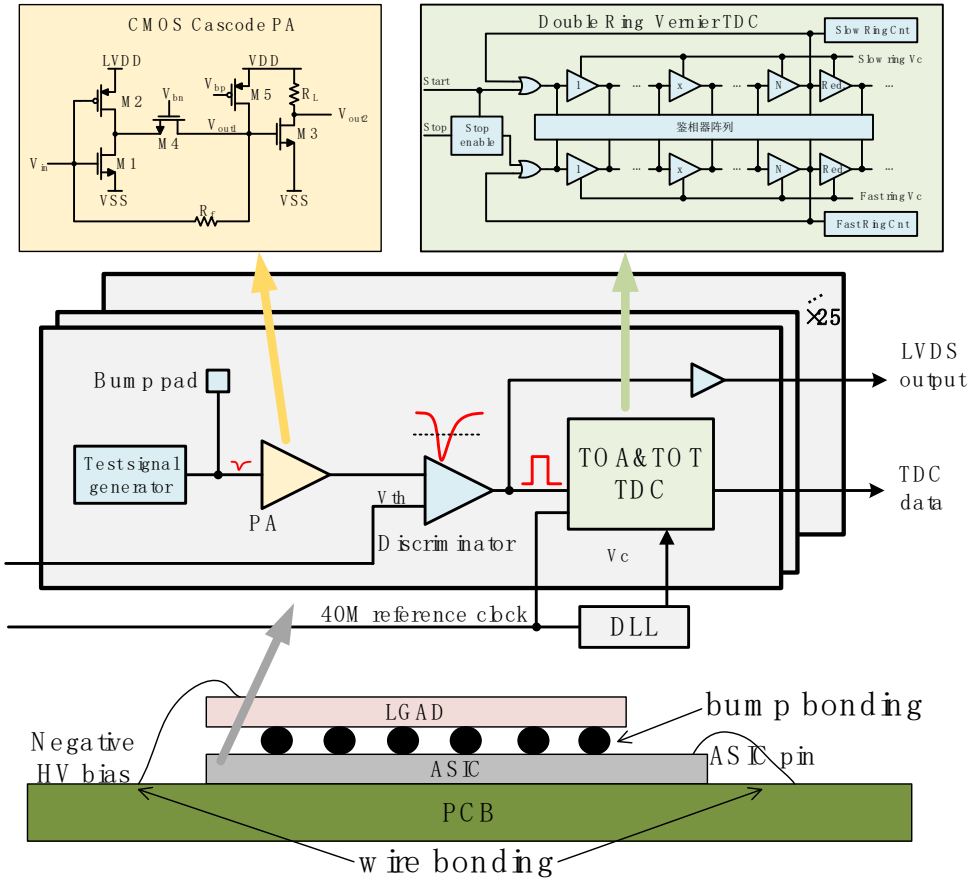




Example of domestic readout ASIC: LATIC

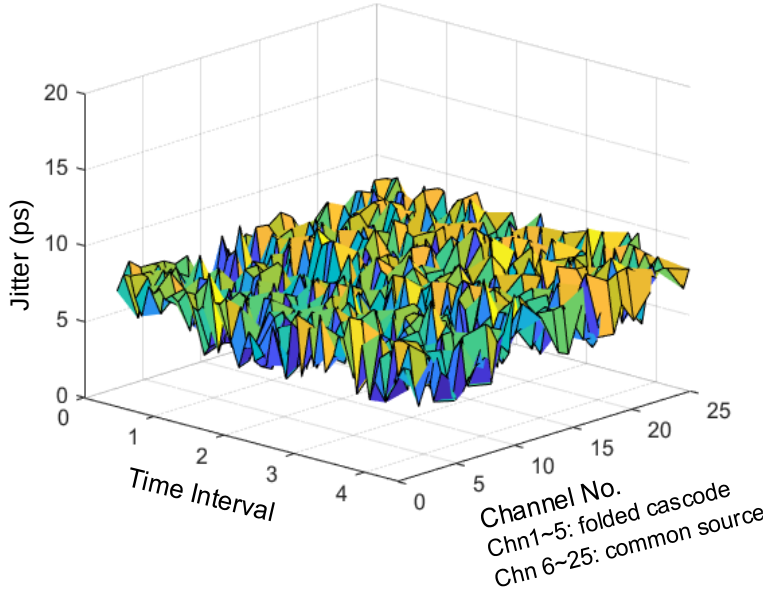
LATIC: LGAD Amplification and Timing IC (Designed by USTC group)

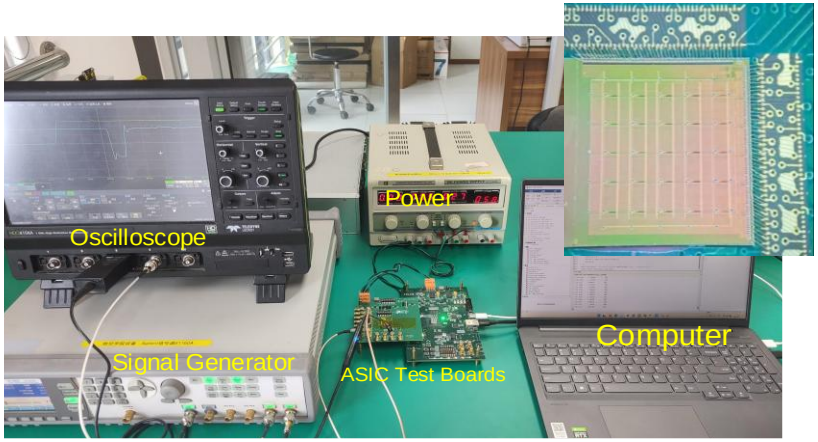
- Design Target
  - To achieve high time precision front-end digital readout at low power consumption
- Core functions
  - Preamplifier
  - Discriminator
  - Time to Digital Converter
- Research progress
  - Finished the design of AFE ASIC and TDC ASIC, separately
  - Finished the design of 5×5 array full functional chip

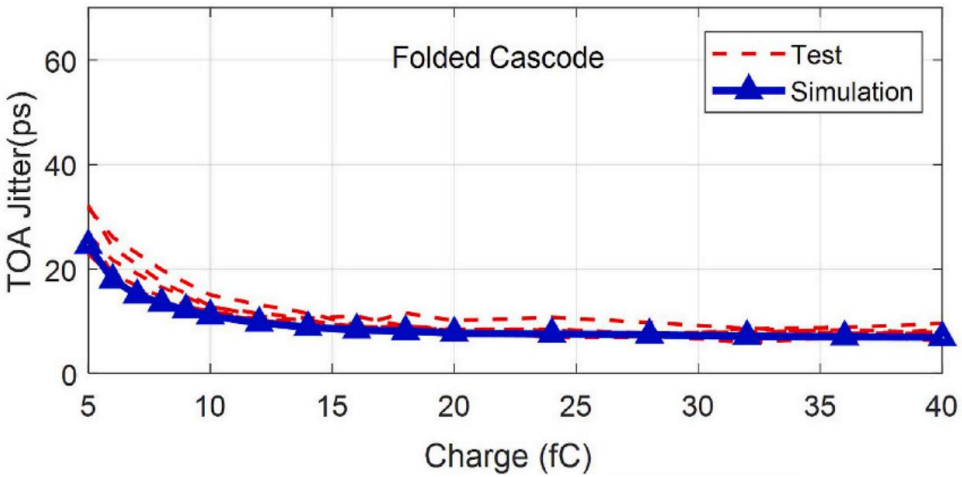


LATIC

- LATIC Performance
  - TDC：Double Ring Vernier TDC
    - ~ 5 ps time precision
  - Jitter of AFE + TDC
    - < 20 ps @ 10 fC, 4 pF
    - < 10 ps @ large signal (>15 fC)
  - Power consumption per channel: 3 mW

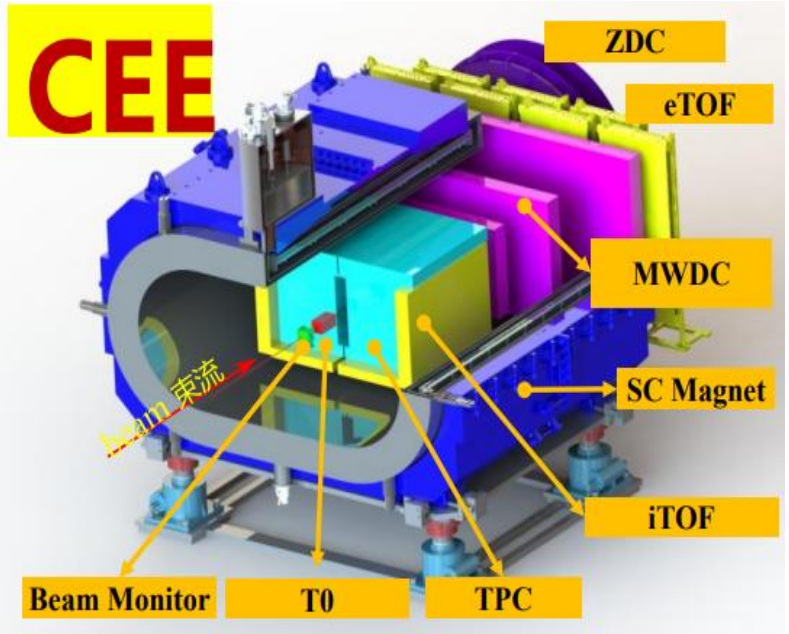






CEE electronics

- NSFC National Major Research Instruments: CEE
- Responsible for the TOF readout electronics, MWDC back-end digitization and the CEE clock system; the FPGA TDC was used to reach 10 ps system timing.

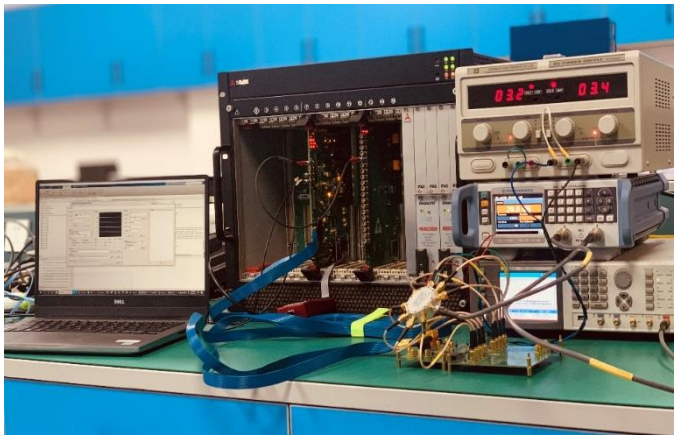


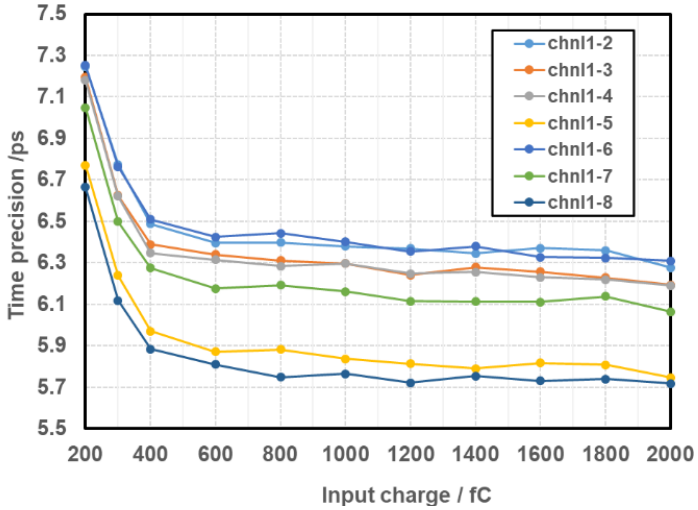
NSFC National Major Research Instrument Program

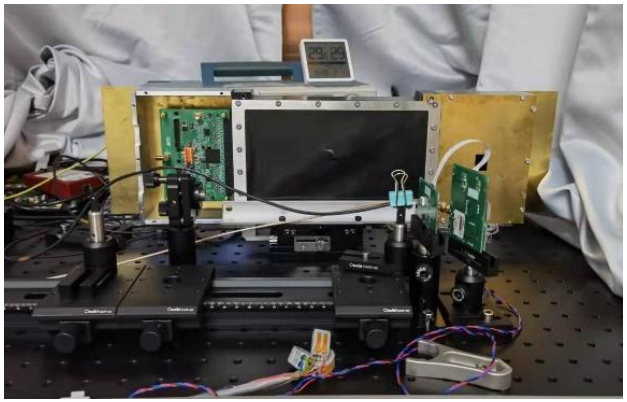
- Start-time detector (T0)
  - 32 readout units
  - 50 ps intrinsic time resolution (<250 ps per channel)
- Internal time-of-flight detector
  - Internal time-of-flight, iTOF
  - ~1500 readout units
  - 400 channels, ~30 ps intrinsic time resolution
  - Others, ~50 ps intrinsic time resolution
- Endcap time-of-flight detector
  - Endcap time-of-flight, eTOF
  - ~1344 readout units
  - 60 ps intrinsic time resolution

TOF readout electronics

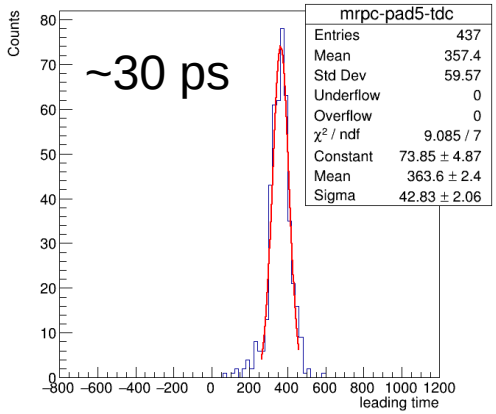
- Better than 10 ps with NINO ASICs and an FPGA TDC







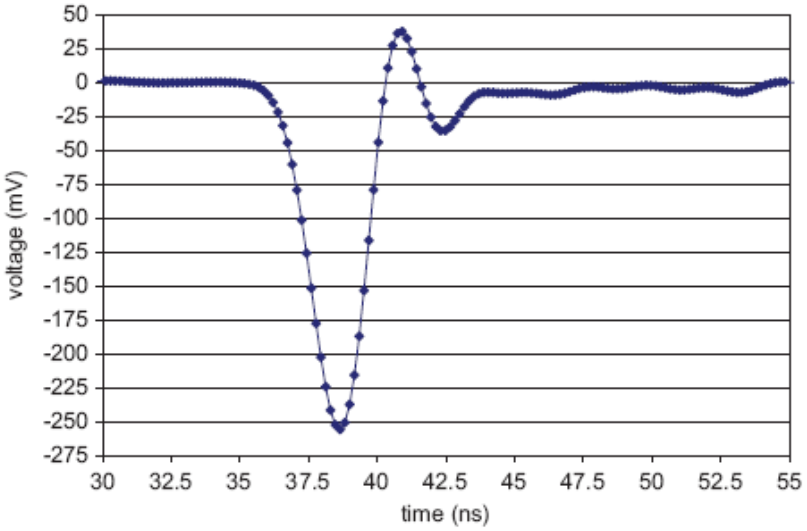




Outline

- Precision front-end measurement
  - High-precision charge measurement
  - High-precision time measurement
  - High-speed waveform digitization
  - Silicon pixel detector readout
- Data aggregation and transmission
  - High-speed interface circuits
  - Data aggregation
  - Optical signal transceiver

High-speed waveform digitization



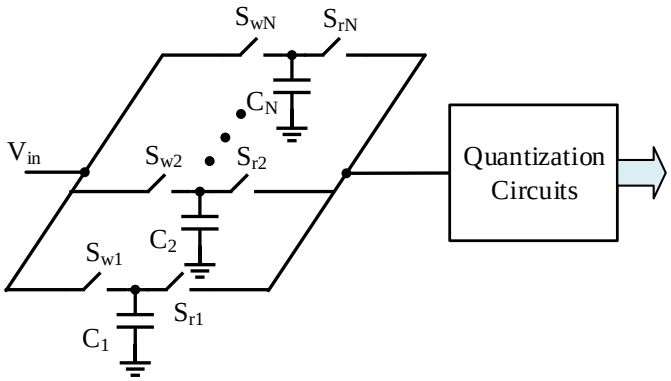
- Advances in analog-to-digital converters (ADCs) make very high-speed waveform digitization feasible
- Sampling rate ~ Gsps

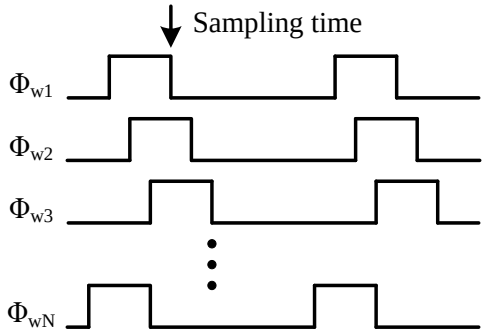
- Waveform leading-edge analysis:
  - ⇨ time information
- Digital integration (area):
  - ⇨ charge information

- Advantages over conventional time and charge measurement:
  - ◇ Get original waveform information as fully as possible
  - ◇ Handles arbitrary and irregular waveform signals

Switched Capacitor Array

- Switched capacitor array (SCA) enables very high-speed analog waveform sampling





- The principle is to separate high-speed sampling from quantization
  - Very high-speed sampling is performed by the switched capacitor array, and a slower quantizer then digitizes the stored samples
- This is suitable for the nuclear and particle experiments
- It avoids the complexity and power consumption of very high-speed ADCs and the need for extra buffers and interfaces

Typical SCA ASICs

Chip	Process	Sampling Rate(Gsps)	Sampling Depth	Input Type	On-chip Digitization	Noise	Chn. No.	Power mW/ch
ARS1	800 nm	~ 1	128	Single-ended	8 bits	4 mV	4	47.5
MATACQ	800 nm	~ 2	20 x 128	Single-ended	/	< 0.2 mV	1	/
SAM	350 nm	~ 2	16 x 16	Single-ended	/	0.7 mV	2	150
ATWD	200 nm	~ 2	128	Single-ended	10 bits	1 mV	4	37.5
LABRADOR3	250 nm	~ 4	260	Single-ended	12 bits	1.3 mV	9	/
DRS4	250 nm	~ 5	1024	Differential	/	0.35 mV	9	17.5 @2 GSps
PSEC4	130 nm	~ 10	256	Single-ended	12 bits	0.7 mV	6	16.7
SAMPIC	180 nm	~ 5	64	Single-ended	11 bits	< 1 mV	16	11.25
IHEP+Tsinghua +USTC	180 nm	~ 1	256	Single-ended	12 bits	/	8	/
FEEWAVE（IHEP）	180 nm	~ 5	256	Differential	10 bits	< 1 mV	6	25
CCNU	130 nm	~ 2	256	Single-ended	/	4.96 mV	4	/
USTC	180 nm	~ 14	512	Differential	12 bits	0.87 mV	8	/

International SCA — analog readout

- **DRS4**

Channels: 9

Input type: differential

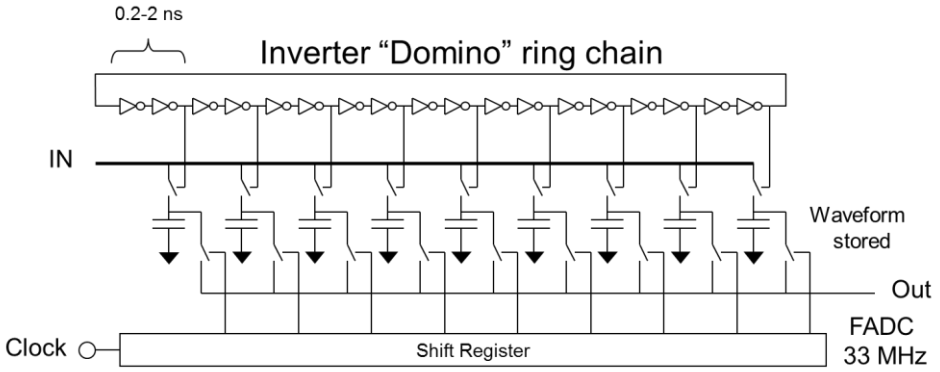
Sampling rate: ~5 Gsps

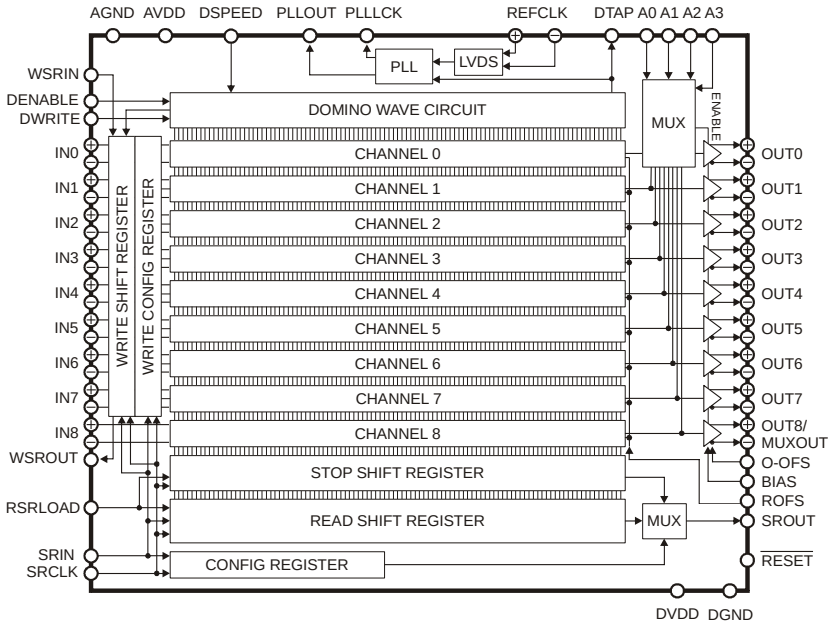
Sampling depth: 1024

Input dynamic range: 1 V

Noise: 0.35 mV

Power: 140 mW





International SCA — digital readout

➢ PSEC4

Channels: 6

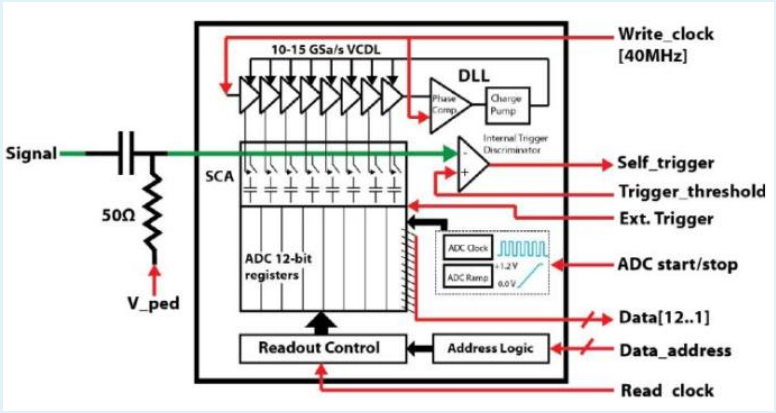
Sampling rate: ~10 Gsps

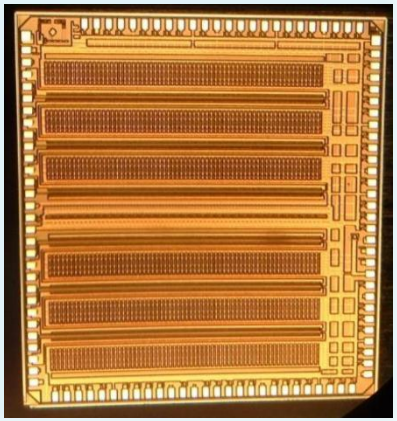
Sampling depth: 256

Input dynamic range: 1 V

Noise: 0.7 mV

Power: 100 mW





➢ SAMPIC

Channels: 16

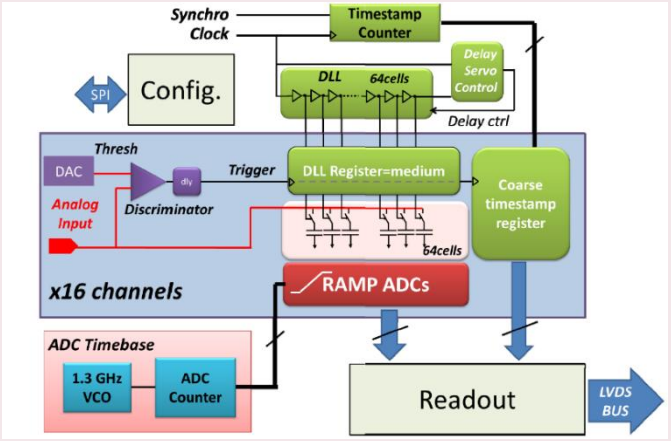
Sampling rate: ~5 Gsps

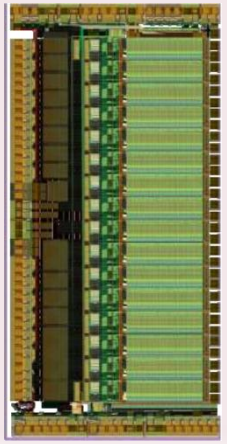
Sampling depth: 64

Input dynamic range: 1 V

Noise: <1 mV

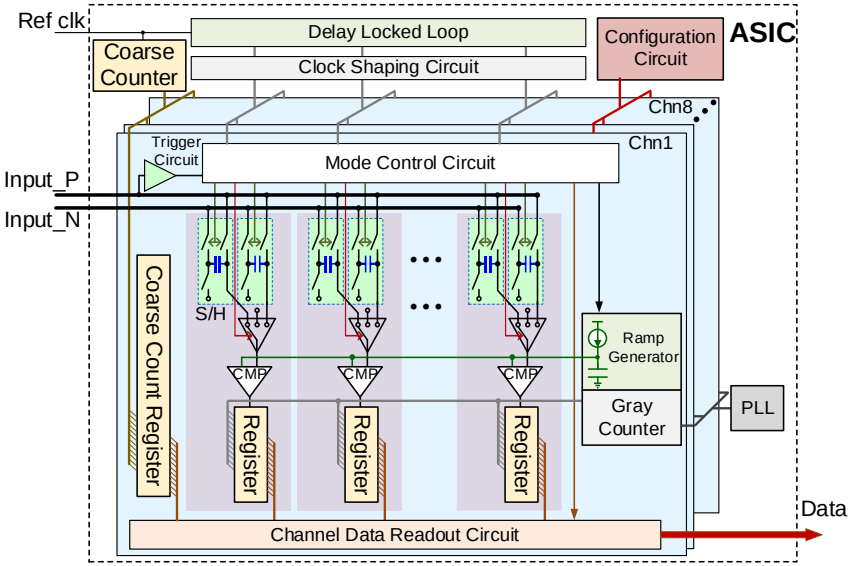
Power: 180 mW

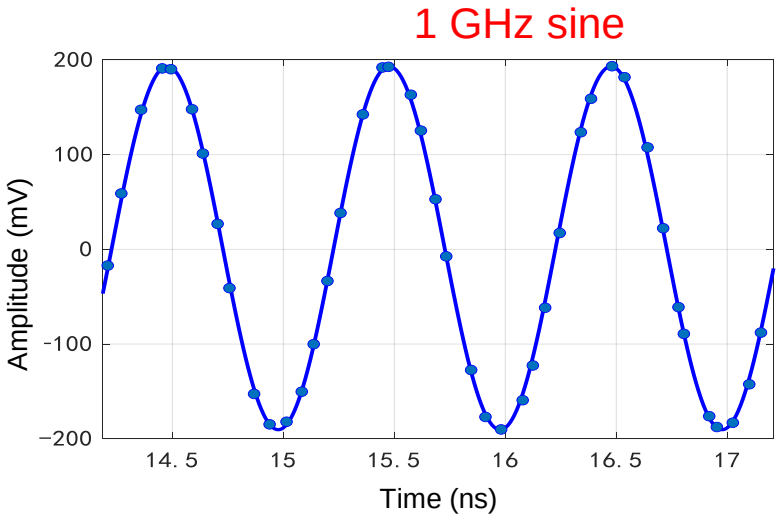


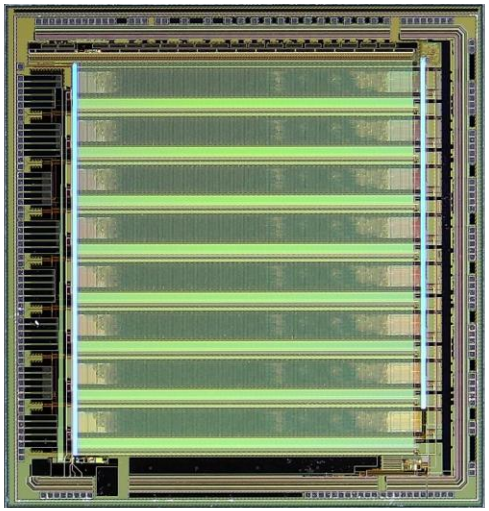


Example of Domestic SCA

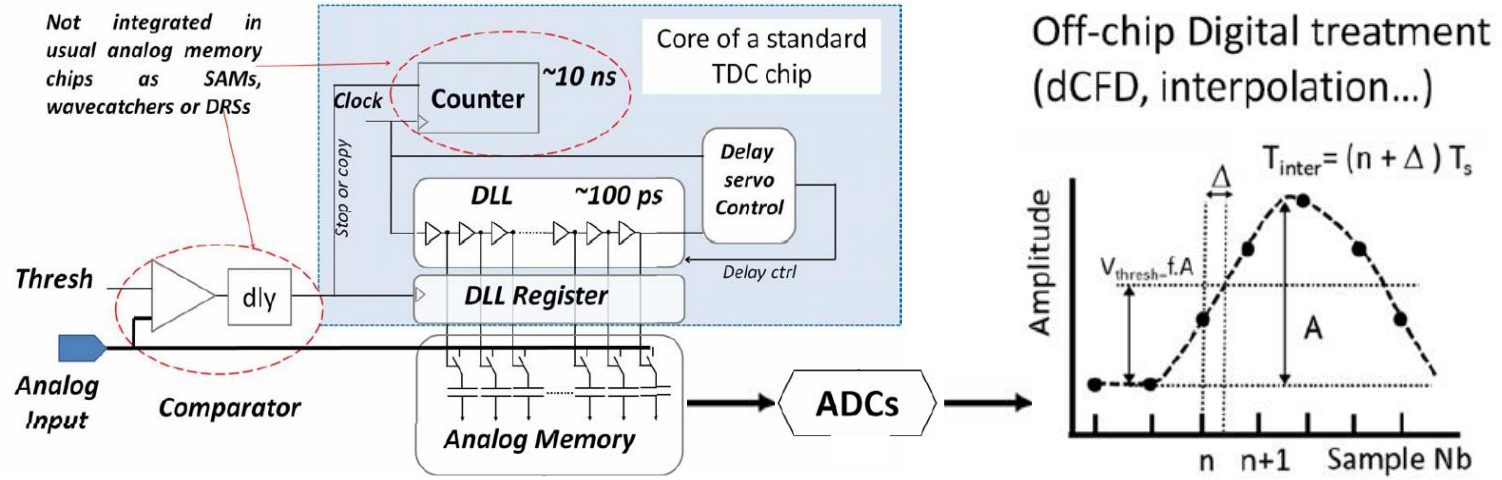
- Channels: 8
- Input type: differential
- Sampling rate: ~14 Gsps
- Sampling depth: 512
- Input dynamic range: 1.4 V
- Readout: digital
- Quantization: 12 bits
- Noise: <1 mV

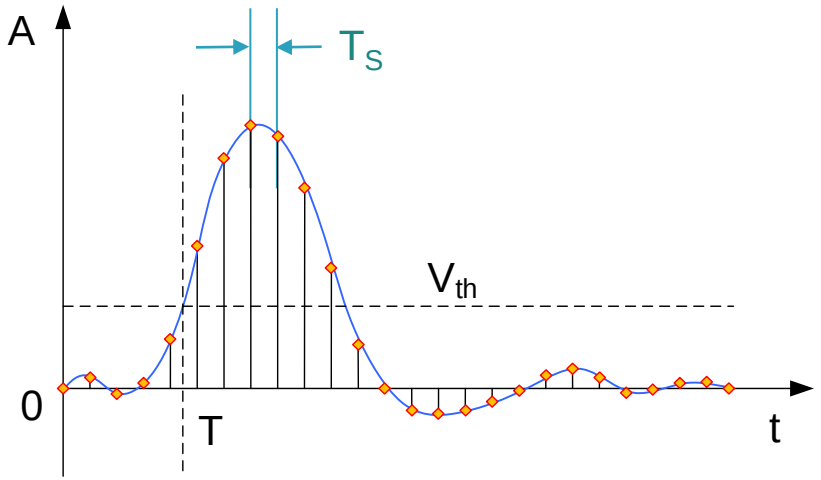






SCA for high-precision timing

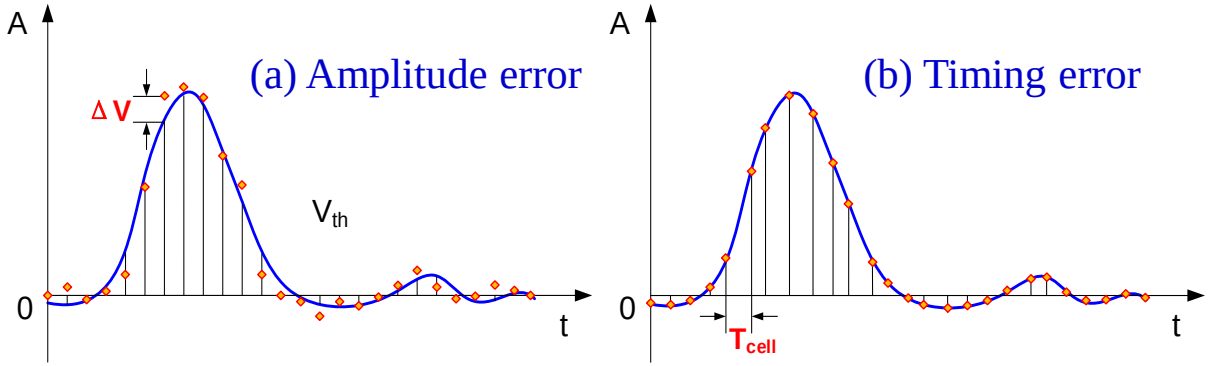




- High-speed sampling of the detector waveform allows the signal time to be extracted by numerical fitting.
- Raising the sampling rate f_S improves timing precision, and numerical fitting can reach a precision better than the sampling period $T_S = 1/f_S$.

Calibration algorithms for SCA

- The sample-and-hold cells in an SCA are not identical, so calibration and correction methods must be developed.
- Global timing calibration

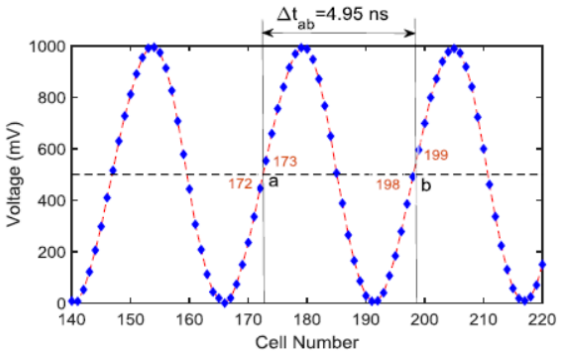


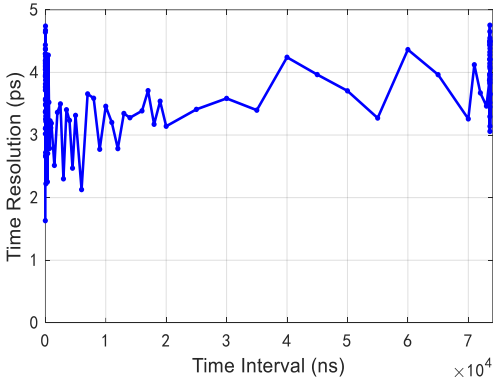
- Overdetermined linear equations-based calibration

$$\alpha \Delta t_{n_1} + \sum_{i=n_1+1}^{n_2-1} \Delta t_i + \beta\, \Delta t_{n_2} = T_S$$

$$\alpha = \frac{V_{n_1+1} - V_{DC}}{\Delta V_{n_1}}, \beta = \frac{V_{DC} - V_{n_2}}{\Delta V_{n_2}}$$

$$\begin{pmatrix} 0 & \cdots & 0 & \alpha_1 & 1 & \cdots & 1 & \beta_1 & 0 & \cdots & 0 \\ 0 & \alpha_2 & 1 & \cdots & 1 & \beta_2 & 0 & 0 & 0 & \cdots & 0 \\ \cdots & 1 & \beta_3 & 0 & 0 & \cdots & 0 & 0 & \alpha_3 & 1 & \cdots \\ & & & & & \vdots & & & & & \\ 1 & \cdots & 1 & \beta_M & 0 & 0 & \cdots & 0 & \cdots & 0 & \alpha_M \end{pmatrix} \cdot \begin{pmatrix} \Delta t_1 \\ \Delta t_2 \\ \Delta t_3 \\ \vdots \\ \Delta t_N \end{pmatrix} = \begin{pmatrix} T_S \\ T_S \\ T_S \\ \vdots \\ T_S \end{pmatrix}$$





- Zero-crossing time intervals
- Iterative period refinement
- The least-squares solution of the overdetermined system gives the sampling interval

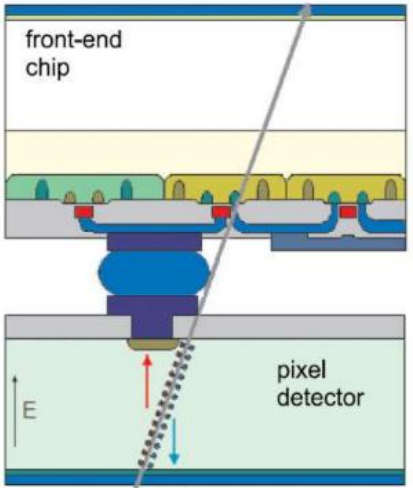
<5 ps over a wide range

Outline

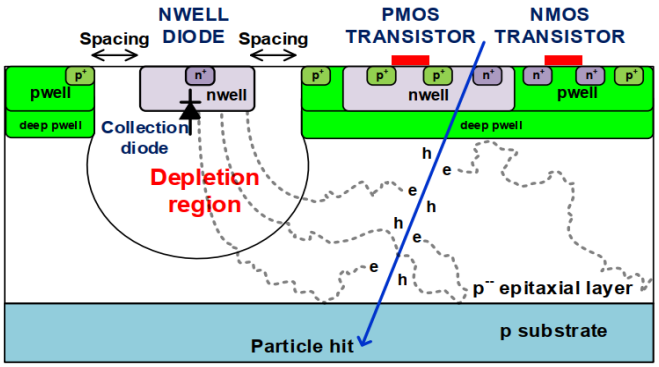
- Precision front-end measurement
  - High-precision charge measurement
  - High-precision time measurement
  - High-speed waveform digitization
  - Silicon pixel detector readout
- Data aggregation and transmission
  - High-speed interface circuits
  - Data aggregation
  - Optical signal transceiver

Pixel Detectors

- **Hybrid pixels**
  - Advantages:
    - Sensor and readout circuit can be optimized separately
    - Excellent radiation hardness
    - Fast timing and high rate capability
  - Disadvantages：
    - Relatively large material budget
    - Hybridization: complex, expensive



- **Monolithic active pixel sensors (MAPS)**
  - Advantages:
    - Easier integration, lower cost
    - Potential of low material budget
    - Higher spatial resolution
  - Disadvantages:
    - Smaller signal and longer collection time
    - Radiation tolerance limitation

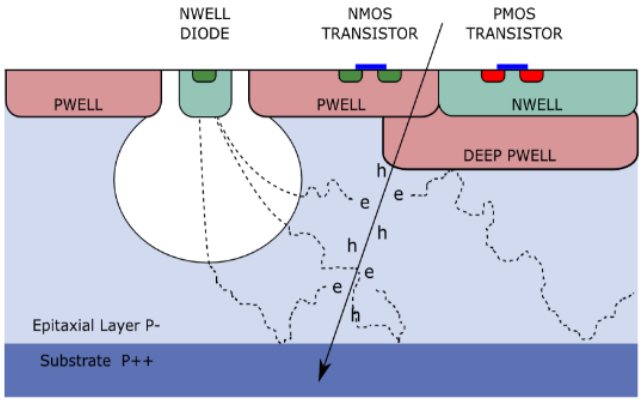


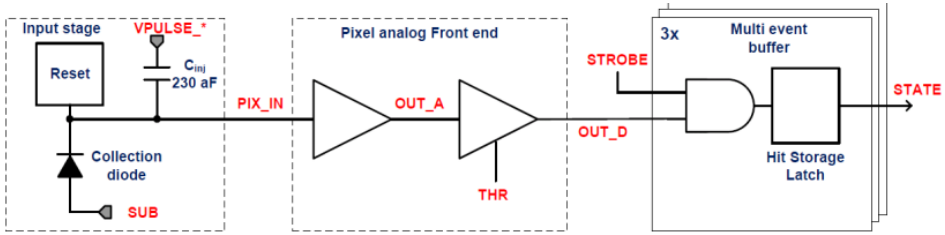
Silicon Pixel Readout ASIC

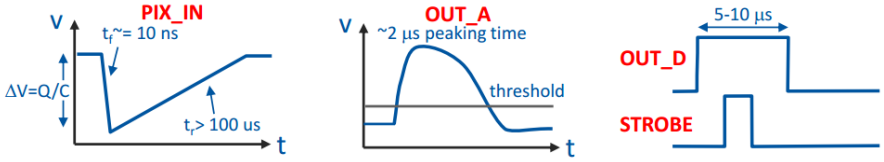
Chip	Process	Array Size	Pixel Size	Experiment	Type
FEI3	250 nm	18×160	50 ×400 μm^2	ATLAS pixel detector	hybrid
FE-I4	130 nm	80×336	50 ×250 μm^2	ATLAS pixel detector	hybrid
Timepix3	130 nm	256×256	55 ×55 μm^2	GEM-TPCs	hybrid
HEPS-BPIX4	130 nm	20×32	55 ×55 μm^2	HEPS	hybrid
EMPIX	180 nm	32×8	150 ×150 μm2	/	hybrid
ULTIMATE	350 nm	928×960	20.7 ×20.7 μm2	RHIC STAR	monolithic
ALPIDE	180 nm	512×1024	28 ×28 μm^2	ALICE ITS	monolithic
ATLASPix3	180 nm	132×372	150 ×50 μm^2	ATLAS pixel detector	monolithic
Mupix10	180 nm	250×256	80 ×80 μm^2	Mu3e	monolithic
TJ-Monopix2	180 nm	512×512	33 ×33 μm^2	ATLAS pixel detector	monolithic
CLICTD	180 nm	16×128	300 ×30 μm^2	CLIC	monolithic
JadePix3	180 nm	512×192	16×23.1 μm^2	CEPC	monolithic
TaiChuPix-2	180 nm	192×64	25×25 μm^2	CEPC	monolithic
MIC5	180 nm	356×398	20×30 μm^2	CEPC	monolithic
Topmetal-M2	130 nm	400×512	45×45 μm^2	/	Topmetal+MAPS
Topmetal-S2/CEE	130 nm	/	/	0νββ/CEE	Topmetal
CharTPix	130 nm	576×144	33×33 μm2	STCF	MAPS
COFFEE3	55 nm	48 × 12	40×145 μm2	LHCb UP	HV-CMOS
CHiR1	55 nm	256×64	38×175 μm2	LHCb UP	HV-CMOS

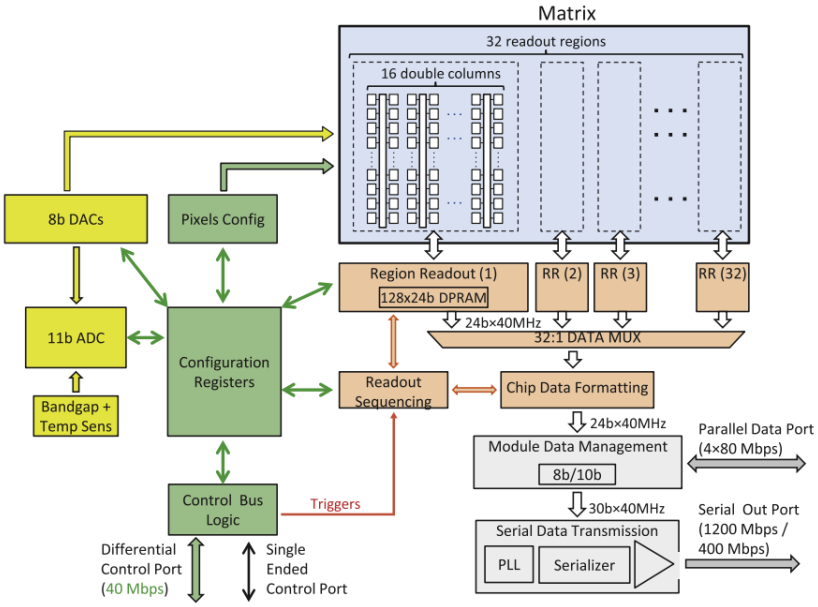
ALPIDE

- MAPS for the ALICE ITS upgrade
  - Process: TJ 180 nm (High resistivity p-type epitaxial layer on a p-type substrate)
  - Array size: 512 × 1024
  - Pixel size: 28 μm × 28 μm
  - Chip size: 15 mm × 30 mm
  - Power: < 40 mW/cm^2



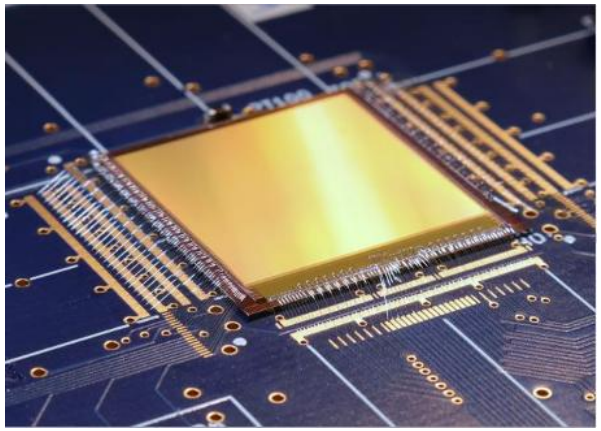


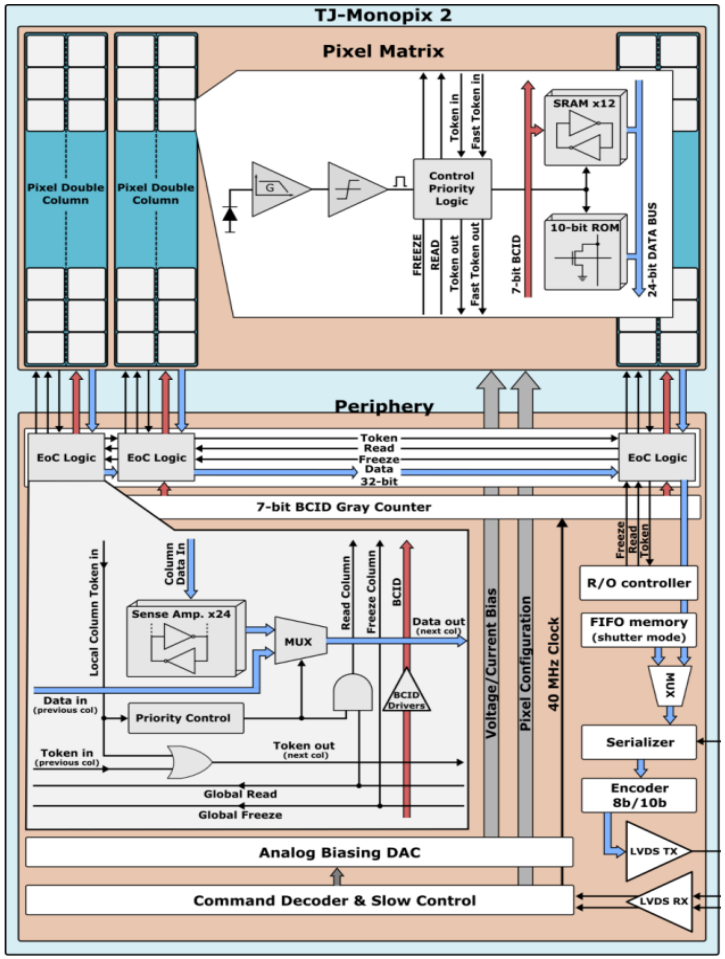




TJ-Monopix

- MAPS for the HL-LHC ATLAS Inner Tracker
  - Process: Modified TJ 180 nm
  - Array size: 512 × 512
  - Pixel size: 33.04 μm × 33.04 μm
  - Chip size: 20 mm × 20 mm
  - Power: 170 mW/cm^2
  - With TOA and TOT

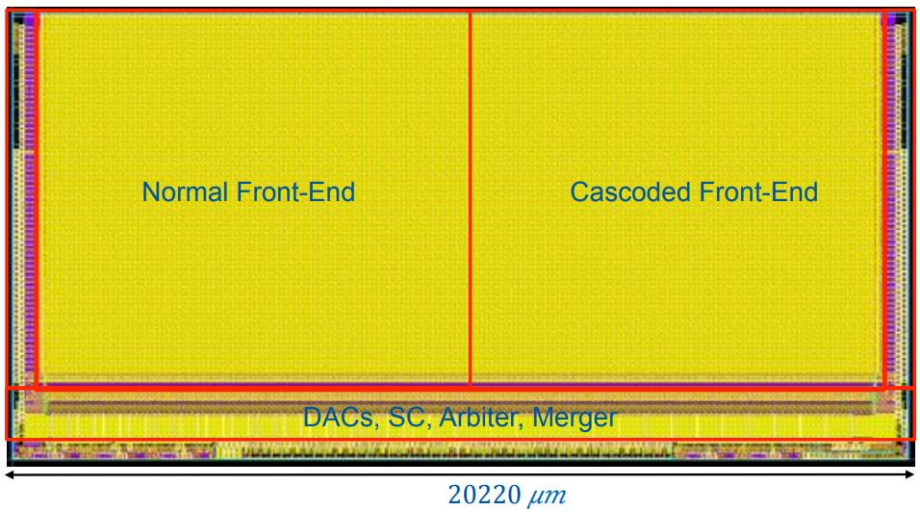


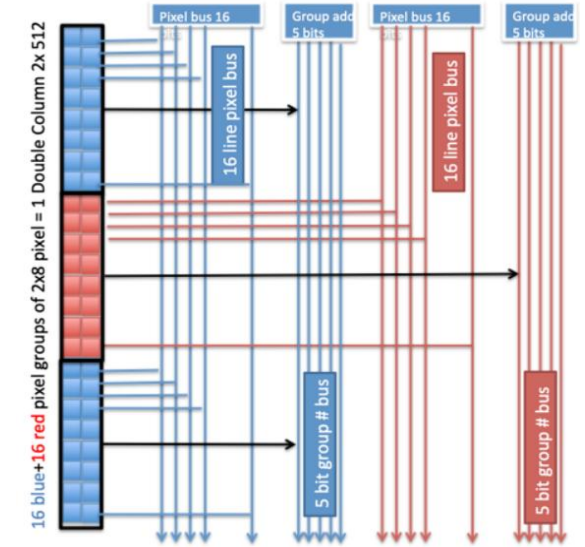


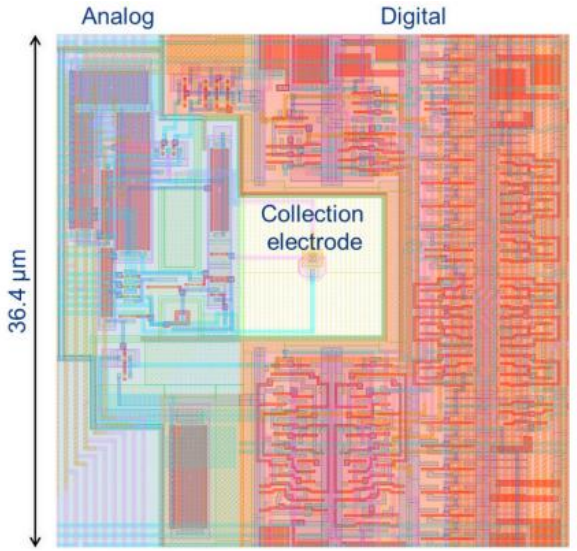
TJ-Monopix2 Block diagram

MALTA

- MAPS for the HL-LHC ATLAS Inner Tracker
  - Process: Modified TJ 180 nm
  - Array size: 512 × 512
  - Pixel size: 36.4 μm × 36.4 μm
  - Chip size: 18.3 mm × 18.3 mm
  - Asynchronous Readout: No clock in matrix





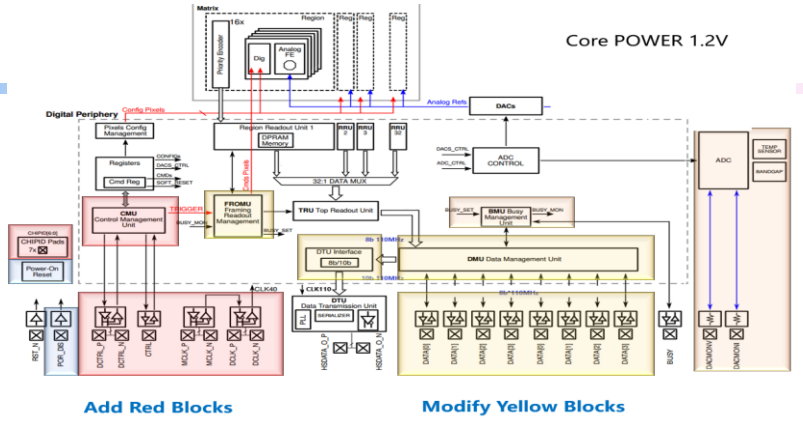


Example of domestic MAPS: MIC6

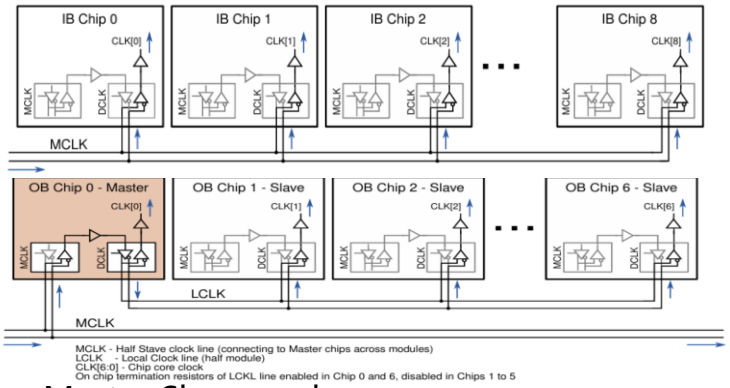
Modifications based on MIC6_V3 -> V4

- Add clock interconnection between chips
- Add control management unit (CMU) to replace SPI
- Add master-slave transmission mode
- Differential signals are used for clock and control signals
- Increase output data rate to 1.2Gbps
- Add on-chip LDO

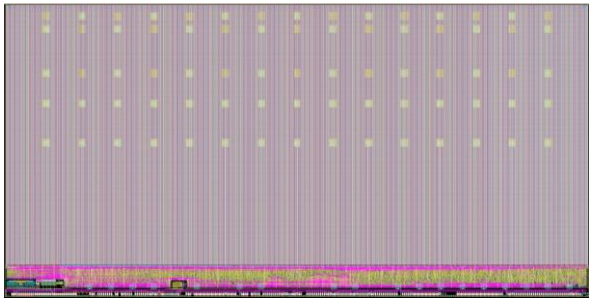
Process	**GSMC-130 nm**
Core Voltage	**1.2V**
Chip Size	**30 mm×15 mm**
Pixel Array	**980×497**
Pixel Size	**30.53 um×26.8 um**
Readout Mode	**AERD**
Output data rate	**1.2Gbps**
Encoding	**8B10B**
Slow Control	**MLVDS Control Bus**
Cascade Readout	**master-slave data aggregation and transmission**



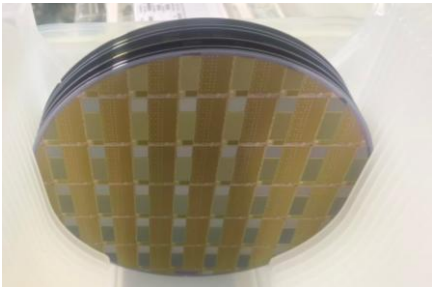
MIC6 V4 block diagram



Master-Slave mode



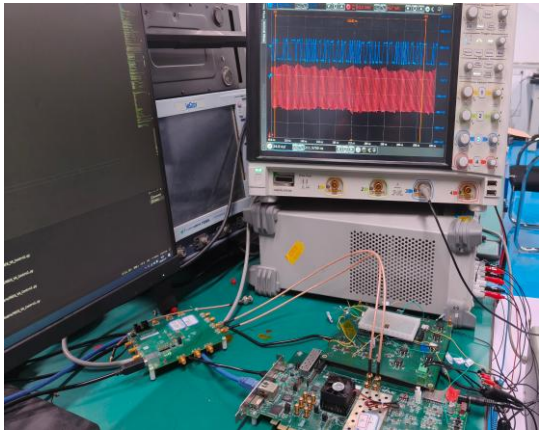
Layout of MIC6_V4



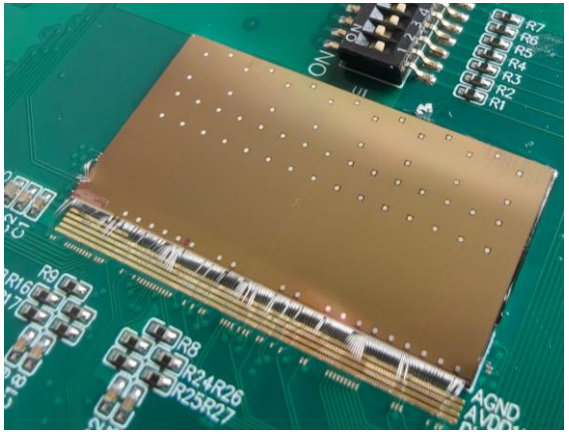
MIC6_V4 wafer

MIC6

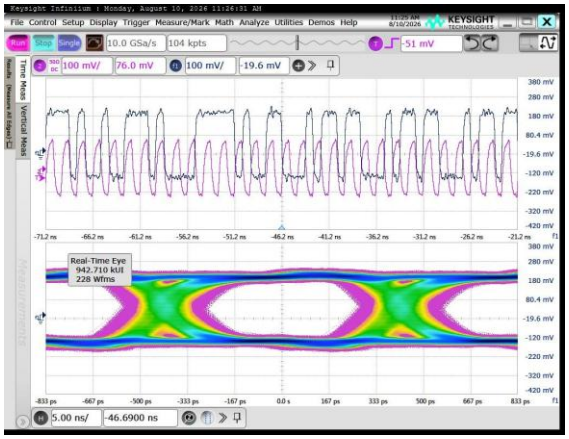
Test System of MIC6_V4



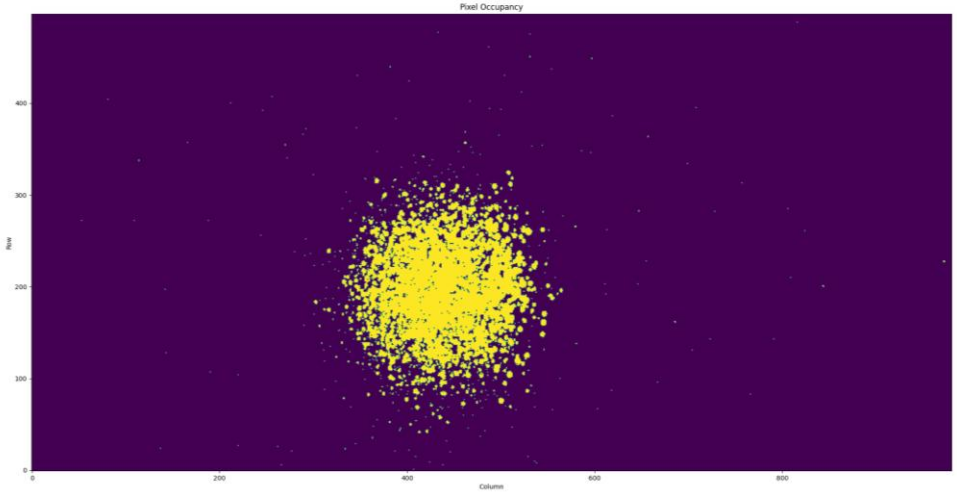
MIC6_V4 chip

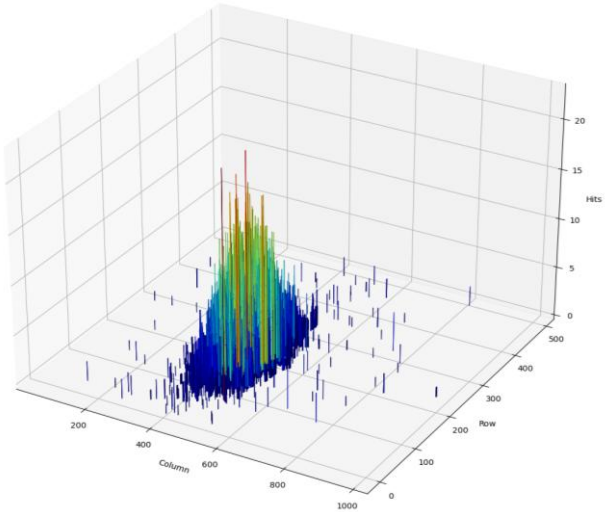


Eye diagram @1.2 Gbps



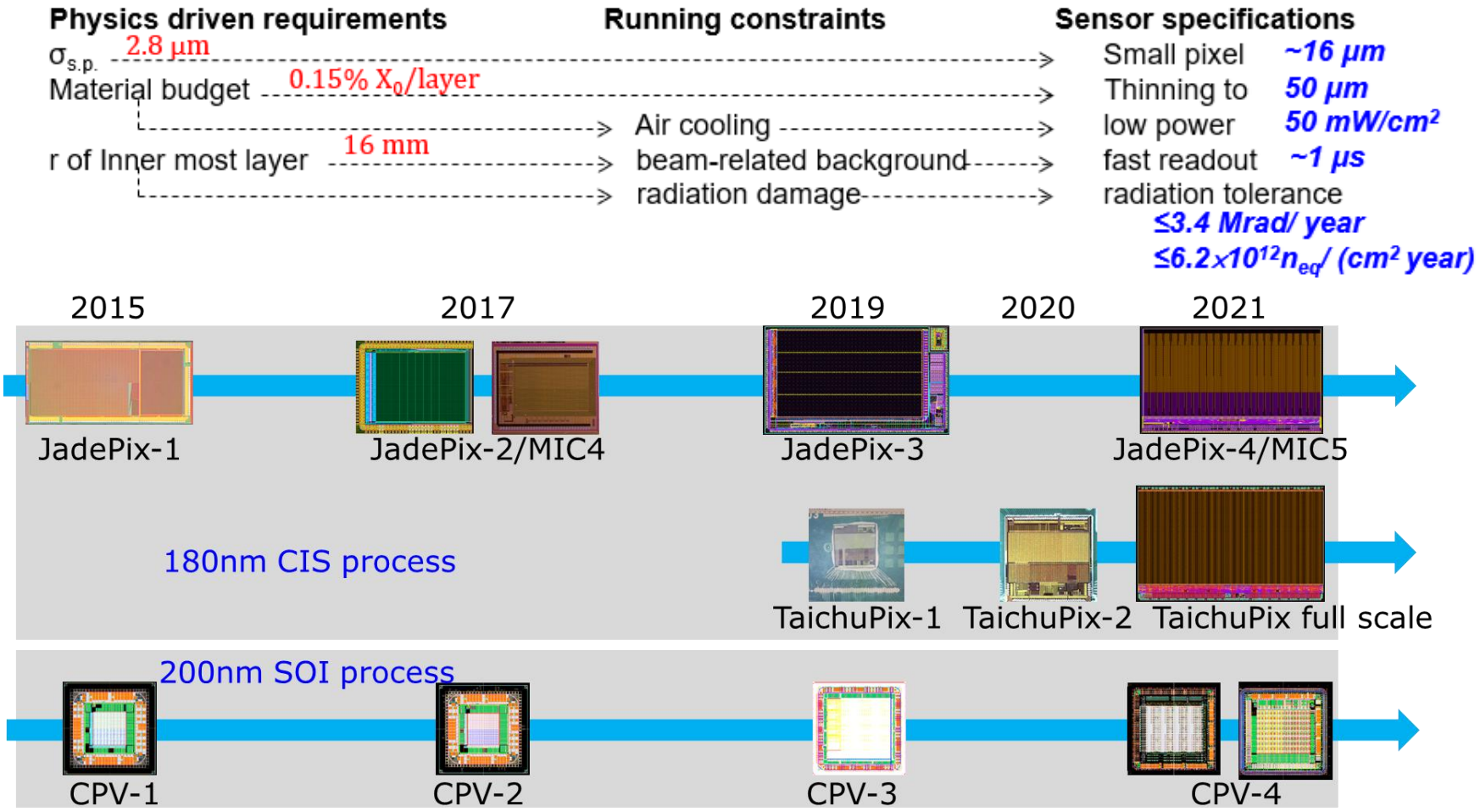
^{241}Am Test using MIC6_V4





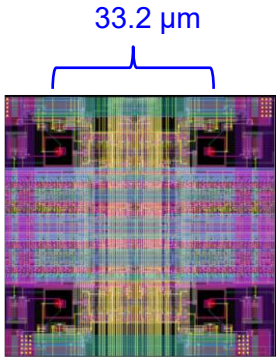
CEPC vertex detector R&D (IHEP)

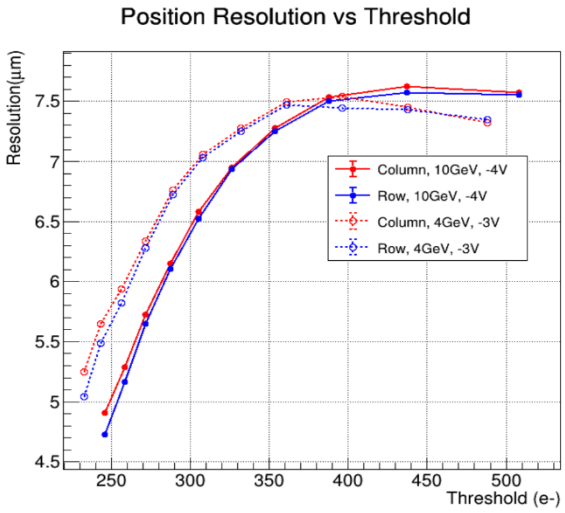
- The vertex detector poses major challenges for chip design
- Three parallel R&D routes with broad domestic and international collaboration

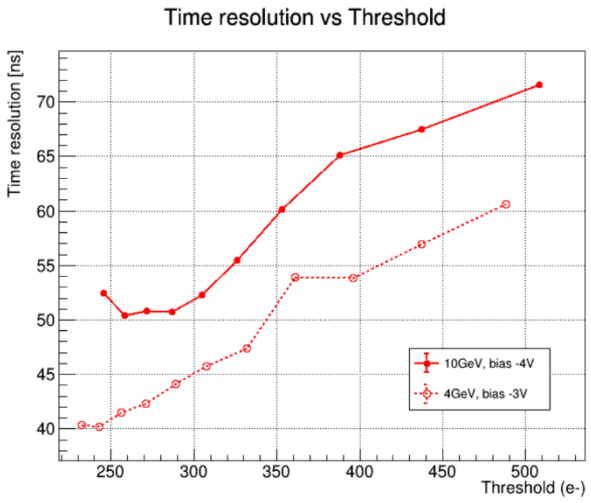


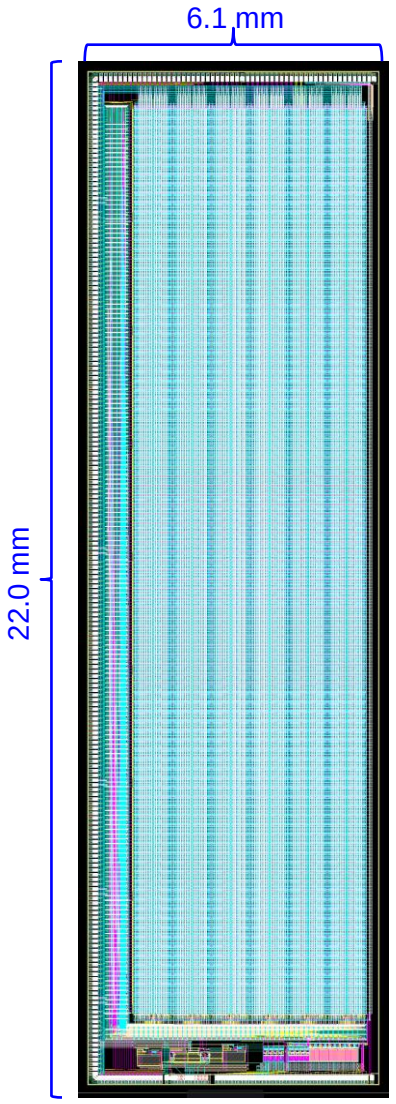
CharTPix

- Designed for Super Tau-Charm Facility Inner Tracker
- Position, Time and Charge measurement with low power consumption (Low material budget)
  - Pixel Pitch: 33 μm×33 μm
  - Pixel Array: 576 rows × 144 columns
  - Position resolution: up to 5 μm
  - Time resolution: up to 50 ns



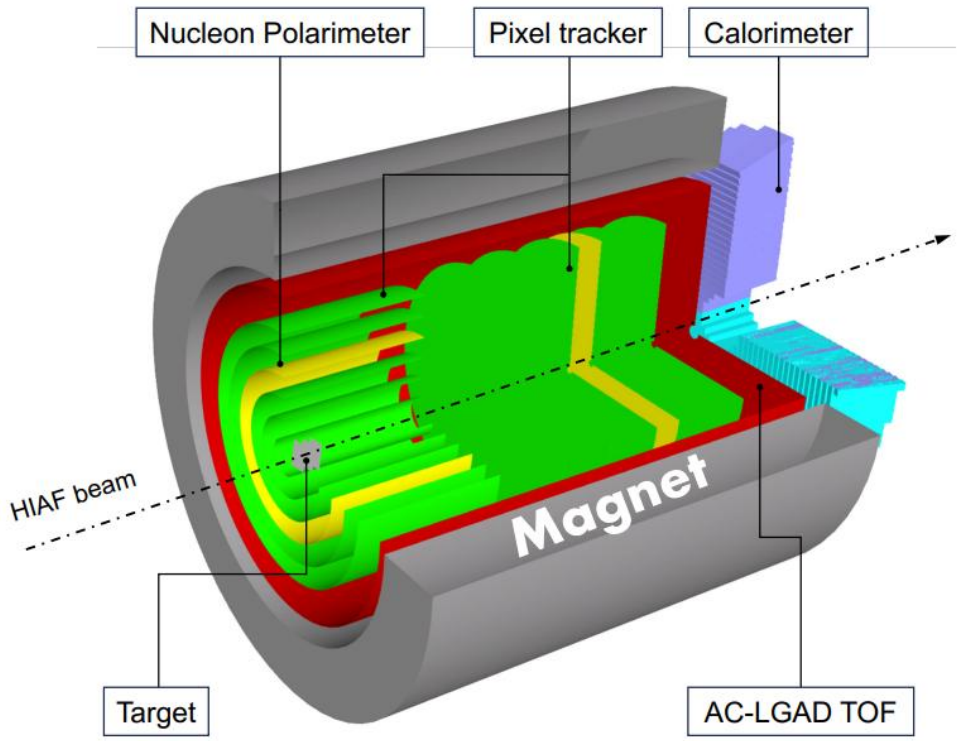






layout

H-NS structure



Key sub systems：

- **Pixel tracker**
- **LGAD TOF**
- Target
- Nucleon Polarimeter
- Calorimeter
- **Electronics**
- Magnet
- Beamline
- Mechanics + Engineering

1) Λ (p) polarization, hadron spectra, spin structure, …;
2) High μ_B properties, QCD critical point, …

Outline

- Precision front-end measurement
  - High-precision charge measurement
  - High-precision time measurement
  - High-speed waveform digitization
  - Silicon pixel detector readout
- Data aggregation and transmission
  - High-speed interface circuits
  - Data aggregation
  - Optical signal transceiver

Data chain options

- FPGA
  - Programmable device
  - Flexible
  - Abundant resource
  - High speed data interface
  - High cost
  - High system complexity
  - System radiation hard design

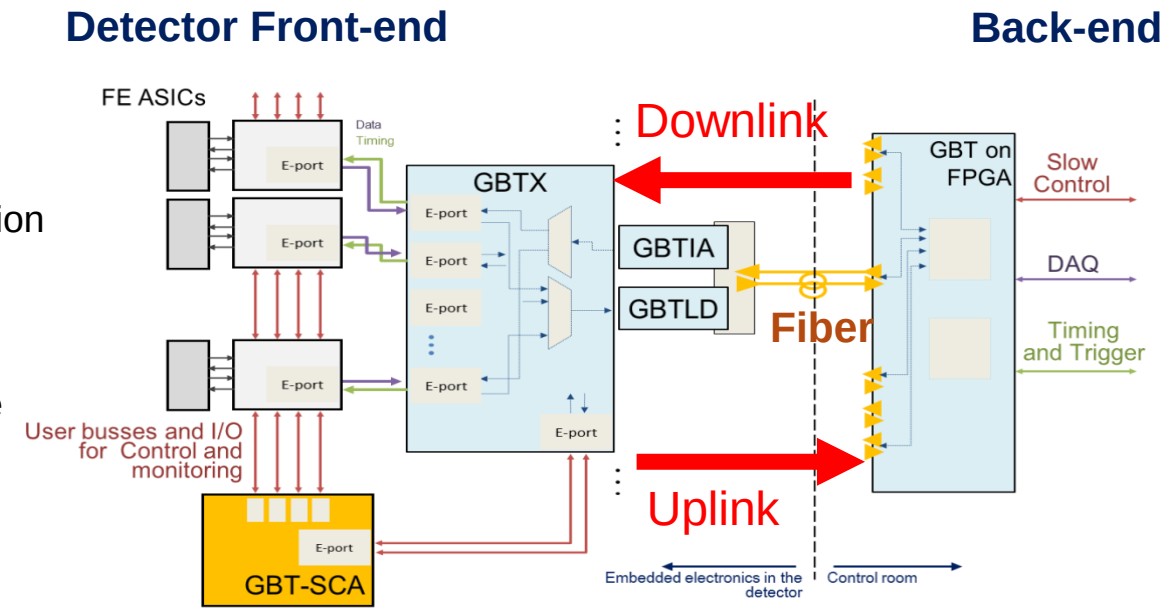


- ASIC
  - Specifically designed chip
  - Much effort in chip design & testing
  - High speed data interface
  - Low cost in massive production
  - Low system complexity
  - Chip level radiation hard design

- ASIC-based technique is very important for large scale application.
- Categorization in functionality and systematic R&D is necessary.

High-speed Data Transmission System in HEP

- **FE/ROC ASIC**:
  data collection & processing
- **SCA ASIC**:
  slow control, cmd & config distribution
- **GBTx**:
  bi-directional data interface ASIC
- **VTRx**: Customized optical module
  - **GBLD**:
    high-speed laser driver ASIC
  - **GBTIA**:
    high-speed low noise
    transimpedance amplifier ASIC

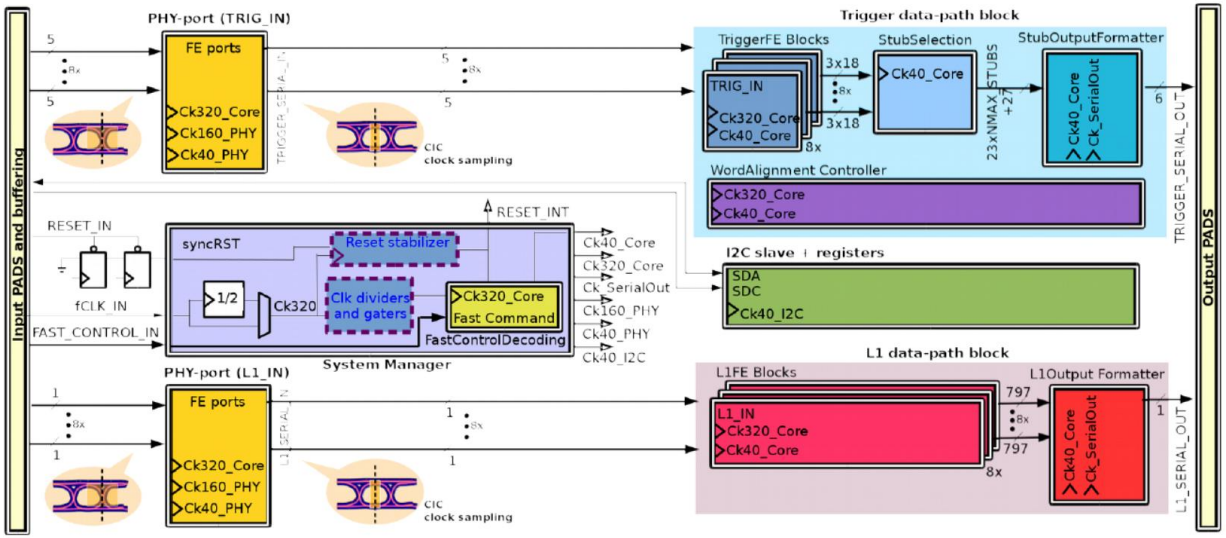


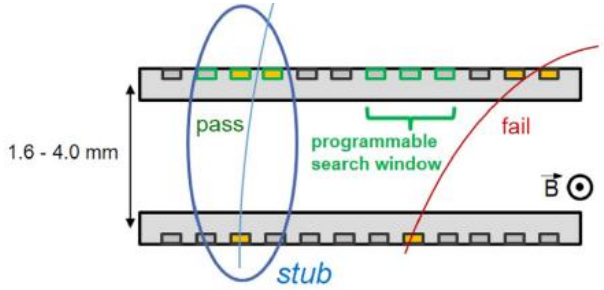
Bi-directional Optical data transmission scheme developed by CERN

- Optical data transmission between the front-end and back-end is widely used in particle physics experiments.
- Versatile Link Project: A typical system developed by CERN.
  - Aims to build a high-speed, radiation-tolerant, bi-directional optical data transmission system for the particle physics experiments applications.

CIC ASIC

- The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip and Strip-Strip modules of the Phase-II CMS Outer Tracker upgrade at HL-LHC.



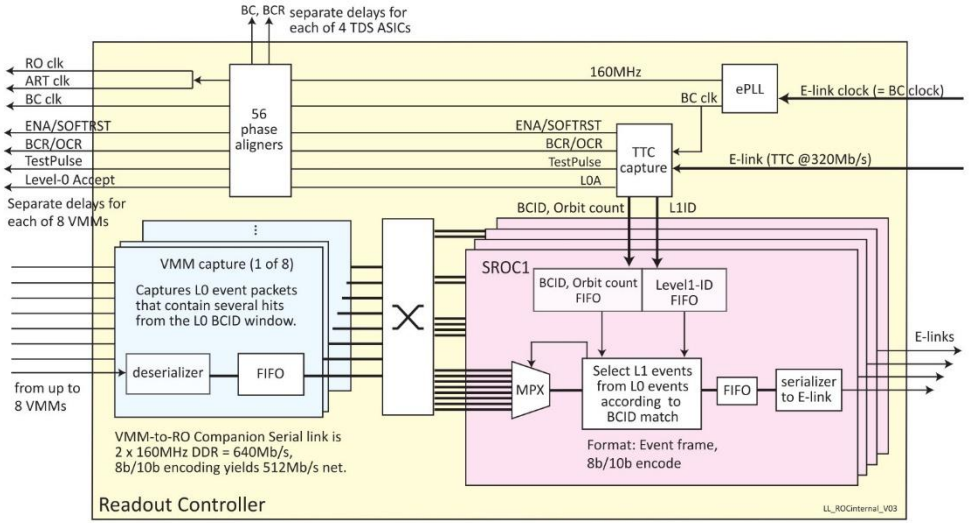


- Input: 48 lines @ 320 MHz, connected to 8 FE chips
  - Each FE chip, 5-bit trigger data and 1-bit L1 data
- Output： 7 lines @320/640MHz
  - 6 lines for trigger data and 1 line for L1 data
- Data compression

VMM ROC ASIC

- VMM ROC is used for handling , filtering and real-time packet processing of ATLAS muon detector data

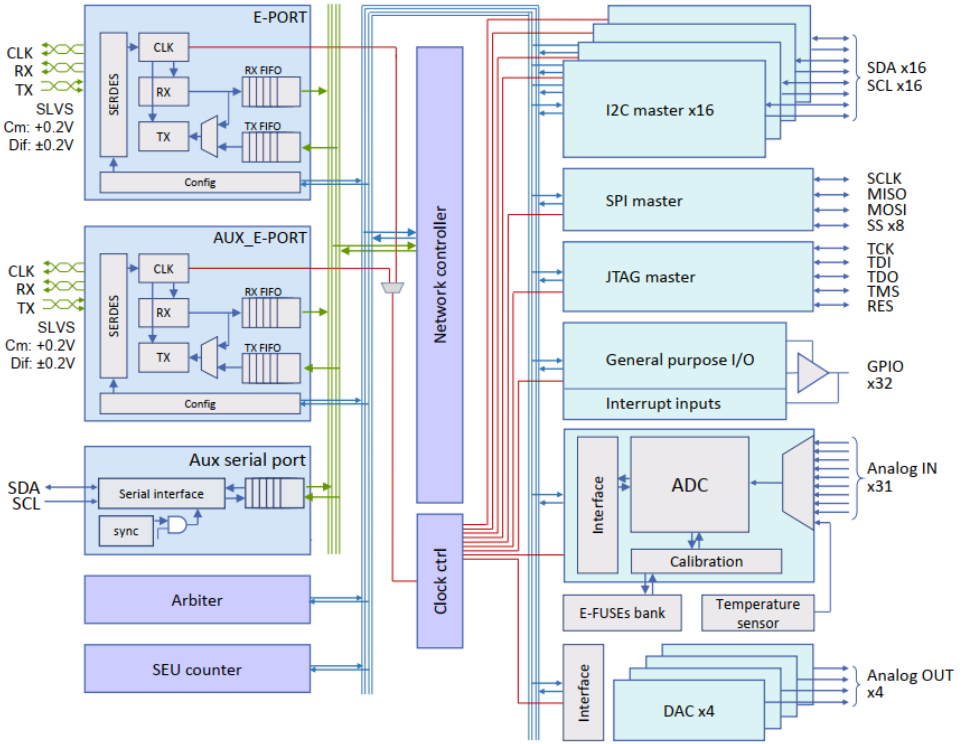
  - Input
    - 8 channel / Data rate: 640 Mbps
  - Output
    - 4 channel / Data rate: 640/320/160/80Mpbs (DDR)
  - TTC rate: 320 Mbps (DDR)
  - Configurable X Bars
  - Multi-channel data aggregation
  - Output clk 80/160/320MHz clock signal to VMM, TDS, ART
  - Send soft reset /BC reset/Test Pulse



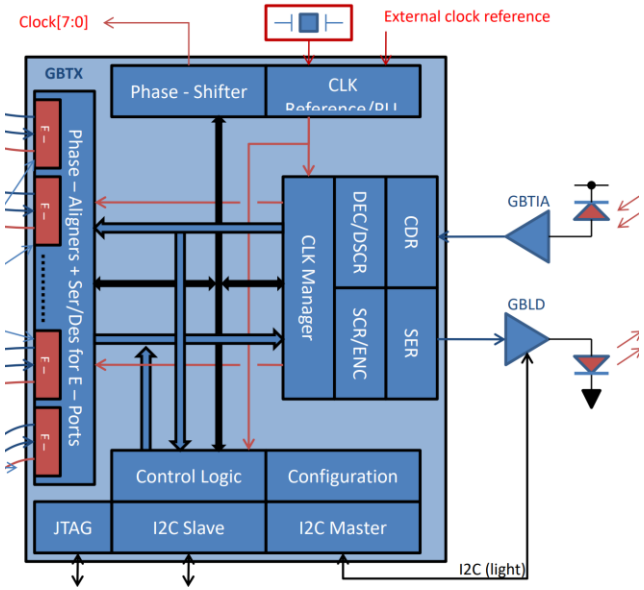
Slow Control ASIC

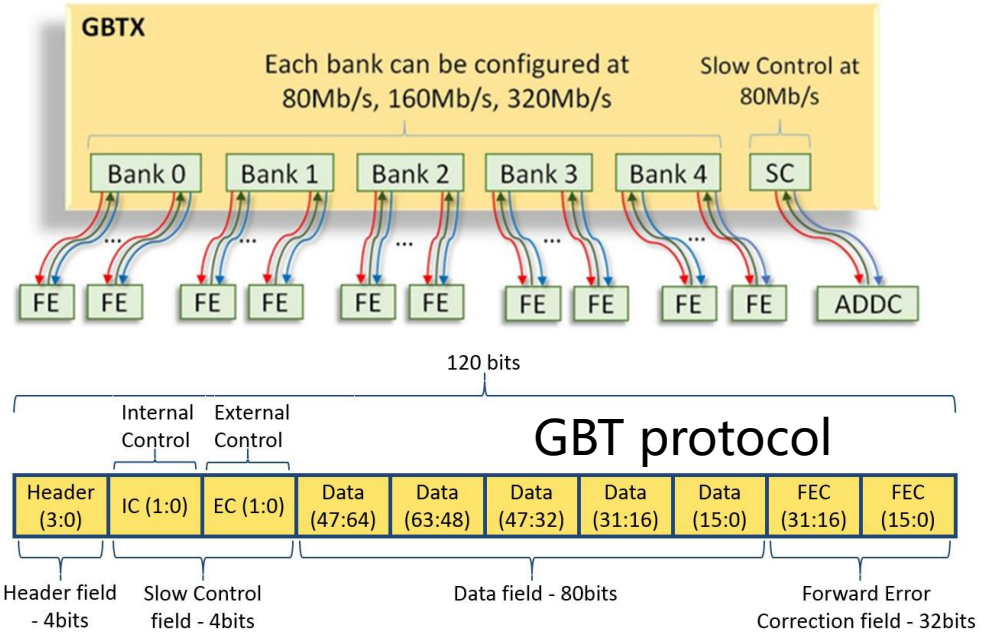
- GBT-SCA ASIC provides slow control signals for configuring and monitoring FE and detectors.

- Variety of protocol buses and functions
  - 32 bit Parallel Interface Adapter (GPIO)
  - 16 independent I^2C master serial bus channels
    SPI master，8 individual slave
  - JTAG serial bus master channel
  - 12-bit ADC（31 bit analog inputs）
  - 4 DAC channels，8 bit resolution
  - Temperature monitoring module



GBTx & LpGBT ASIC

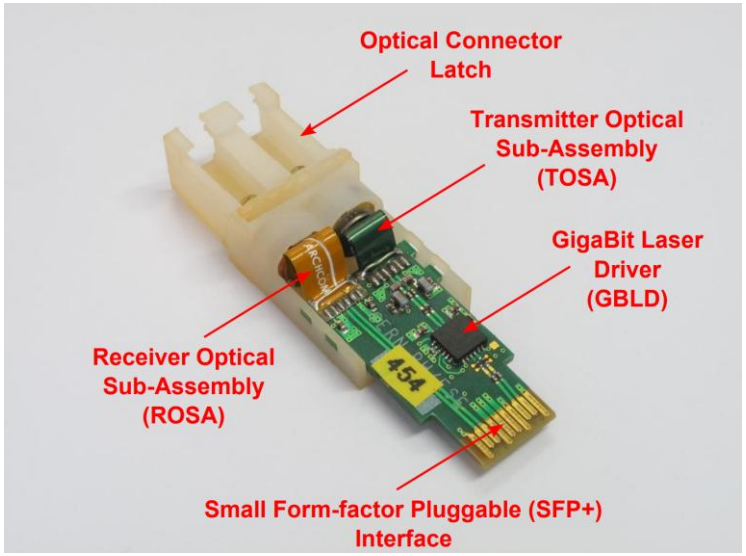




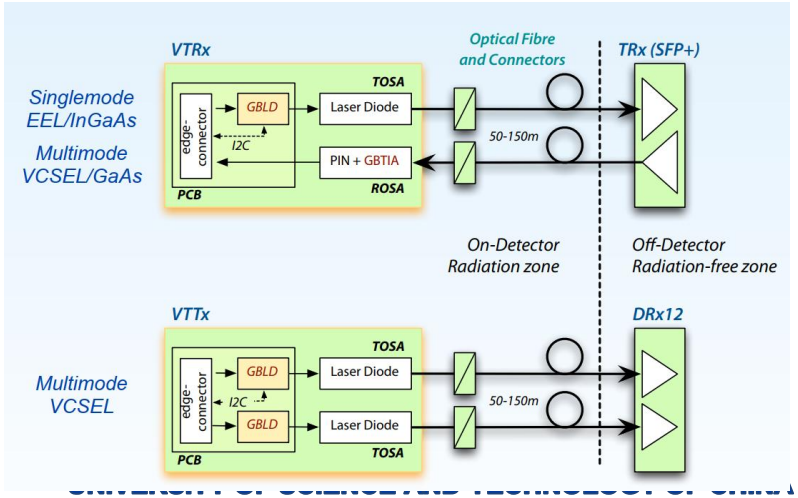
- GBTx ASIC
  - Input:
    - -40 channels @ 80Mbps
    - -20 channels @ 160Mbps
    - -10 channels @ 320Mbps
  - Output： 4.8 Gbps
  - Power： 2.2 W / 1.5V
  - BGA 400 pin
  - 130 nm CMOS

- LpGBT ASIC is the upgraded of the GBTx
  - Input：
    - Input channel: 28/14/7
    - Data rate: 160/320/640 Mbps @ output 5.12 Gbps
    - Data rate: 320/640/1280 Mbps @ output 5.12 Gbps
  - Output: 5.12 Gbps /10.24 Gbps
  - Power： 1.2V
  - BGA 289 pin
  - 65 nm CMOS

Optical Fiber Transceiver ASIC



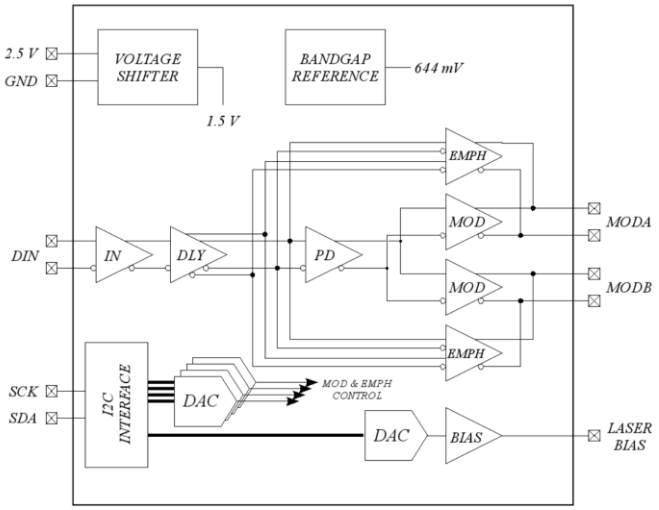
VTRx Optical Module Developed by CERN

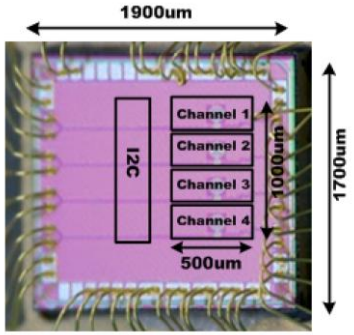


- VTRx (Versatile Link Transceiver) is a customized optical module developed by CERN. It is a pluggable module that integrates the laser, PIN-diode, GBLD, GBTIA and related optical components and mechanics.

- This module was first developed using TOSA and ROSA components as the single-channel form (1Tx + 1Rx), and updated to **VTRx+** using the laser array and array driver to achieve the parallel-channel form (4Tx + 1Rx, configurable).

GBLD & GBTIA ASIC

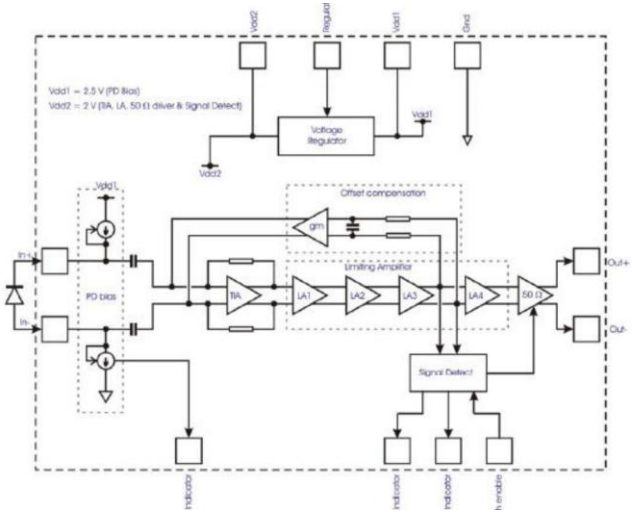


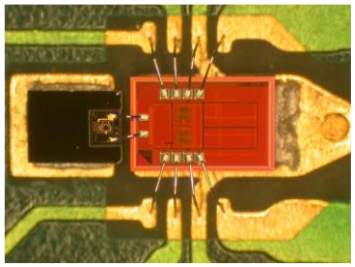


LDQ10 ASIC（GBLD ASIC in 65nm ）

- Upgrade to 65nm CMOS
- 4 x 10 Gbps/ch
- Four-channel laser array driver

- GBLD is a laser driver ASIC. It amplifies the high-speed serial data from GBTx ASIC, and drives the VCSEL laser to emit light.
- This lase driver ASIC was first developed under 130nm CMOS technology (GBLD, 5 Gbps/ch), and updated to the four-channel array form (4 x 10 Gbps/ch) in 65nm CMOS technology.





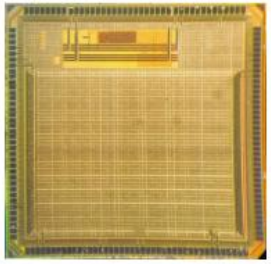
GBTIA ASIC

- 130 nm CMOS
- 2.56 Gbps/ch
- Downlink

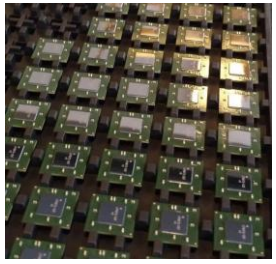
- GBTIA is a transimpedance amplifier ASIC. It amplifies the high-speed current signal from PIN-Diode as part of the downlink optical-to-electrical conversion.
- This ASIC was first developed under 130nm CMOS technology (GBTIA), and updated to the lpGBTIA using 65nm CMOS technology.

Summary of GBT & VTRx

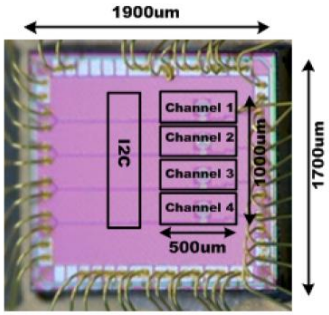
- The first generation of the GBT ASICs is based on 130 nm CMOS technology (around 2011). 2.56 Gbps Downlink + 5 Gbps uplink.
- The second generation of the GBT ASICs is based on 65 nm CMOS technology (around 2019). 2.56 Gbps Downlink and 10 Gbps uplink.
- In future, more advanced process (28nm, …), higher data rate, lower power…



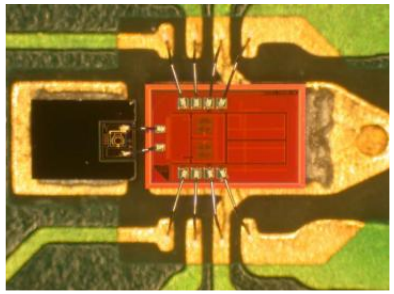
GBT_SCA
130nm CMOS



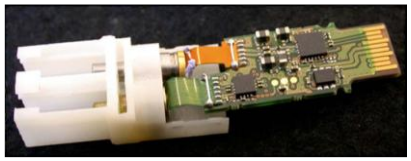
lpGBTx
65nm CMOS



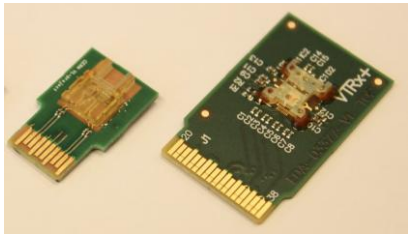
GBLD (LDQ10)
65nm CMOS



GBTIA
130 nm CMOS



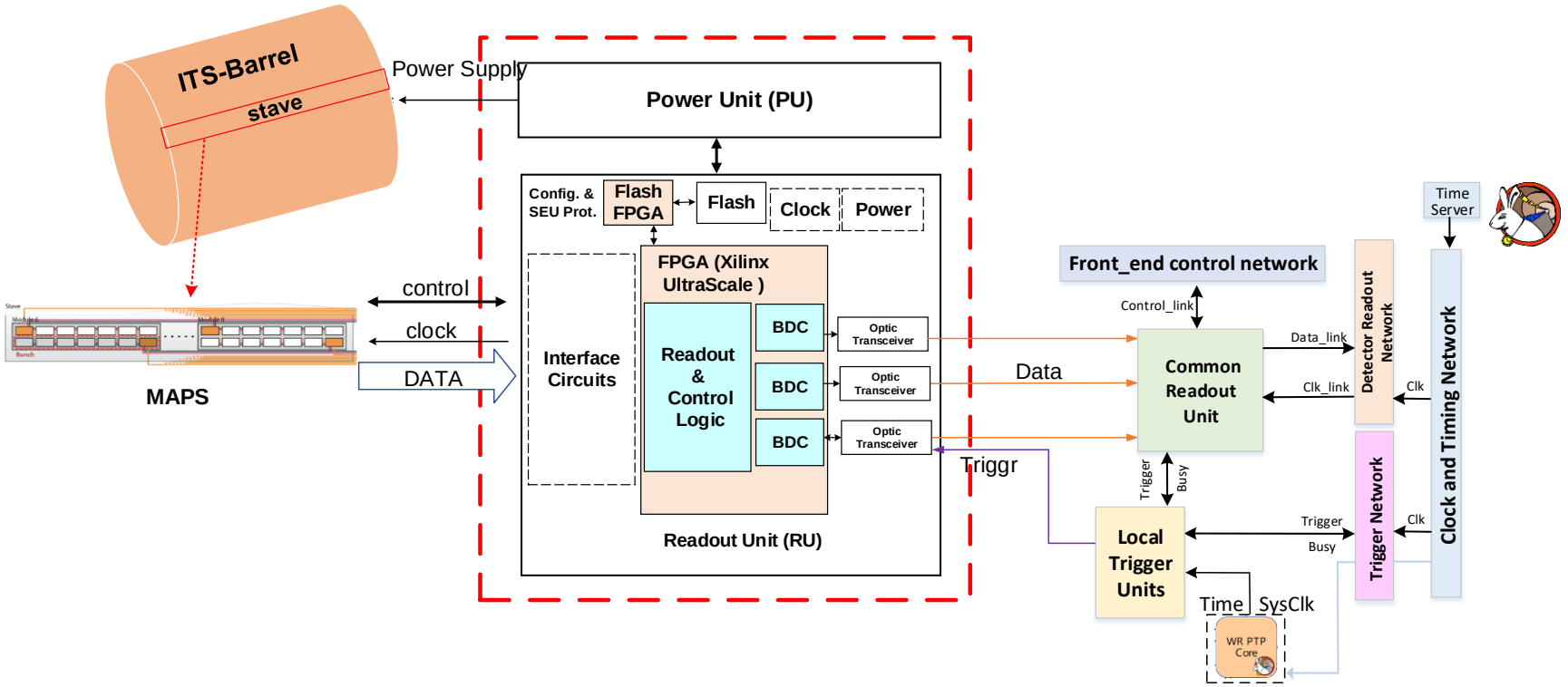
1Tx
1Rx



4Tx
1Rx

VTRx+ optical module

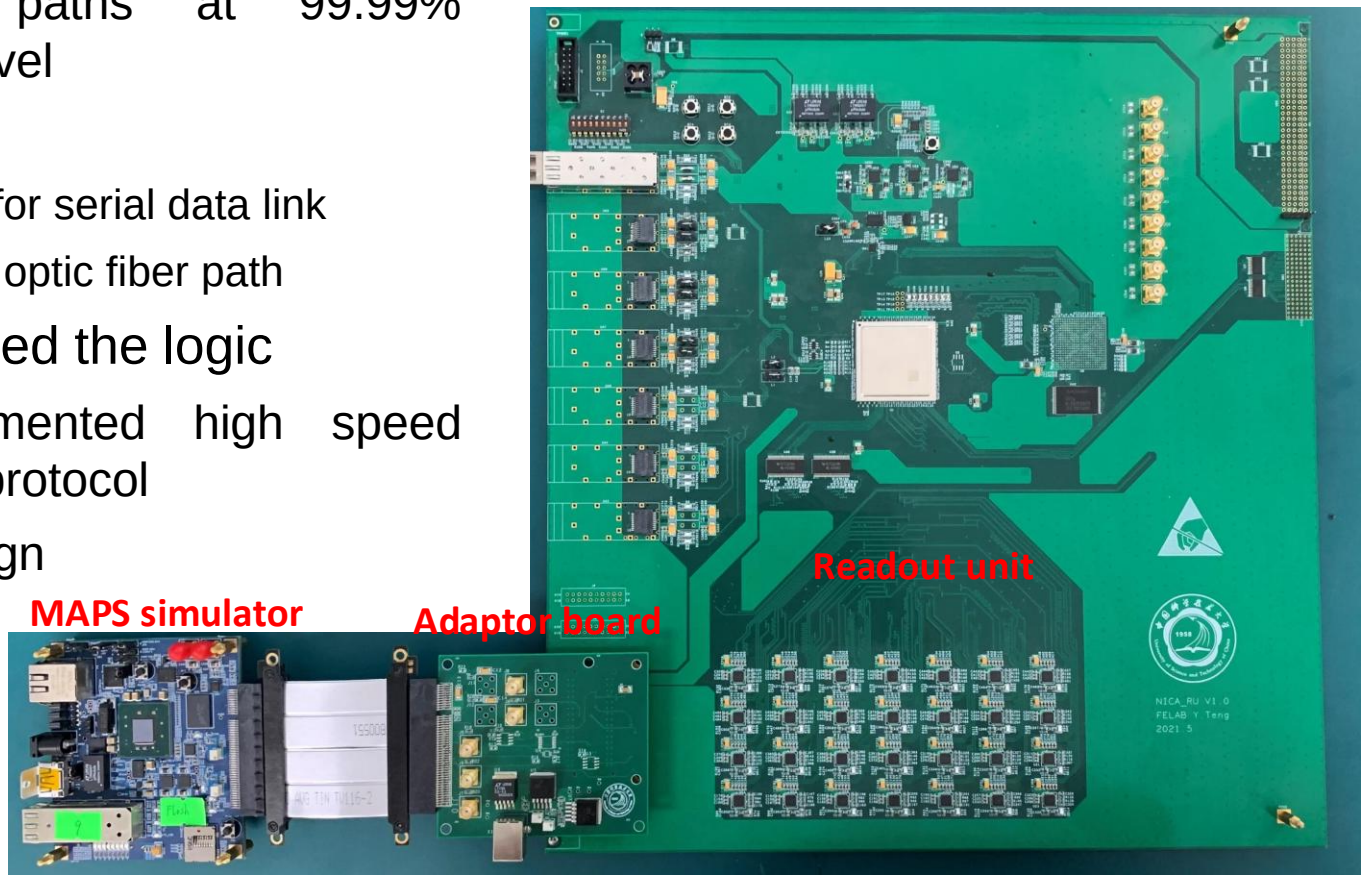
FPGA based Readout Unit



- Control and read out the data from MAPS stave
- SRAM-FPGA receives control/trigger signals and delivers packed data to CRU
- BDTC function integrated into the SRAM-FPGA
- A Flash-FPGA to monitor and protect the SRAM-FPGA from SEU based on scrubbing

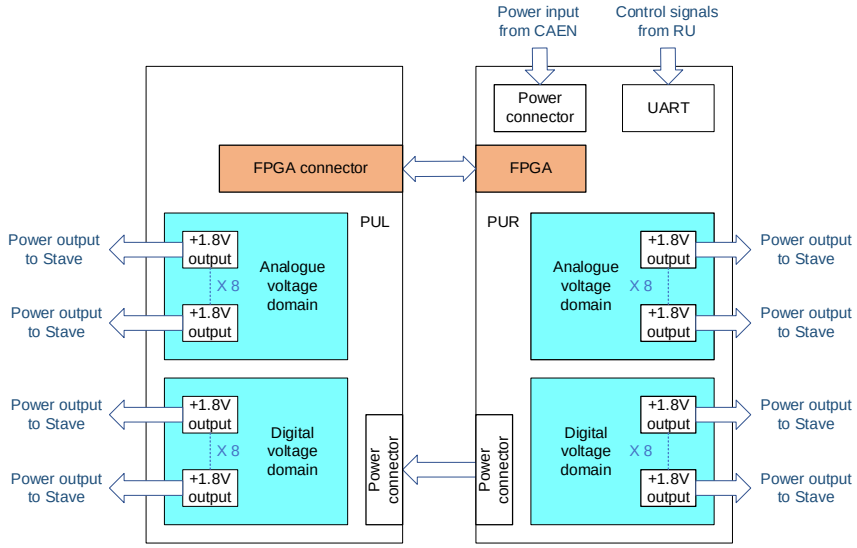
ITS-FPGA based Readout Unit

- Tested and verified the circuits
  - BER < 10^{-12} for serial data links and optic fiber paths at 99.99% condidence level
  - Data rates:
    - 400 Mbps for serial data link
    - 5 Gbps for optic fiber path
- Tested and verified the logic
  - FPGA implemented high speed data transfer protocol
  - Scrubber design



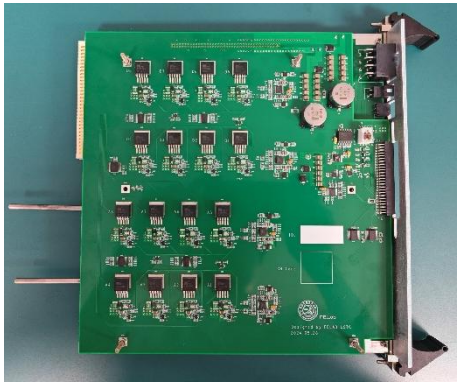
ITS-Power Board

- One PB is composed by two independent PU (PUR and PUL)
- Each PU contains 8 channels of analogue output (1.8V/250mA) and 8 channels of digital output (1.8V/1.5A)
- A flash FPGA on PUR controls both PUR and PUL and is responsible for communication with RU

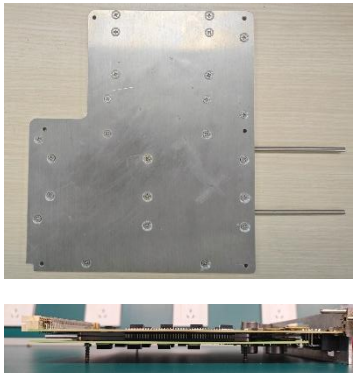




PUR



PUL

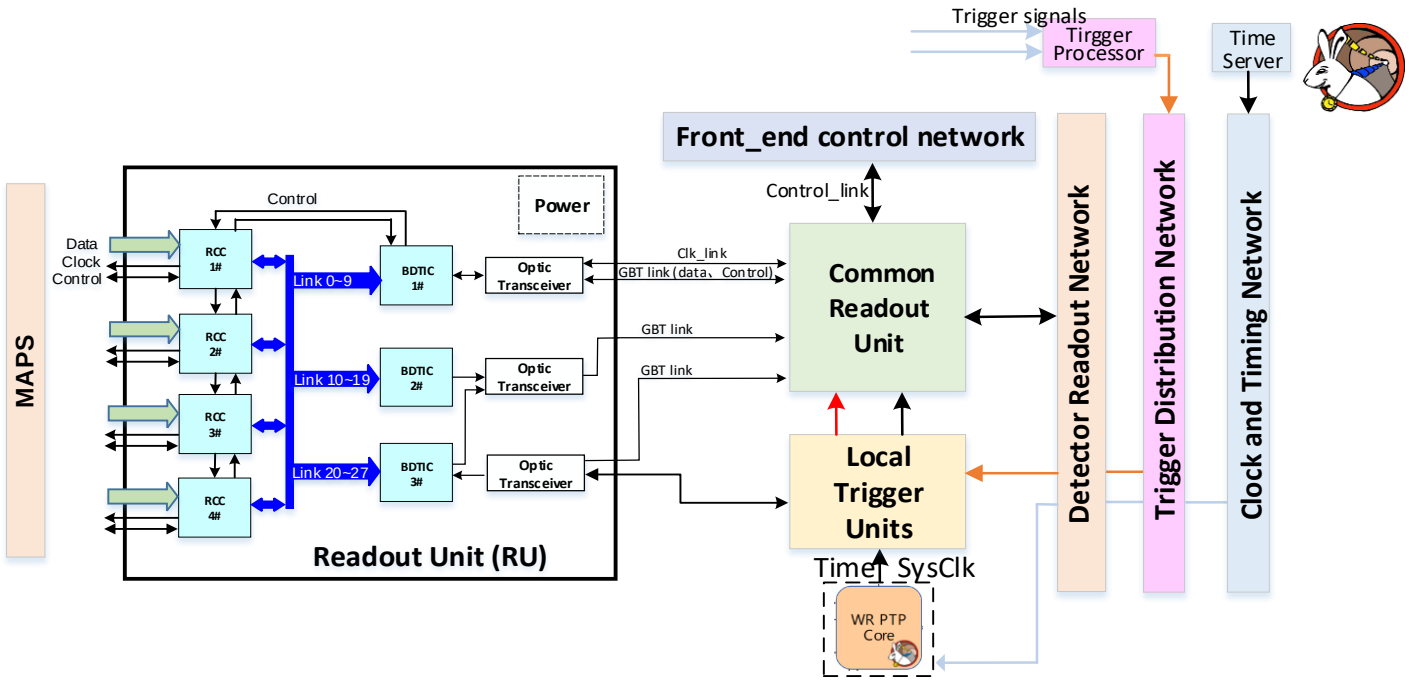


Cooling plate



Front Panel

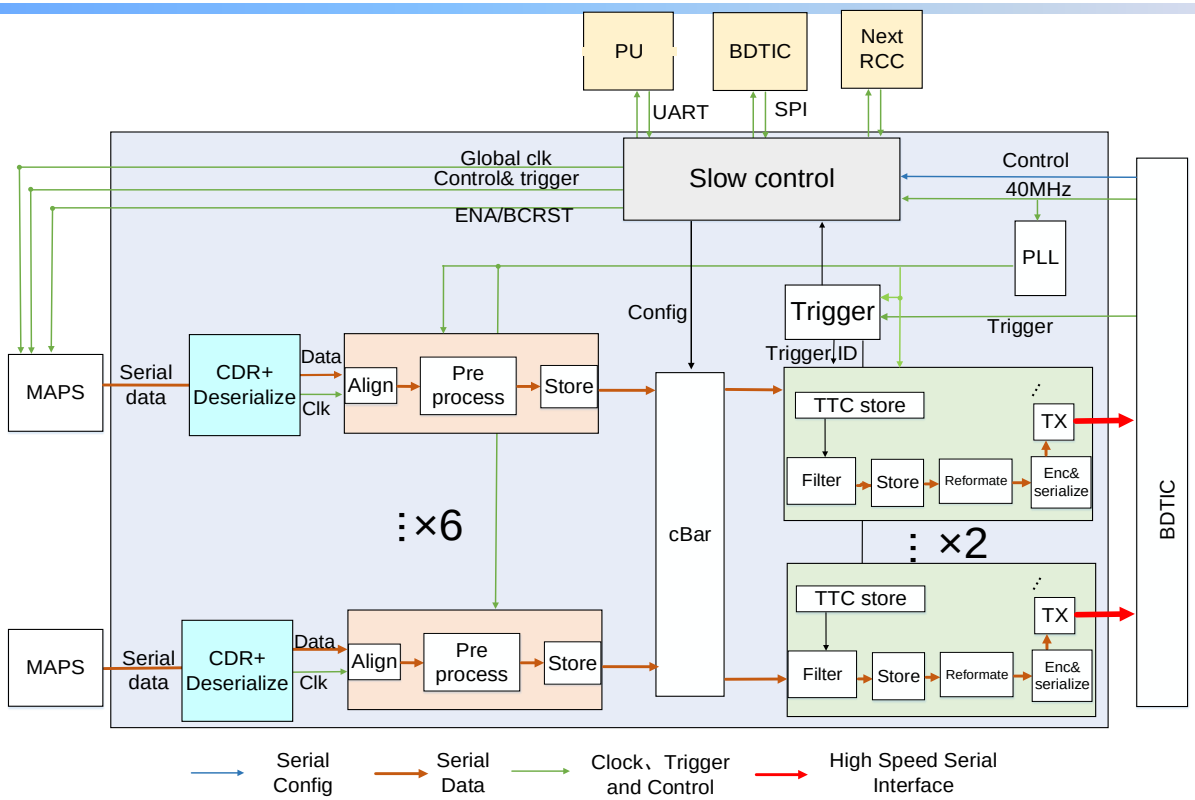
ITS- ASIC based RU



- ASIC group replace the function of FPGA, form the complete data and control link;
- **RCC: Readout and Control Chip**
  - ✓ MAPS data receive and processing, Slow control, Clock and Trigger
- **BDTC: Bi-directional Data-transceiver Chip**
  - ✓ high speed bidirectional data transfer
- Optical Transceiver : Laser-driver/receiver ASIC to modulate serial data on a laser

RCC ASIC

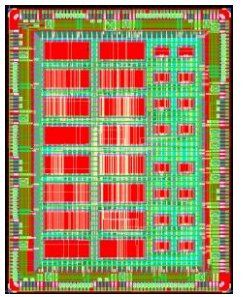
RCC: Readout and Control Chip

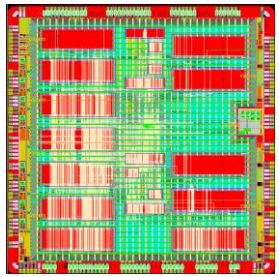


- RCC integrates the functionalities of Assembler, Buffer, Aggregator, and Data Packet processing for the MAPS detectors.
- Adjust and distribute control, trigger and clock information for MAPS/GBT/PU.
- RCC also optimizes the bandwidth utilization and reduces the number of required data links.

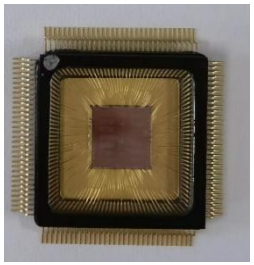
RCC ASIC

- MAPS Link:
  - ✓ Data link: 400 Mbps / 8 channels → 1.2 Gbps
  - ✓ Cfg link: 40 Mbps / Bi-directional
- Link to BDTC:
  - ✓ Data link: 160/320/640/1280 Mbps (configurable)
  - ✓ 1/2/4 channels
  - ✓ Cfg link: 80 Mbps
  - ✓ Trigger link :320 Mbps
  - ✓ Clock : 40 MHz
- Provides Control, Trigger and Clock information for the detector Realize the function of data reorganization
- Trigger / Trigger-less
- Integrated CDR & PLL
- SPI for BDTIC / UART for PU cfg & monitor
- SRAM ECC & Critical logic TMR protection

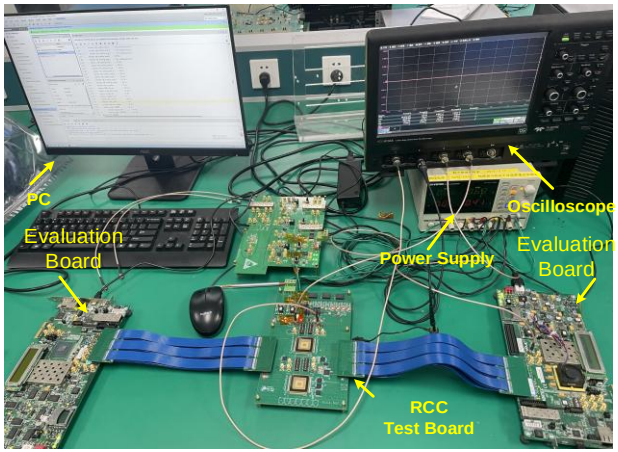






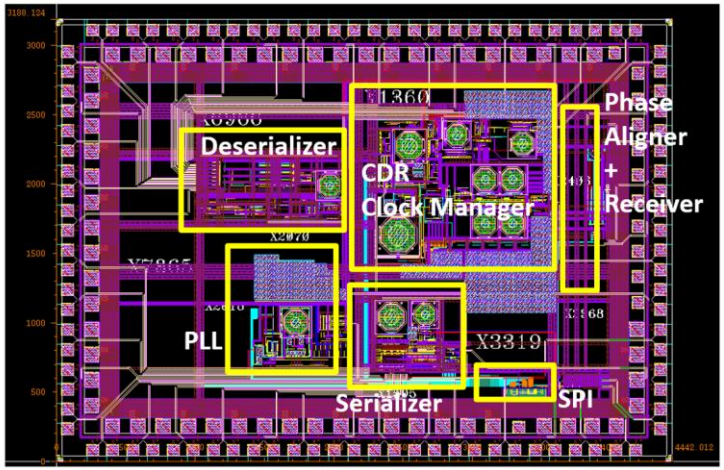


V0 V1

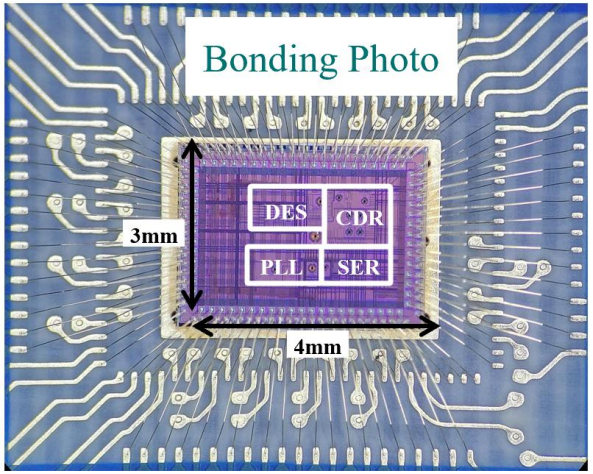


BDTC ASIC

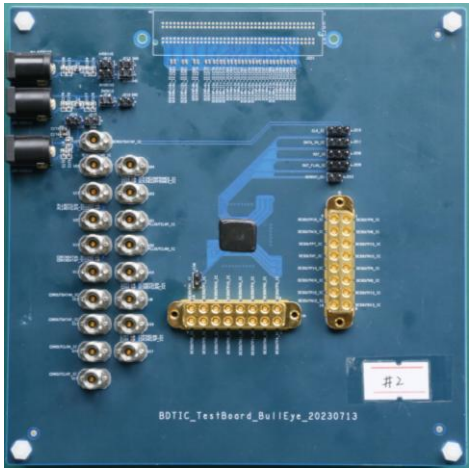
BDC: Bi-directional Data-transceiver Chip



Data Interface ASIC Layout



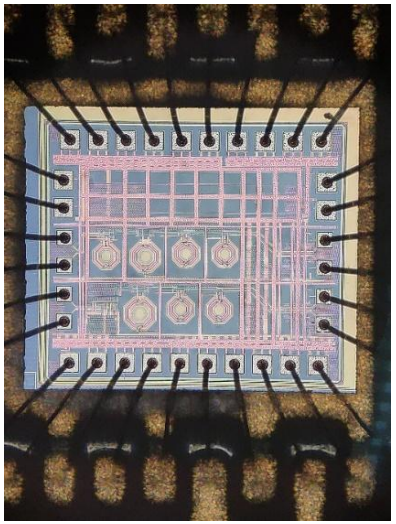
ASIC Bonding Diagram



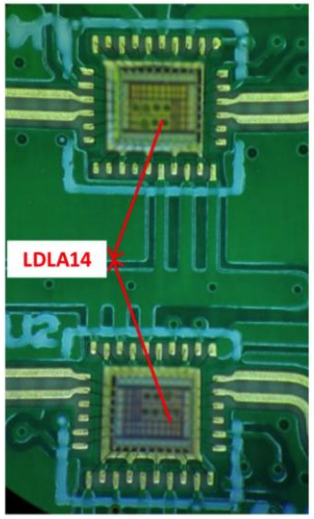
ASIC Test Board

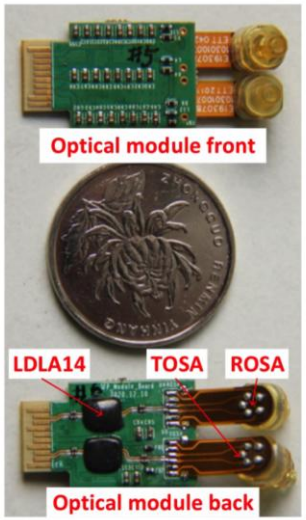
- The first prototype of the data interface ASIC has been designed and verified, including the following analog cores.
  - 5.12 GHz PLL
  - 2.56 GHz Clock and Data Recovery (CDR)
  - 16:1 Serializer
  - 2.56 Gbps 1:16 Deserialzier
- Based on 55nm CMOS Technology
- Die size: 3 mm x 4 mm 166 Pins

Optical Transceiver- Laser Driver and Receiver ASICs

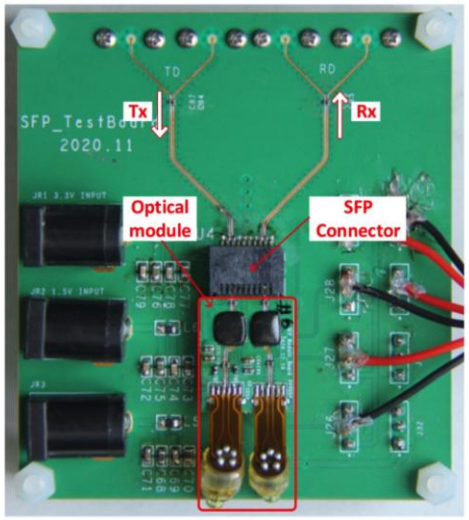


LDLA ASIC Layout





ASIC Bonding Diagram

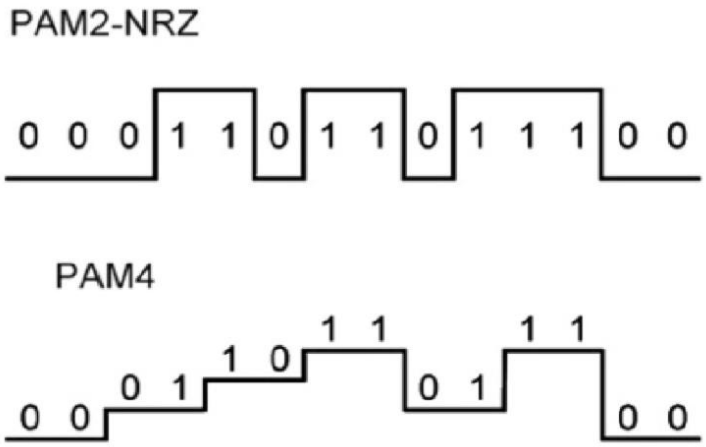


ASIC Test Board

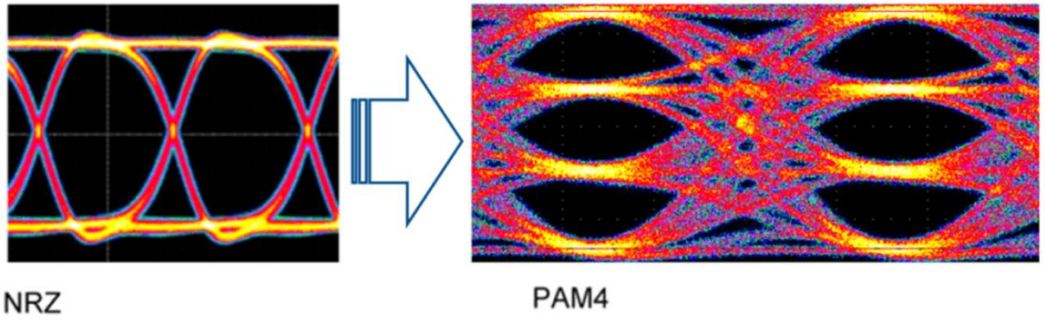
LDLA ASIC integrated in the customized optical module (SFP-like, 1Tx+1Rx) for test

- The first prototype of laser driver ASIC (LDLA) has been designed and verified.
- The ASIC has been integrated within the customized optical module, and verified.

Optical Transceiver- Higher Speed Research



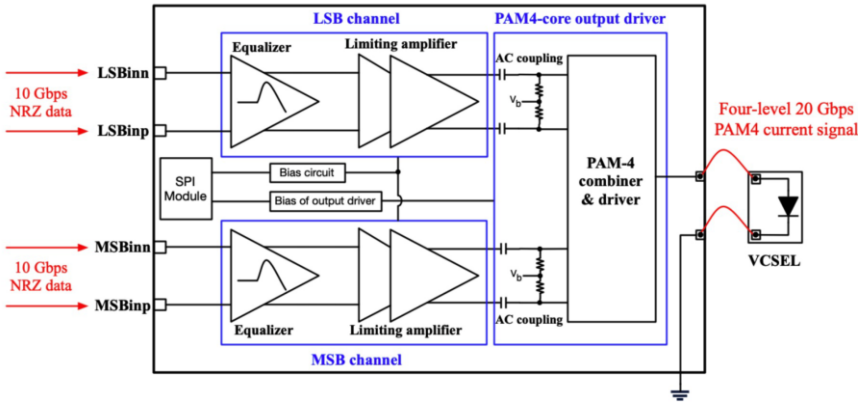
NRZ signal and PAM4 signal



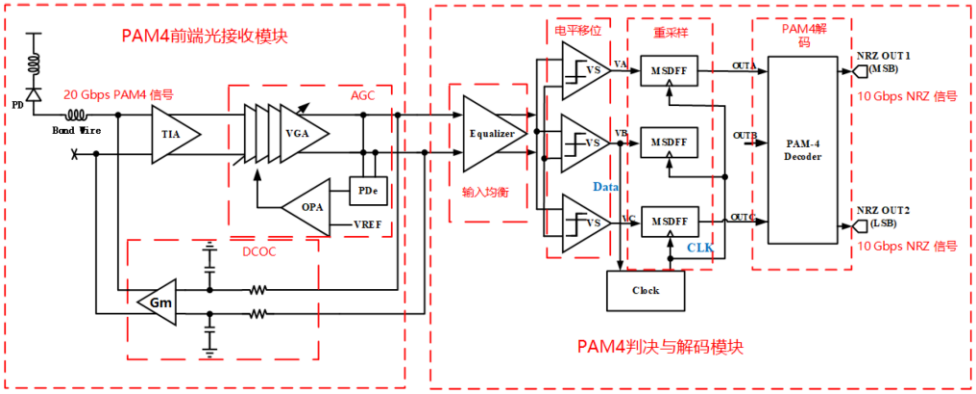
NRZ and PAM4 eyediagrams

- For higher speed optical data transmission development (two ways):
  - Use more peaking techniques in ASIC circuit design, and use more advanced process in ASIC manufacture for higher intrinsic analog bandwidth.
  - Use different signal modulation format, e.g. Pulse Amplitude Modulation 4-level (PAM4).

Optical Transceiver- Higher Speed Research



20Gbps/ch+ PAM4 VCSEL Driver ASIC Block Diagram



20Gbps/ch+ PAM4 Receiver ASIC Block Diagram

- PAM4 VCSEL Driver ASIC is under design. The core issue for this ASIC:
  - To combine and transform two regular NRZ signals into a 4 voltage level signal with enough amplitude and linearity.

- PAM4 Receiver ASIC is under design. The core issue for this ASIC:
  - To amplify the signal, and recover two NRZ signals from the PAM4 signal with enough bandwidth.

Summary

- Electronics system is a key component in large nuclear and particle physics experiments.
- The main task of the electronics is to extract time, charge and position with high precision from the random, weak and fast detector signals, then process the data in real time and transfer them to the back-end.
- Development of physics experiments drive technical progress of electronics in this field toward:
  - Higher precision: charge, time, and position
  - Higher speed: continuously increasing data transfer and processing capability
  - Higher density: higher channel density, more functionalities integrated

Thanks