

Serial Powering Test

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Quick reminder



L: GNDD, R: GND

L: SLDO input VinA
R: SLDO input VinD

L: VDDAser
R: VDDDser

- Chip: ATLASPix3
- 8 chips

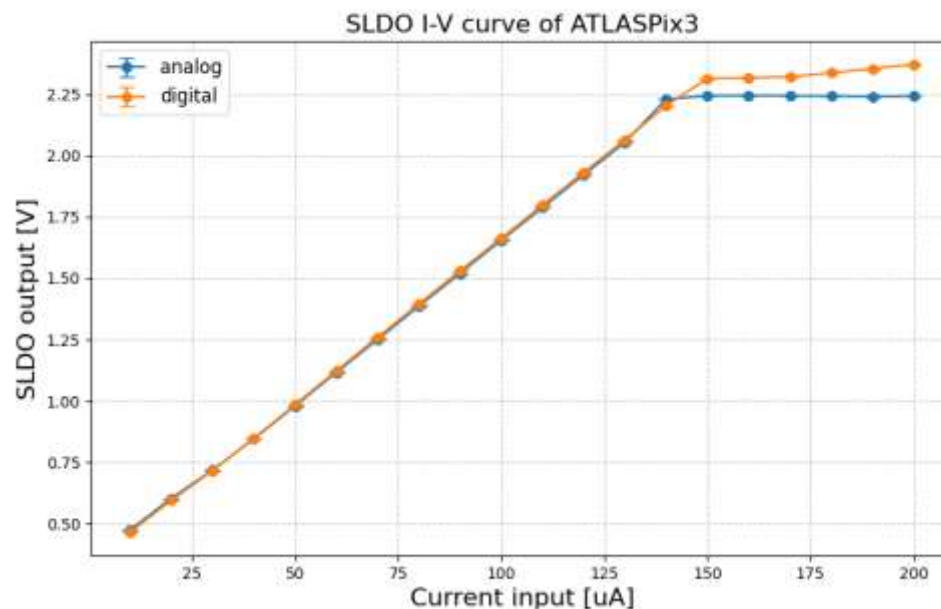
260318 used	
IHEP Band 02	chip1, analog(2.242V) and digital(2.371V) both OK.
IHEP-APX3.1-06	chip2, analog(1.705V) and digital(1.446V) both are slightly small
IHEP Band 011	chip3, analog(0.923V) is very small, digital(2.268V) usable
IHEP Band 09	chip4, analog(1.334V) is slightly small, digital(2.293V) usable
ATLASPix3.1-IHEP-3.102	chip5(high current)
260331 used	
IHEP Band #14	chip6 delaminated, both analog and digital unusable
IHEP-APX3.1-05	chip7, analog(1.599V) and digital(1.662V) both are slightly small
IHEP Band 013	chip8, analog(2.467V) and digital(2.498V) both usable.

- ATLASPix3

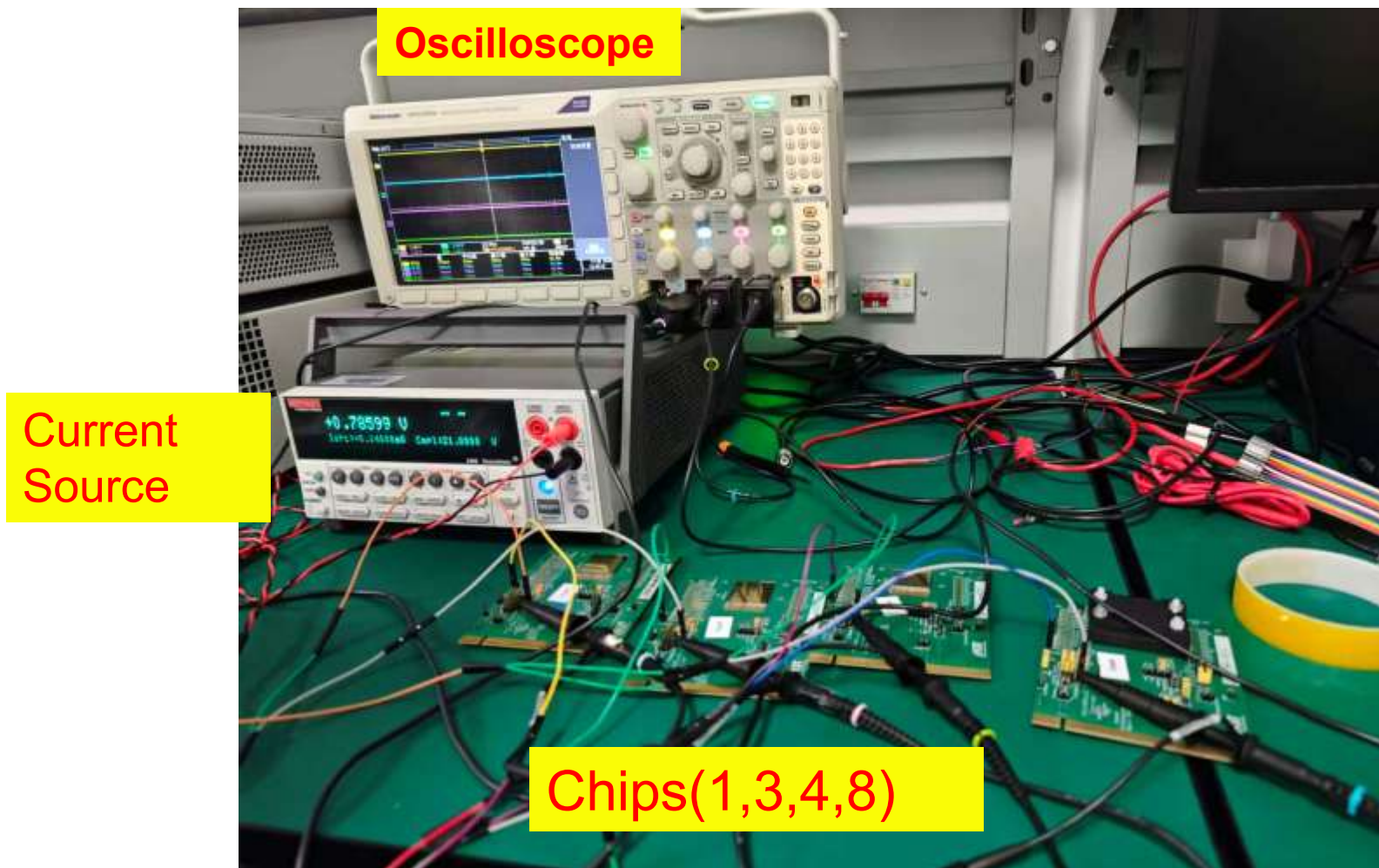
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Chips 1, 3, 4, and 8 have been selected for subsequent multi-chip testing.

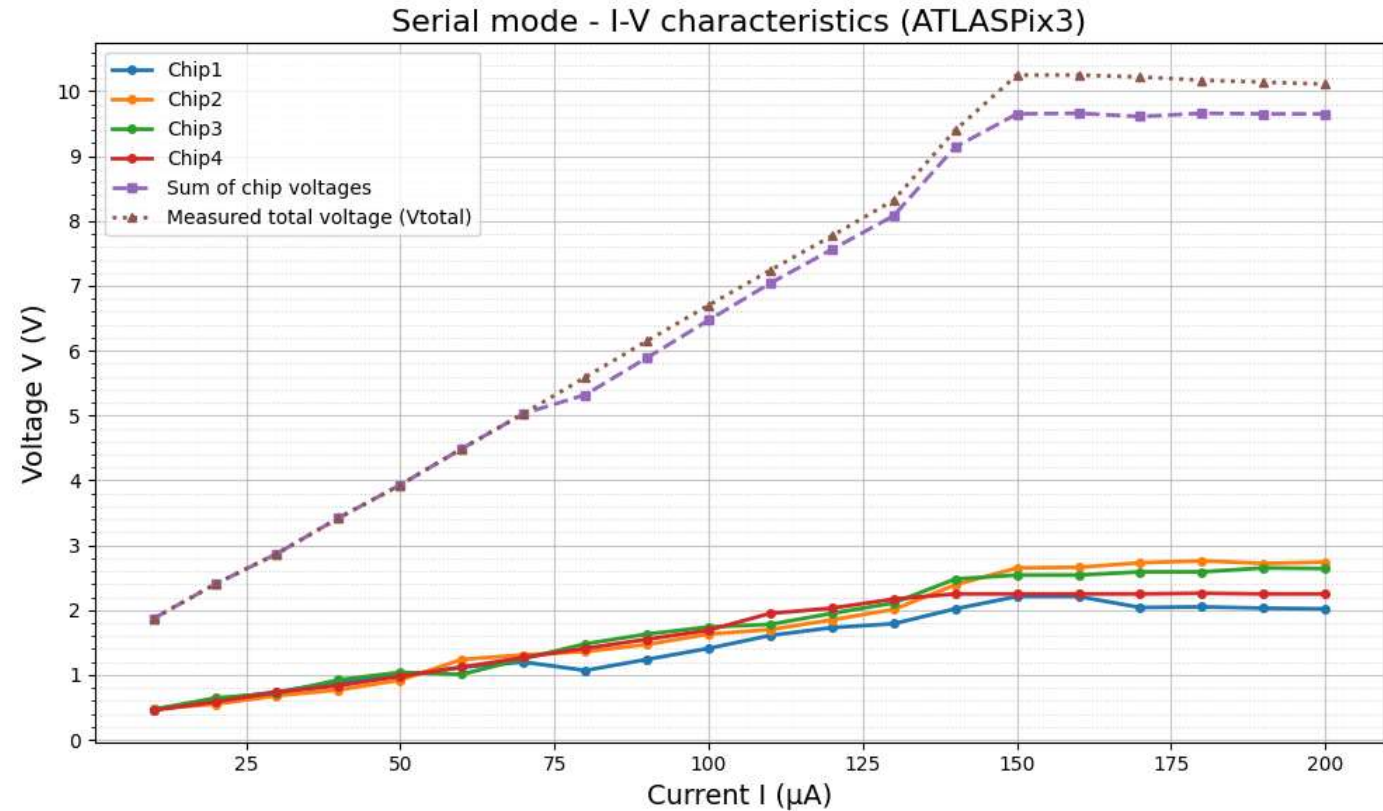
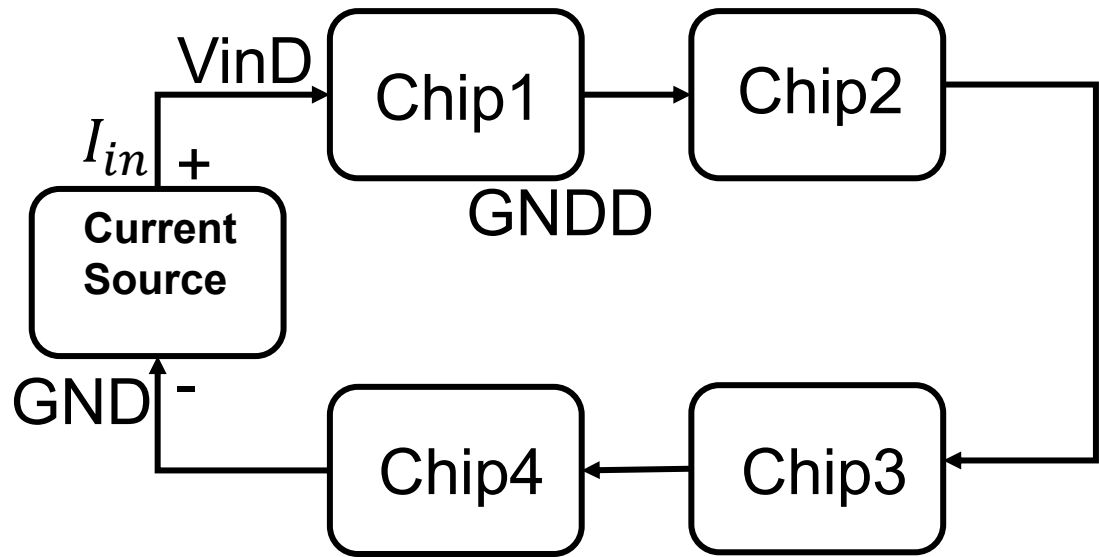
- Chip1 results



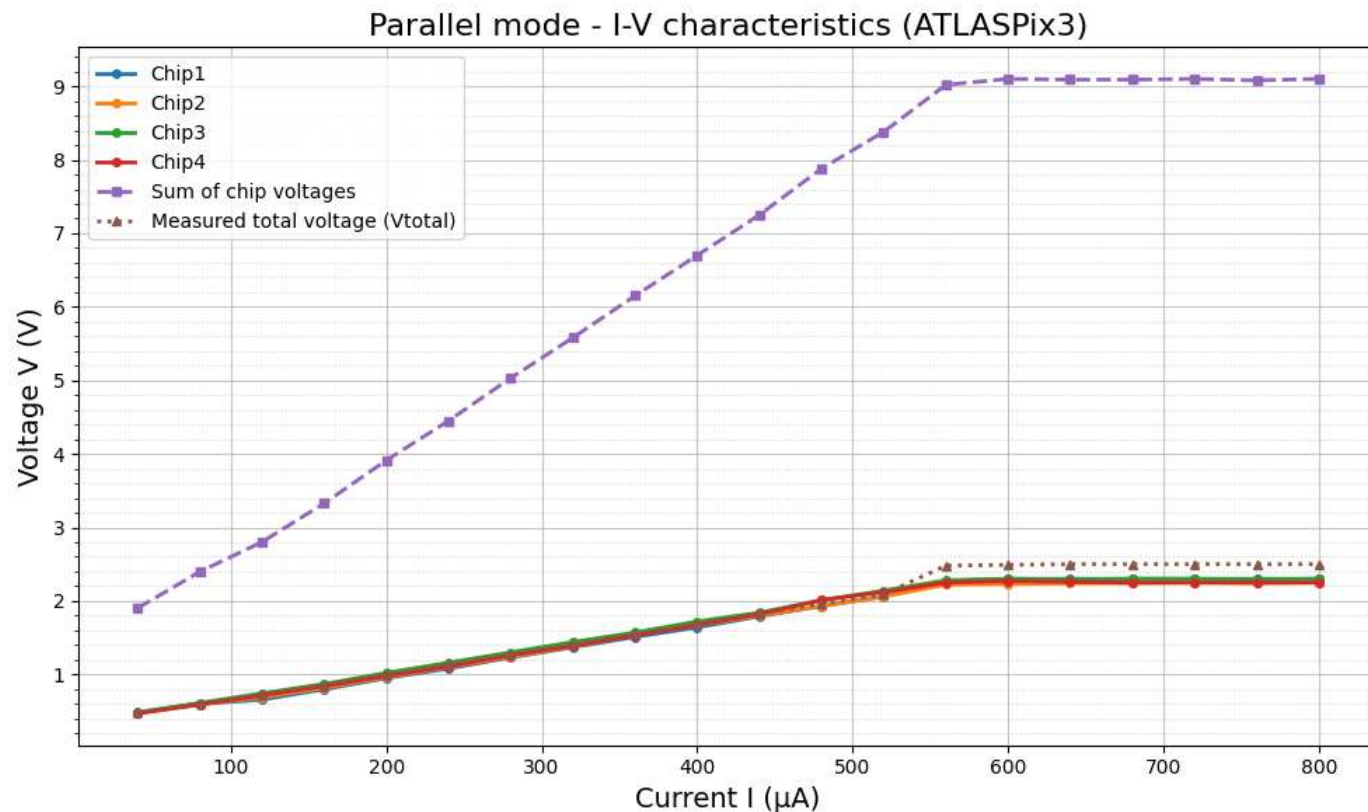
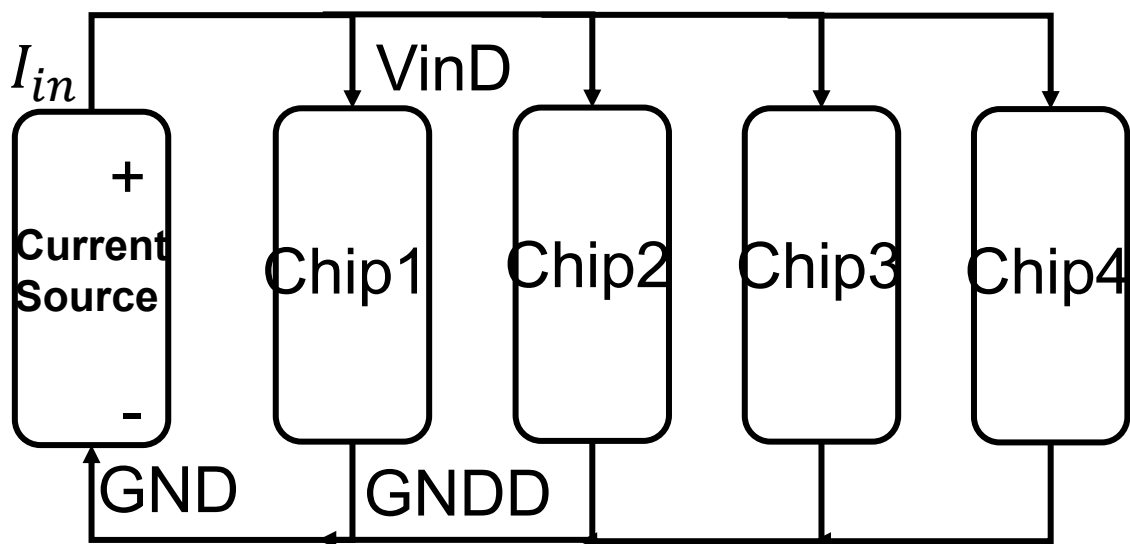
Test setup



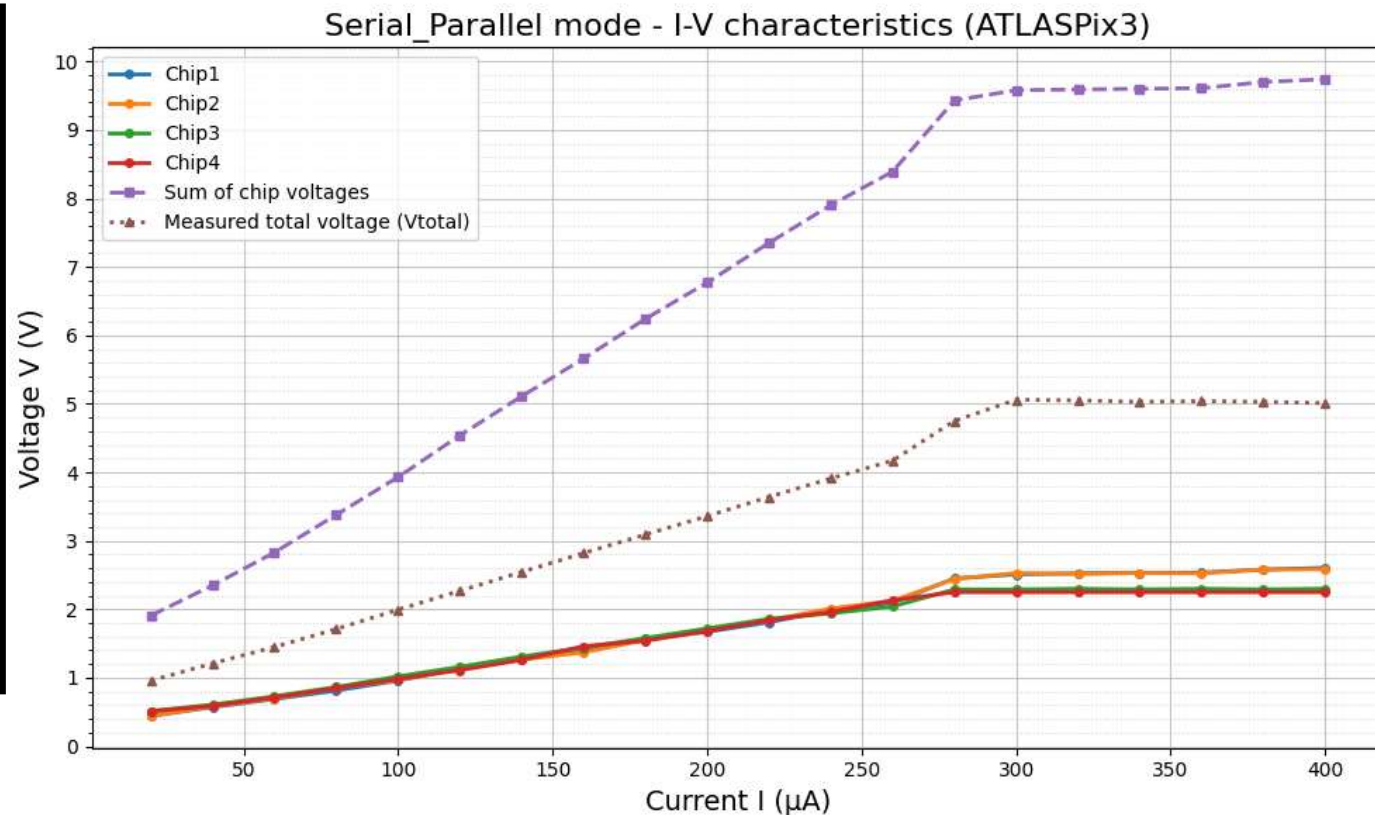
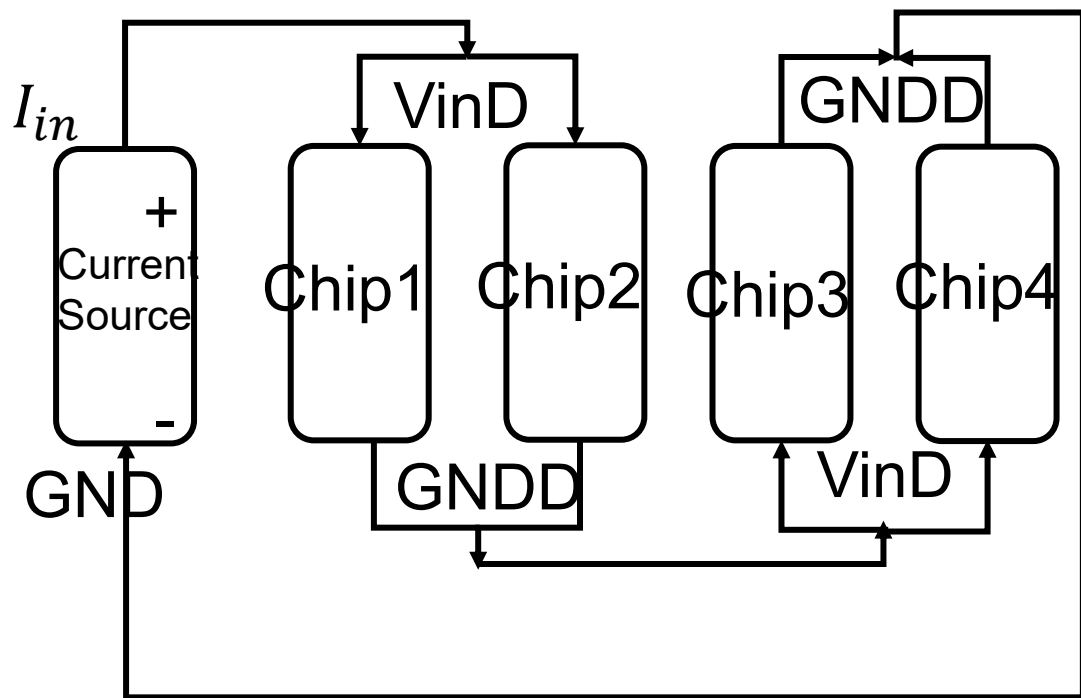
Test the digital output of all chips.



- The SLDO works normally, each chip's voltage is automatically regulated, and the link is stable.



- In the low-current region, the consistency of the chip output voltages is good
- For currents $\geq 560 \mu\text{A}$, the voltages of each chip stabilize around 2.30 V, with a maximum deviation of 2.6%.



- Modules with parallel chips in series power supply
- Within each group, parallel chip voltage deviation $<4\%$
- Total voltage rises with current and stabilizes at high current — system works normally

- Testing chips with the probe card.
- Serial powering test using a 1×4 test board.