Serial Powering Test

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Quick reminder

L：GNDD，R：GND

L：SLDO input VinA
R：SLDO input VinD

L：VDDAser
R：VDDDser

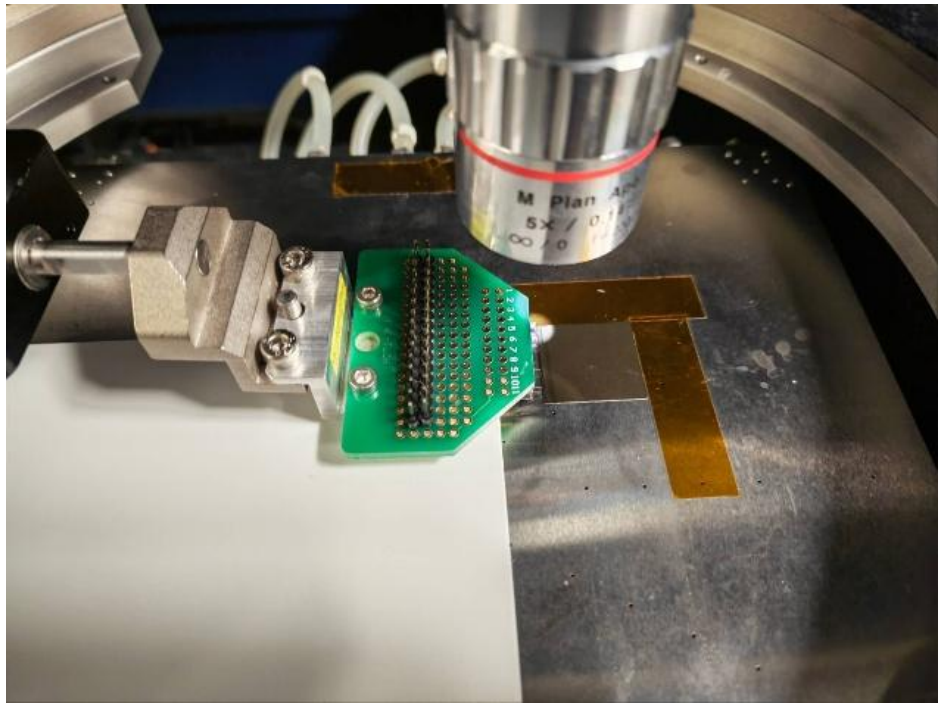
- Chip：ATLASPix3
- 8 chips

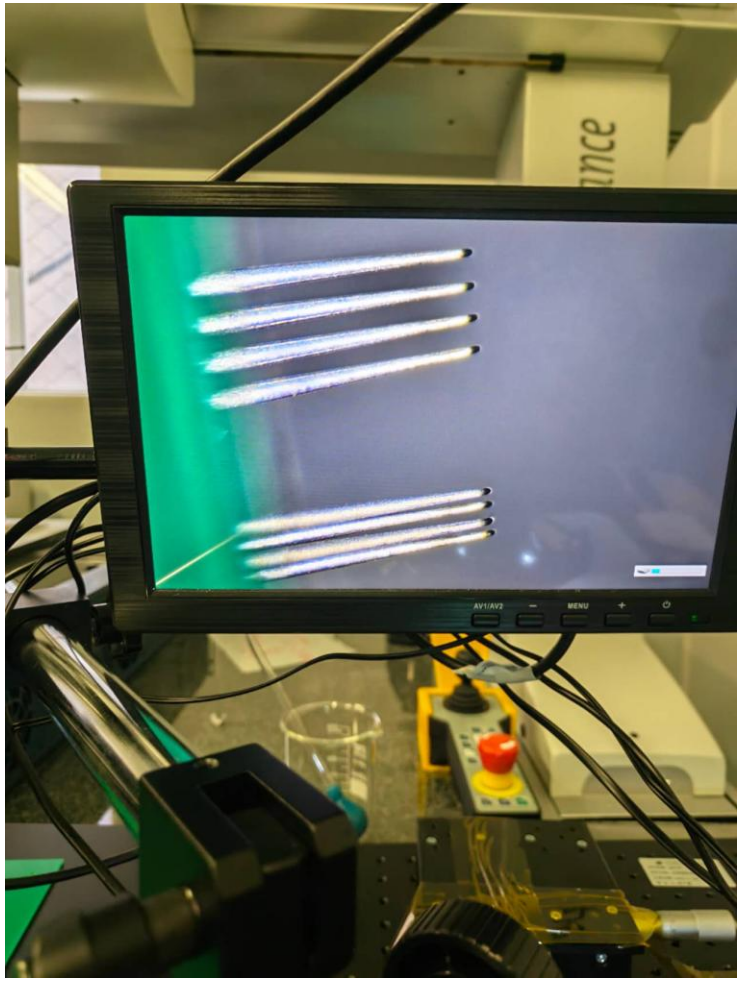
260318 used	
IHEP Band ø2	chip1，analog(2.242V) and digital(2.371V) both OK.
IHEP-APX3.1-06	chip2，analog(1.705V) and digital(1.446V) both are slightly small
IHEP Band ø11	chip3，analog(0.923V) is very small, digital(2.268V) usable
IHEP Band ø9	chip4，analog(1.334V) is slightly small, digital(2.293V) usable
ATLASPix3.1-IHEP-3.102	chip5(high current)
260331 used	
IHEP Band #14	chip6 delaminated, both analog and digital unusable
IHEP-APX3.1-05	chip7，analog(1.599V) and digital(1.662V) both are slightly small
IHEP Band ø13	chip8，analog(2.467V) and digital(2.498V) both usable.

Chips 1, 3, 4, and 8 have been selected for subsequent multi-chip testing.

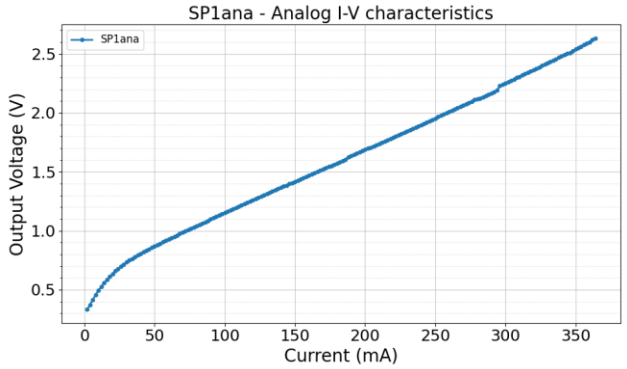
Bare chip test

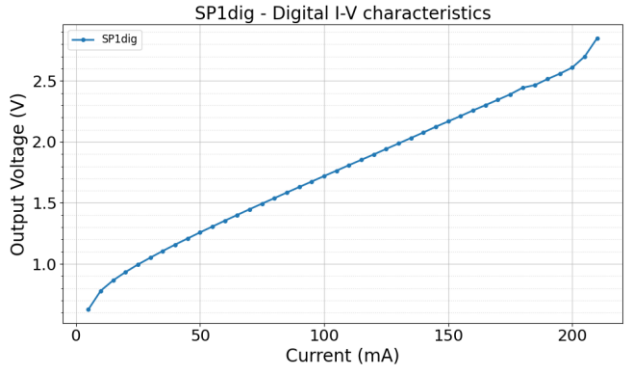
- Testing bare chips with the probe card
- Analog and digital output are both tested

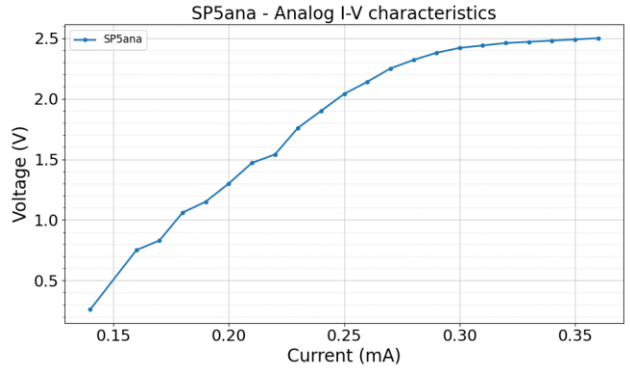


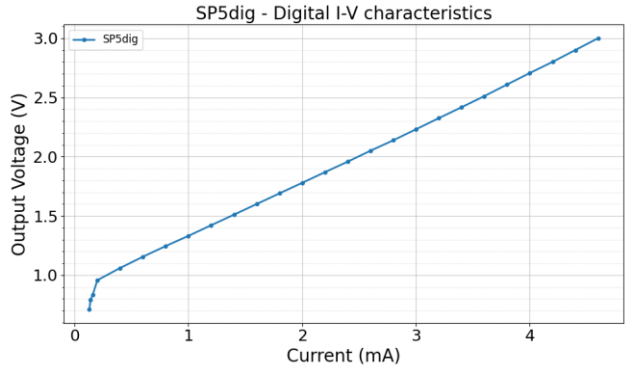


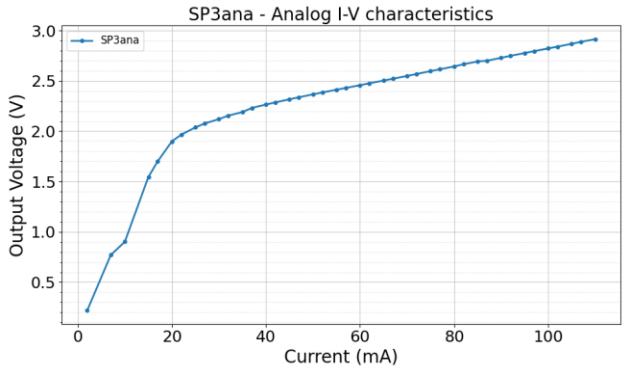
Bare chip test

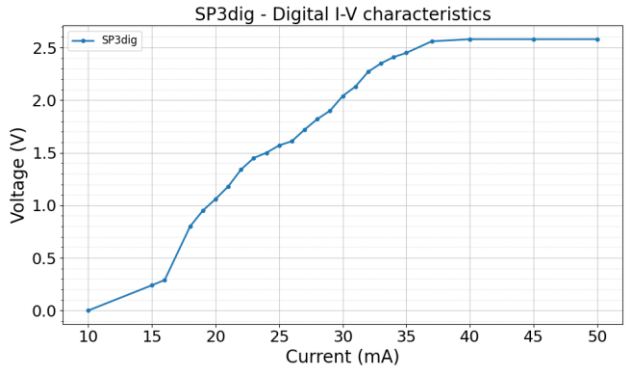


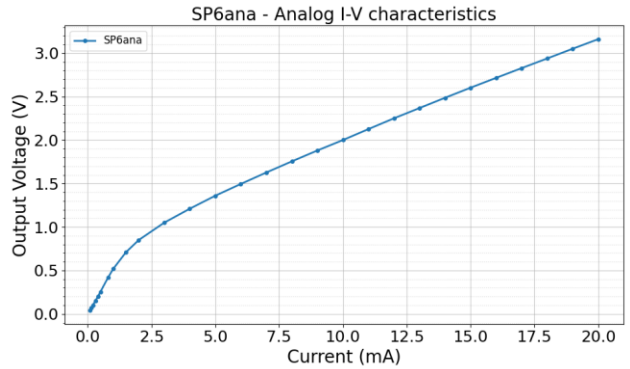


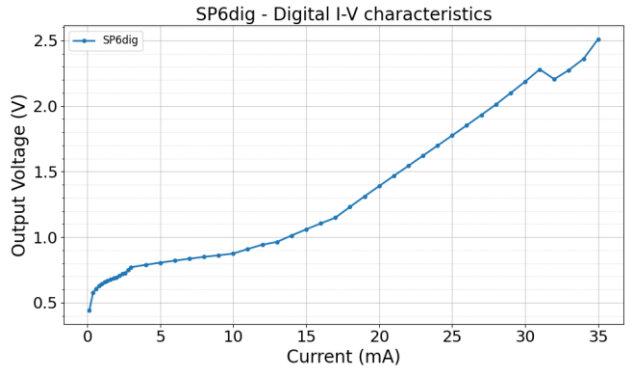


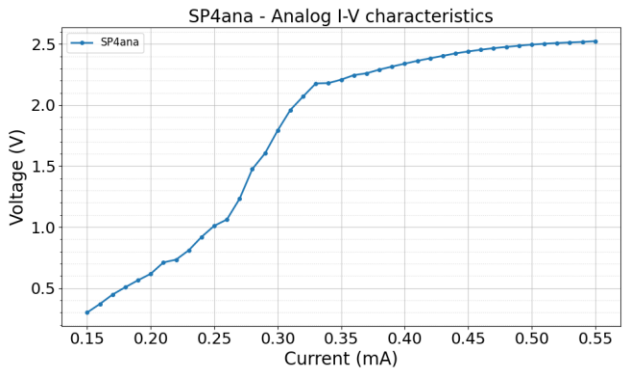


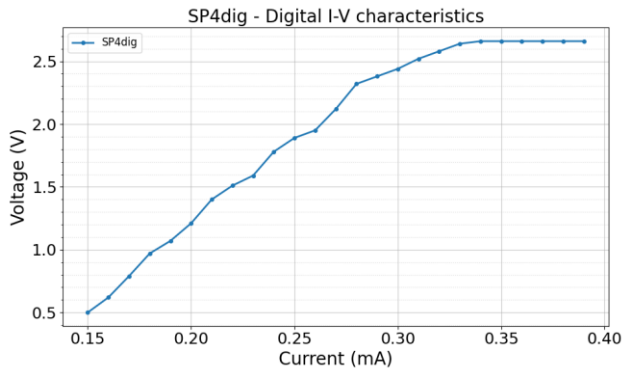


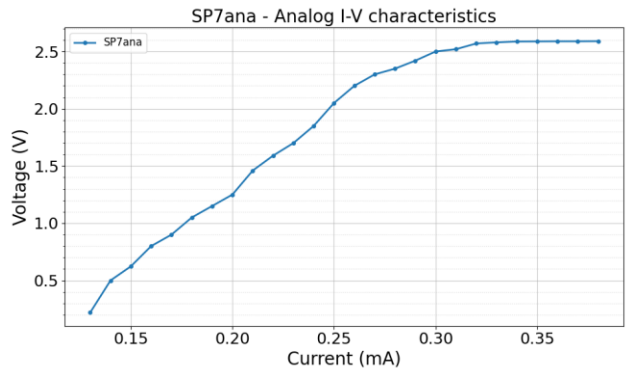


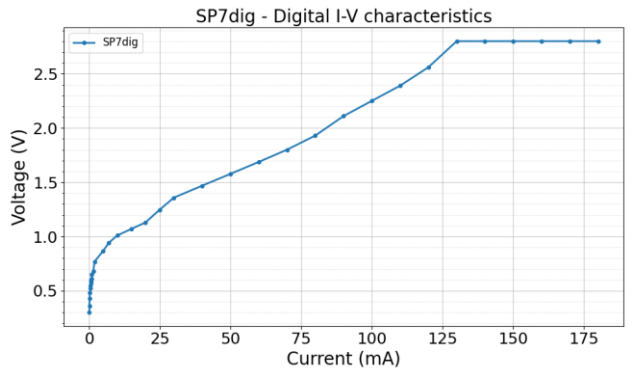












Bare chip test

- Not every chip shows a saturation voltage
- The supply current ranges differ significantly
- Faut's thesis mentions Table 5.1 summarizes chip failure reasons based on I–V plots, but the version we received only starts from Chapter 6.2.3.

Summary of test

Chip_Name	VDDA(V)	VDDD(V)	InputCurrent ana(mA)	InputCurrent dig(mA)	
SP1	2.57	3.14	364.0	210	No Saturation
SP2	/	/	/	/	Data forgot to saved
SP3	3.02	2.53	110.0	50.0	Saturation
SP4	1.95	2.65	0.6	0.4	Saturation
SP5	2.50	2.71	0.4	4.6	Analog Saturation
SP6	2.45	3.02	20.0	35.0	No Saturation
SP7	2.54	2.8	0.4	180.0	Saturation