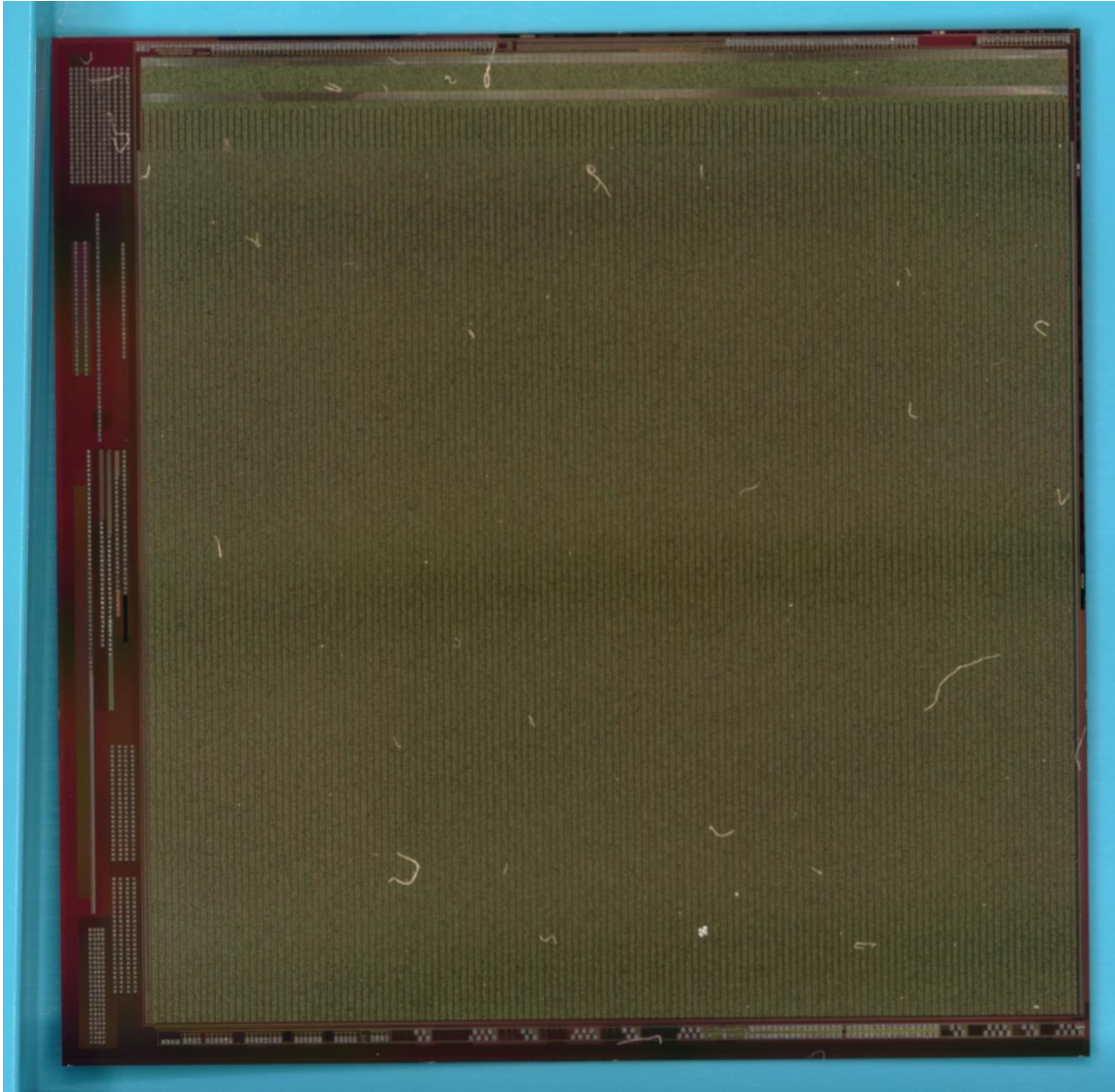




50 μ m ATLASPix3.1 Probe Setup

Fuat Ustuner, Yanyan Gao, Hussain Al Saleh

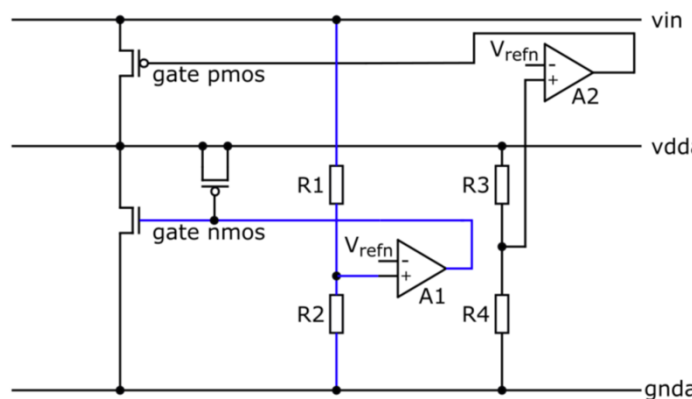
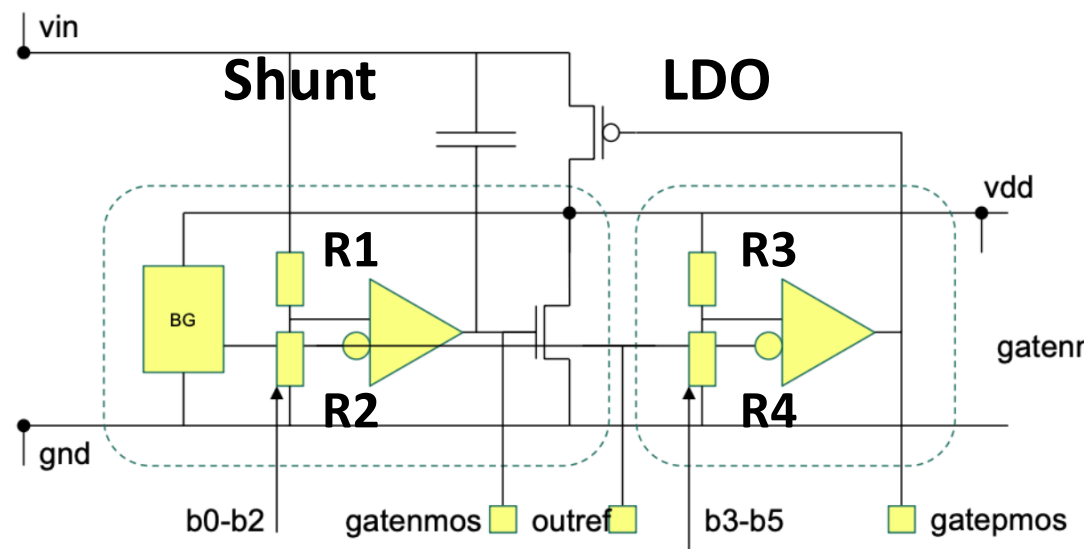
Overview



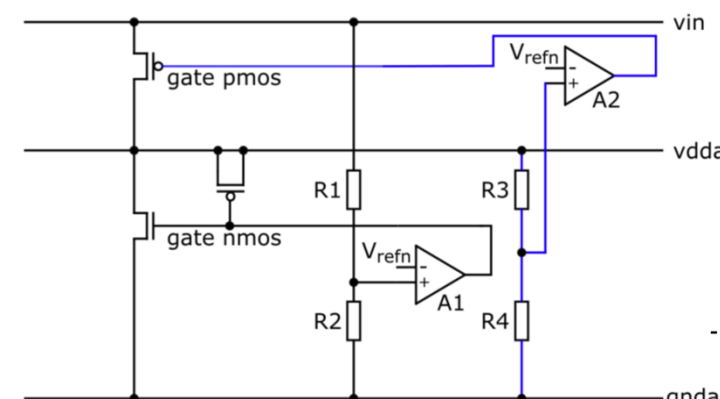
- Brief recap about ATLASPix3.1 SLDO circuit.
- Probing setup used at Edinburgh.
- Setup connection diagram and 50 μm ATLASPix3.1 pad structure.
- SLDO I–V curves for a single bare chip under different configurations.

Shunt-LDO Regulators on the Chip

- ATLASPix3.1 has **fully functional two shunt-low dropout regulators**.
 - **Digital & Analog domains (VDDD/A)**
 - 3-bits (b0-b2) to **tune load current**
 - 3-bits (b3-b5) to **tune VDDs**
- **V_{in}** is created from constant current via regulators.
- **VDDD/A** presents the **regulated voltage** (output of the shunt-LDOs) to use the chip for operation.

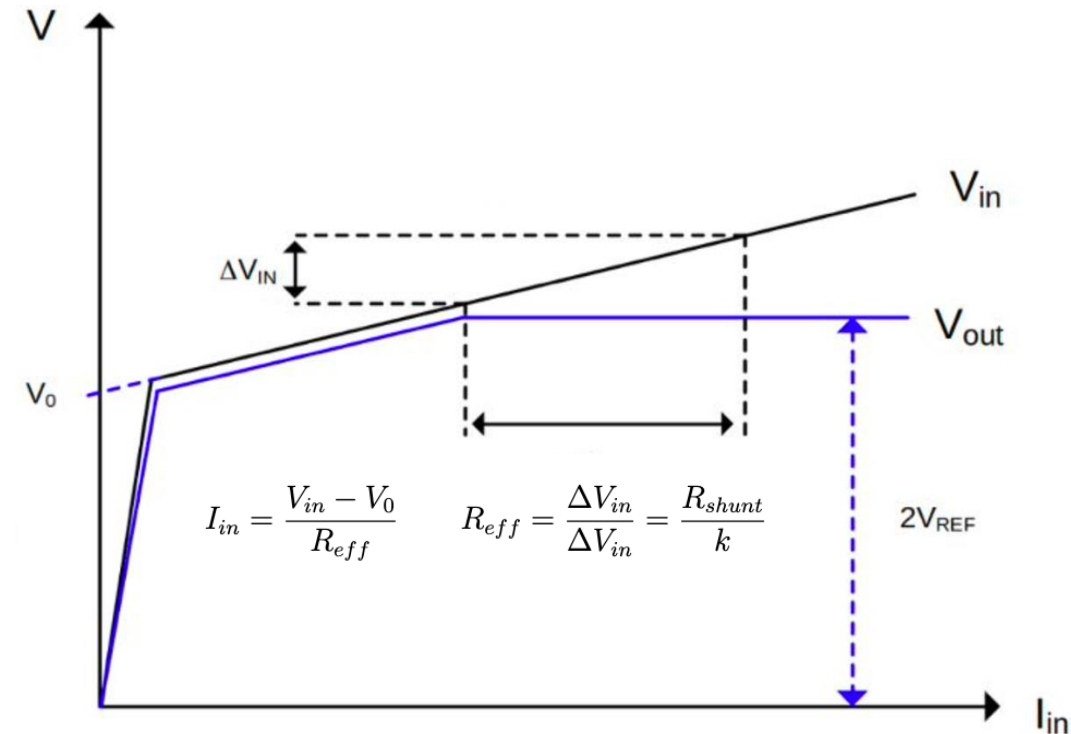


Shunt: allows for the constant current operation, extra current protection

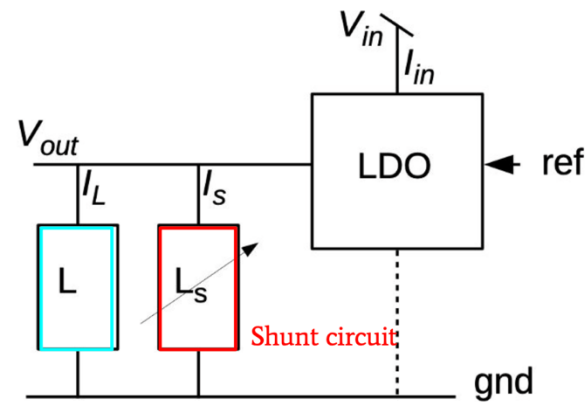


LDO: regulates VDDD/A

Shunt-LDO Characterisation



J.Chan Serial Powering for ATLAS ITk Pixel Modules



- Verify the **ohmic behavior** & compare theoretical prediction.
- Recording operation current (I_{in}) and the regulated output level.
- Single chip shunt-LDO characterisation (After regulation starts:
 - $2V_{ref} \sim V_{DDA}/D$,
 - $I_{in} > I_L$

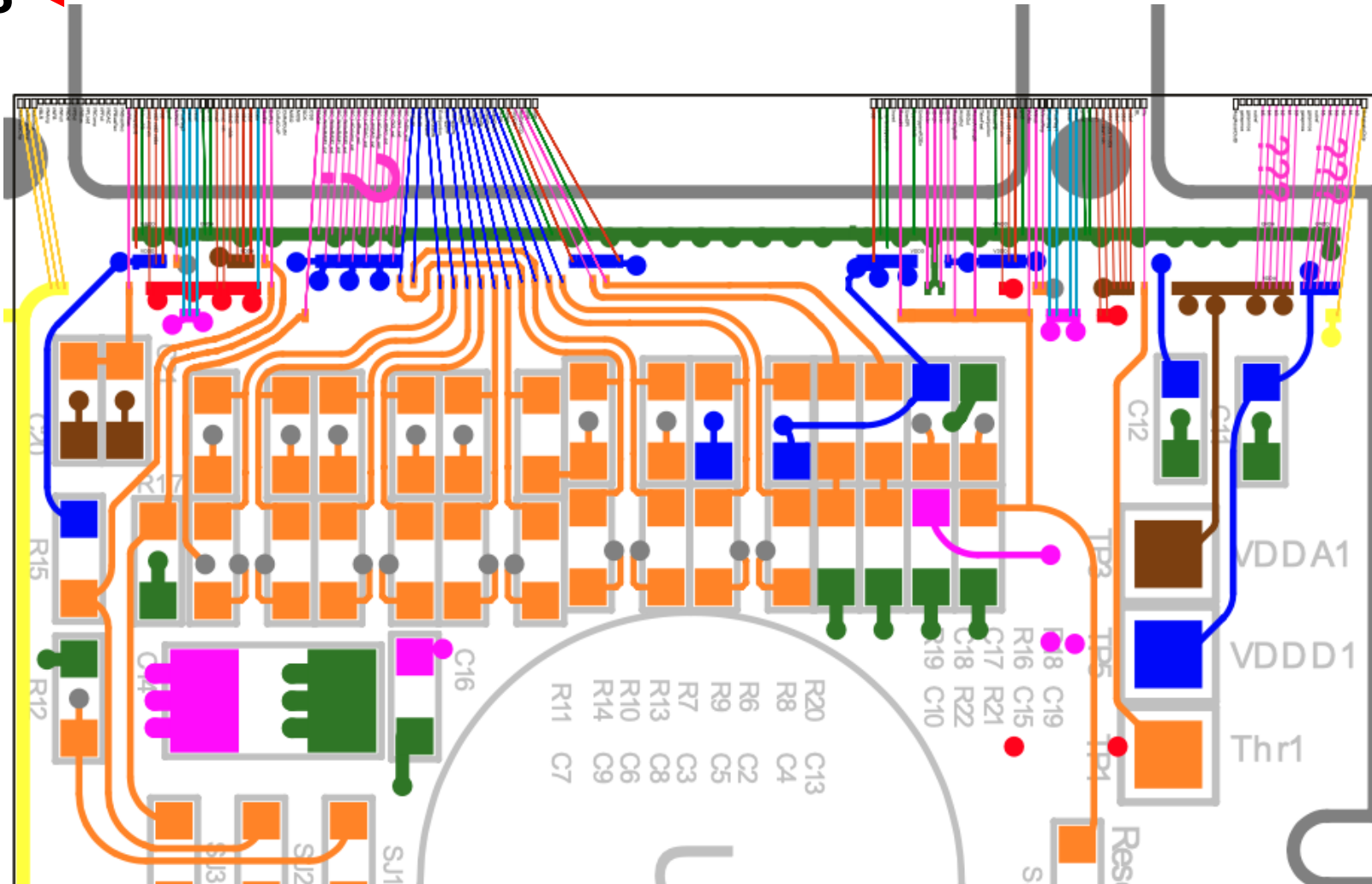
Probe Setup at Edinburgh



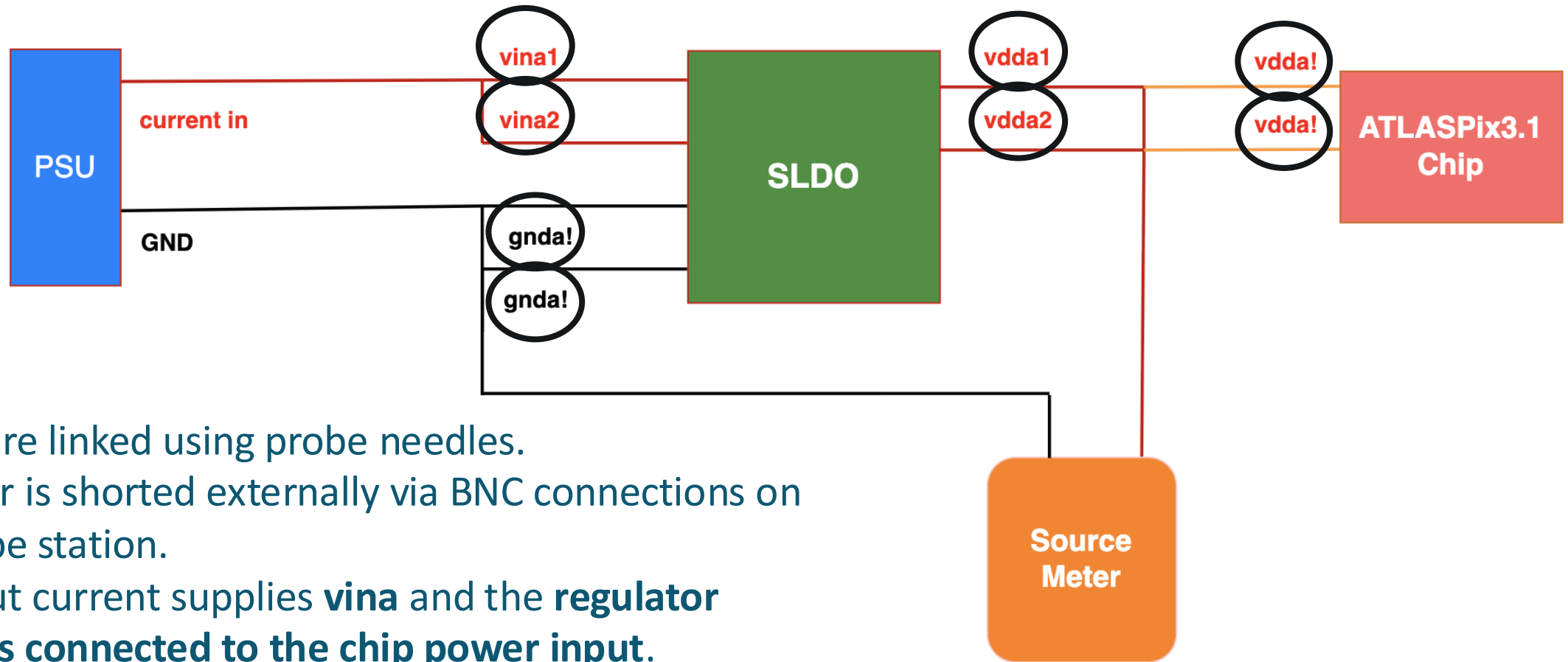
ATLASPix3.1 Pad Mapping

Pad 138

Pad 1

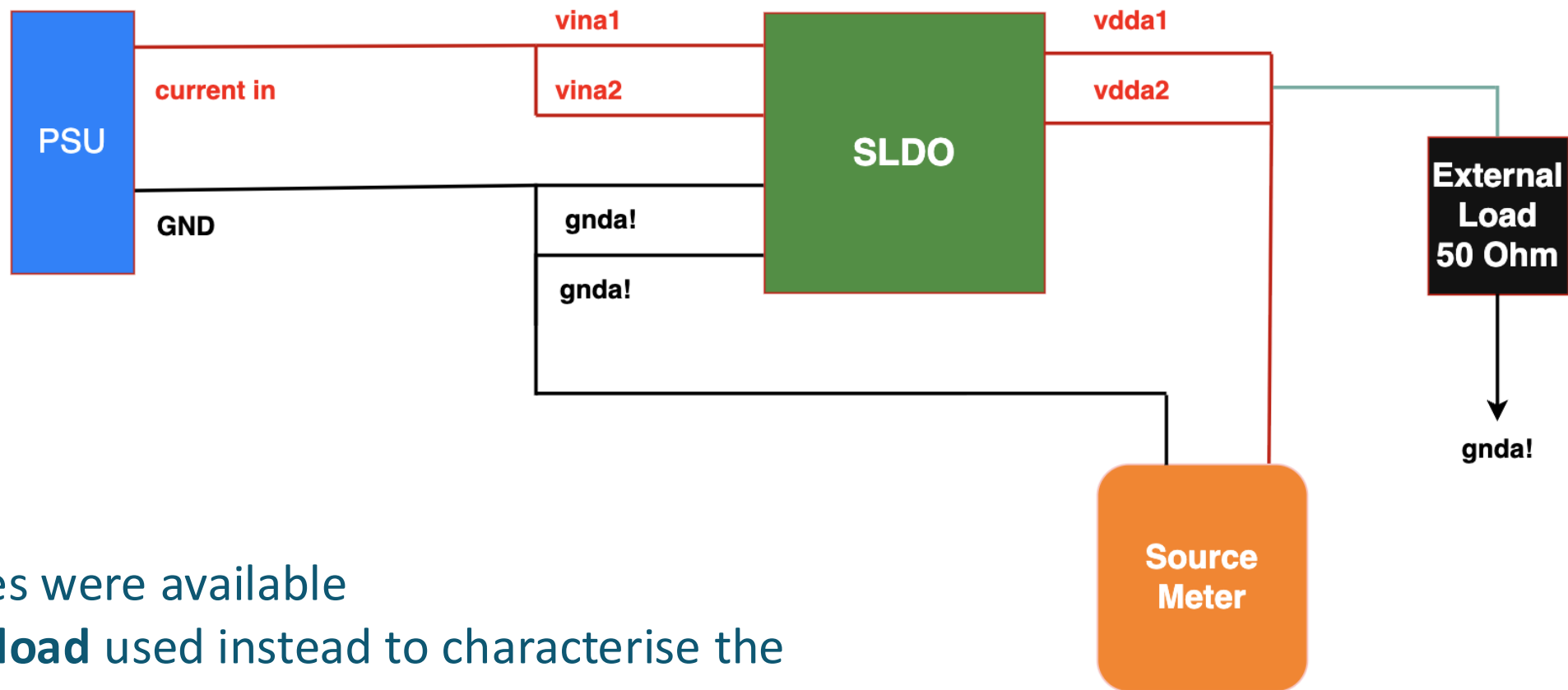


Probe Setup Connection for SLDO



- **8 pads** are linked using probe needles.
- Each pair is shorted externally via BNC connections on the probe station.
- The input current supplies **vina** and the **regulator output is connected to the chip power input**.
 - Otherwise, the SLDO output would see an open circuit (infinite load)
 - Feedback loop, overshoot of the output, oscillations.

Probe Setup Connection for SLDO



- Only six probes were available
- **50Ω external load** used instead to characterise the SLDO.
 - This external load did not show the chip actual load response!

Setup for Analog Domain

Vdda2, pad 106

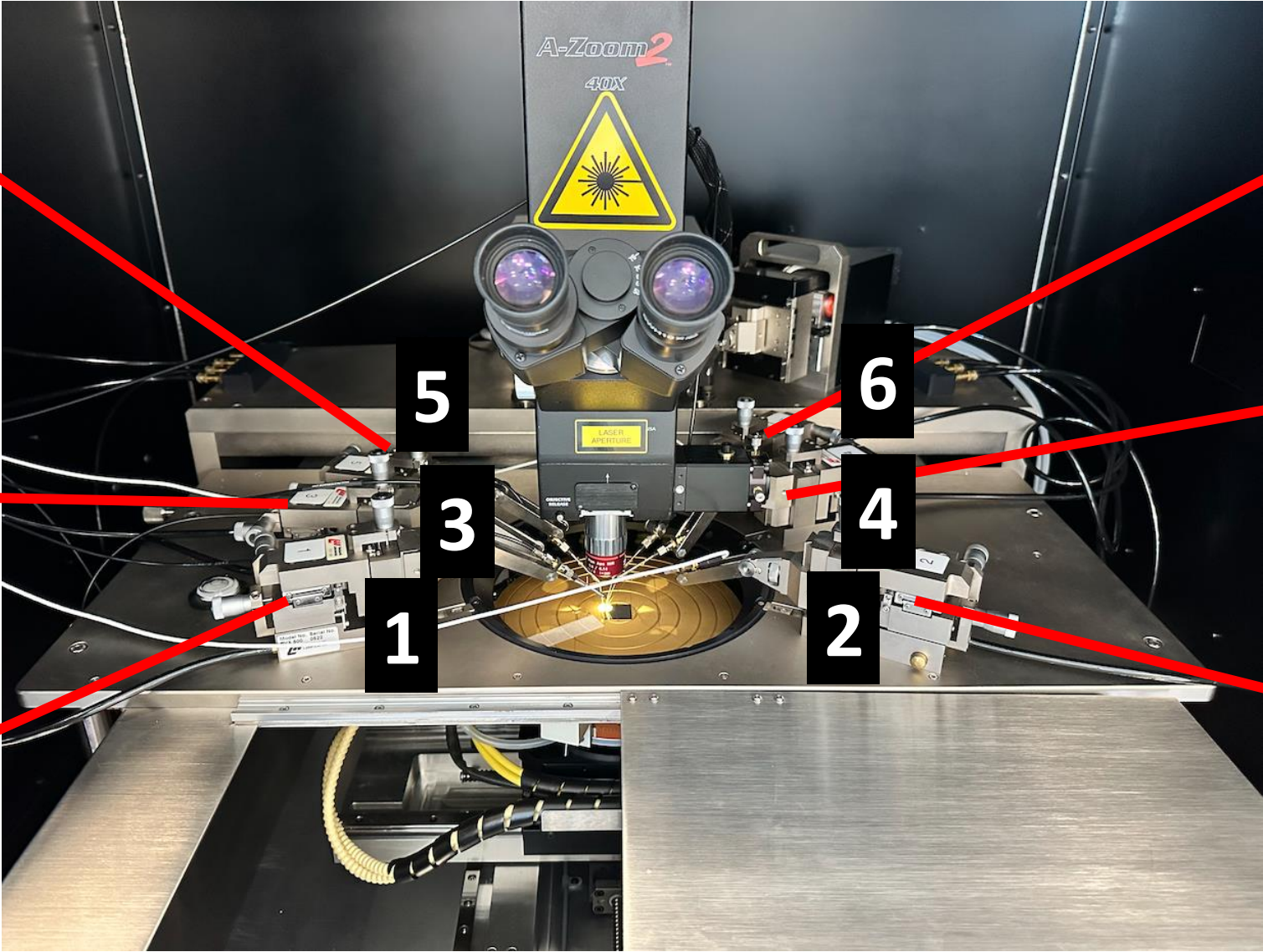
Vdda1, pad 26

Vina2, pad 108

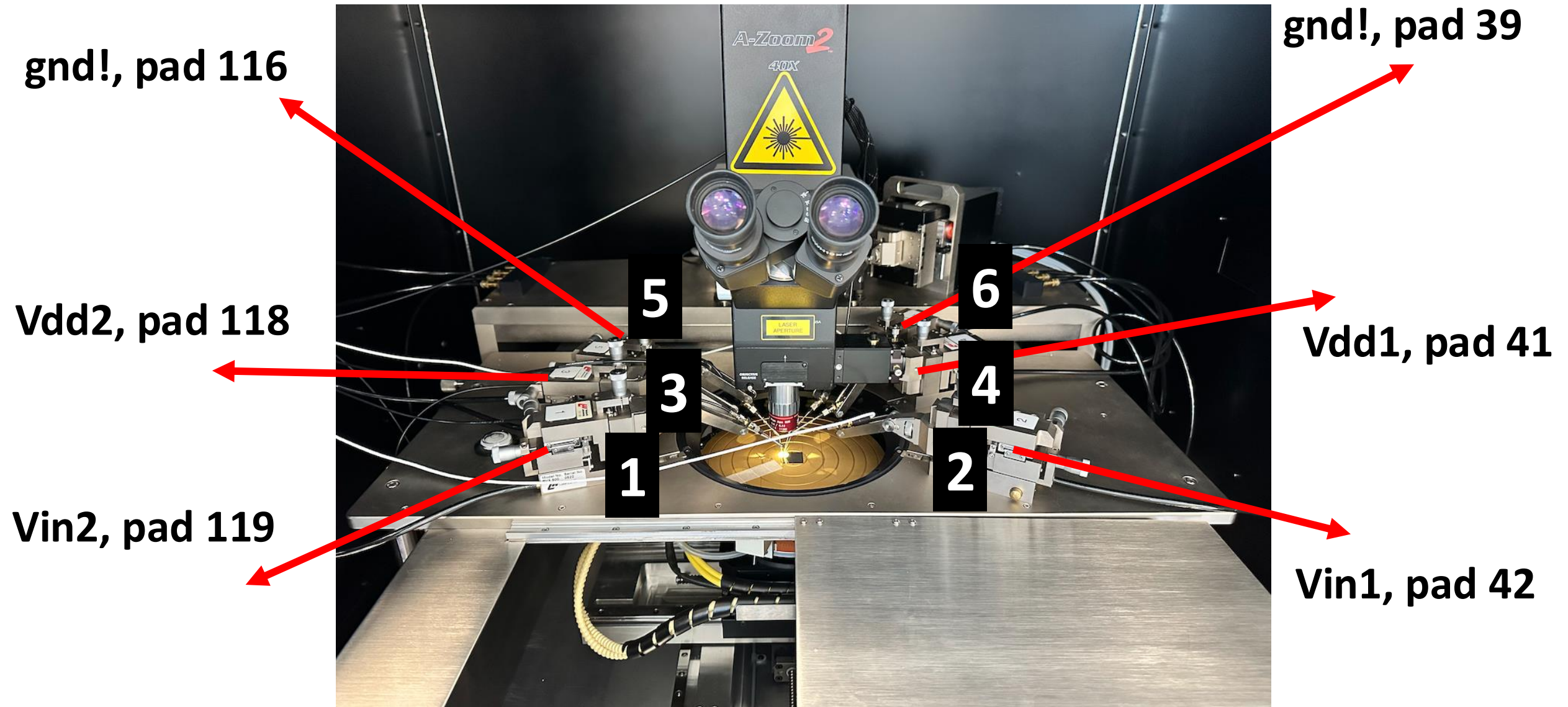
Vina1, pad 28

gnda!, pad 110

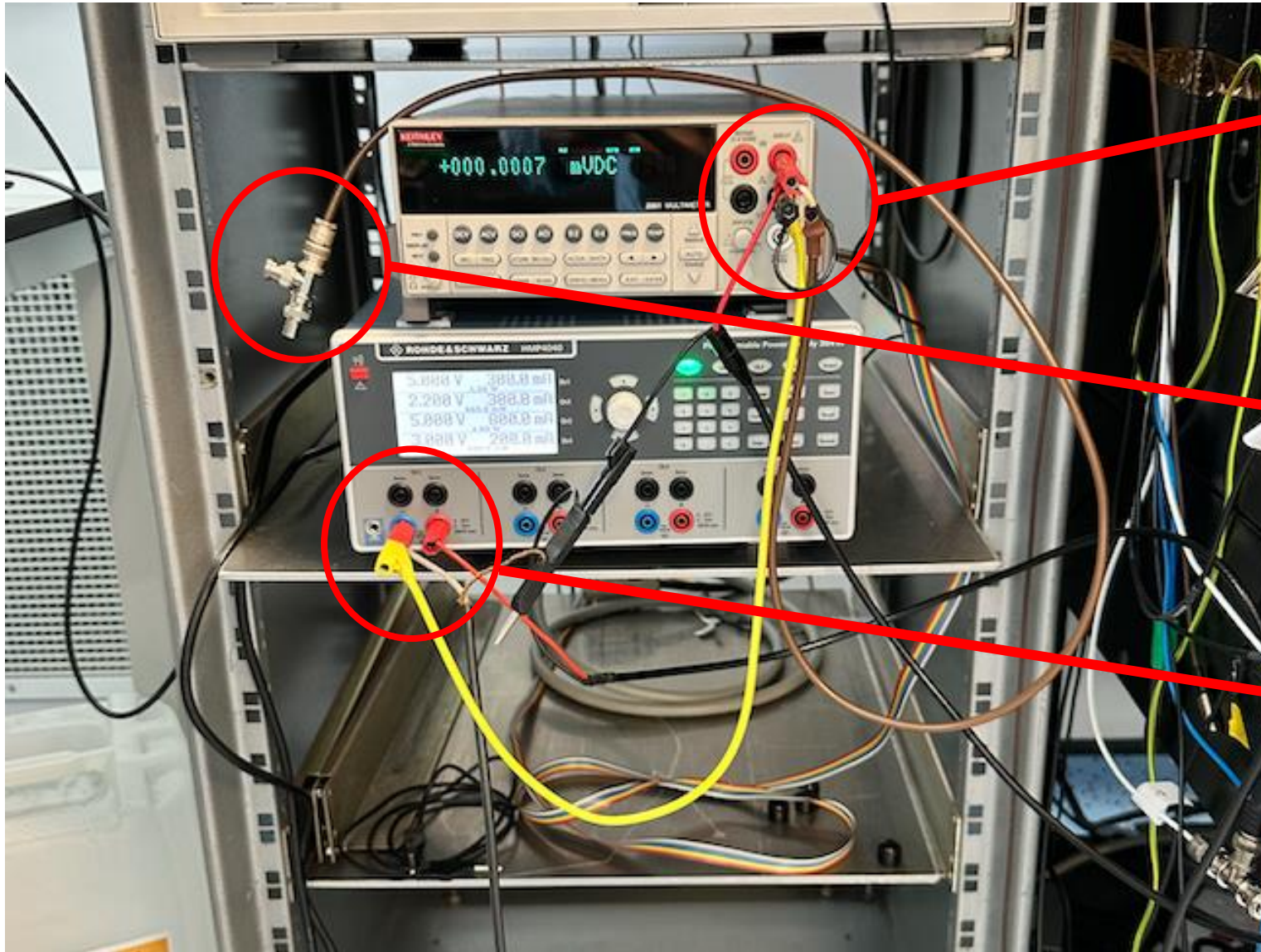
gnda!, pad 30



Setup for Digital Domain



PSU Source Meter Setup



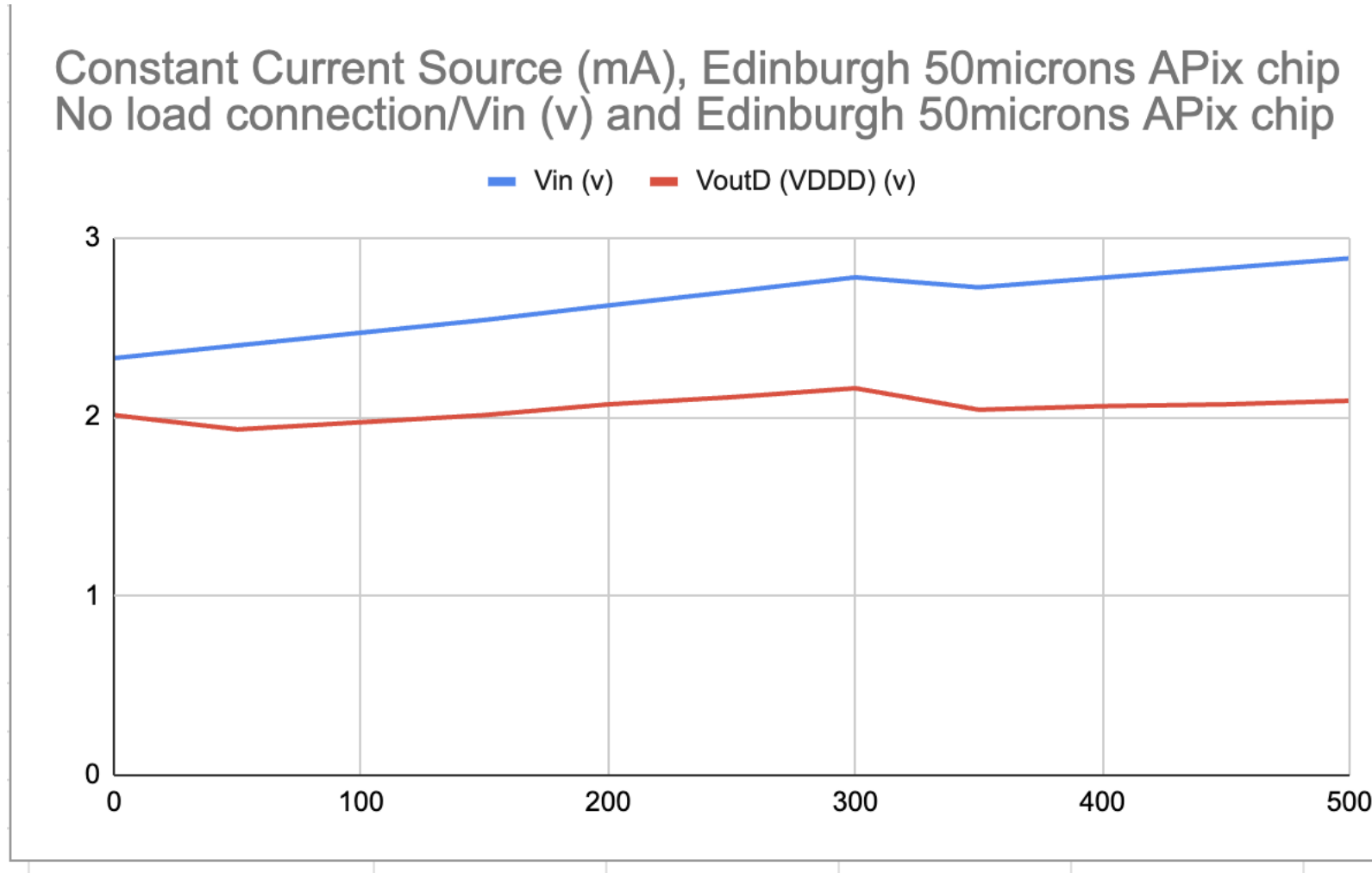
vdda1 & vdda2

External load, 50Ω

Gnd! and Vina1&Vina2

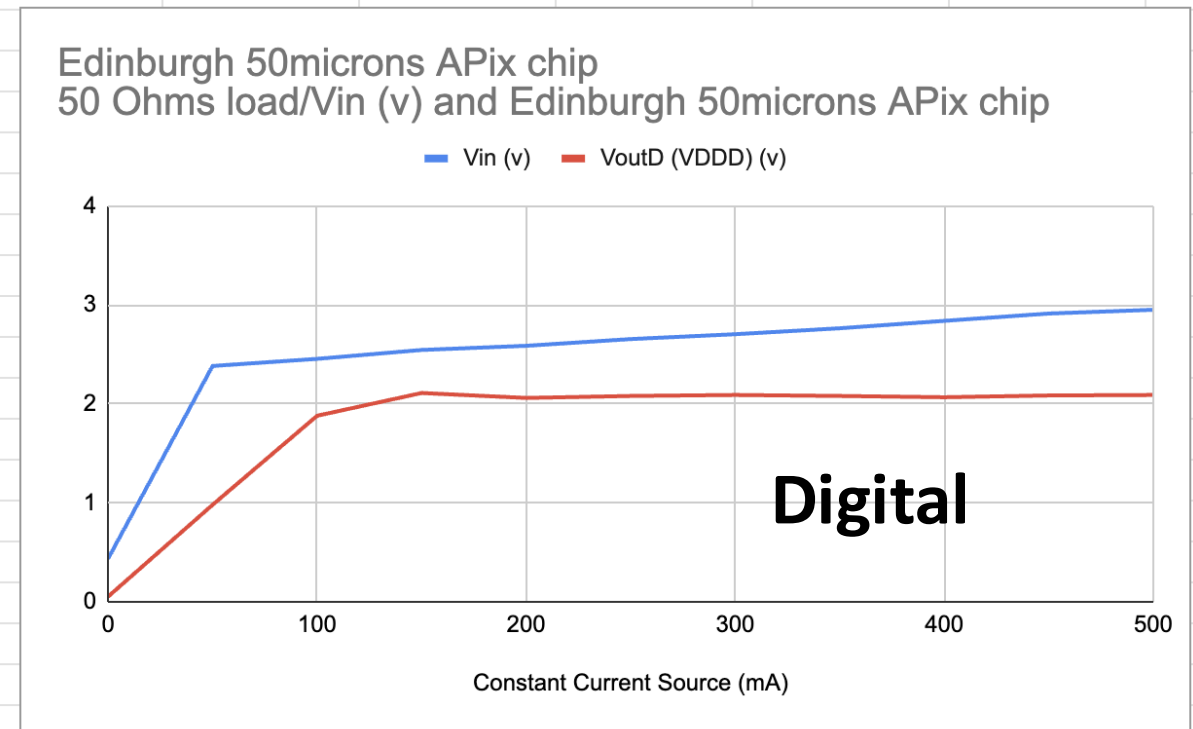
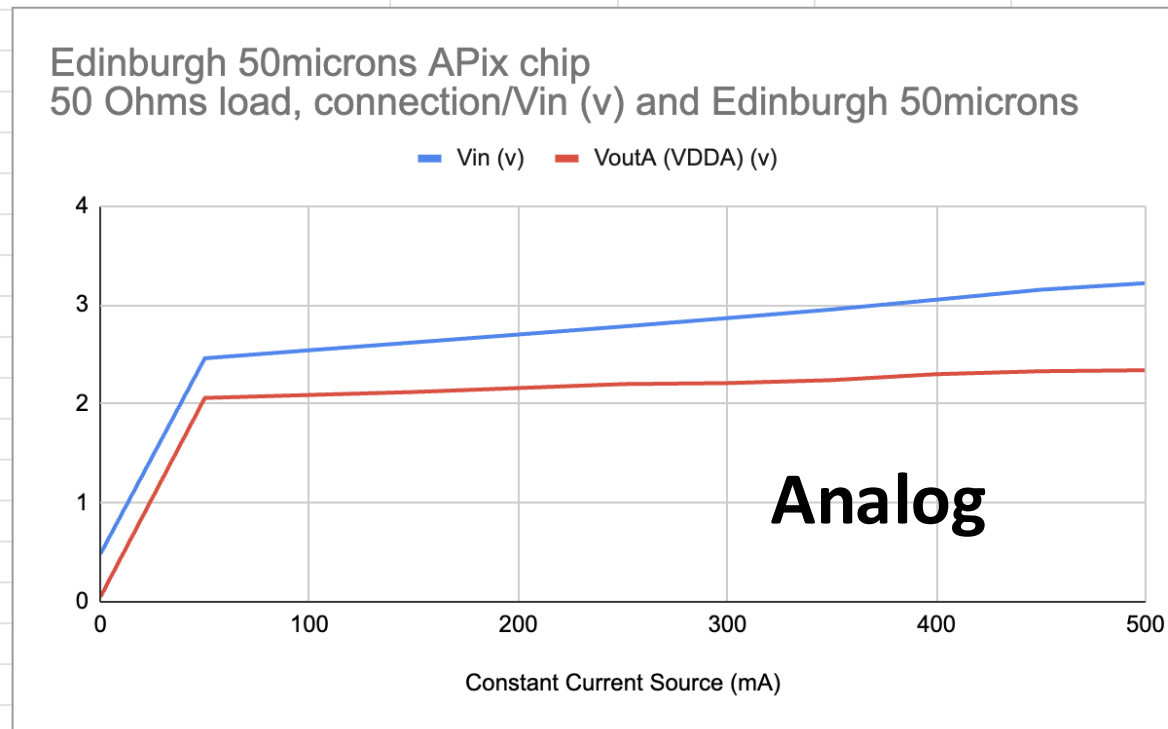
Digital Domain SLDO IV

Constant Current Source (mA), Edinburgh 50microns APix chip
No load connection/ V_{in} (v) and Edinburgh 50microns APix chip



- **No load connection to the output of the SLDO regulator.**
- **It regulates immediately and does not follow normal behaviour.**

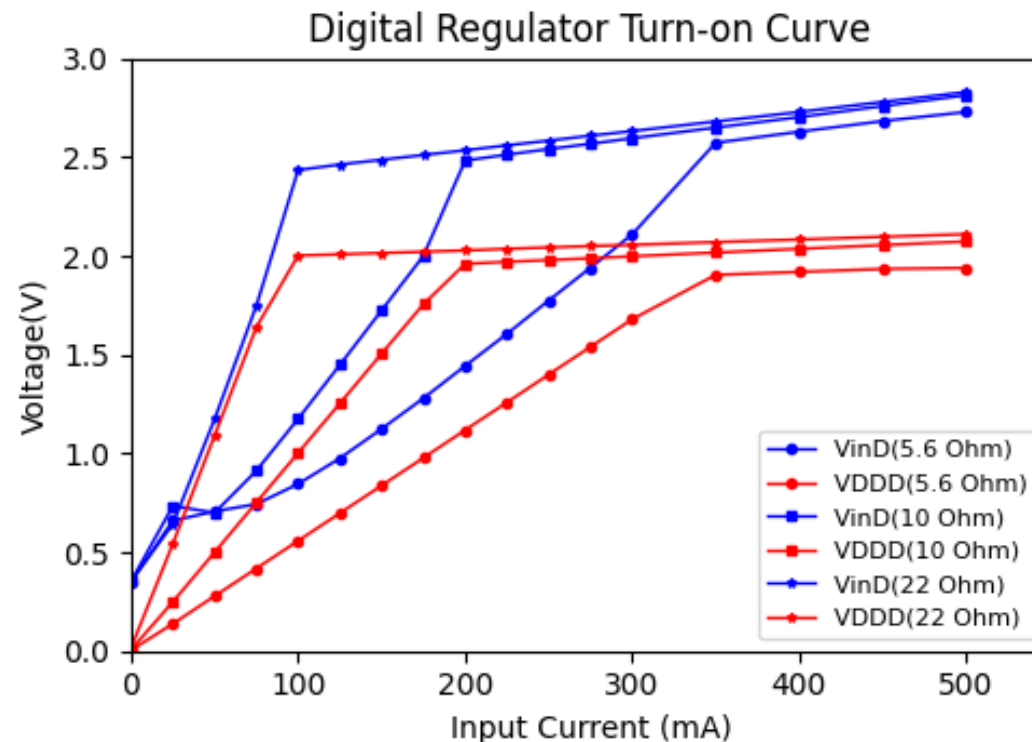
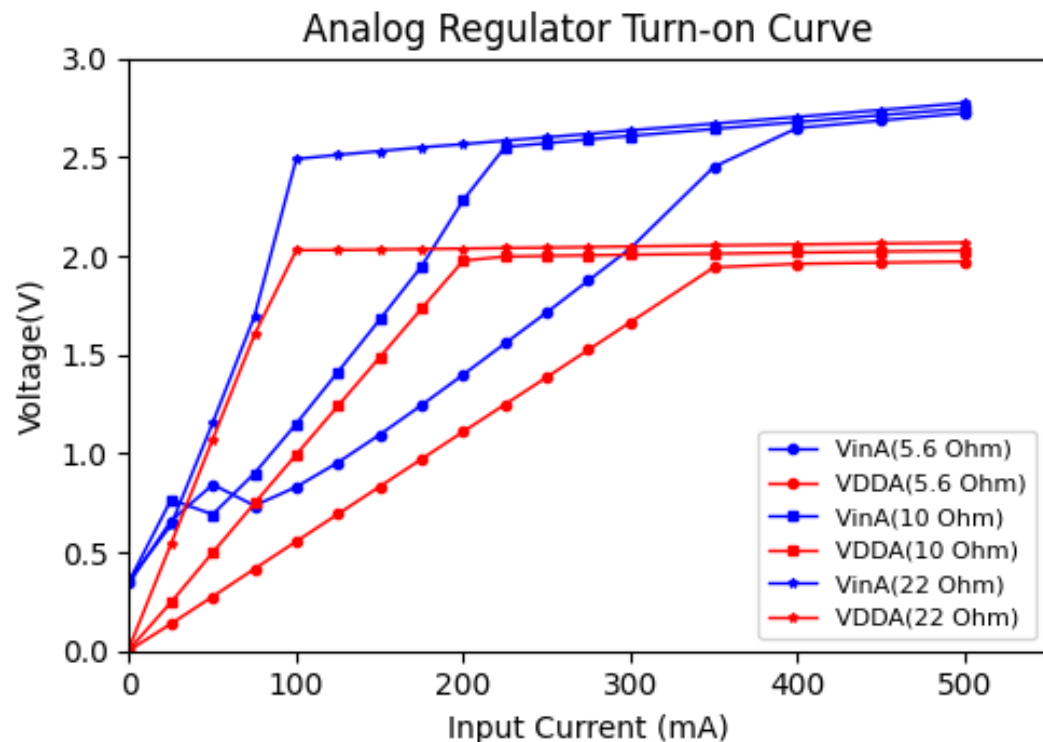
SLDO IV for both domains



- **After external 50Ω load**, the output of the SLDO regulator.
- The external load was used to mimic the chip load. (not exactly the same)
- The load currents are **~50mA and ~180 mA for analog and digital domains**, respectively.
- The output of regulators is **~2V** as expected.

SCC External Load SLDO IV

ATLASPix3.1 Chip W5-14 External Load DAC Regulator Turn-on Curves



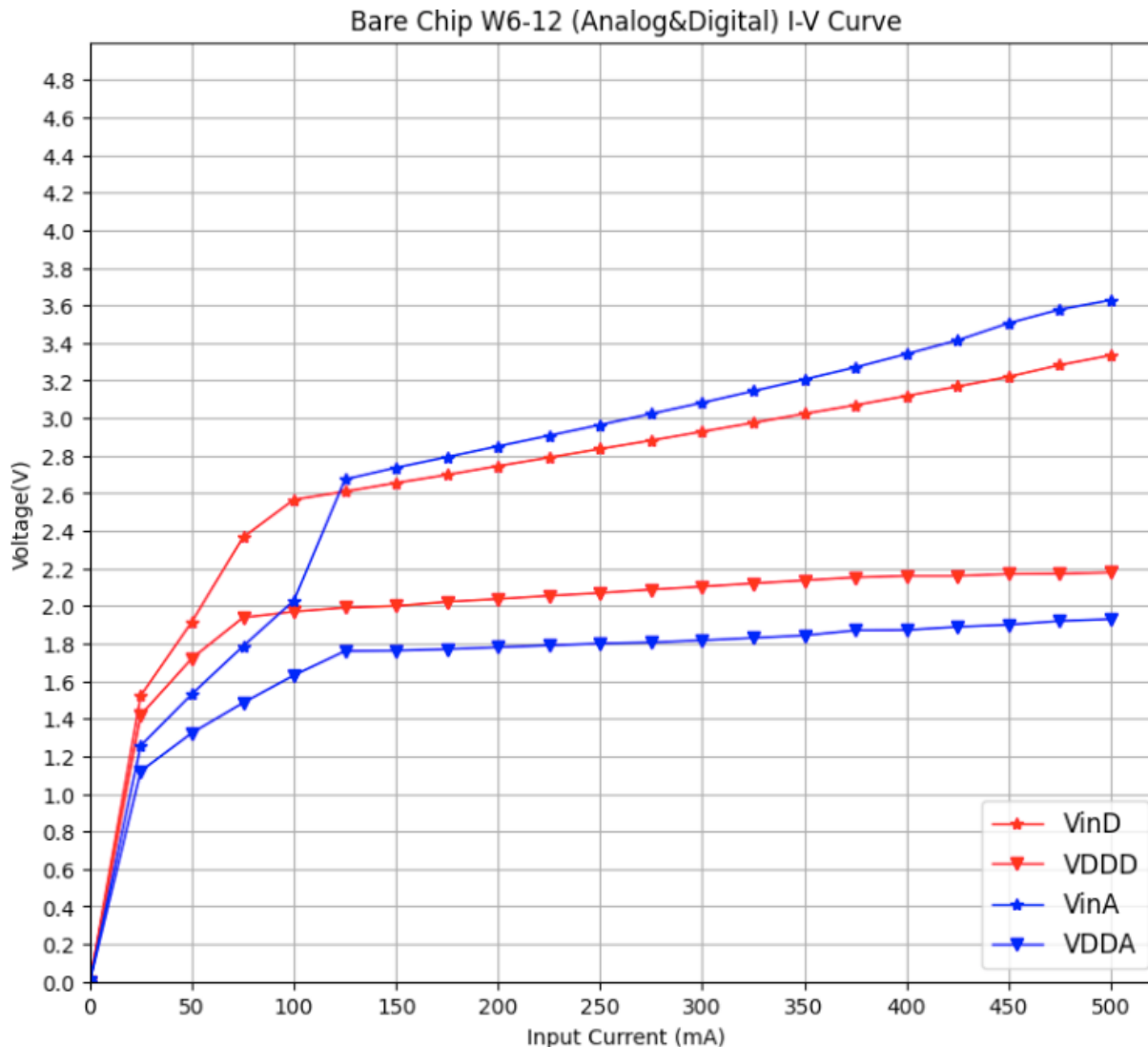
- The measurements with **SCC level**.
- For normal operation, the chip itself acts as the primary load for the SLDO.
- **External load was connected to SLDO.**
- SLDO response under increased load conditions.

Summary

- A probe setup for **50 μ m ATLASPix3.1 SLDO** testing was established at Edinburgh.
- Probe limitations required a **50 Ω external load**.
- No-load conditions caused immediate, **non-ideal regulation**.
- The external load enabled expected **\sim 2 V SLDO** operation.
- **Analog and digital domains showed functional regulation**.
- The setup provides a basis for future **SLDO measurements**.

Backup

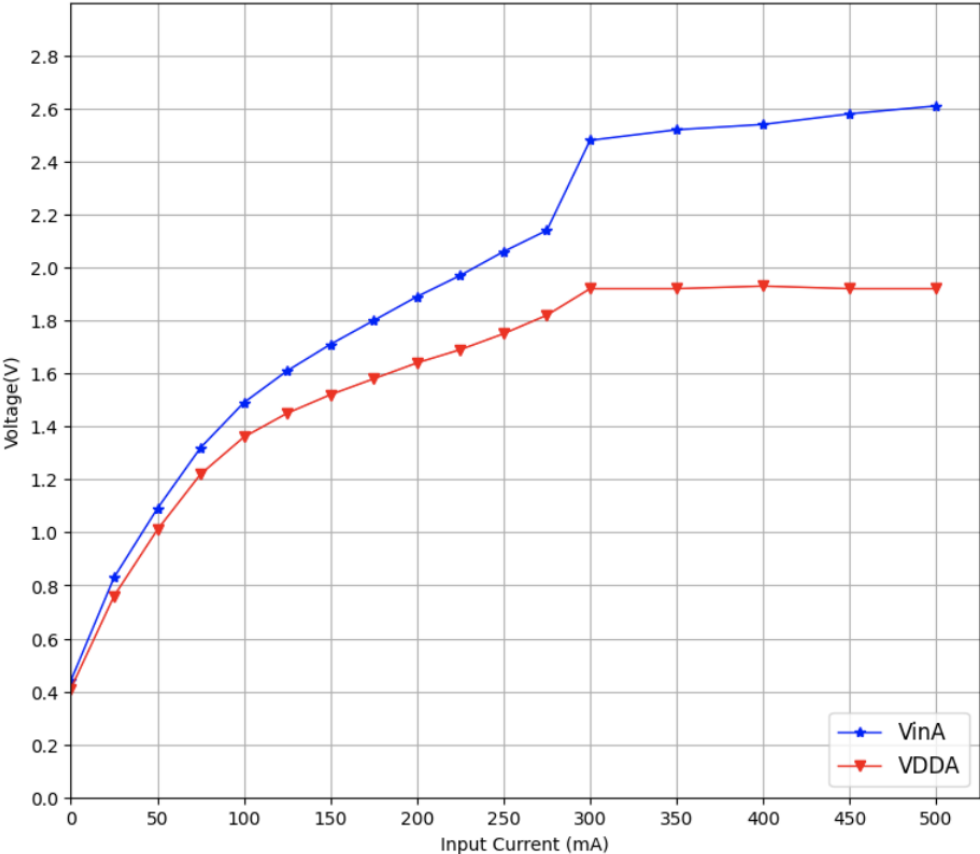
Bare Chip SLDO IV for both domains (at Milano)



- Previous measurement by using the probe setup at Milano.
- It shows both domains.
- Each domain was tested separately.

SCC SLDO IV

ATLASPix3.1 W5-14 Shunt-LDO (Analog) I-V Curve



ATLASPix3.1 W5-14 Shunt-LDO (Digital) I-V Curve

