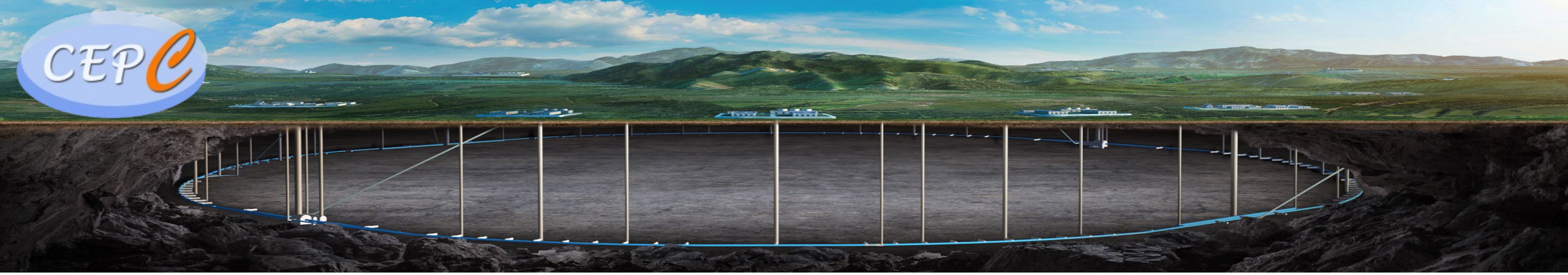


R&D Plan for CEPC OTK

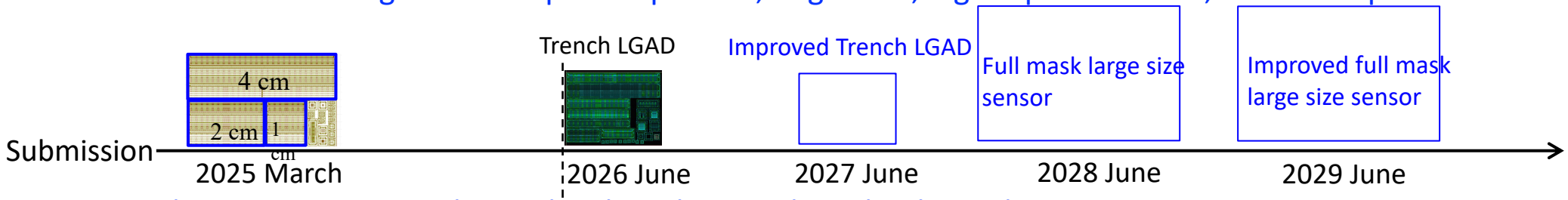
Qi Yan

On behalf of the CEPC Silicon Tracker Group

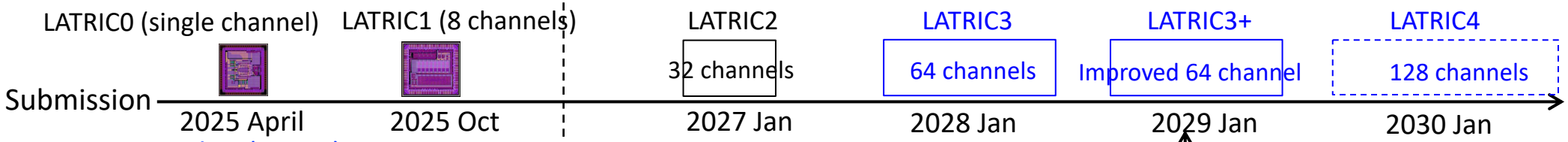
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Latest Outer Silicon Tracker R&D Plan

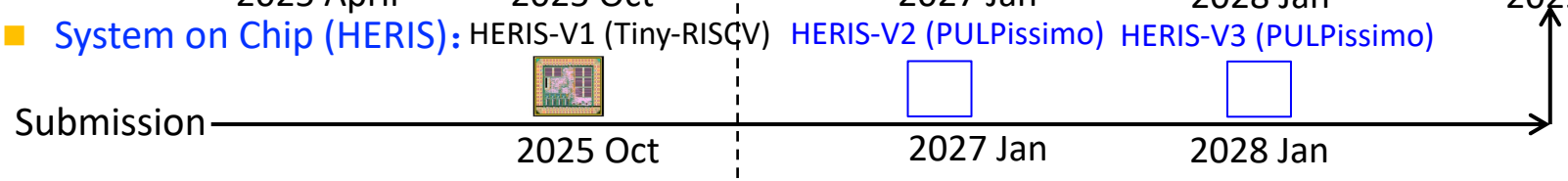
- LGAD sensors are evolving toward improved process, larger size, higher performance, and lower power consumption:



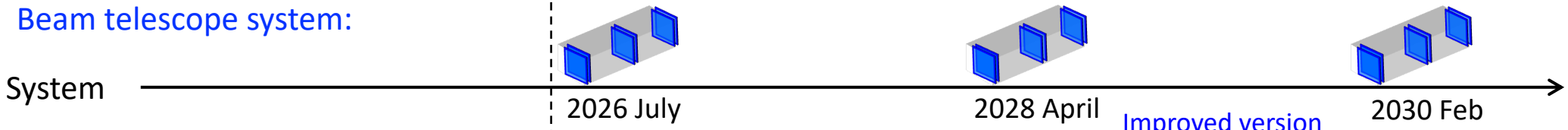
- LGAD readout ASIC, LATRIC, is being developed towards multi-channels:



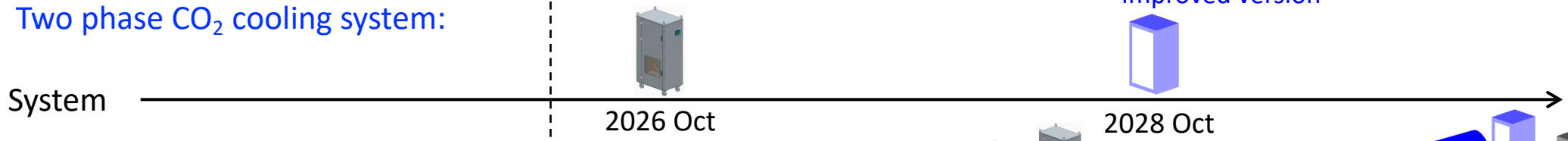
- System on Chip (HERIS):



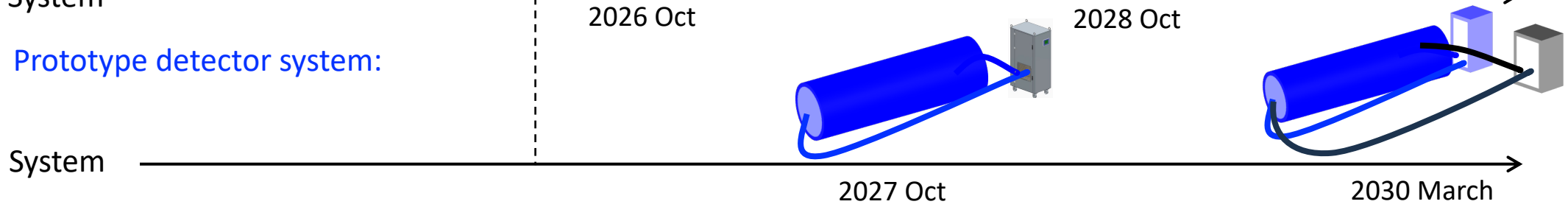
- Beam telescope system:



- Two phase CO_2 cooling system:

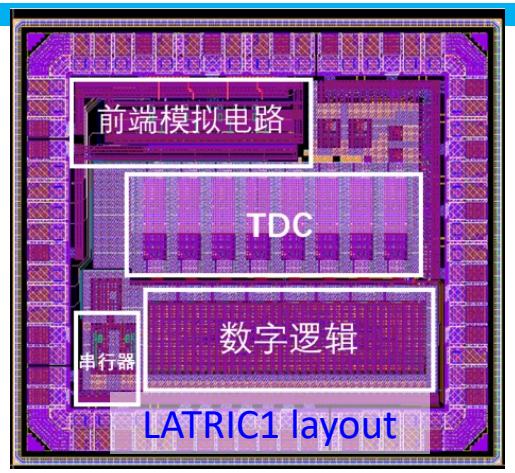


- Prototype detector system:

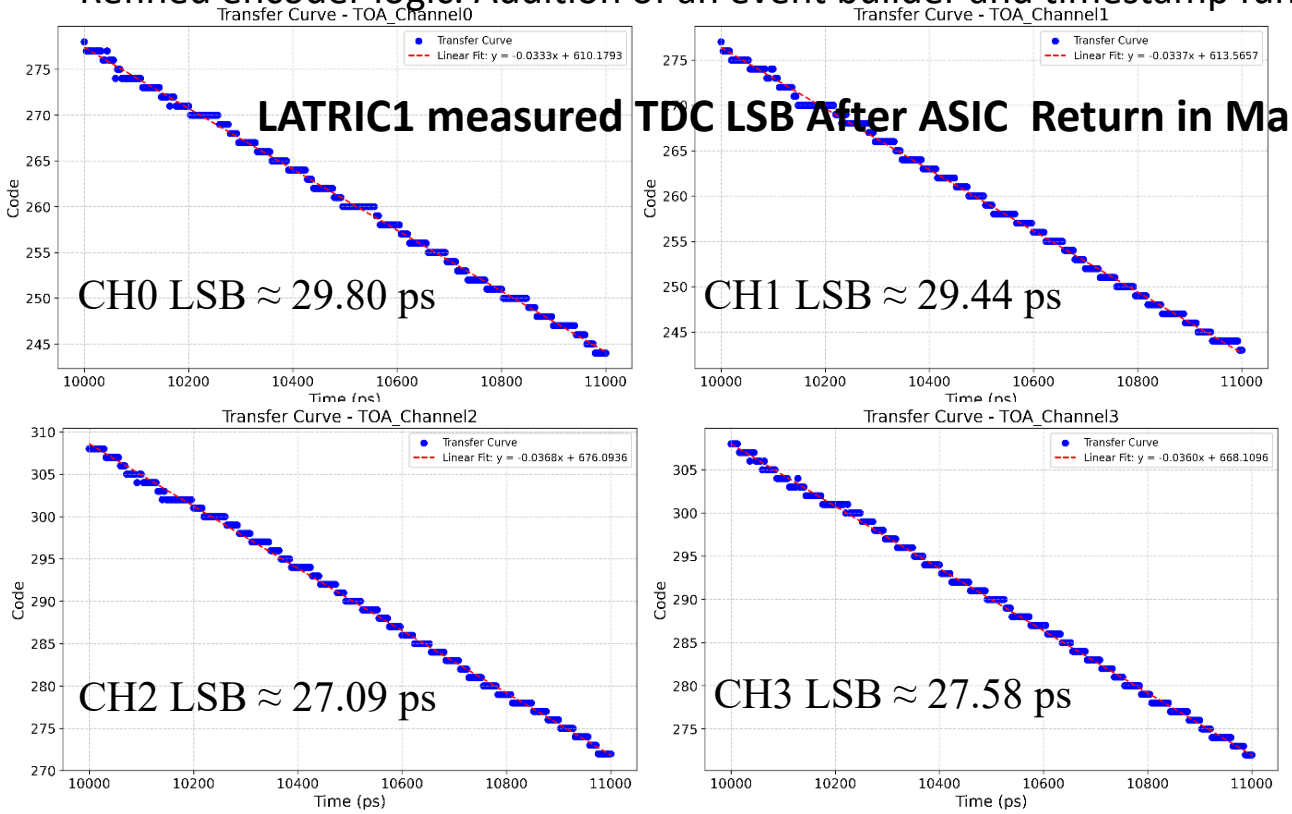


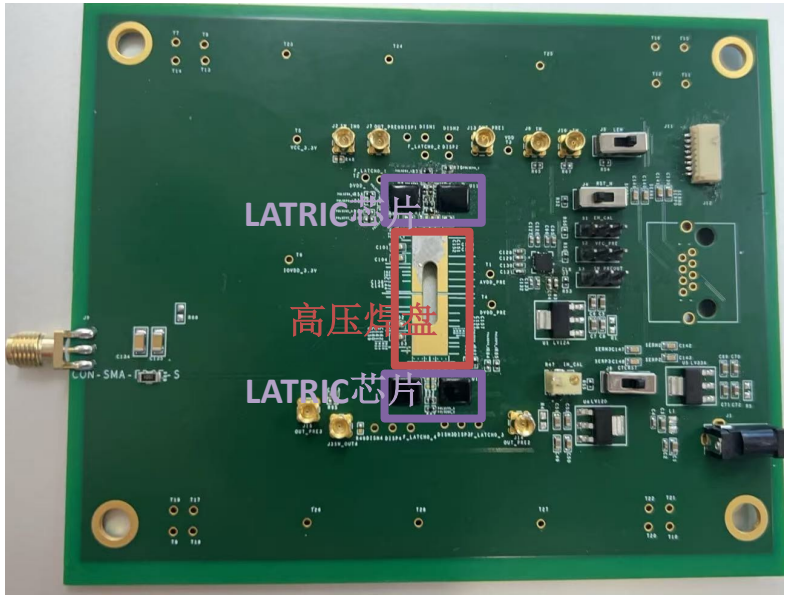
Latest Progress of the LATRIC Readout ASIC

- The second version readout ASIC, LATRIC1, adopts an 8-channel was designed and submitted for tape-out in October 2025.
  - The channel pitch is **100 µm.** Four channels integrate the analog front-end and TDC. The other four channels consist of TDCs connected to differential pulse receivers.
- Performance optimizations include:
  - An enhanced analog front-end with increased preamplifier gain to improve the signal-to-noise ratio.
  - Refined encoder logic. Addition of an event builder and timestamp functionality, etc.



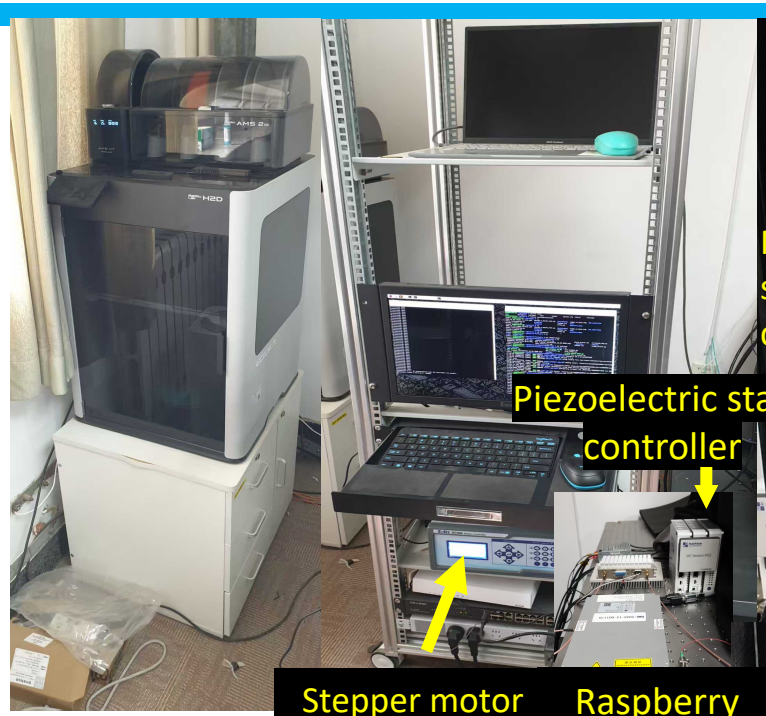
LATRIC1 measured TDC LSB After ASIC Return in March 2026

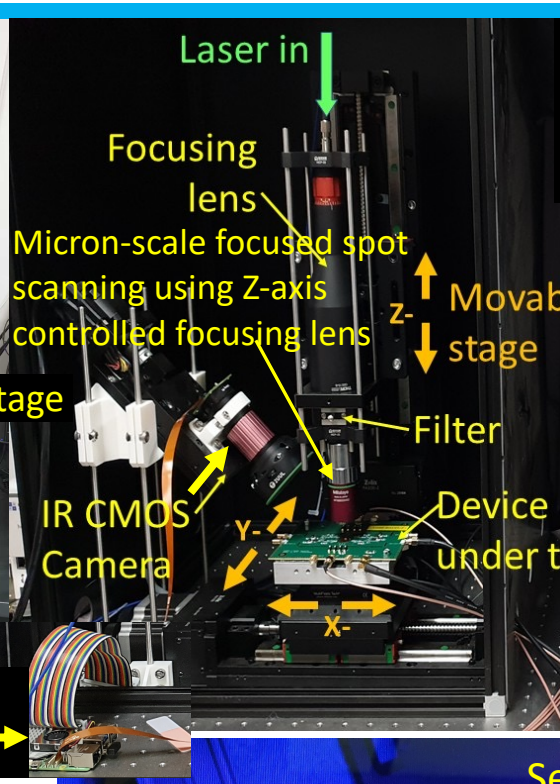




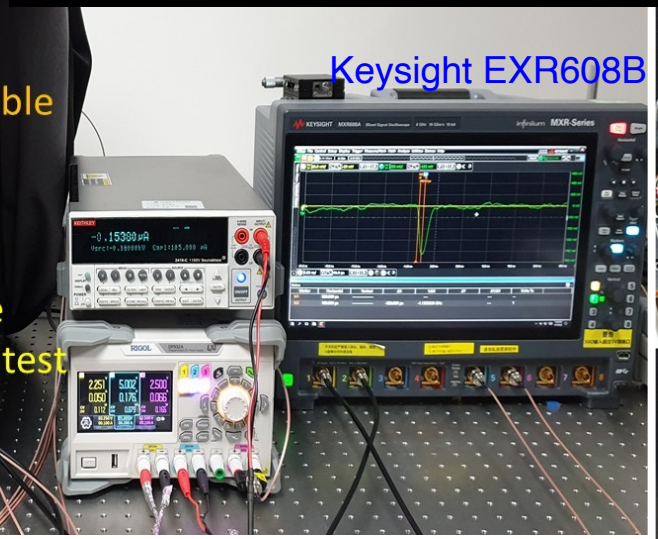
The latest designed LATRIC1-Sensor Integration Test Board

Sensor and LATRIC Combined Test Setup

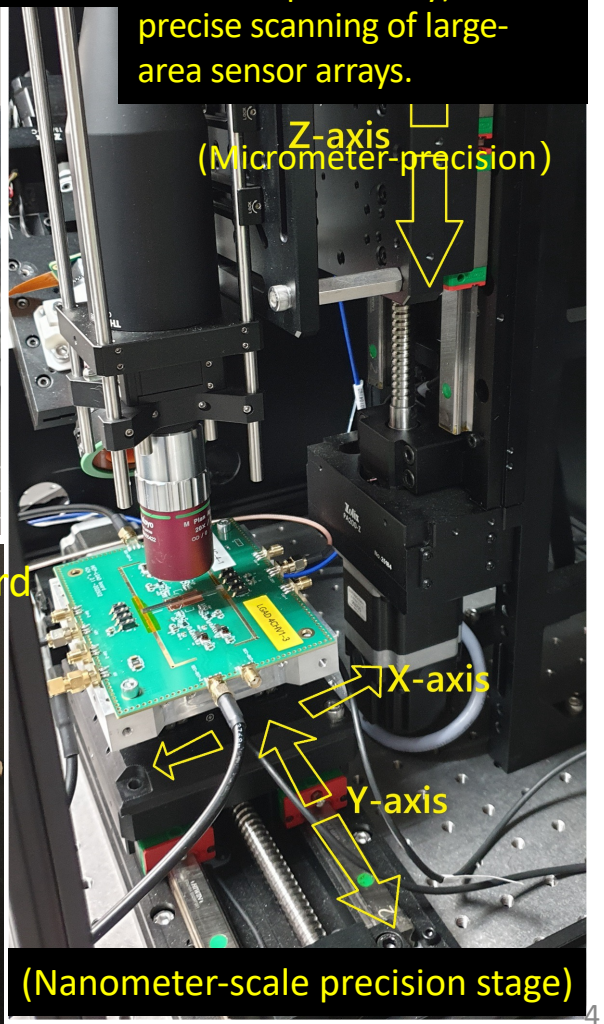


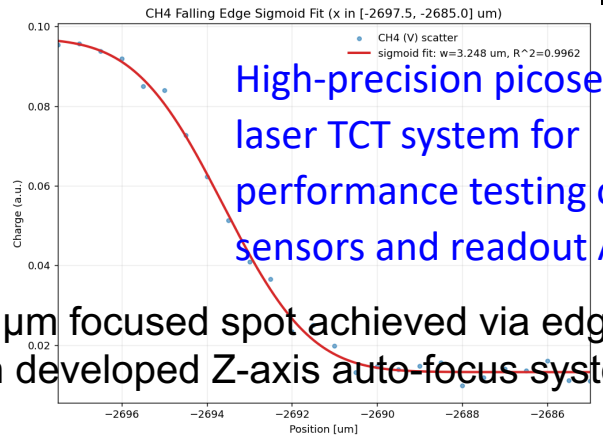


A 1064 nm infrared laser. The pulse width is about 8 ps, with a tunable laser rate ranging from 24 kHz to 24 MHz.



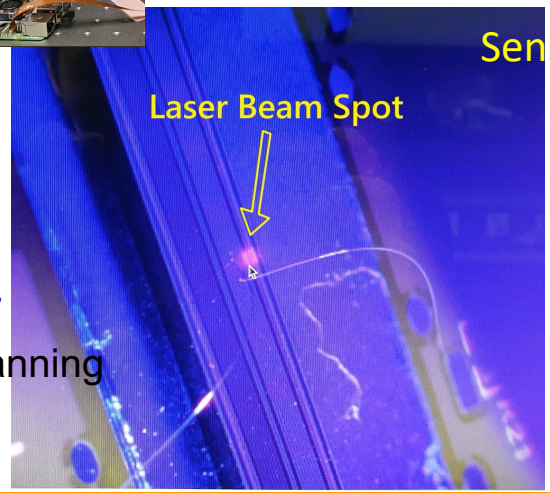
High-precision 3D stage with programmable 3-axis motors and piezo stage (10 nm step, 100 nm repeatability) for precise scanning of large-area sensor arrays.



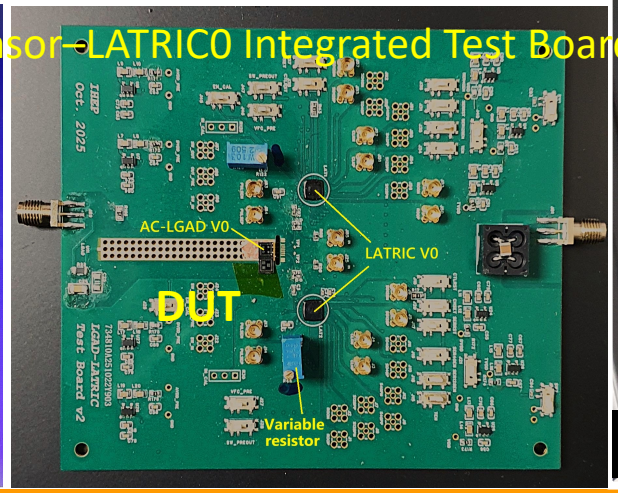


High-precision picosecond laser TCT system for performance testing of sensors and readout ASICs.

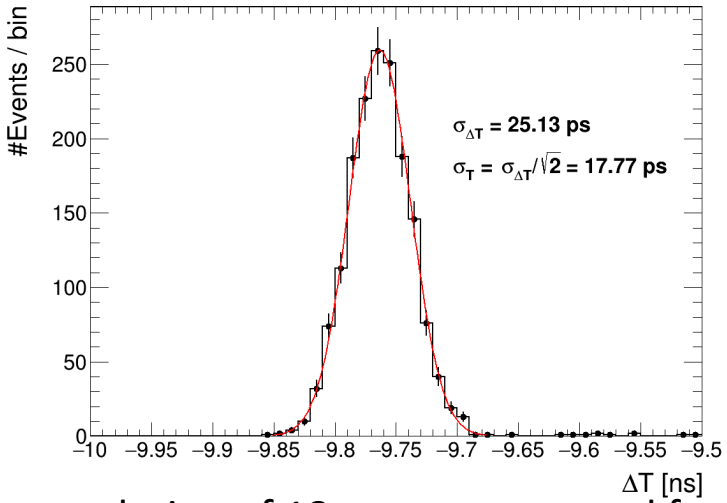
2-3 μm focused spot achieved via edge scanning with developed Z-axis auto-focus system



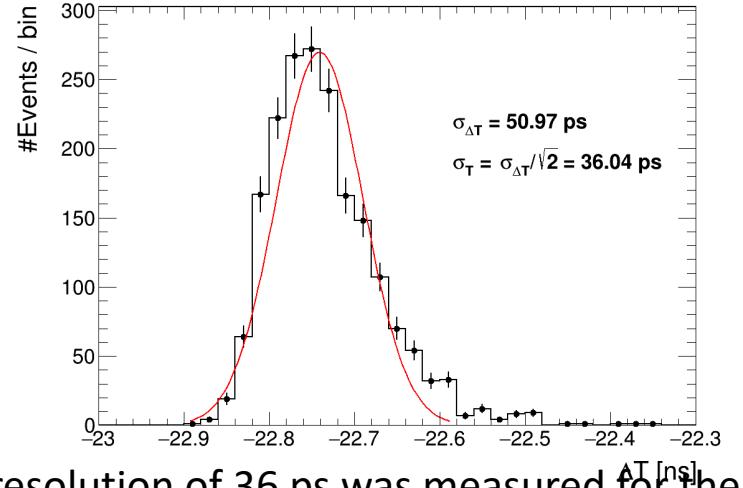
Sensor–LATRIC0 Integrated Test Board



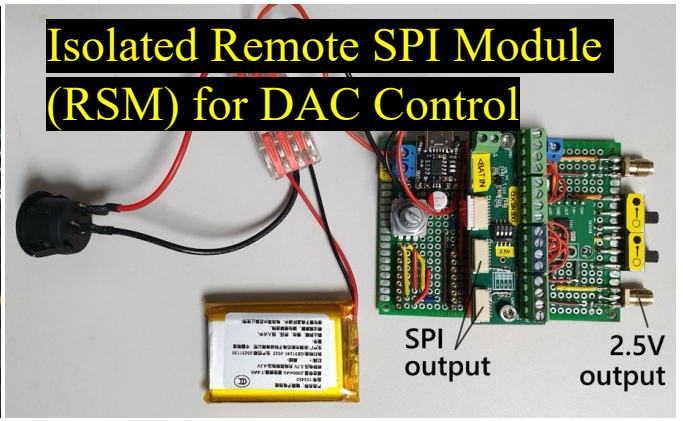
LATRIC0 (Single Channel) and Sensor Combined Test



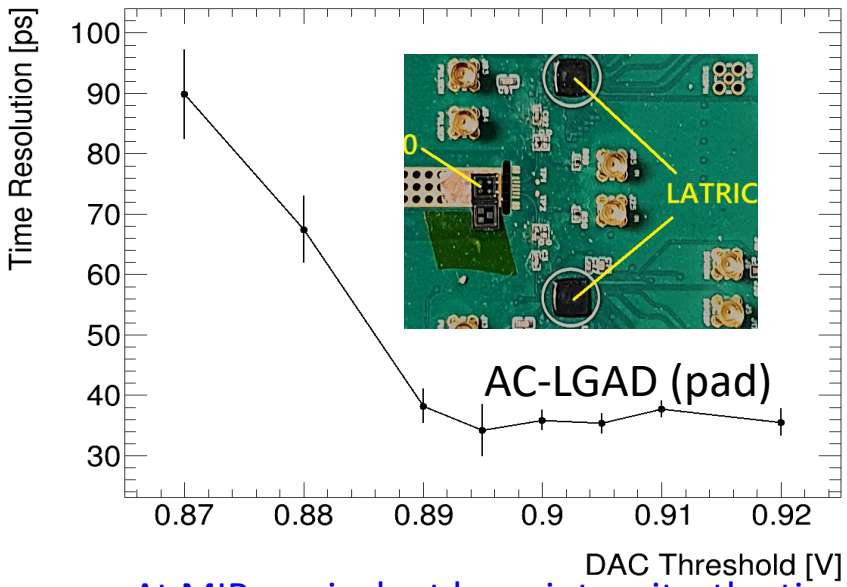
A time resolution of 18 ps was measured for the combined LGAD+LATRIC at 100% laser intensity.

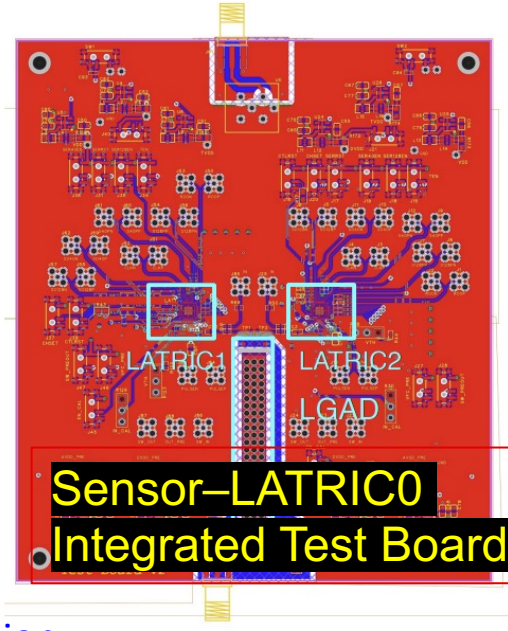


A time resolution of 36 ps was measured for the combined LGAD+LATRIC at a MIP-equivalent laser intensity (0.5%).



Time difference measured with two LATRIC0 chips





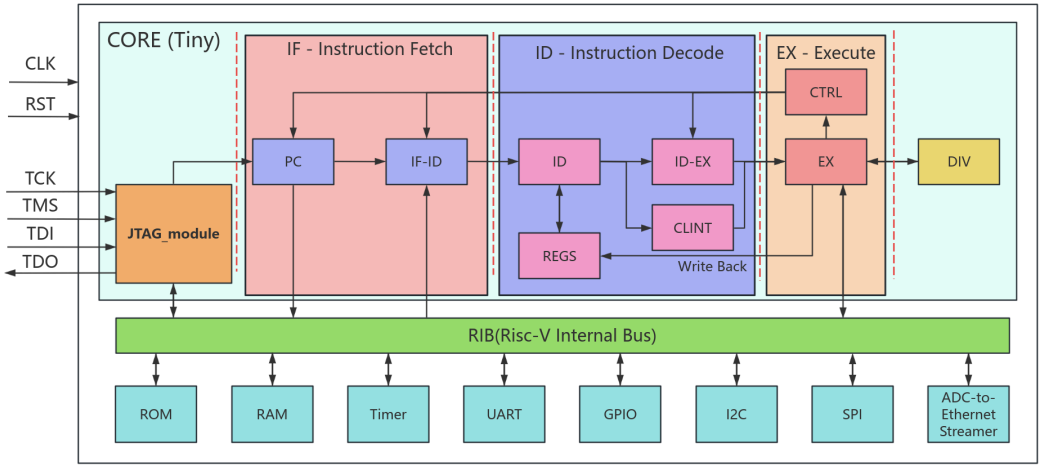
At MIP-equivalent laser intensity, the time resolution improves with increasing threshold and stabilizes at about 36 ps in the 0.89–0.92 V range.

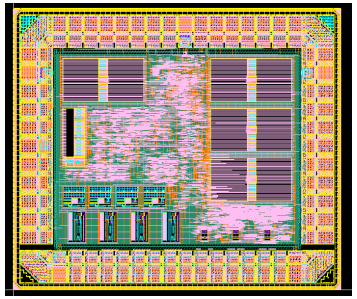
Development of the First System-on-Chip (SoC)

- HERIS: Radiation-Hard RISC-V SoC for High Energy Physics

  Traditional ASICs are based on fixed hardware logic and lack flexibility for next-generation detectors. HERIS introduces a programmable SoC architecture (CPU, memory, bus, and peripherals), enabling a transition from passive readout to intelligent, adaptive front-end systems. HERIS-V1 (based on TinyRISC-V) was initiated in early 2025. The full design flow—including RTL development, FPGA validation, and digital backend integration—was completed, and the chip was taped out in October 2025 using a 55 nm CMOS process. In the future, HERIS will be integrated with the LATRIC readout ASIC to realize a “high-precision measurement + on-chip intelligence” architecture.

  - Core (Tiny RiscV)
    - RV32IM指令集
    - 三级流水线
    - CoreMark/MHz = 2.4
  - JTAG接口
    - 支持OpenOCD
    - 支持GDB调试启动
  - 外设
    - 4 KB ROM, 32 KB RAM
    - 支持I2C, UART, and SPI
    - 集成ADC数据收集模块并通过UDP协议传输





- 55 nm 工艺制程
- 工作频率 50 MHz
- 芯片面积 1.020 x 1.196 mm
- 工作电压 1.2 V

Test of HERIS-V1 SoC Chip

```
PS E:\fpga\Tools\xpack-openocd-0.12.0-6\bin> .\openocd.exe -f .\tinyriscv_JTAG_HS2.cfg
xPack Open On-Chip Debugger 0.12.0+dev-01850-geb6f2745b-dirty (2025-02-07-10:08)
Licensed under GNU GPL v2
For bug reports, read
        http://openocd.org/doc/doxygen/bugs.html
Info : clock speed 1000 kHz
Info : JTAG tap: riscv.cpu tap/device found: 0x1e200a6f (mfg: 0x537 (Wuhan Xun Zhan Electronic Technology), part: 0xe200
, ver: 0x1)
Info : datacount=3 progbufsize=1
Info : Examined RISC-V core; found 2 harts
Info :  hart 0: XLEN=32, misa=0x0
Info : [riscv.cpu] Examination succeed
Info : [riscv.cpu] starting gdb server on 3333
Info : Listening on port 3333 for gdb connections
Info : Listening on port 6666 for tcl connections
Info : Listening on port 4444 for telnet connections
```

- The on-board EEPROM has been successfully verified to operate via the I2C protocol

```
int main() {
    uart_init();
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);

    uint16_t test_addr  = 0x1234;
    uint8_t test_data  = 0xAC;

    eeprom_write_byte(test_addr, test_data);
    uint8_t read_back = eeprom_read_byte(test_addr);
```

UART输出

```
== I2C Master Final Test Program ===
[I2C] Write: Addr=0x1234 Data=0xAC
  > Config Check: Slave=0x53, Addr=0x1234, Data=0xAC
[I2C] Read: Addr=0x1234
```

断电后再次运行

串口调试助手 + TCP/UDP

端口名：COM5
波特率：115200
数据位：8
校验位：None
停止位：1
RI DSR CTS DTR RTS

- First power-on: OpenOCD works normally, ROM code runs successfully.

```
--- RISC-V Bootloader Started ---
Initializing SD card on SPI channel 1...
SD_INIT: Failed on CMD0
!!! FATAL: SD Card initialization failed. Halting. !!!
Target RAM size: 14336 bytes. Need to read 28 blocks from SD card.
Starting to copy data from SD:@0x0 to RAM:@0x10000000...
```

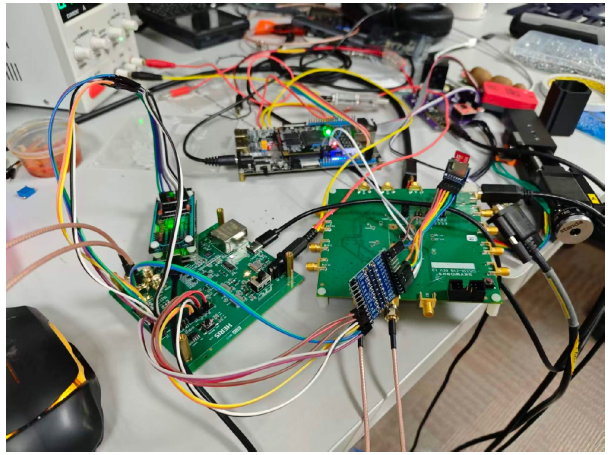
UART输出

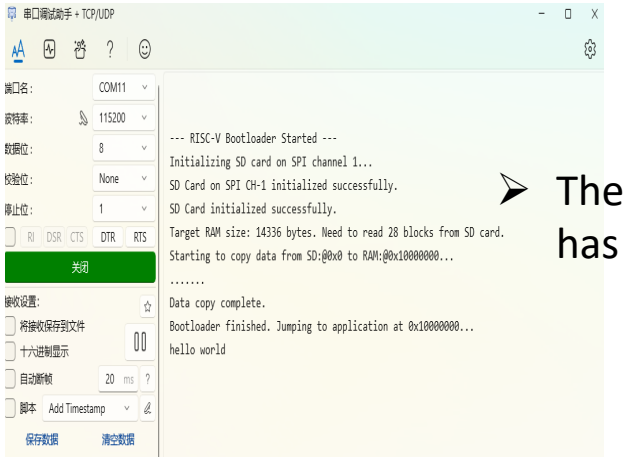
```
int main() {
    uart_init();
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);

    uint16_t test_addr3 = 0x0123;
    uint8_t read_back3 = eeprom_read_byte(test_addr3);
    uint16_t test_addr2 = 0x1234;
    uint8_t read_back2 = eeprom_read_byte(test_addr2);

    xprintf("[I2C] Verification: Read1 0x%02X, Read2 0x%02X\n", read_back3, read_back2);
```

```
=== I2C Mater Final Test Program ===
[I2C] Read: Addr=0x0123
[I2C] Read: Addr=0x1234
[I2C] Verification: Read1 0xFF, Read2 0xAC
```

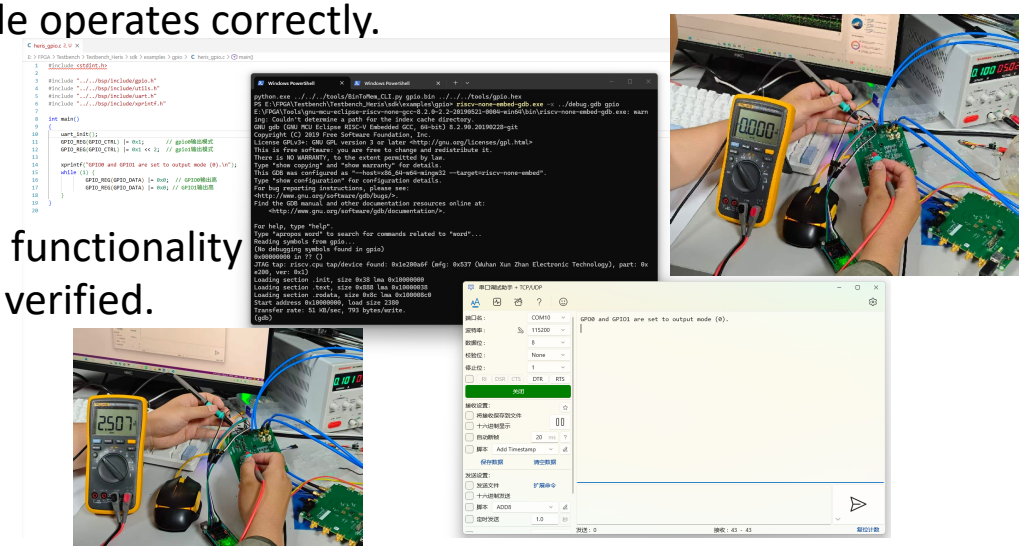
The first RISC-V Soc chip, HERIS-V1, has been successfully validated.

- The ROM and SD card boot functions work properly, and the SPI module operates correctly.





- The GPIO functionality has been verified.



HERIS-V1 Performance Test

CoreMark Benchmark Statistics

Test Configuration

Item	Value
CPU Architecture	RV32IM Softcore
Benchmark	CoreMark
Iterations	100
Compiler	GCC 8.2.0
Optimization	`-O2 -funroll-loops -finline-functions`
Memory Mode	STATIC
Assumed Timer Clock	50 MHz

HERIS-V1 benchmark score

CoreMark Results Summary

Run	Total Ticks	Time (s)	CoreMark	CoreMark/MHz
1	47,140,681	0.943	106.07	2.121
2	57,254,527	1.145	87.33	1.747
3	57,254,216	1.145	87.33	1.747
4	57,254,809	1.145	87.32	1.746
5	57,254,522	1.145	87.33	1.747
6	57,254,148	1.145	87.33	1.747
7	57,255,302	1.145	87.31	1.746
8	57,256,313	1.145	87.30	1.746
9	57,253,503	1.145	87.33	1.747
10	36,131,525	0.723	138.38	2.768
11	57,254,188	1.145	87.33	1.747
12	57,254,522	1.145	87.33	1.747
13	57,254,203	1.145	87.33	1.747

#	Total Ticks	CoreMark	CoreMark/MHz
1	264,551,913	18.90	0.378
2	25,685,150	194.66	3.893
3	55,131,135	90.69	1.814
4	29,876,551	167.35	3.347
5	57,253,579	87.33	1.747
6	57,243,713	87.35	1.747
7	29,906,285	167.19	3.344
8	57,254,426	87.33	1.747
9	41,493,461	120.50	2.410
10	46,612,237	107.27	2.145
11	54,497,797	91.75	1.835
12	48,237,510	103.65	2.073
13	28,275,053	176.83	3.537
14	57,253,726	87.35	1.747
15	13,635,777	366.68	7.334
16	25,475,668	196.27	3.925
17	57,253,893	87.35	1.747
18	57,253,672	87.36	1.747
19	57,253,673	87.36	1.747
20	26,854,754	186.19	3.724
21	57,250,967	87.40	1.748
22	58,844,737	84.97	1.699
23	57,253,266	87.36	1.747
24	55,910,085	89.43	1.789
25	6,725,030	743.49	14.870
26	57,254,283	87.33	1.747
27	57,253,680	87.36	1.747
28	57,255,110	87.32	1.746
29	57,255,184	87.33	1.747
30	57,254,539	87.33	1.747
31	56,236,672	88.91	1.778
32	57,253,678	87.36	1.747
33	49,780,037	100.44	2.009
34	57,253,673	87.36	1.747
35	310,466,500	16.11	0.322
36	57,253,210	87.36	1.747

Frequency: 50 MHz; maximum operating frequency: 150 MHz.

Performance benchmark：

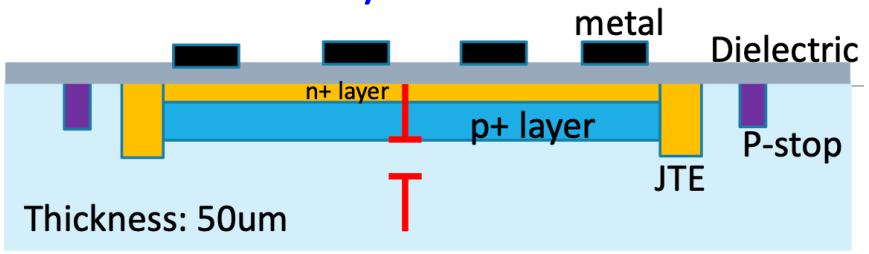
- **ARM Cortex-M0/M0+：** 0.9 ~ 1.0
- **PicoRV32 (RISC-V)：** 0.5 ~ 0.8
- **HERIS-V1：** achieves a score of 1.75, consistent with FPGA results.
- **VexRiscv / 蜂鸟 E203：** 1.5 ~ 2.2
- **ARM Cortex-M3 / M4：** 3.3 ~ 3.4

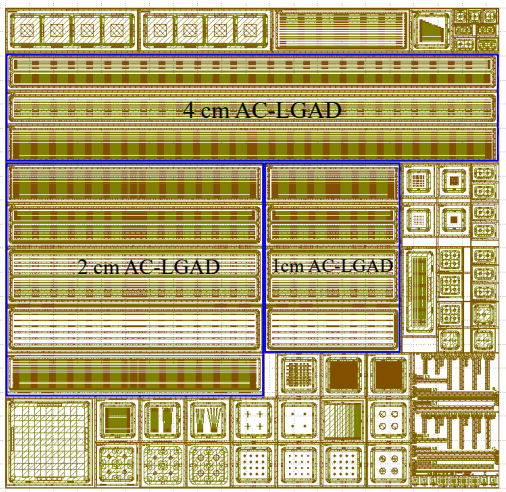
Latest Status of LGAD Sensor

AC-LGAD microstrip sensors (≥2 cm × 2 cm), aiming at optimal position resolution, timing resolution, and lower power consumption. The latest tape-out was submitted in 2025. To date, 7 out of 18 wafers have been fabricated, and process optimization are ongoing. 2 wafers with lower n+ dose been delivered in May 2026.

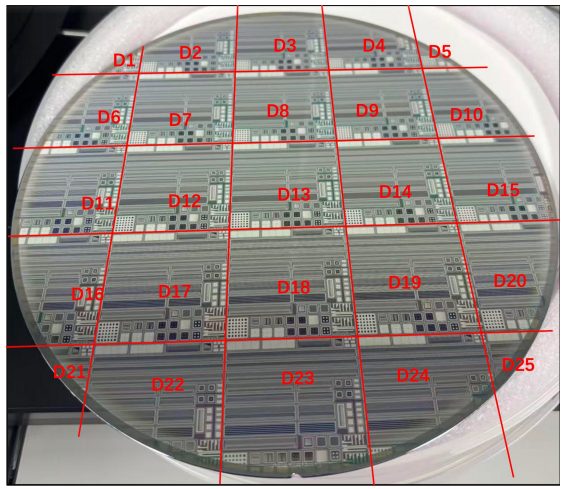
The design explores different microstrip geometries, including:

- strip length: 1 cm, 2 cm, and 4 cm
- strip pitch: 100 µm, 200 µm, and 500 µm
- electrode width: 25 µm, 50 µm, and 100 µm
- The n^+ doping is tuned to optimize position resolution performance, and the EPI thickness is optimized to reduce capacitance and thus lower readout power consumption.

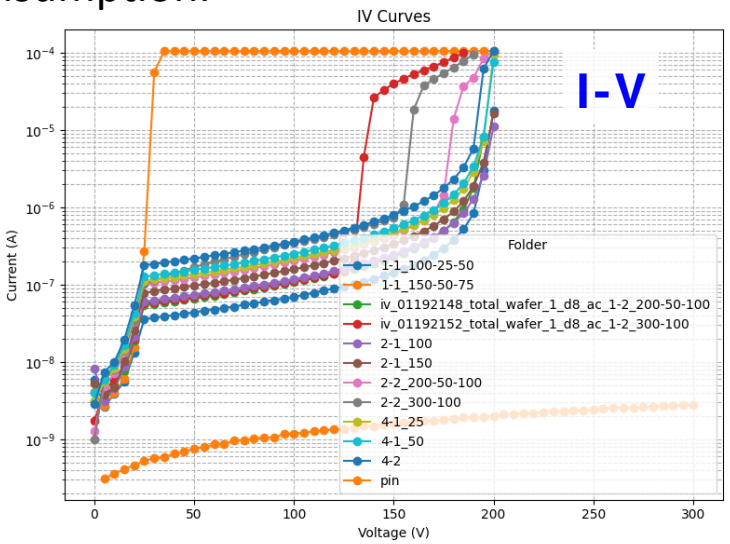


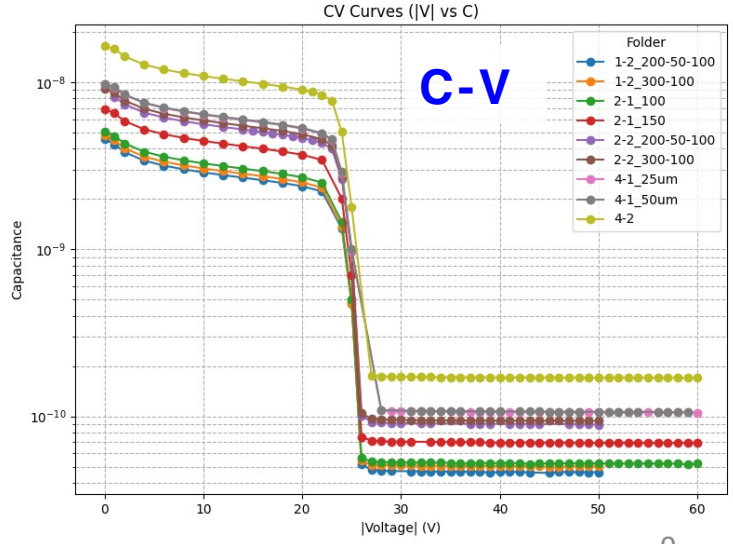


AC-LGAD LAYEROUT



AC-LGAD Wafer

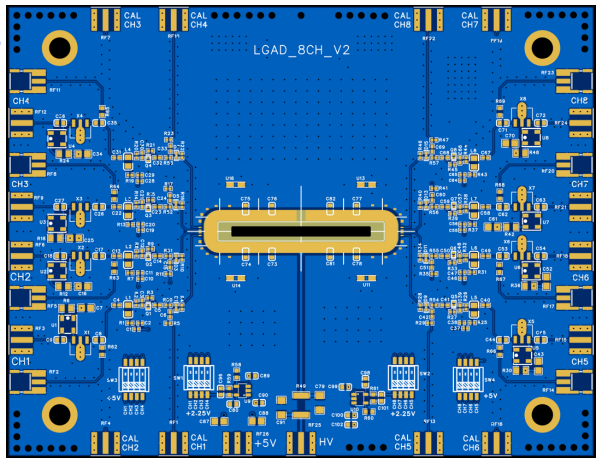


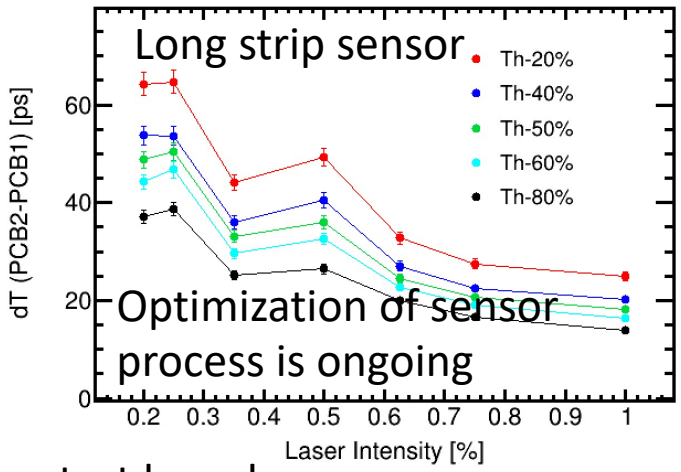


Next LGAD Sensor R&D Plan

Compared AC-LGAD with different process parameters

- Different n+ dose, different coupling capacitance, different pad-pitch size, different strip length



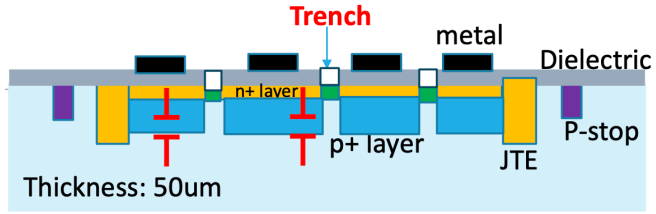


New designed 8 channel strip sensor test board

Tape out other wafers with different process parameters： 11 wafers in IME

New submission is planed in June, 2026

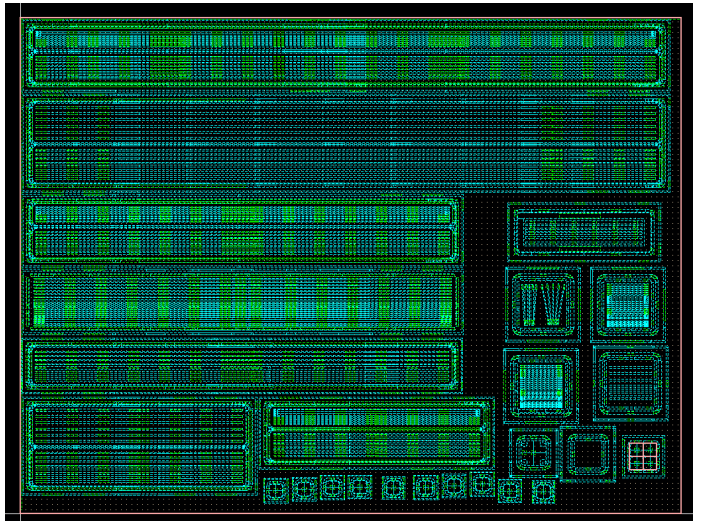
- isolated AC-LGAD, isolated DC-LGAD (DC-RSD)



Trenched LGAD

$C = \varepsilon_0 * \varepsilon_r * A \downarrow / d$

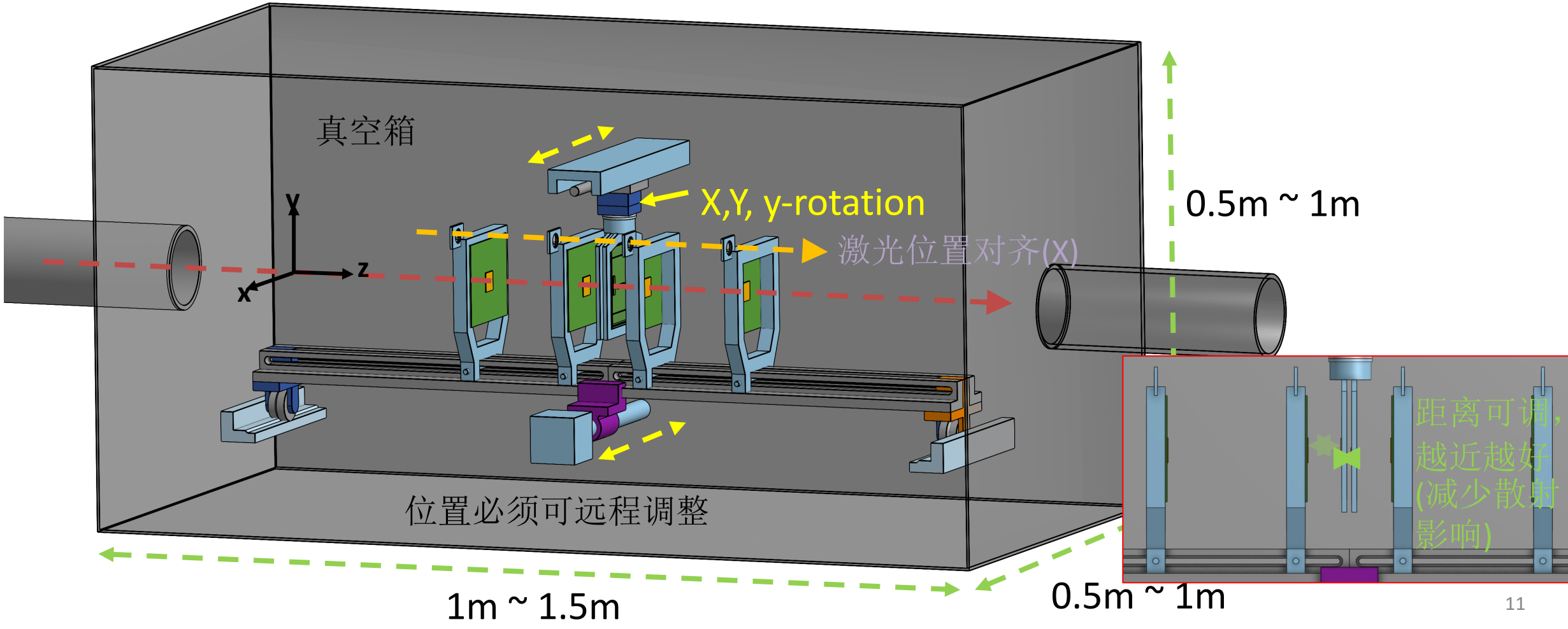
Trench-isolated LGAD: a key step toward final performance, reducing capacitance for large-area, high-precision, low-power operation.



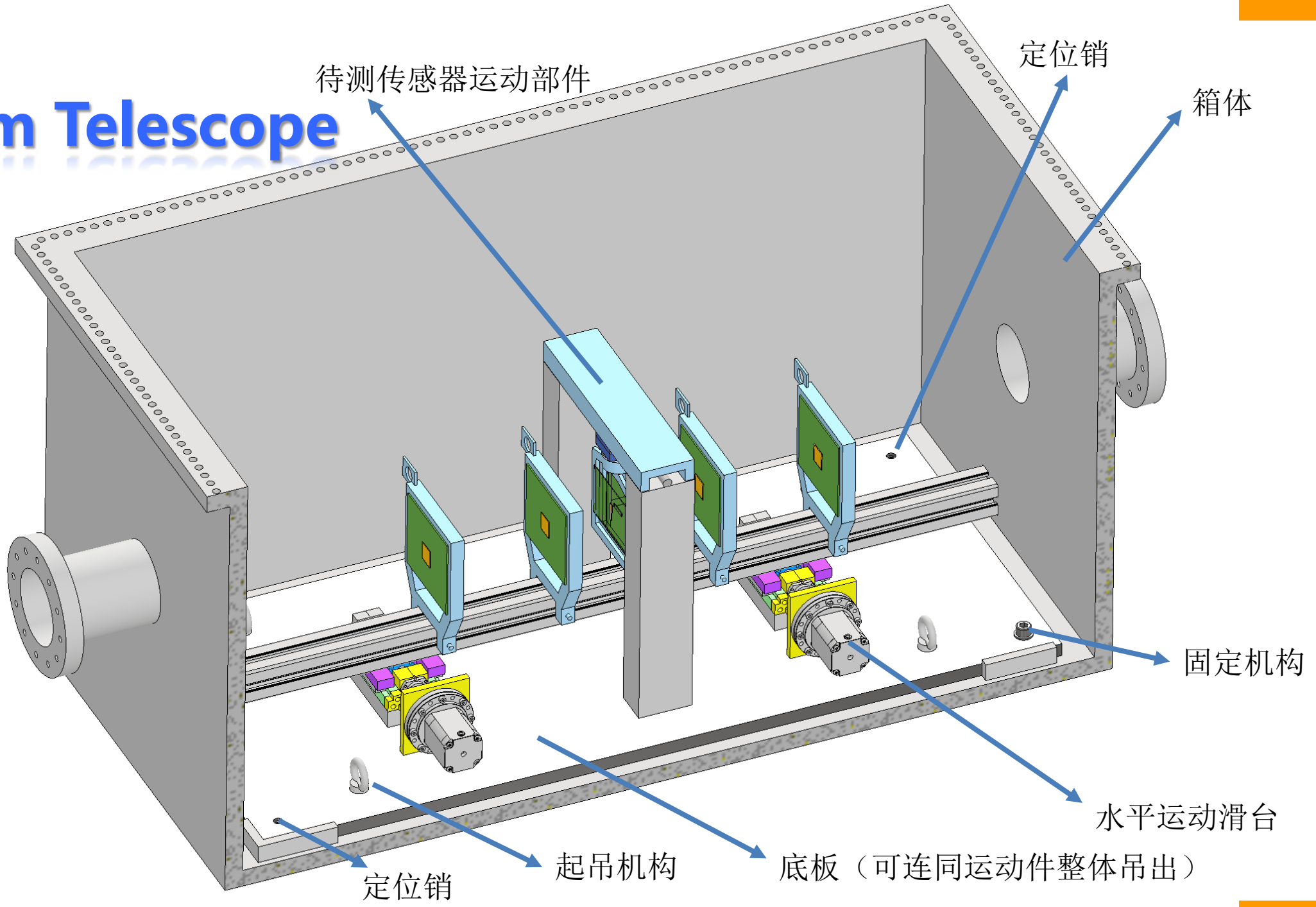
➢ The process and structure simulation, design of LGAD with isolation structure is ongoing

Development of the Beam Telescope for BT

A test beam campaign for the next sensor/ASIC validation is planned. The beam telescope design is currently ongoing, with completion planned within 1–2 months. The vacuum valve box is also also under design, and the beam tests are planned to be carried out in China (could be at the PWFA facility at IHEP).

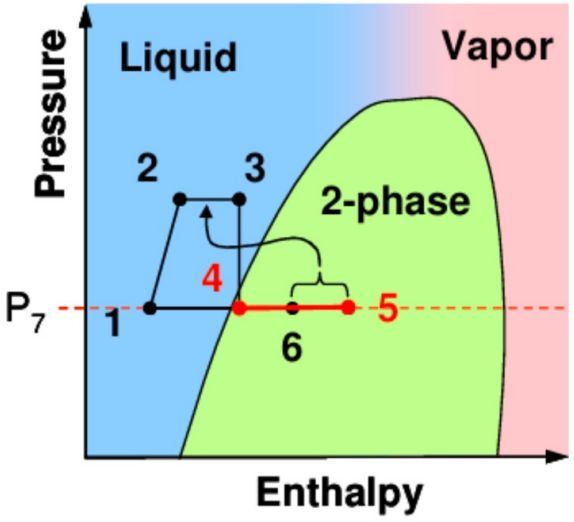


LGAD Beam Telescope

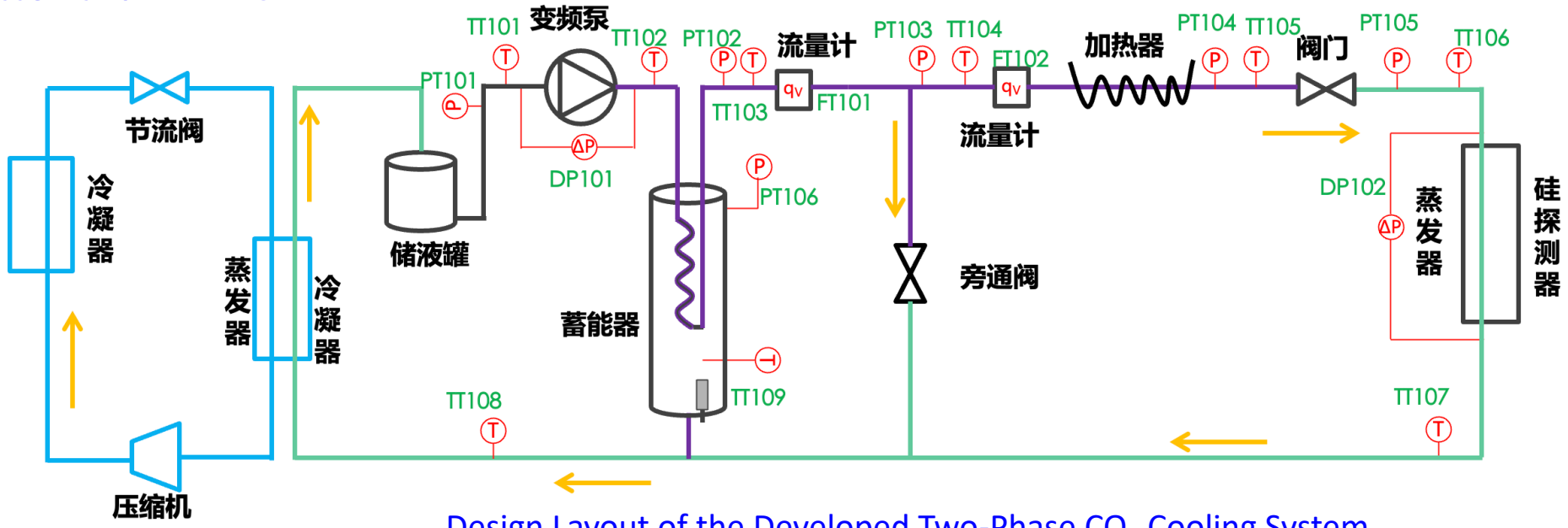


Development of Two-Phase CO_2 Cooling System

We are developing the first two-phase CO_2 cooling system together with TIPC. The integrated system is going be completed in October 2026. The system features a compact and portable design, with a nominal heat load capacity of ~1.2 kW (upgradeable to >2 kW), an operating temperature range from –40 °C to 20 °C, and a temperature stability better than ±1 °C.



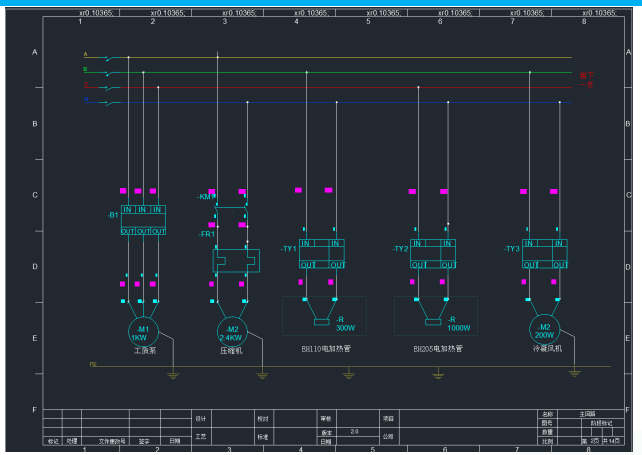
P–h Diagram of the Two-Phase CO_2 Cooling System

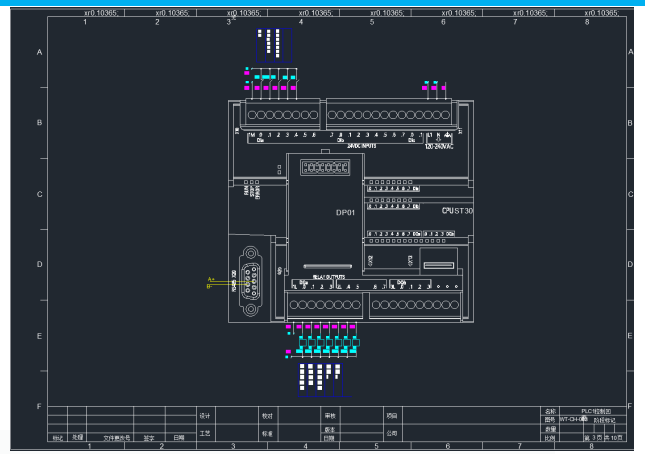


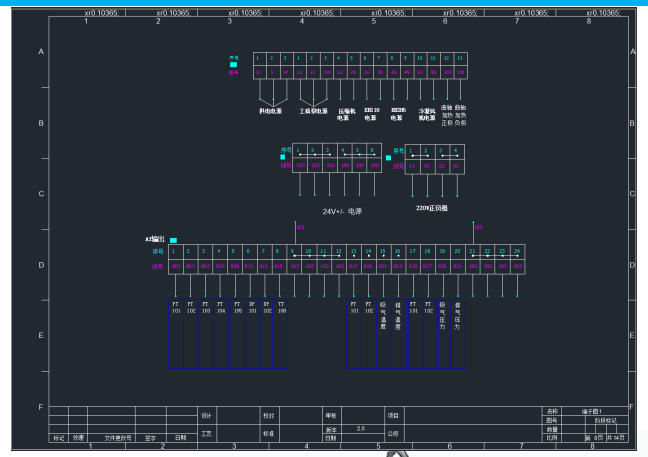
Design Layout of the Developed Two-Phase CO_2 Cooling System

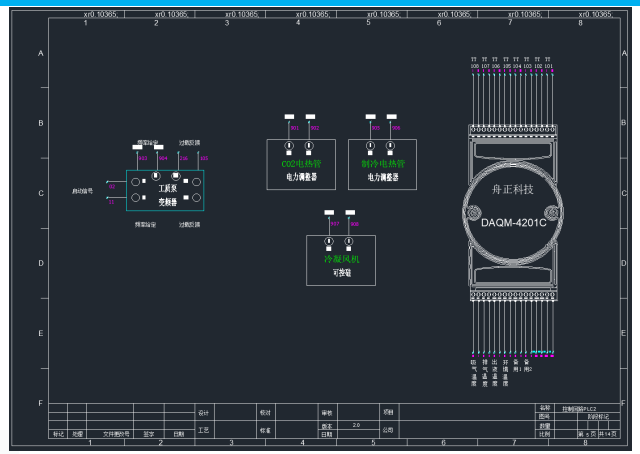
The system can be integrated with a variety of thermal load systems, making it suitable for different experimental setups and application requirements. The system features a compact layout with a total weight of approximately 100 kg. It also provides a scalable platform for the development of larger cooling systems.

Design of the CO_2 Cooling System



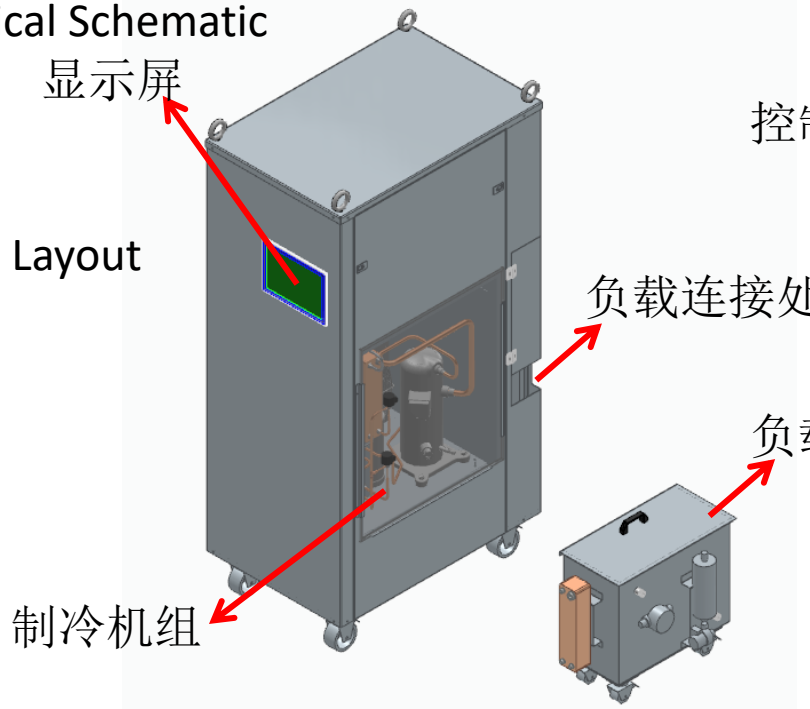


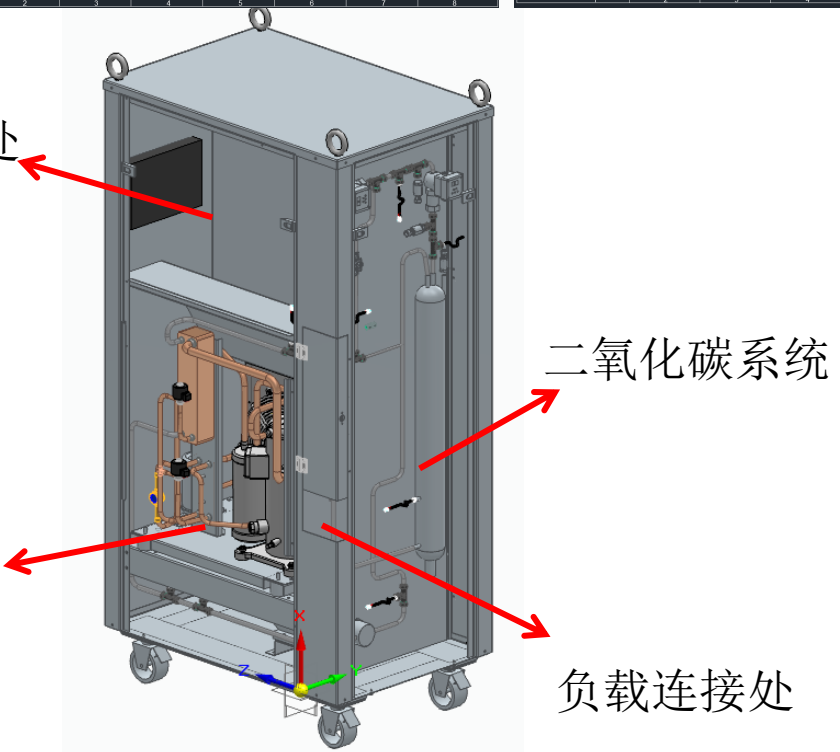




- System Electrical Schematic

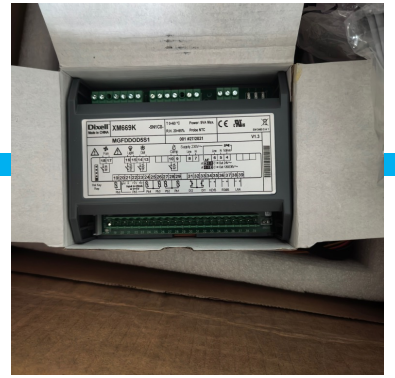
- System Design Layout





压缩机

板式换热器



膨胀阀驱动

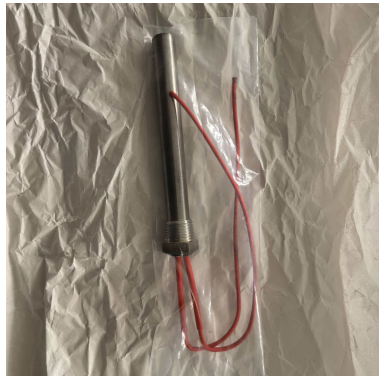
过滤器-R404A

视液镜-R404A

油分离器

增焓阀驱动

温度传感器



加热棒

压力传感器

过滤器-CO2

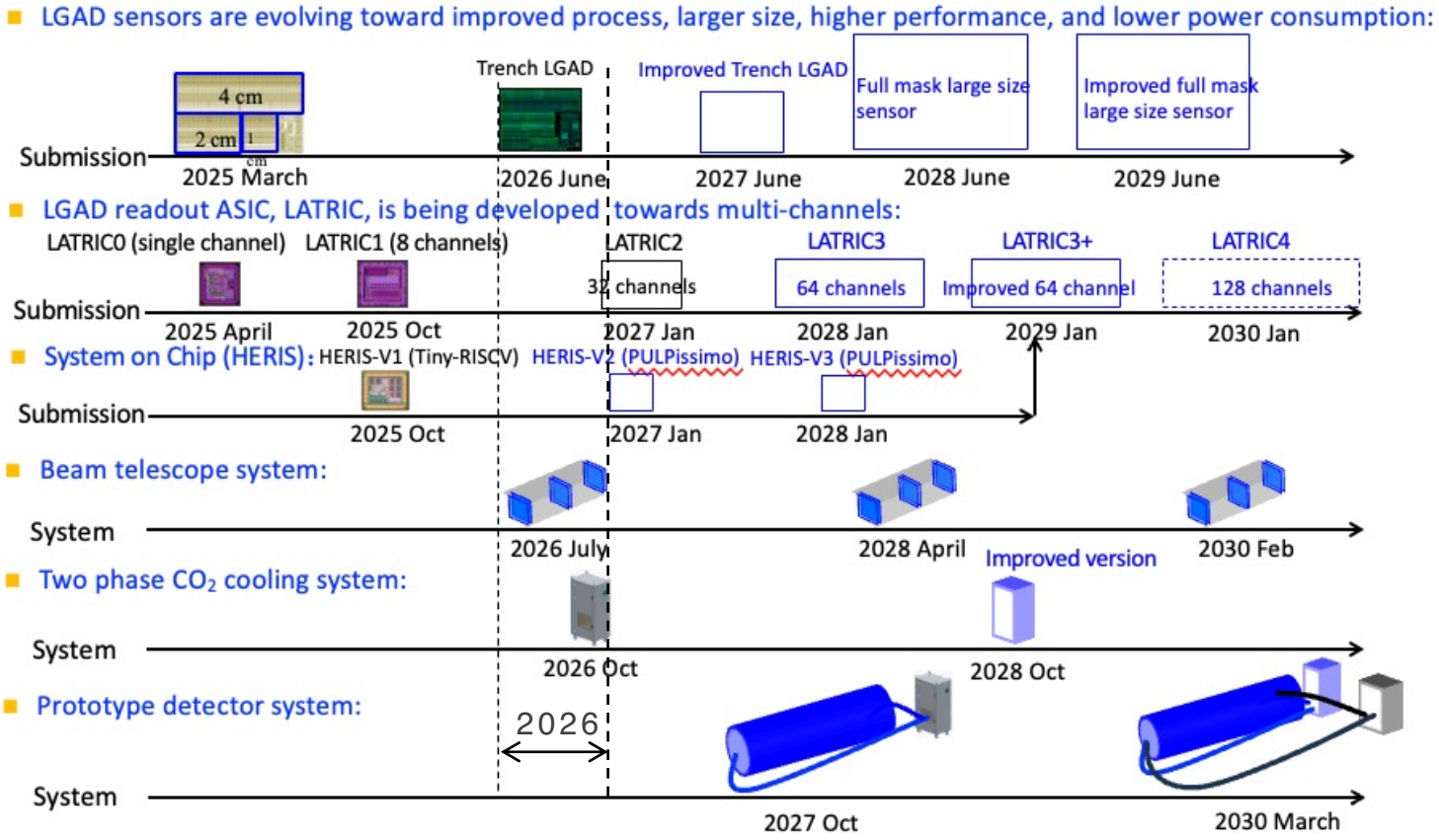
差压传感器

流量计

视液镜-CO2

Integration of the complete system is ongoing and is scheduled to be completed before October 2026.

Plan and Others



2026 plan: tape-out of trenched LGAD, development of LATRIC2 readout ASIC (32 channels), R&D of HERIS-V2 SoC; beam telescope construction and beam test, and development of two-phase CO_2 cooling system with full system integration tests.

- Team funding support: None; personnel talent program funding only.
- The project aims at engineering-oriented research with a strong focus on silicon tracker development. It establishes an integrated R&D framework covering sensors, dedicated readout electronics, and mechanical and cooling systems.