

# Silicon Inner Tracker R&D plan

- HVCMOS sensor development
  - Characterization of COFFEE3/CHiR (2026)
  - Submission of quarter-size validation chip (Q4 2026/Q1 2027)
  - Submission of full-size full-function chip (End 2027)
- Development of innovative integration approaches
  - NSFC application submitted, R&D started
  - Serial powering validation: chip functions implemented in CHiR, module-level validation ongoing with ATLASPix, later with COFFEE-series chips
  - Wireless transmission using mm-wave: prototyping in realistic material
- Module and system level prototyping
  - Assembly study initially with dummy sensors, later with large COFFEE/CHiR chips
  - Mechanical and cooling study
  - Barrel prototype in slice tests expected by end 2028
  - Endcap prototype expected by end 2029