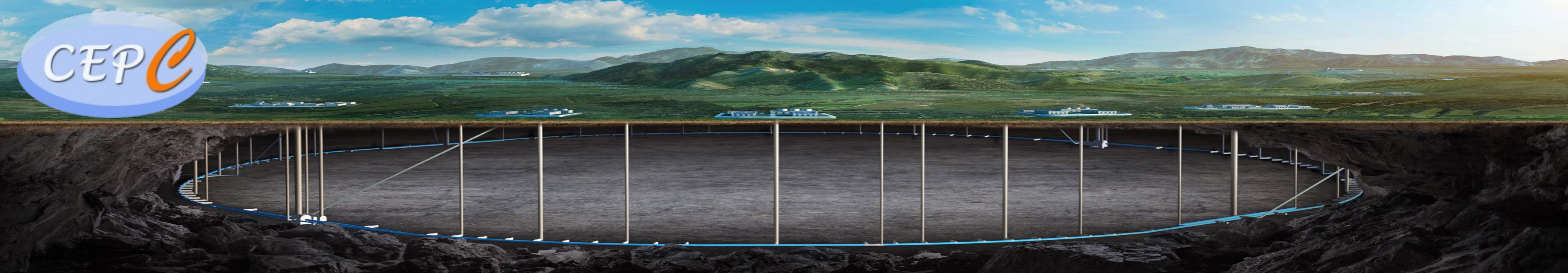


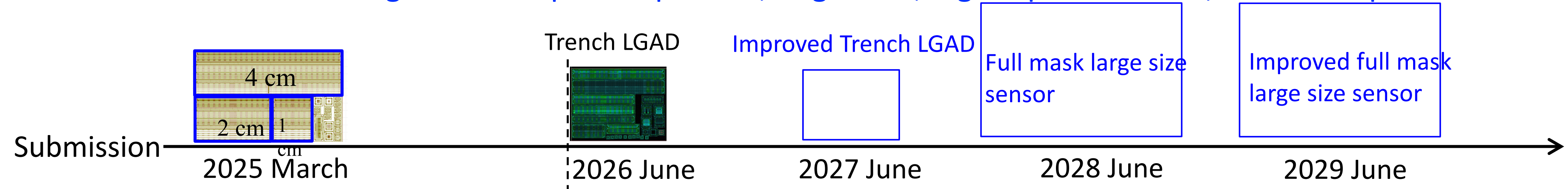
Latest Progress on the CEPC OTK

Zhengze Chang, Jiaolong Chen, Siyu Chen, Yuxin Cui, Kun Hu, Xiaoping Jing, Gang Li, Lei Liu, Xiaohui Qian, Xin Shi, JiaJian Teoh, Chuanye Wang, Kaining Wang, Xiongbo Yan, Xiyuan Zhang, Yihan Zhang, Zhihang Zhang, Mei Zhao, Zhanhong Zhao, Qi Yan*

June 24, 2026

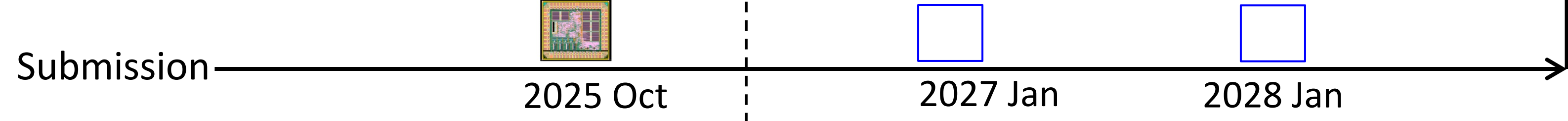
Latest Outer Silicon Tracker R&D Plan

- LGAD sensors are evolving toward improved process, larger size, higher performance, and lower power consumption:

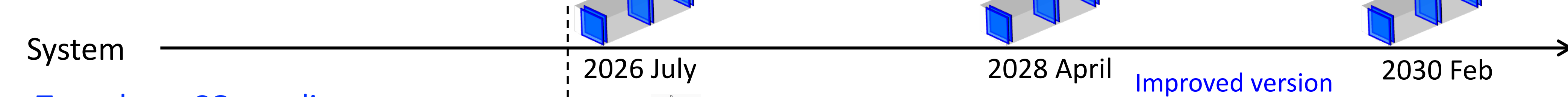


- LGAD readout ASIC, LATRIC, is being developed towards multi-channels:

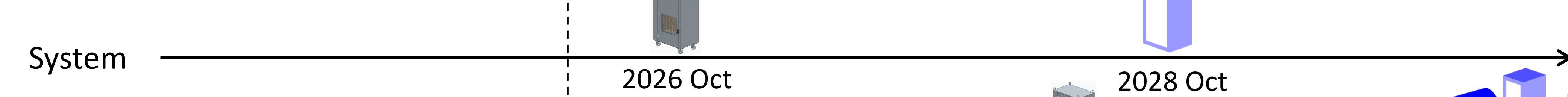
- System on Chip (HERIS): HERIS-V1 (Tiny-RISCV) HERIS-V2 (PULPissimo) HERIS-V3 (PULPissimo)



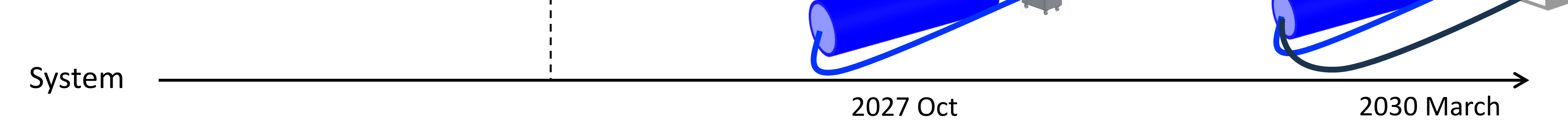
- Beam telescope system:



- Two phase CO_2 cooling system:

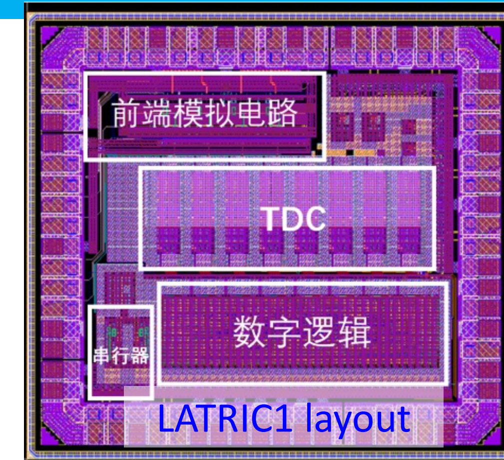


- Prototype detector system:



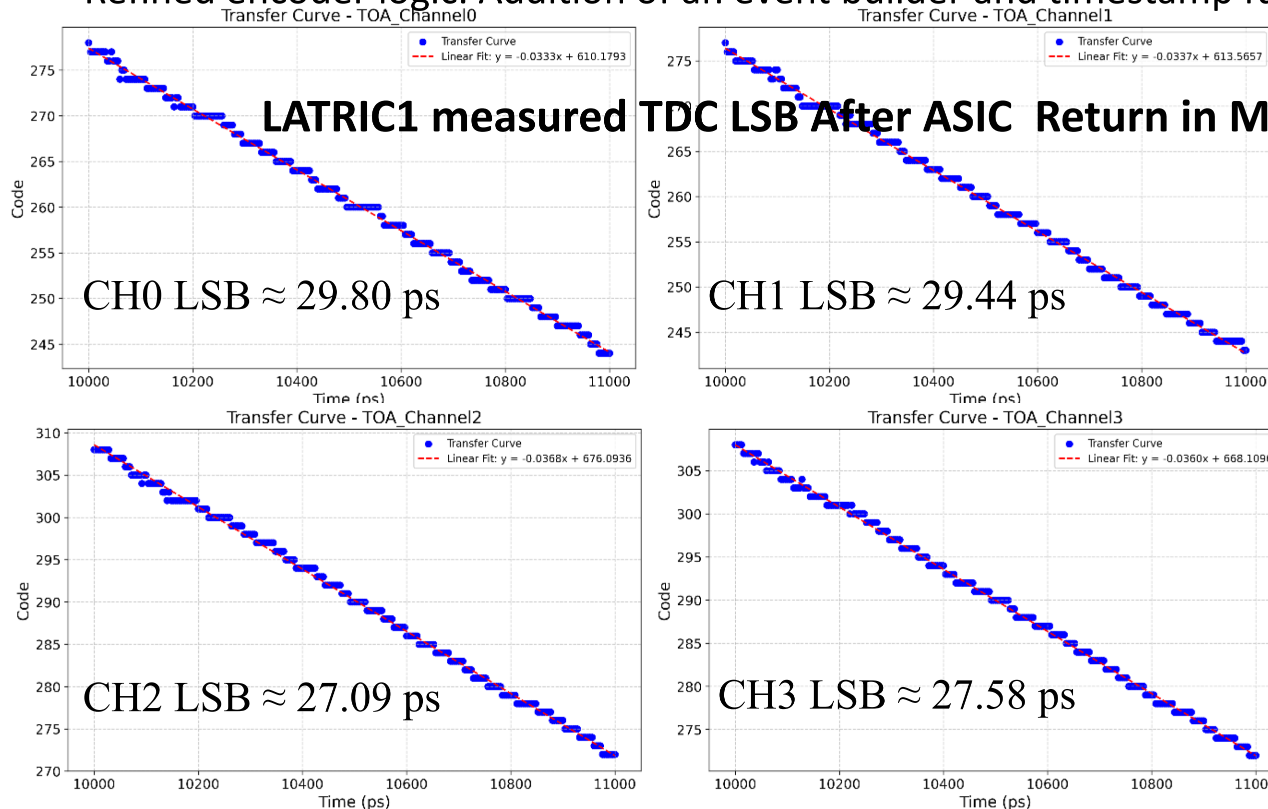
Latest Progress of the LATRIC Readout ASIC

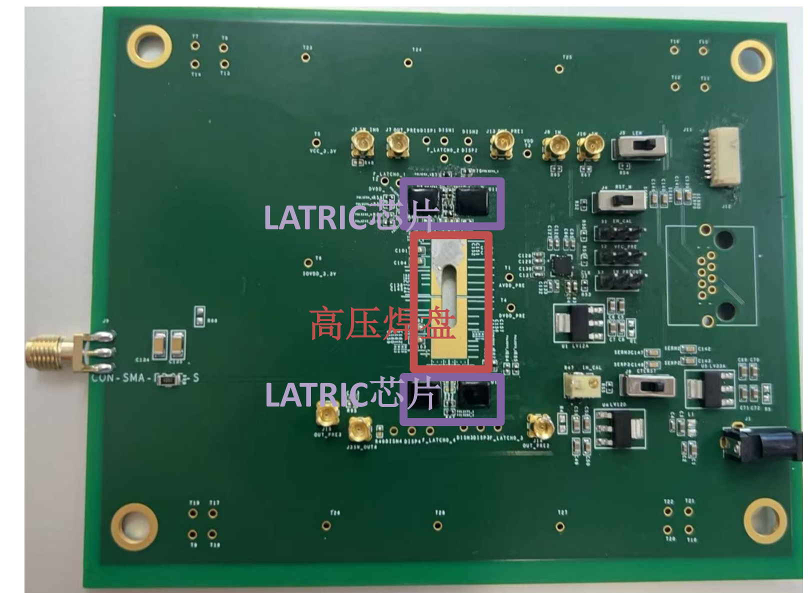
- The second version readout ASIC, LATRIC1, adopts an 8-channel was designed and submitted for tape-out in October 2025.
  - The channel pitch is **100 μm.** Four channels integrate the analog front-end and TDC. The other four channels consist of TDCs connected to differential pulse receivers.
- Performance optimizations include:
  - An enhanced analog front-end with increased preamplifier gain to improve the signal-to-noise ratio.
  - Refined encoder logic. Addition of an event builder and timestamp functionality, etc.



LATRIC1 layout

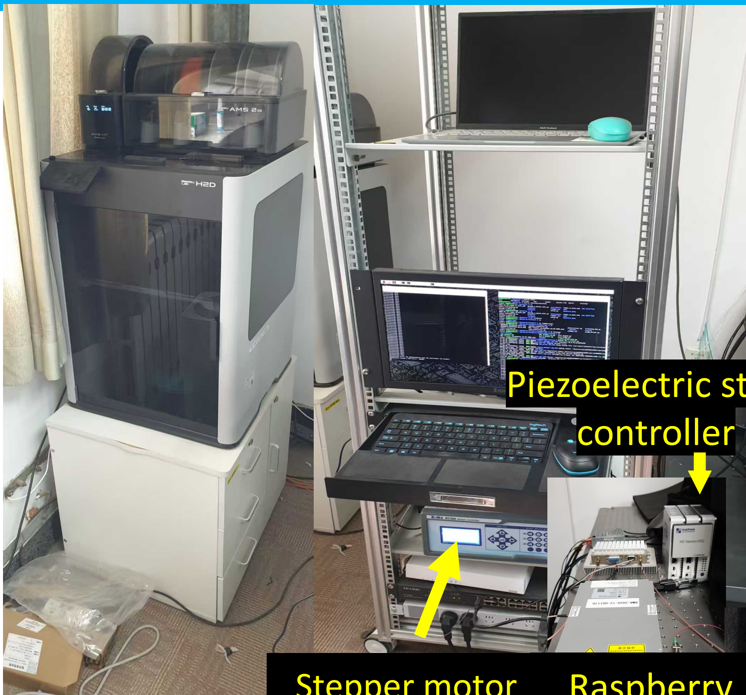
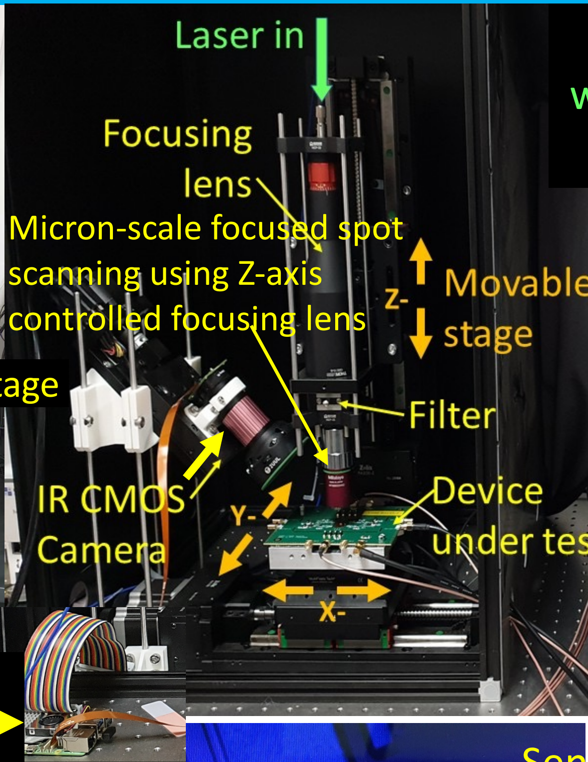
LATRIC1 measured TDC LSB After ASIC Return in March 2026



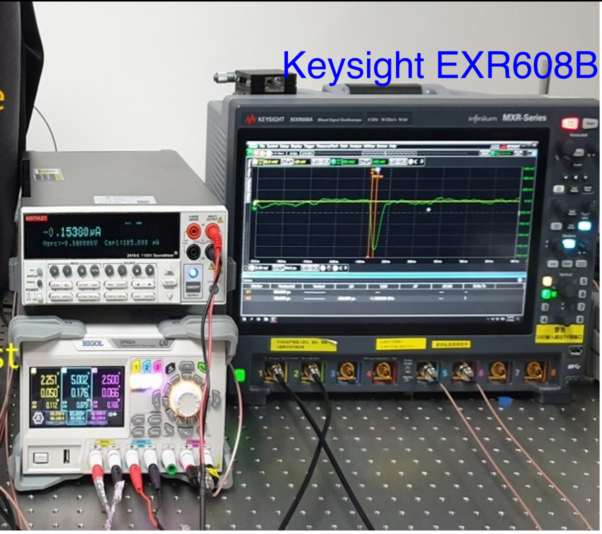


The latest designed LATRIC1-Sensor Integration Test Board

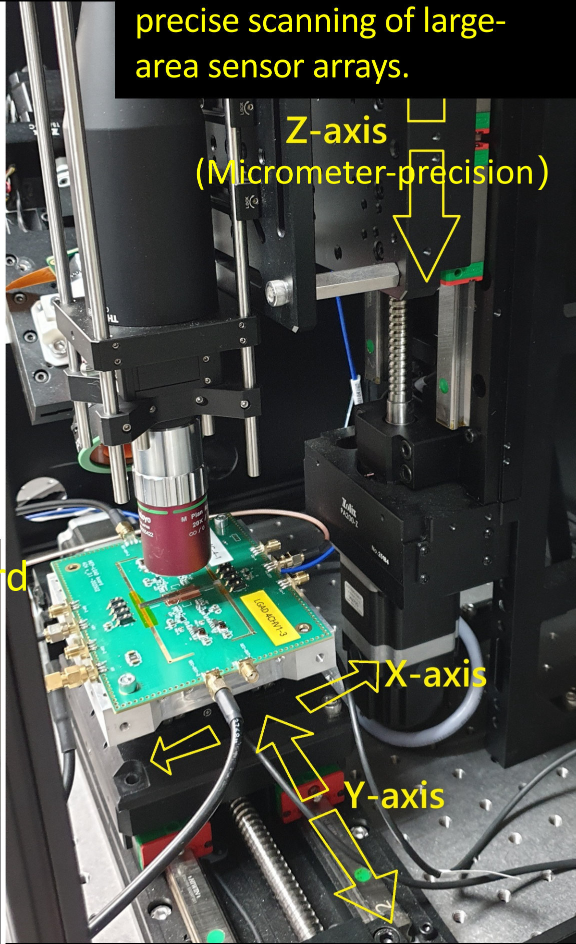
Sensor and LATRIC Test Setup

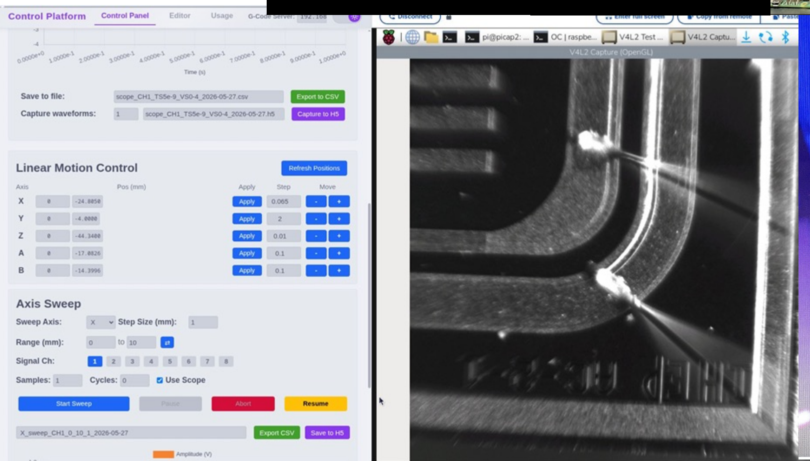
A 1064 nm infrared laser. The pulse width is about 8 ps, with a tunable laser rate ranging from 24 kHz to 24 MHz.

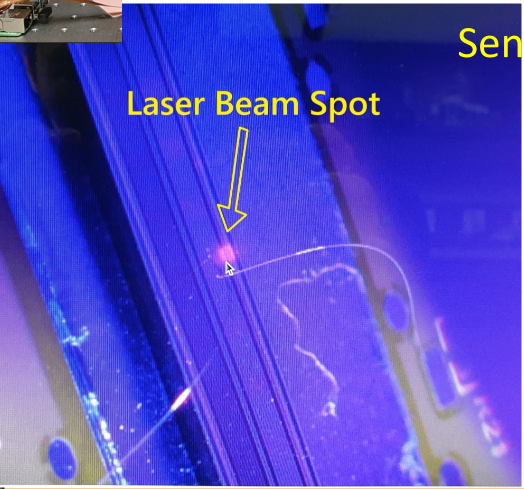


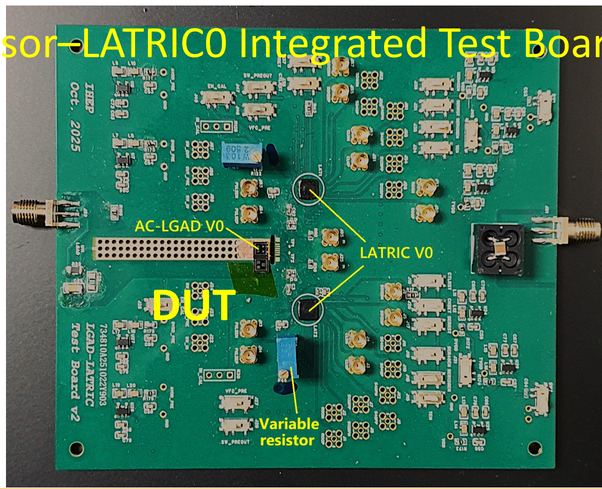
High-precision 3D stage with programmable 3-axis motors and piezo stage (10 nm step, 100 nm repeatability) for precise scanning of large-area sensor arrays.



(Nanometer-scale precision stage)

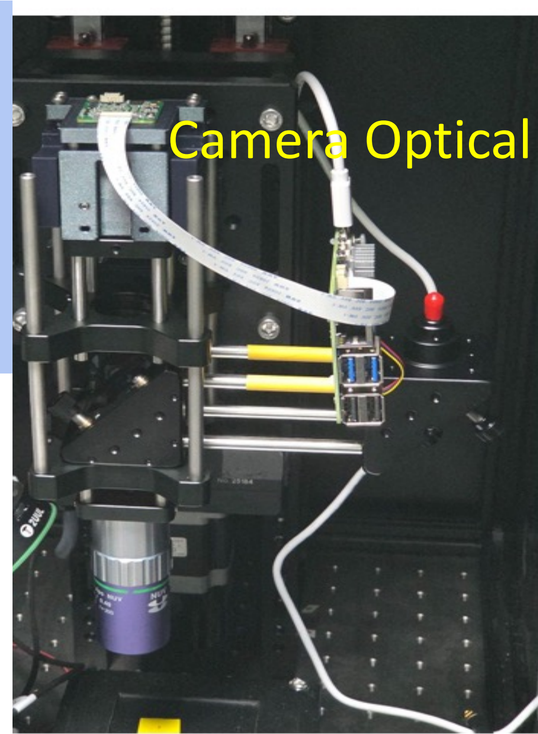
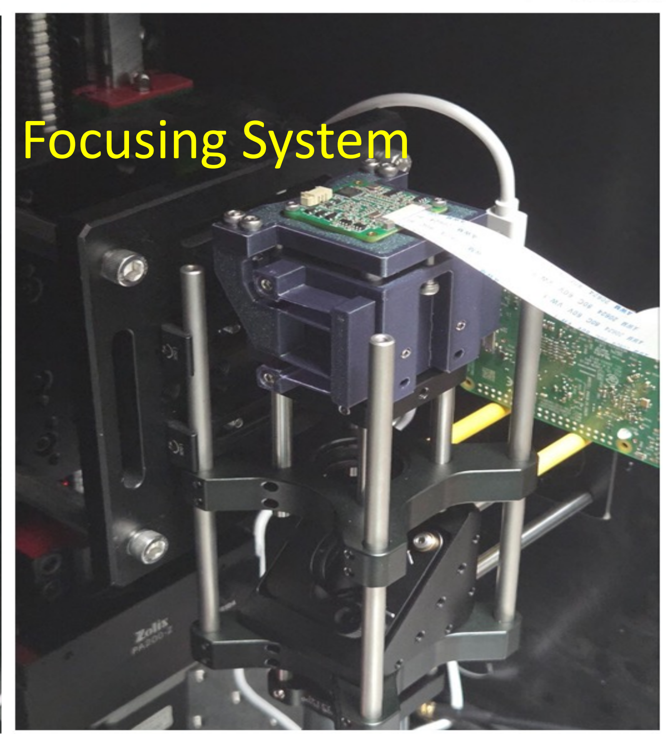


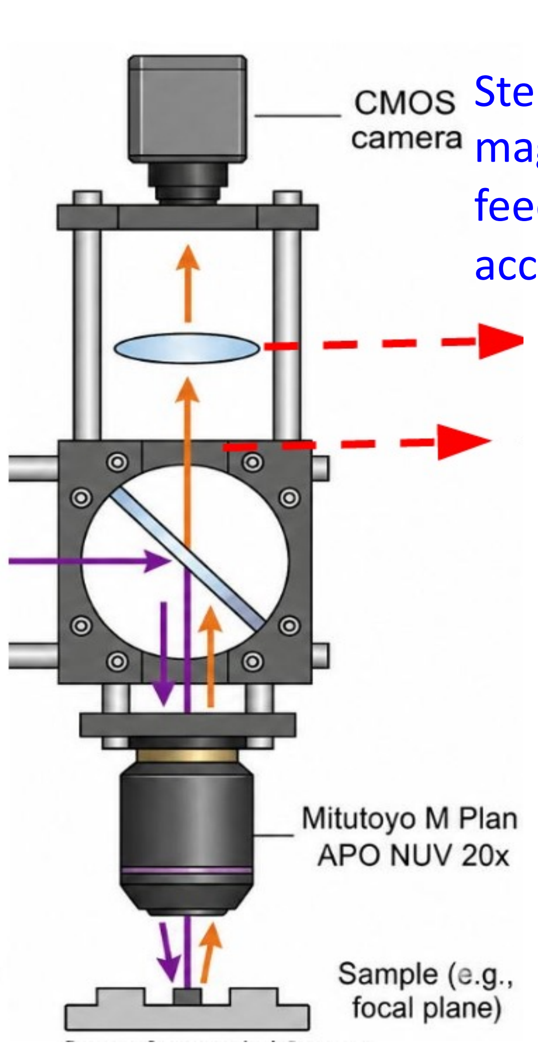




Sensor-LATRIC0 Integrated Test Board

In addition to the infrared test system, a customized UV laser test platform for SiC sensor has been developed. Both Si and SiC sensor development activities share a unified R&D framework with common test infrastructure, front-end electronics, and system integration resources.



Stepper motor with magnetic encoder feedback: positioning accuracy <0.1 μm

- 355 nm UV laser
- Repetition rate: 1–10 Hz
- Pulse width: ~10 ns

Automatic Focusing with CMOS Camera

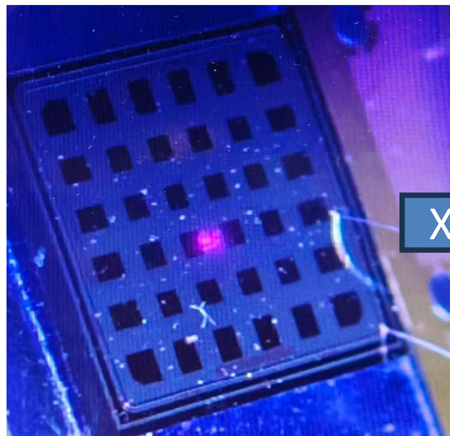
Precision DUT positioning control

Raspberry Pi

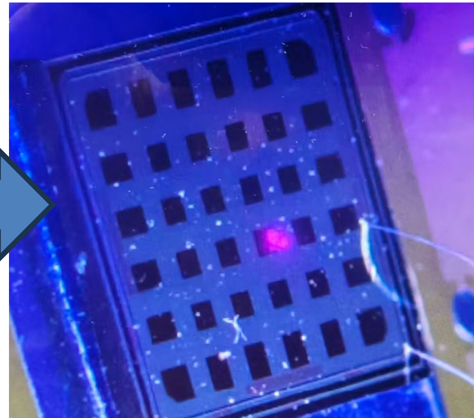
Y
X
Z

Hardware–Software Co-Designed Test System (Automated Knife-Edge Laser Scanning)

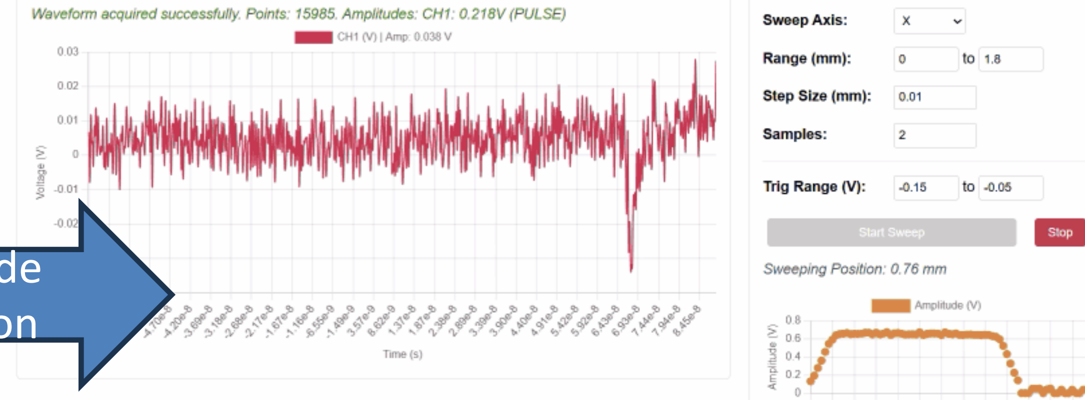
Automatic piezo-stage motion control → Data acquisition and transfer → Laser spot analysis → Automatic Z-axis adjustment → Iterative optimization of Z_0 (micron-level focusing precision) to minimize the laser spot size



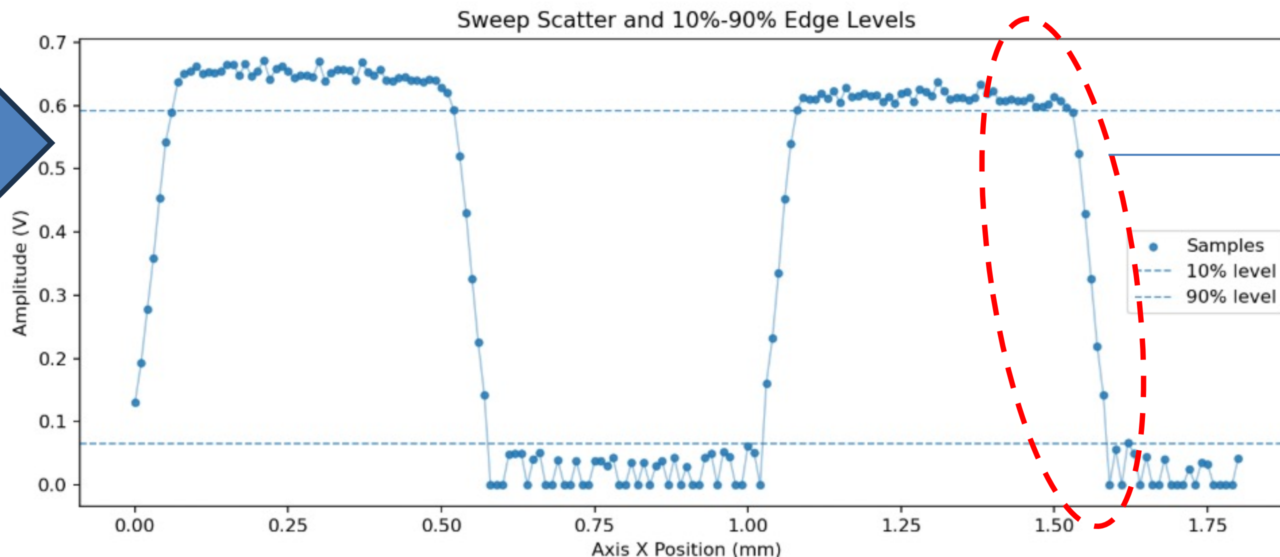
X-axis motion

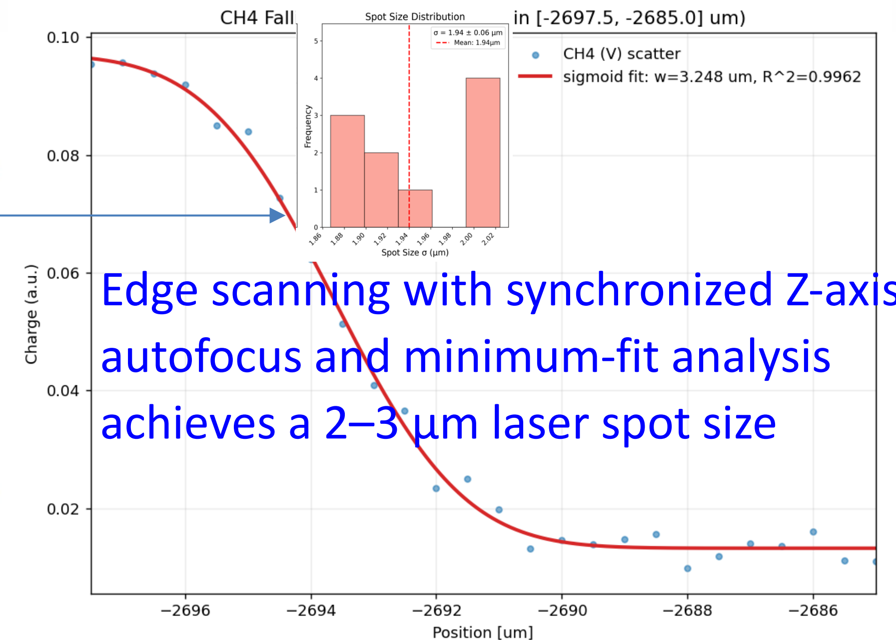


Amplitude extraction



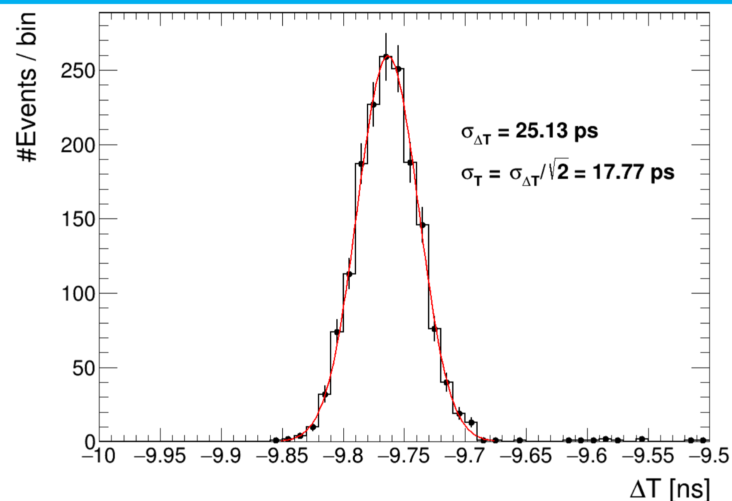
Scan output



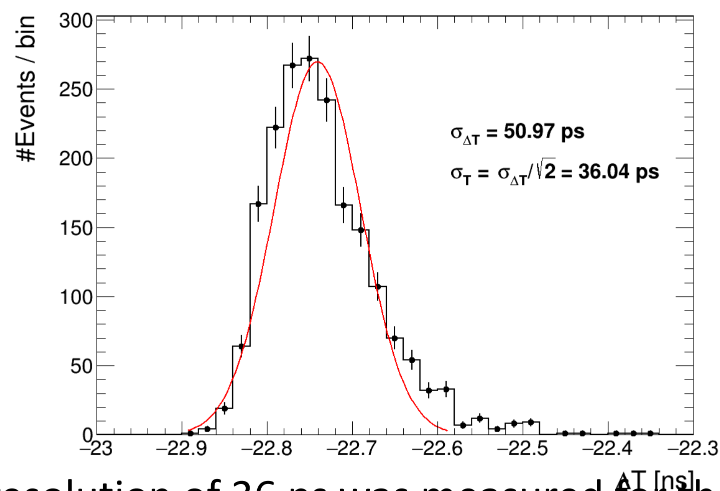


Edge scanning with synchronized Z-axis autofocus and minimum-fit analysis achieves a 2–3 µm laser spot size

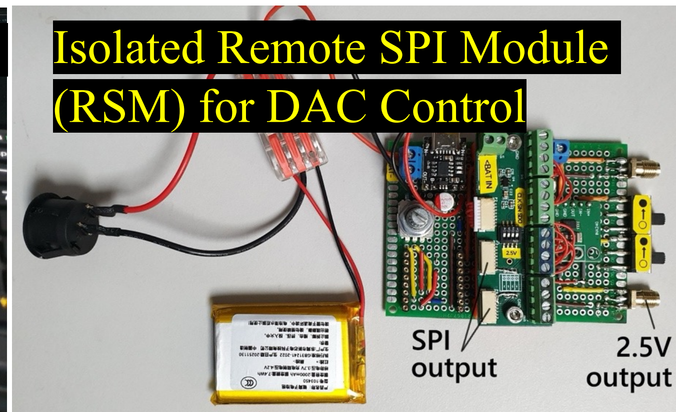
LATRIC0 (Single Channel) and Sensor Combined Test



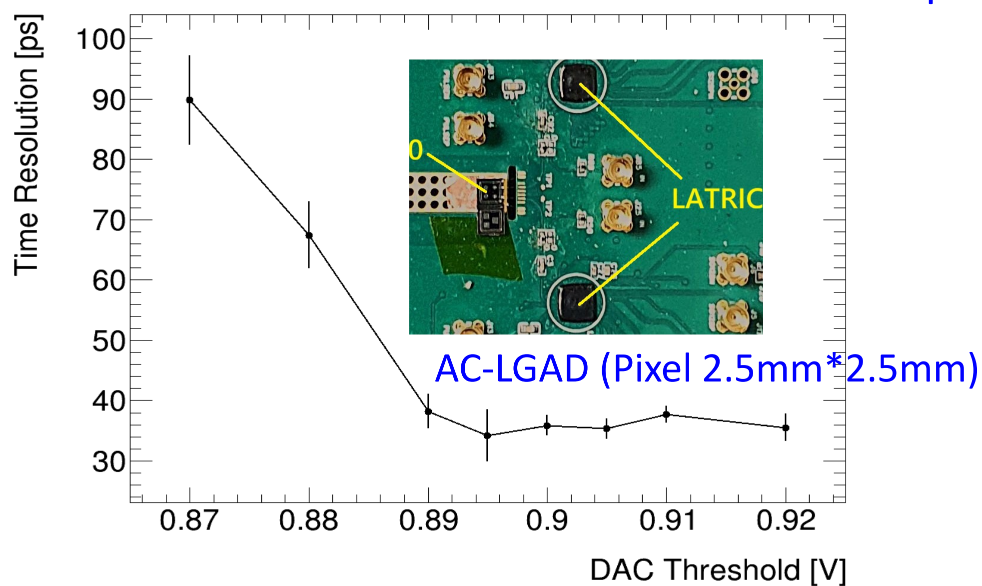
A time resolution of 18 ps was measured for the combined LGAD+LATRIC at 100% laser intensity.

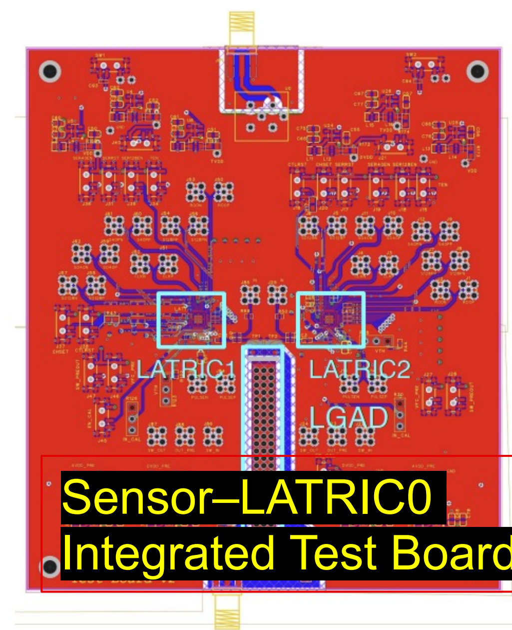


A time resolution of 36 ps was measured for the combined LGAD+LATRIC at a MIP-equivalent laser intensity (0.5%).



Time difference measured with two LATRIC0 chips





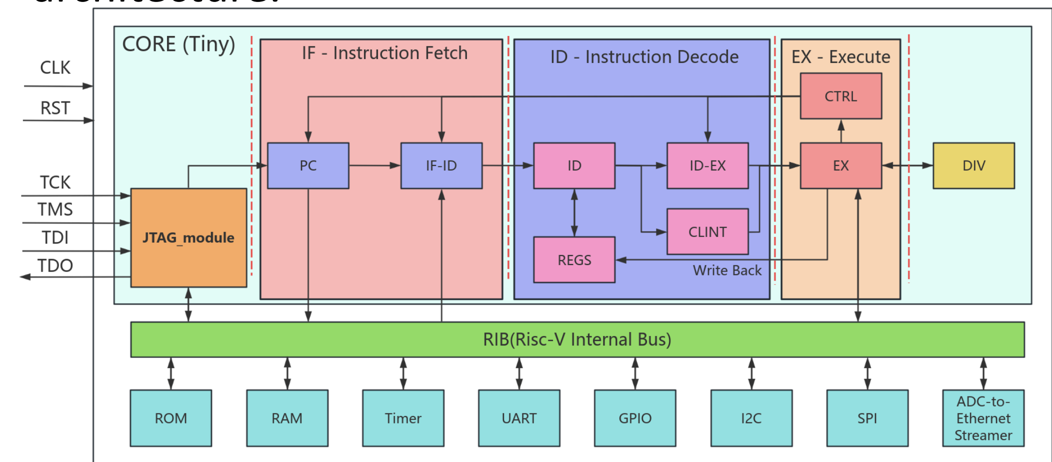
At MIP-equivalent laser intensity, the time resolution improves with increasing threshold and stabilizes at about 36 ps in the 0.89–0.92 V range.

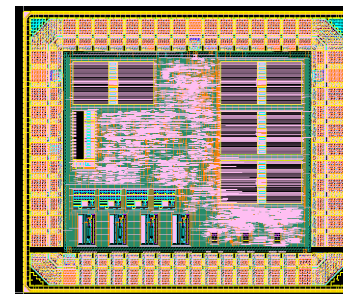
Development of the First System-on-Chip (SoC)

- HERIS: Radiation-Hard RISC-V SoC for High Energy Physics

Traditional ASICs are based on fixed hardware logic and lack flexibility for next-generation detectors. HERIS introduces a programmable SoC architecture (CPU, memory, bus, and peripherals), enabling a transition from passive readout to intelligent, adaptive front-end systems. HERIS-V1 (based on TinyRISC-V) was initiated in early 2025. The full design flow—including RTL development, FPGA validation, and digital backend integration—was completed, and the chip was taped out in October 2025 using a 55 nm CMOS process. In the future, HERIS will be integrated with the LATRIC readout ASIC to realize a “high-precision measurement + on-chip intelligence” architecture.

- Core (Tiny RISC-V)
  - RV32IM instruction set
  - 3-stage pipeline
  - CoreMark/MHz = 2.4
- JTAG interface
  - OpenOCD support
  - GDB debug support
- Peripherals
  - 4 KB ROM, 32 KB RAM
  - I²C, UART, and SPI interfaces
  - Integrated ADC data acquisition module with UDP-based data transmission

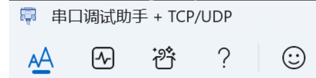




- 55 nm CMOS process
- Operating frequency: 50 MHz
- Chip area: 1.020 × 1.196 mm²
- Operating voltage: 1.2 V

Test of HERIS-V1 SoC Chip

```
PS E:\fpga\Tools\xpack-openocd-0.12.0-6\bin> .\openocd.exe -f .\tinyriscv_JTAG_HS2.cfg
xPack Open On-Chip Debugger 0.12.0+dev-01850-geb6f2745b-dirty (2025-02-07-10:08)
Licensed under GNU GPL v2
For bug reports, read
        http://openocd.org/doc/doxygen/bugs.html
Info : clock speed 1000 kHz
Info : JTAG tap: riscv.cpu tap/device found: 0x1e200a6f (mfg: 0x537 (Wuhan Xun Zhan Electronic Technology), part: 0xe200
, ver: 0x1)
Info : datacount=3 progbufsize=1
Info : Examined RISC-V core; found 2 harts
Info :  hart 0: XLEN=32, misa=0x0
Info : [riscv.cpu] Examination succeed
Info : [riscv.cpu] starting gdb server on 3333
Info : Listening on port 3333 for gdb connections
Info : Listening on port 6666 for tcl connections
Info : Listening on port 4444 for telnet connections
```



串口调试助手 + TCP/UDP

端口名： COM5
波特率： 115200
数据位： 8
校验位： None
停止位： 1

```
--- RISC-V Bootloader Started ---
Initializing SD card on SPI channel 1...
SD_INIT: Failed on CMD0
!!! FATAL: SD Card initialization failed. Halting. !!!
�Target RAM size: 14336 bytes. Need to read 28 blocks from SD card.
Starting to copy data from SD:@0x0 to RAM:@0x10000000...
```

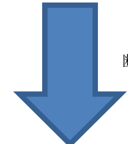
- First power-on: OpenOCD works normally, ROM code runs successfully.

- The on-board EEPROM has been successfully verified to operate via the I2C protocol

```
int main() {
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);
    uint16_t test_addr = 0x1234;
    uint8_t test_data  = 0xAC;

    eeprom_write_byte(test_addr, test_data);
    uint8_t read_back = eeprom_read_byte(test_addr);
```

UART输出

```
== I2C Master Final Test Program ===
[I2C] Write: Addr=0x1234 Data=0xAC
  > Config Check: Slave=0x53, Addr=0x1234, Data=0xAC
[I2C] Read: Addr=0x1234
```



断电后再次运行

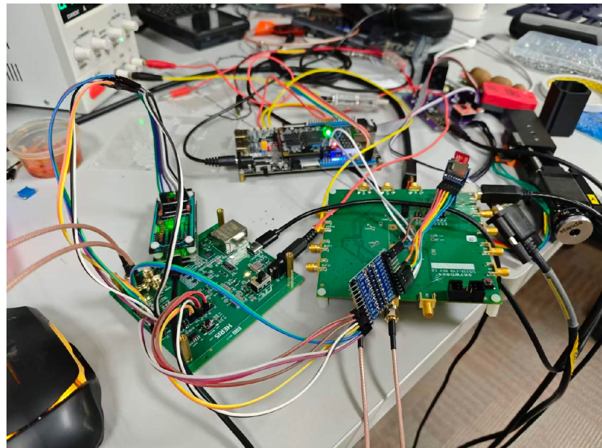
UART输出

```
int main() {
    uart_init();
    xprintf("\n=== I2C Master Final Test Program ===\n");
    i2c_init(50000000, 100000);

    uint16_t test_addr3 = 0x0123;
    uint8_t read_back3 = eeprom_read_byte(test_addr3);
    uint16_t test_addr2 = 0x1234;
    uint8_t read_back2 = eeprom_read_byte(test_addr2);

    xprintf("[I2C] Verification: Read1 0x%02X, Read2 0x%02X\n", read_back3, read_back2);
```

```
=== I2C Mater Final Test Program ===
[I2C] Read: Addr=0x0123
[I2C] Read: Addr=0x1234
[I2C] Verification: Read1 0xFF, Read2 0xAC
```

The first RISC-V Soc chip, HERIS-V1, has been successfully validated.

- The ROM and SD card boot functions work properly, and the SPI module operates correctly.



串口调试助手 + TCP/UDP

端口名： COM11
波特率： 115200
数据位： 8
校验位： None
停止位： 1

```
--- RISC-V Bootloader Started ---
Initializing SD card on SPI channel 1...
SD Card on SPI CH-1 initialized successfully.
SD Card initialized successfully.
Target RAM size: 14336 bytes. Need to read 28 blocks from SD card.
Starting to copy data from SD:@0x0 to RAM:@0x10000000...
.......
Data copy complete.
Bootloader finished. Jumping to application at 0x10000000...
hello world
```

- The GPIO functionality has been verified.

```
GPIO0 and GPIO1 are set to output mode (0).
```

HERIS-V1 Performance Test

CoreMark Benchmark Statistics

Test Configuration

Item	Value
CPU Architecture	RV32IM Softcore
Benchmark	CoreMark
Iterations	100
Compiler	GCC 8.2.0
Optimization	`-O2 -funroll-loops -finline-functions`
Memory Mode	STATIC
Assumed Timer Clock	50 MHz

HERIS-V1 benchmark score

CoreMark Results Summary

Run	Total Ticks	Time (s)	CoreMark	CoreMark/MHz
1	47,140,681	0.943	106.07	2.121
2	57,254,527	1.145	87.33	1.747
3	57,254,216	1.145	87.33	1.747
4	57,254,809	1.145	87.32	1.746
5	57,254,522	1.145	87.33	1.747
6	57,254,148	1.145	87.33	1.747
7	57,255,302	1.145	87.31	1.746
8	57,256,313	1.145	87.30	1.746
9	57,253,503	1.145	87.33	1.747
10	36,131,525	0.723	138.38	2.768
11	57,254,188	1.145	87.33	1.747
12	57,254,522	1.145	87.33	1.747
13	57,254,203	1.145	87.33	1.747

#	Total Ticks	CoreMark	CoreMark/MHz
1	264,551,913	18.90	0.378
2	25,685,150	194.66	3.893
3	55,131,135	90.69	1.814
4	29,876,551	167.35	3.347
5	57,253,579	87.33	1.747
6	57,243,713	87.35	1.747
7	29,906,285	167.19	3.344
8	57,254,426	87.33	1.747
9	41,493,461	120.50	2.410
10	46,612,237	107.27	2.145
11	54,497,797	91.75	1.835
12	48,237,510	103.65	2.073
13	28,275,053	176.83	3.537
14	57,253,726	87.35	1.747
15	13,635,777	366.68	7.334
16	25,475,668	196.27	3.925
17	57,253,893	87.35	1.747
18	57,253,672	87.36	1.747
19	57,253,673	87.36	1.747
20	26,854,754	186.19	3.724
21	57,250,967	87.40	1.748
22	58,844,737	84.97	1.699
23	57,253,266	87.36	1.747
24	55,910,085	89.43	1.789
25	6,725,030	743.49	14.870
26	57,254,283	87.33	1.747
27	57,253,680	87.36	1.747
28	57,255,110	87.32	1.746
29	57,255,184	87.33	1.747
30	57,254,539	87.33	1.747
31	56,236,672	88.91	1.778
32	57,253,678	87.36	1.747
33	49,780,037	100.44	2.009
34	57,253,673	87.36	1.747
35	310,466,500	16.11	0.322
36	57,253,210	87.36	1.747

Frequency: 50 MHz; maximum operating frequency: 150 MHz.

Performance benchmark：

- **ARM Cortex-M0/M0+：** 0.9 ~ 1.0
- **PicoRV32 (RISC-V)：** 0.5 ~ 0.8
- **HERIS-V1：** achieves a score of 1.75, consistent with FPGA results.
- **VexRiscv / 蜂鸟 E203：** 1.5 ~ 2.2
- **ARM Cortex-M3 / M4：** 3.3 ~ 3.4

LATRIC0 Paper Published and HERIS-V1 Paper Submitted This Week

Topical Workshop on Electronics for Particle Physics
Rethymno, Crete, Greece
6–10 October 2025

First prototype of a low-power timing chip for strip LGAD readout: LATRIC0

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2026 JINST 21 C04028

Abstract: LATRIC0 is a single-channel readout chip designed for the Outer Tracker (OTK) of the reference detector on the Circular Electron Positron Collider (CEPC). The OTK employs AC-coupled Low-Gain Avalanche Detector (AC-LGAD) microstrip sensors to achieve high-precision spatial (10 µm) and timing (50 ps) measurements. Fabricated using a 55 nm CMOS process, LATRIC0 integrates an analog front-end amplifier and an event-driven ring-oscillator-based Time-to-Digital Converter (TDC) in a compact architecture. Measurements show that the prototype achieves a Least Significant Bit (LSB) of approximately 30 ps from both Time-over-Threshold (TOT) and Time-of-Arrival (TOA). The TDC core consumes less than 1.0 mW, while the total power of the front-end and TDC together is below 7.0 mW. The measured Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) are within 1 LSB. LATRIC0 not only validates the proposed timing architecture but also establishes a foundation for the development of a future fully functional version with 128 channels and 100-µm channel pitch.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Timing detectors

1 2
HERIS-V1: A 55 nm CMOS RISC-V SoC for High-Energy Physics Instrumentation

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4 Luo[f], Xin Shi[b,g], Jiajian Teoh[b], Xin Tong[b,c], Xiongbo Yan[b,g], Xiyuan Zhang[b,g],
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13 **Abstract**

High-energy physics (HEP) detector readout systems face increasingly stringent constraints on data bandwidth, trigger latency, and power consumption, motivating the integration of programmable edge-computing capabilities into front-end electronics. This paper presents HERIS-V1, a 55 nm CMOS RISC-V-based SoC for HEP instrumentation designed to provide software-defined control, monitoring, and configuration for next-generation detector front-end ASICs. HERIS-V1 adopts a decoupled architecture that separates a lightweight RISC-V supervisory subsystem from a dedicated hardware data-acquisition path. Post-silicon characterization demonstrates stable operation of the customized RISC-V core, which occupies a compact standard-cell area of approximately 250 × 250 µm^2. Operating at a nominal clock frequency of 50 MHz with a 1.2 V core supply, the processor achieves a performance of 1.747 CoreMark/MHz while consuming only 10.8 mW of isolated core power in the idle state. The prototype successfully validates a robust digital framework, including flexible dual-boot initialization, memory-mapped interconnects, and peripheral interfaces such as I^{2}C, SPI, and UART. The successful in-silicon bring-up of HERIS-V1 demonstrates the feasibility of integrating lightweight programmable intelligence into HEP front-end systems, providing a scalable baseline for future detector architectures with enhanced monitoring and control capabilities.

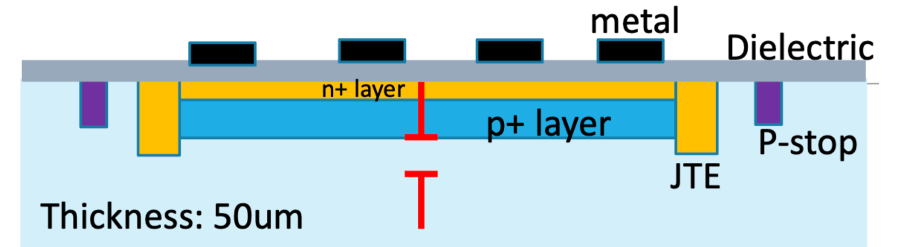
14 *Keywords:* RISC-V, System on Chip, High Energy Physics, Front-end

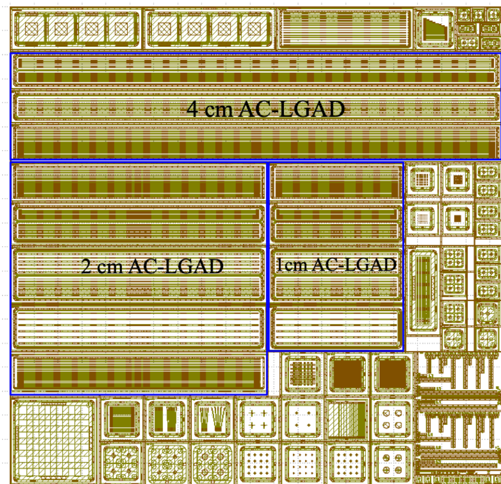
AC-LGAD Sensor with Long Strip

AC-LGAD microstrip sensors (≥2 cm × 2 cm), aiming at optimal position resolution, timing resolution, and lower power consumption. The latest tape-out was submitted in 2025.

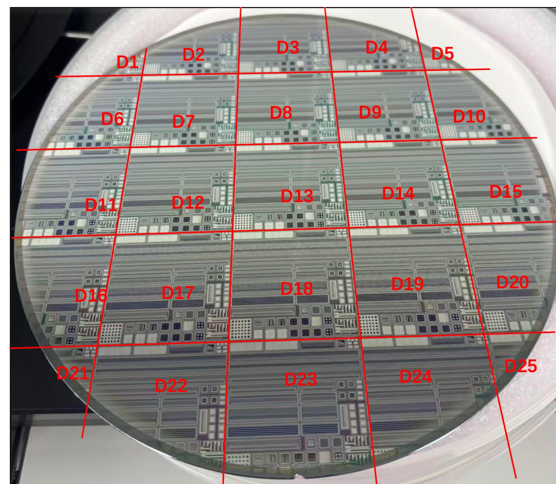
The design explores different microstrip geometries, including:

- strip length: 1 cm, 2 cm, and 4 cm
- strip pitch: 100 µm, 200 µm, and 500 µm
- electrode width: 25 µm, 50 µm, and 100 µm
- The n^{+} doping is tuned to optimize position resolution performance, and the EPI thickness is optimized to reduce capacitance and thus lower readout power consumption.

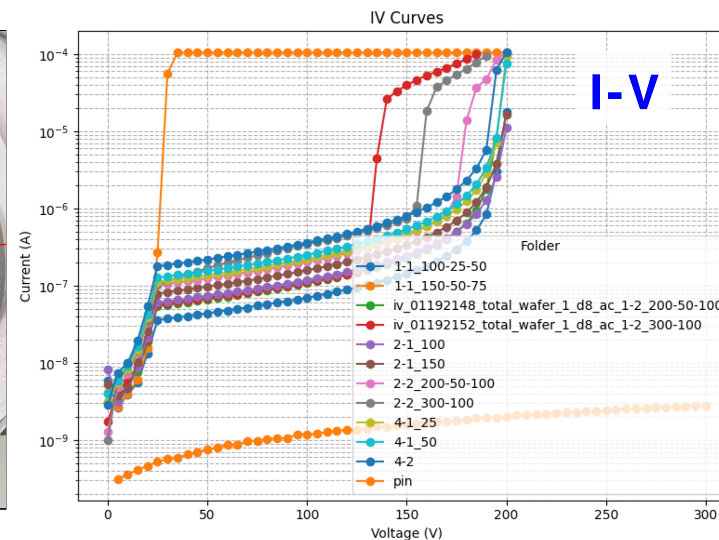


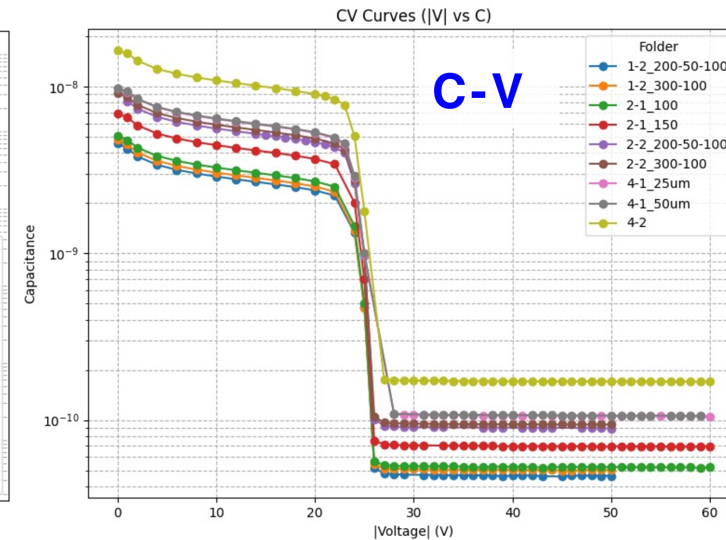


AC-LGAD LAYEROUT



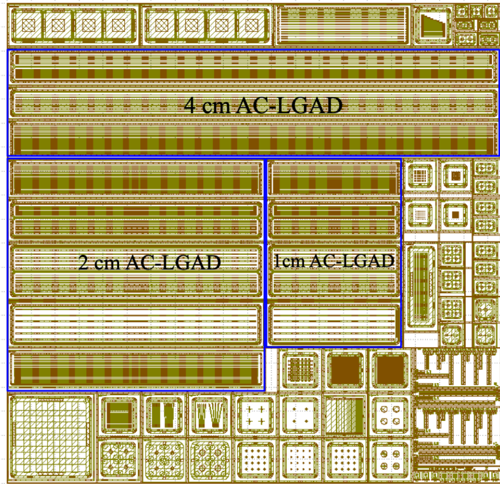
AC-LGAD Wafer





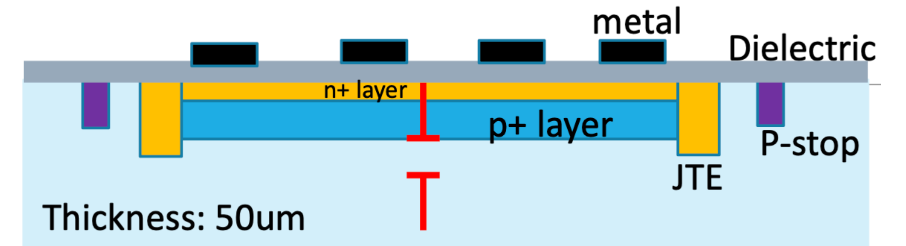
Latest Status of LGAD Sensor

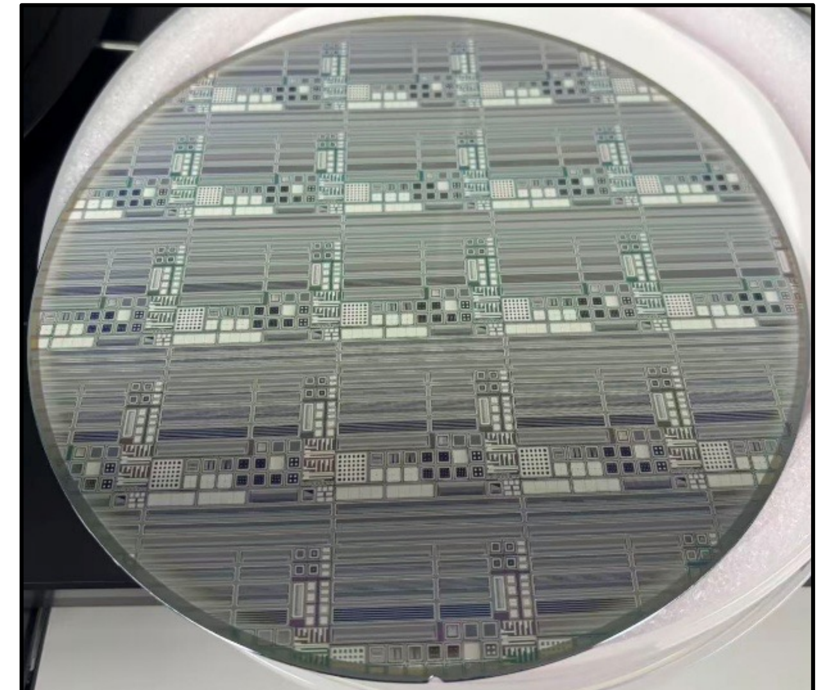
To date, 7 out of 18 wafers have been fabricated, and process optimization are ongoing. In May 2026, 2 wafers with lower n+ dose been delivered in May 2026.



AC-LGAD LAYEROUT

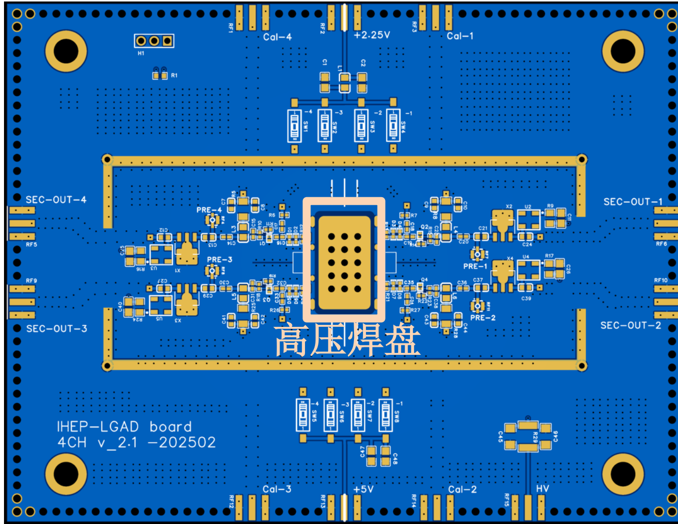
Wafer number	EPI thickness	n+ dose
1	50um	10p
2	50um	10p
3	50um	0.01p
7	80um	10p
8	80um	0.01p
4	50um	1p, 0.1p
5	80um	1p, 0.1p





The primary improvement was in sensor position resolution.

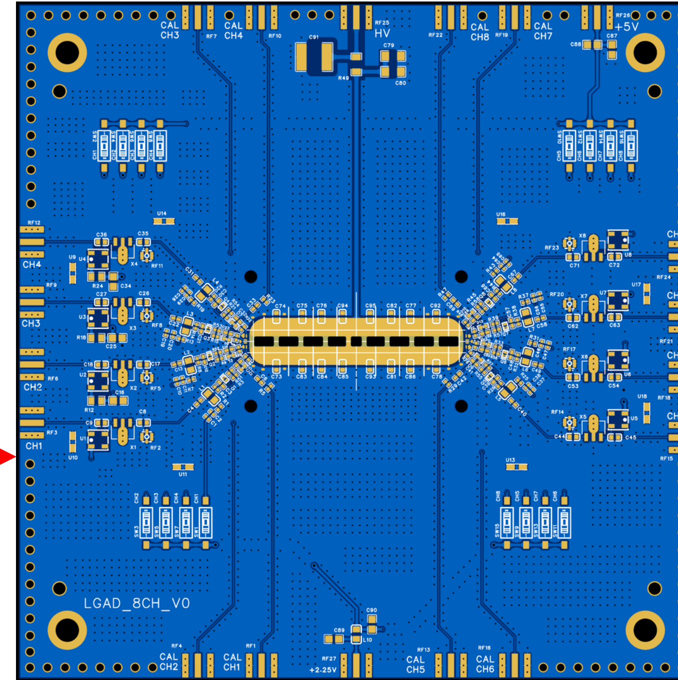
LGAD Pre-Amplifier Board Optimization



10cm x 13cm

V1: 4-Channel LGAD Pre-Amplifier Board:

- Provides high-voltage bias for LGAD sensors.
- Four signal readout channels
- ~100× amplification per channel



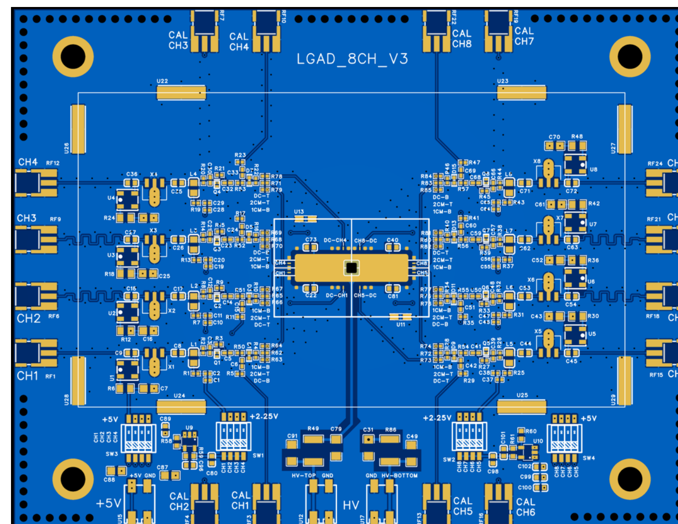
13cm x 13cm

V2: 8-Channel LGAD Pre-Amplifier Board:

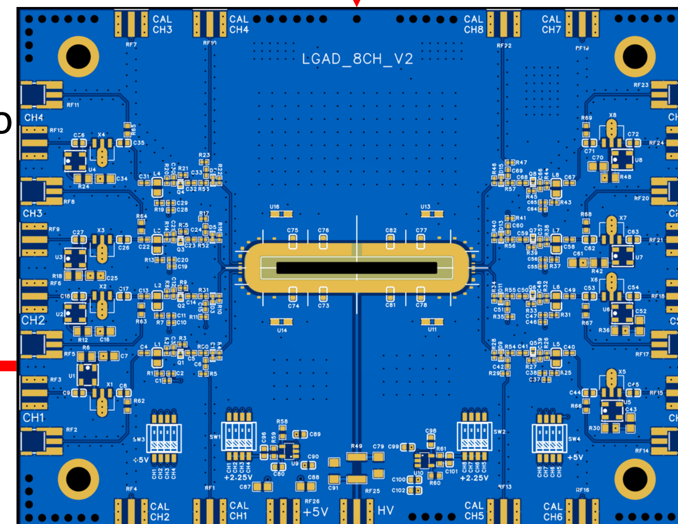
- Increased number of channels
- Extended high-voltage pads for better compatibility with strip sensors
- Optimized HV pad geometry with cut-outs to improve particle detection efficiency

V4: 8-Channel Double-Sided LGAD Pre-Amplifier Board:

- Enabled double-sided to support different LGAD types (pixel and strip)
- Optimized routing with equal-length traces for all 8 channels
- Reduced board thickness to ~5 mm



10cm x 13cm



10cm x 13cm

V3: 8-Channel LGAD Pre-Amplifier Board

- Reduced board size for better integration
- Simplified power connectors for easier cabling
- Optimized HV pad cut-out geometry to further enhance particle detection efficiency

Sensor Characterization

Laser

50% Polarization-maintaining beam splitter 50%

Attenuator and focusing system

Photodiode (PD)

Timing resolution 1.2 ps

LGAD or LGAD+LATRIC

PCB

Trigger

Oscilloscope

Data analysis

DUT sensor

Laser scanning

CH-1
CH-2
CH-3
CH-4

Amplitude [mV]

Time [ns]

PD

CH-1

CH-2

CH-3

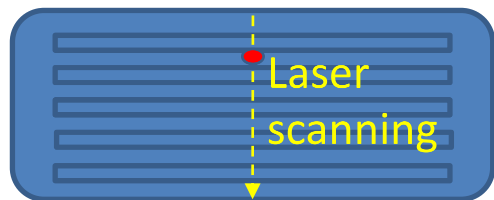
CH-4

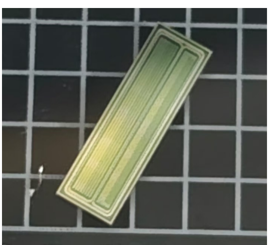
Typical Event Waveform
(Sensor: W4-AC-D9, 0.2% laser intensity)

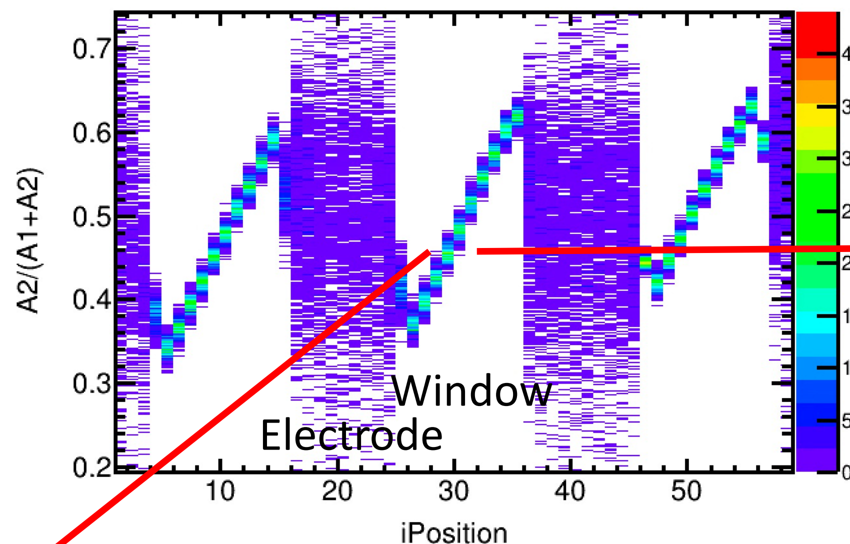
Strip Sensor Spatial Resolution (0.2% Laser)

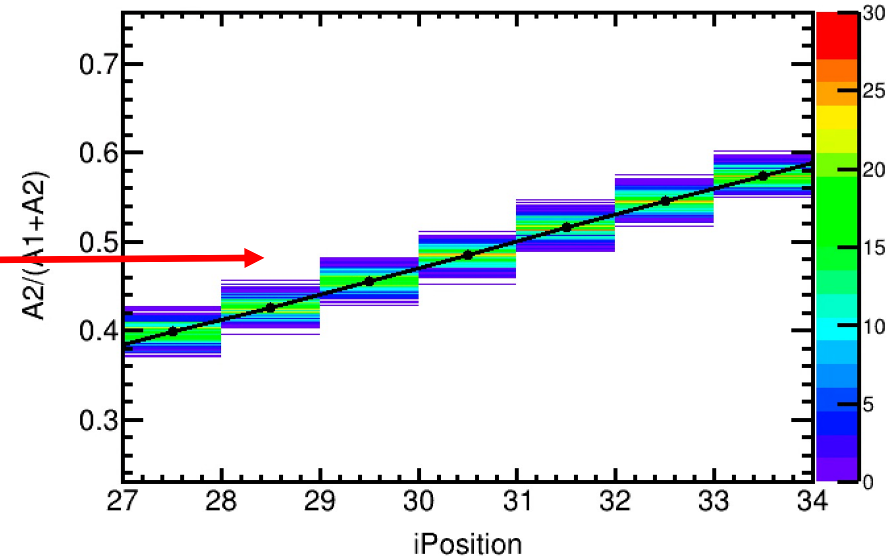
A_2 and A_1 are the waveform amplitudes of the seed (maximum amplitude) strip and the second strip, respectively.

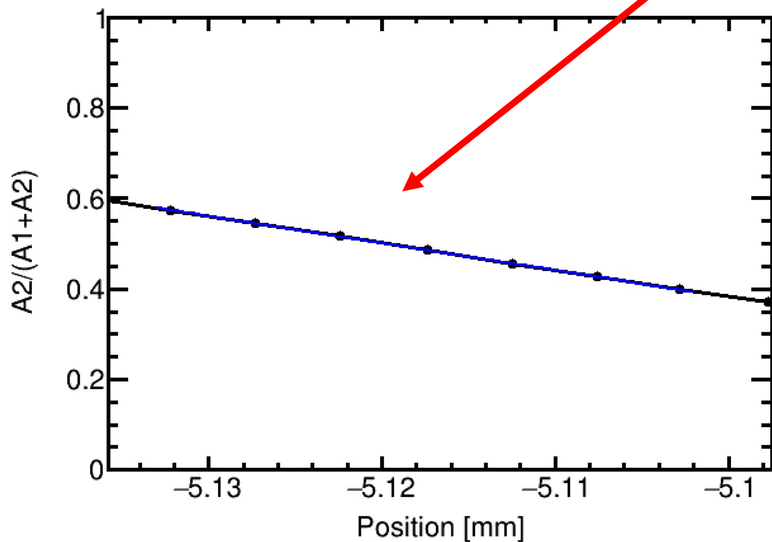
DUT sensor

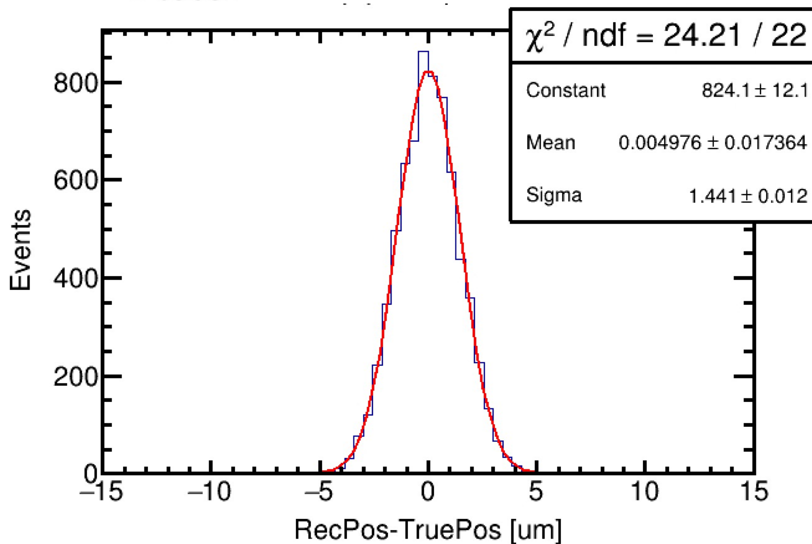






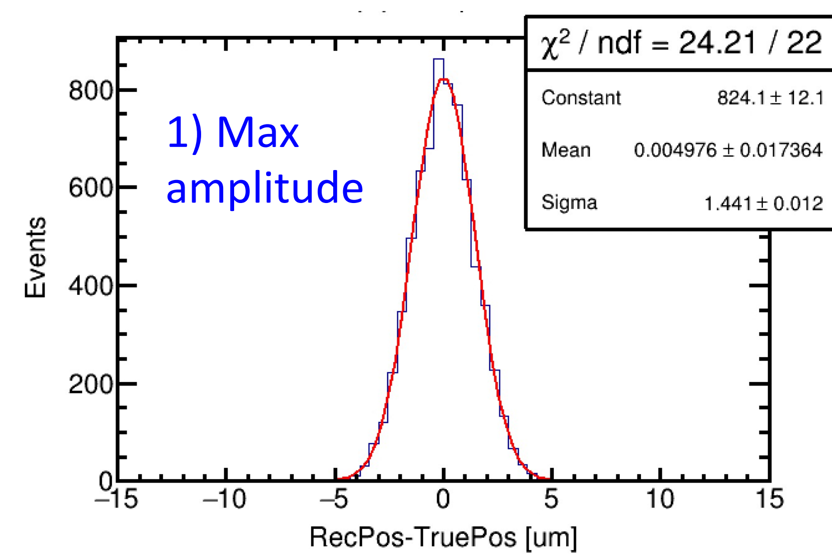


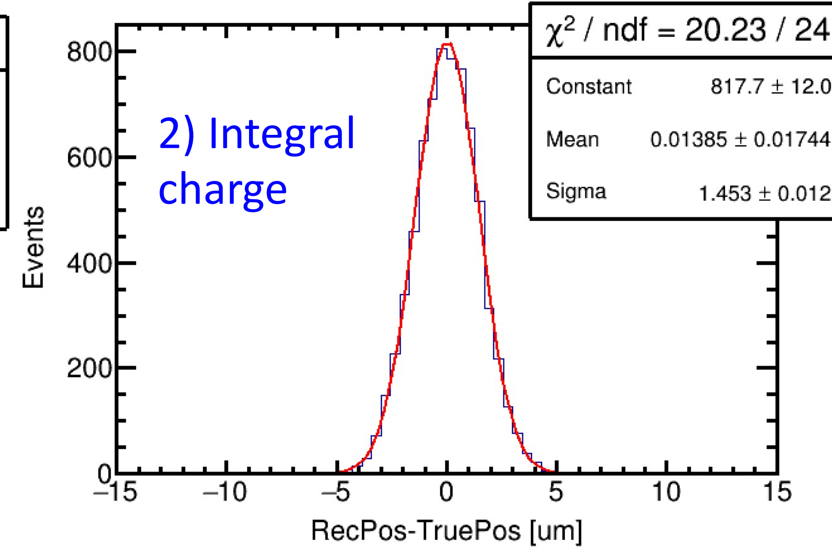


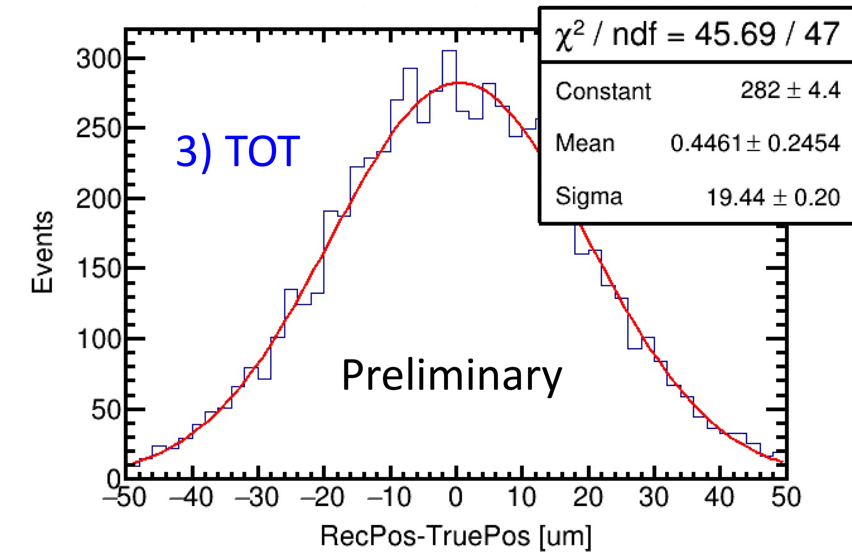


The latest tape-out optimized n^+ strip sensor (W4-AC-D9, 2 cm, n^+ dose = 0.1 p) achieved a spatial resolution of ~1.4 µm.

Sensor Spatial Resolution Using Different Amplitude Estimators

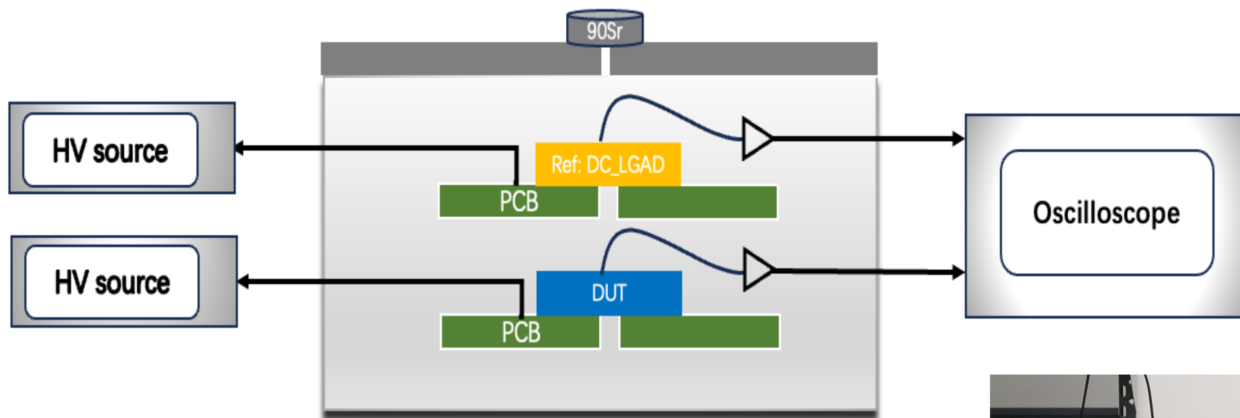




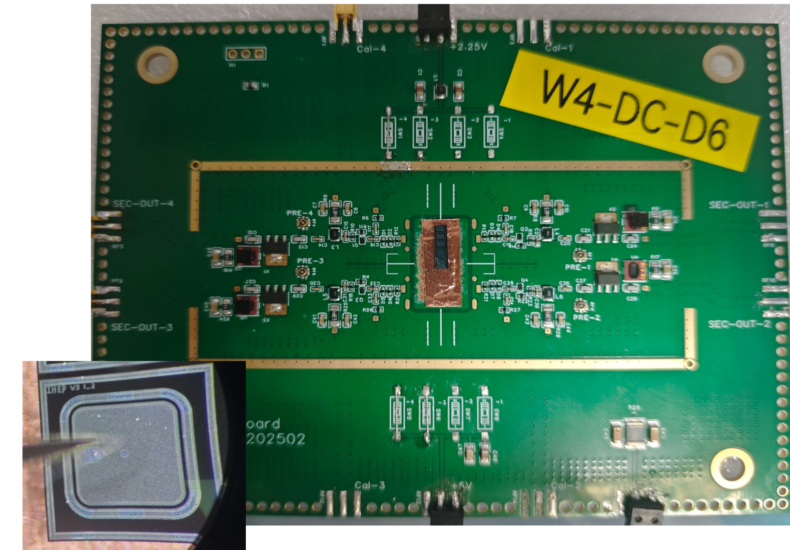


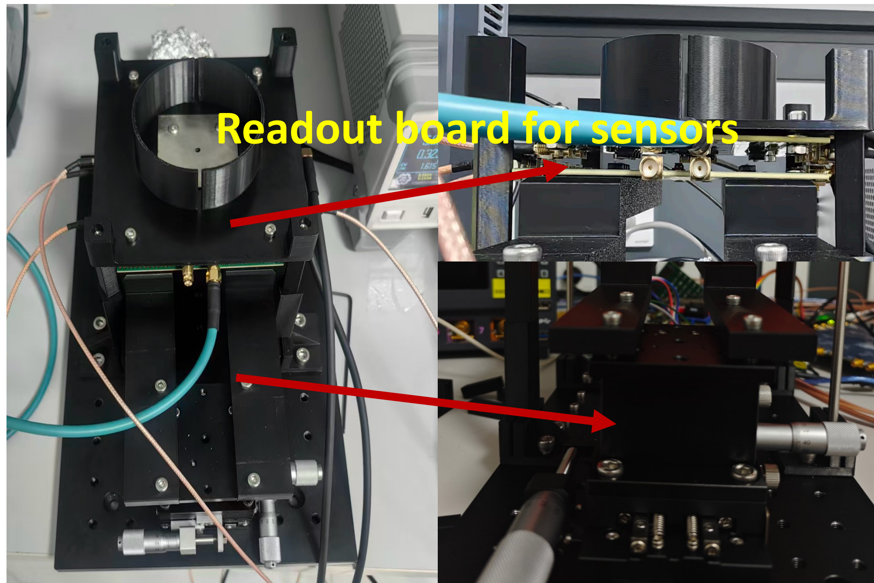
Achieving a spatial resolution below 10 µm using ToT information (LATRIC) with a 100 µm strip pitch appears to be challenging and may offer limited flexibility.

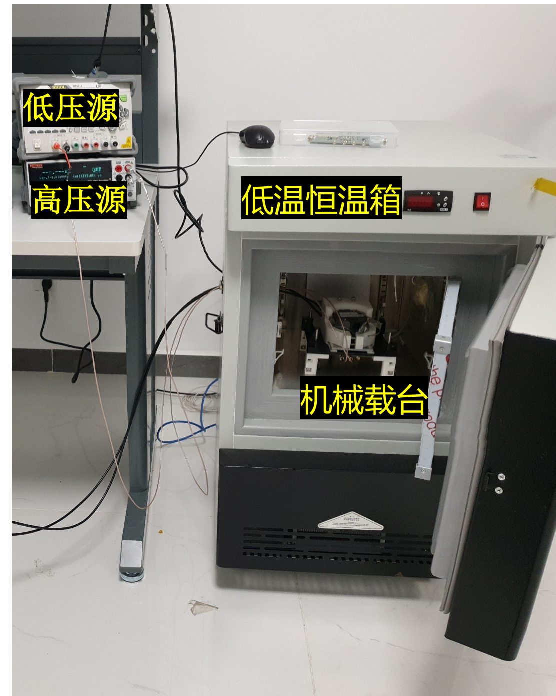
Beta Test for Sensor Timing Resolution

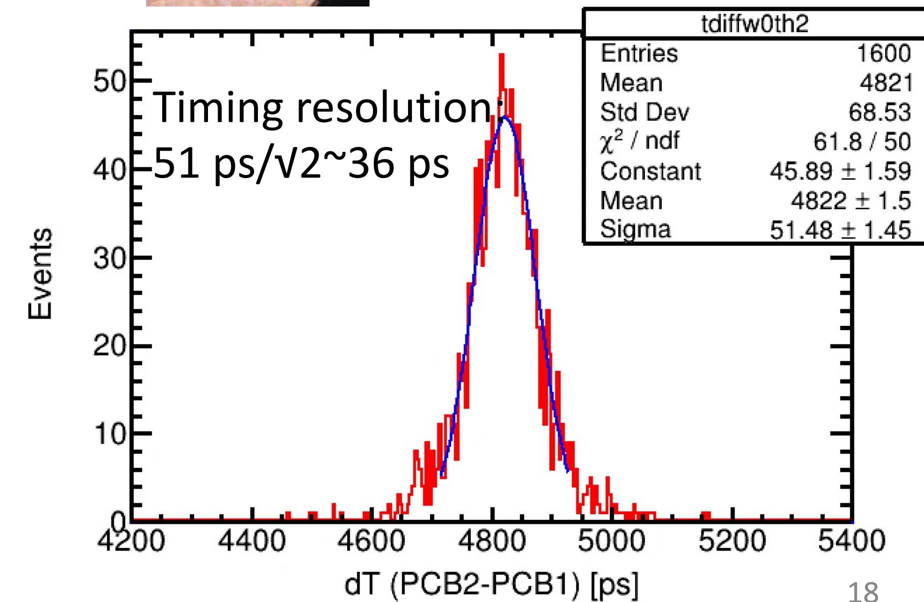


2 DC pads(W4-DC-D6,W4-DC-12):
1.5 mm*1.5mm



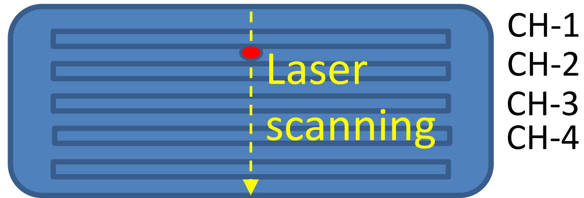


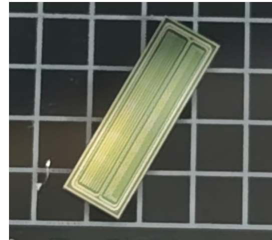


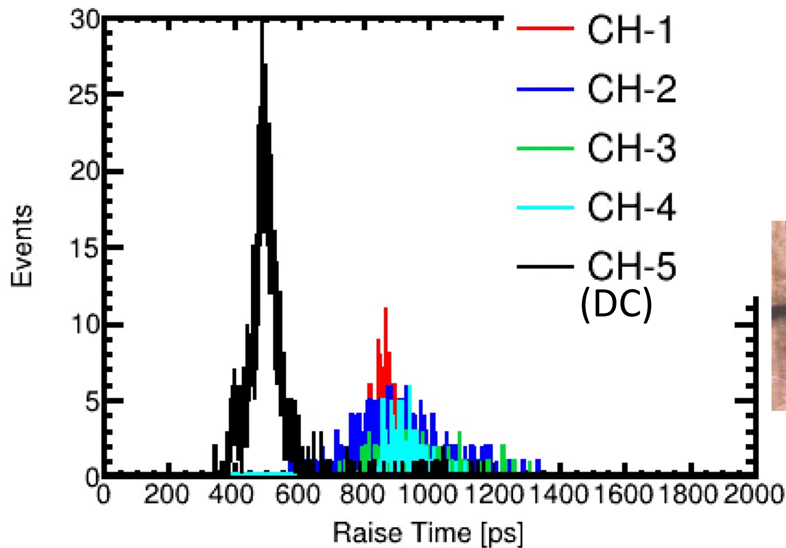


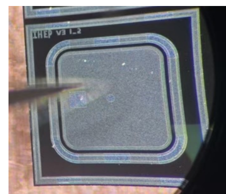
Strip Sensor Timing Resolution

DUT sensor









dT (PCB2-PCB1) [ps]

High Voltage [V]

180, 160, 140, 120, 100, 80, 60, 40

250, 255, 260, 265, 270, 275, 280, 285, 290

Preliminary

CH-3

CH-1

CH-2

Strip Sensor Timing Resolution:
√ (90 90-36*36)~80 ps

The signal rise time of strip sensors is substantially longer than that of pad sensors.

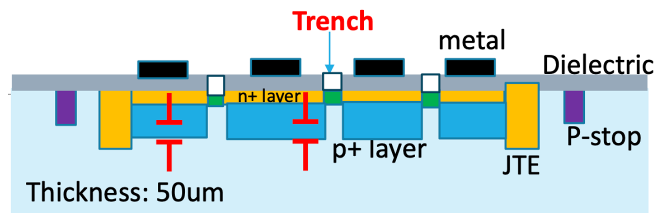
The strip sensor (W4-AC-D9 2, cm) achieved a timing resolution of ~80 ps.

Next LGAD Sensor R&D Plan

Tape out other wafers with different process parameters： 11 wafers in IME

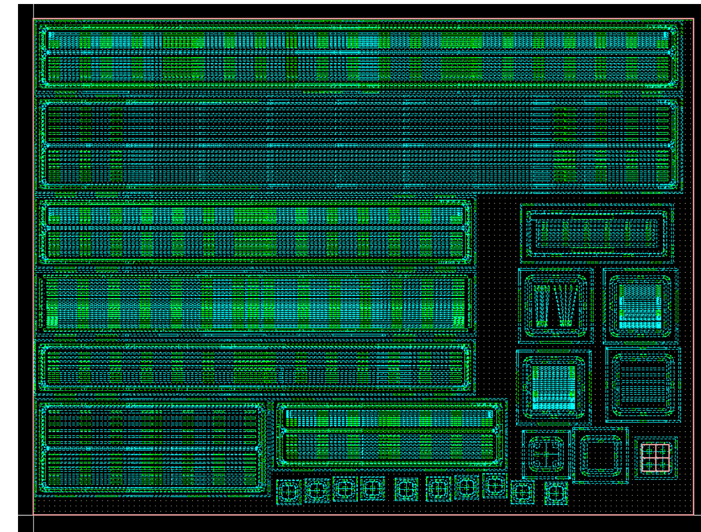
New submission is planed, 2026

- isolated AC-LGAD, isolated DC-LGAD (DC-RSD)



Trenched LGAD

$C = \varepsilon_0 * \varepsilon_r * A\downarrow / d$

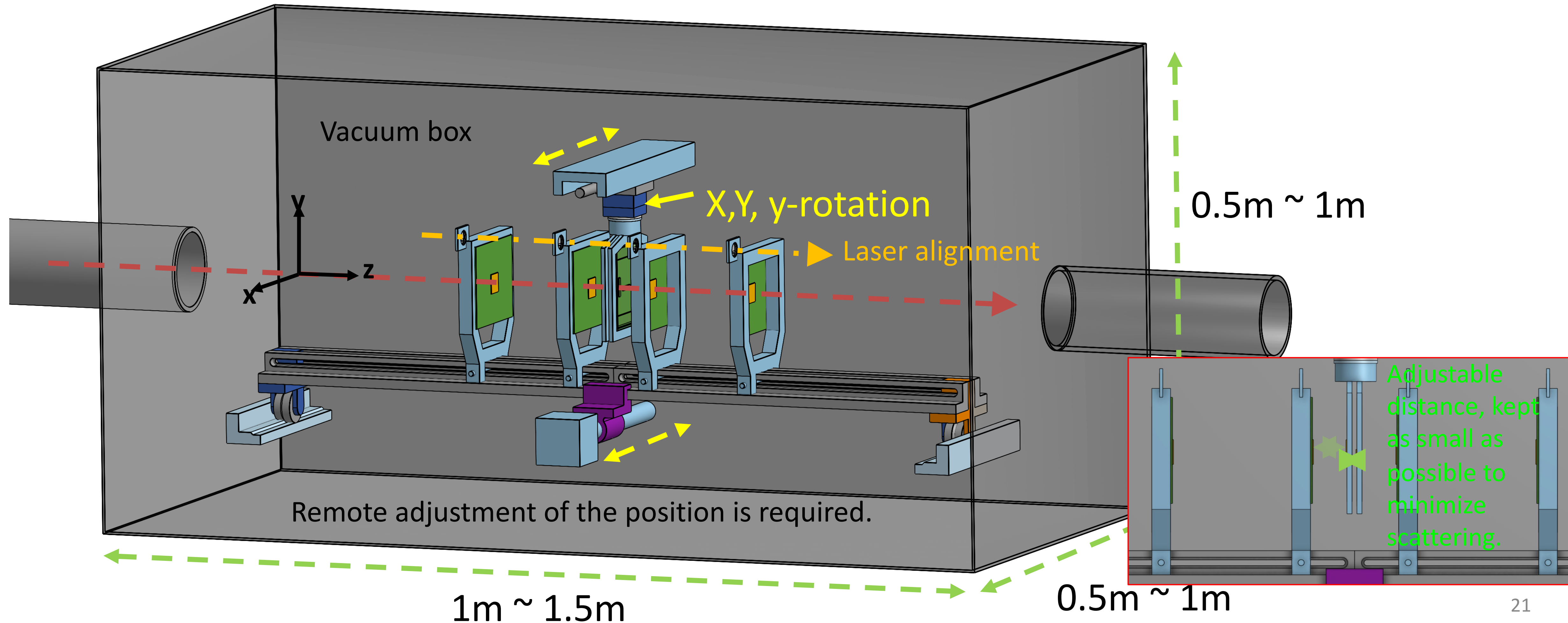


➢ The process and structure simulation, design of LGAD with isolation structure is ongoing

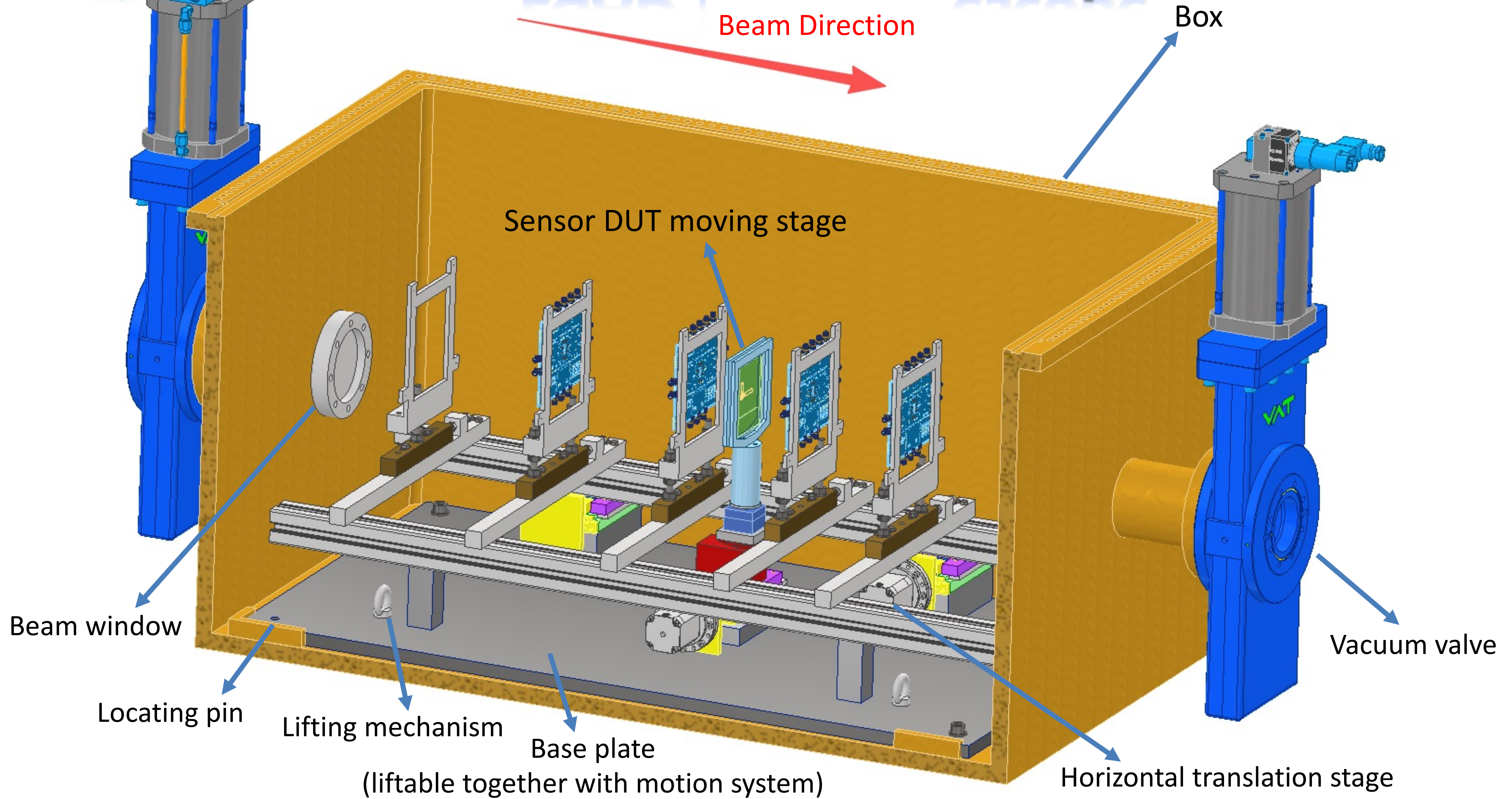
Trench-isolated LGAD: a key step toward final performance, reducing capacitance for large-area, enabling high timing resolution and low-power operation.

Development of the Beam Telescope for BT

A test beam campaign for the next sensor/ASIC validation is planned. The beam telescope design is currently ongoing, with completion planned within 1–2 months. The vacuum valve box is also also under design, and the beam tests are planned to be carried out in China (could be at the PWFA facility at IHEP).

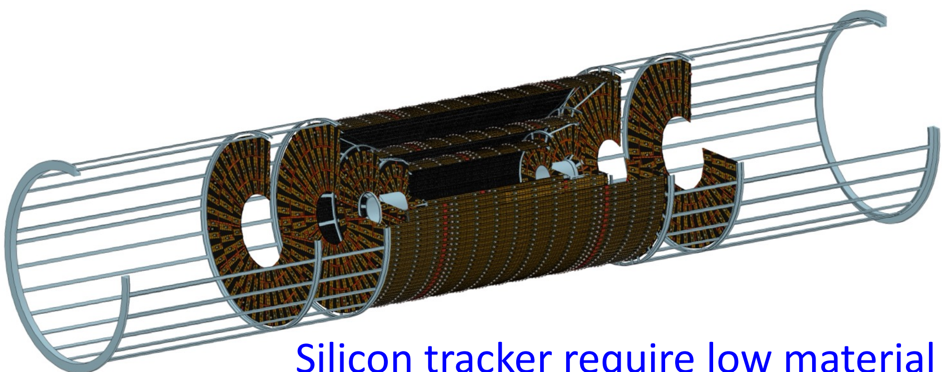


LGAD Beam Telescope



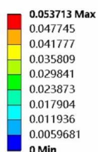
Mechanical Design and Fabrication R&D for Semiconductor Detectors

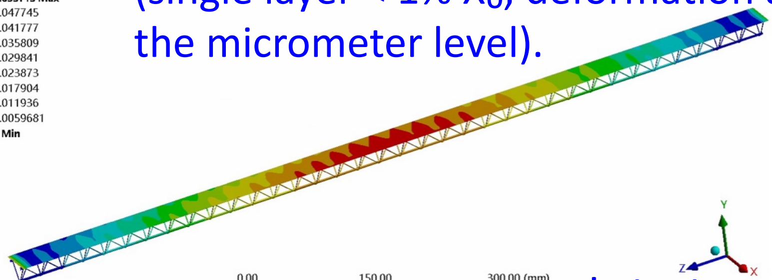
The team conducts research on lightweight carbon-fiber composite structural design, advanced manufacturing processes, thermal management, and cooling integration. The laboratory aims to promote the engineering application of lightweight composite materials and related technologies in semiconductor detectors, providing critical technical support for the development of next-generation particle tracking detectors for high-energy physics experiments.



Silicon tracker require low material budget and minimal deformation (single layer < 1% X_0, deformation at the micrometer level).

D: Static Structural
Total Deformation
Type: Total Deformation
Unit: mm
Time: 1



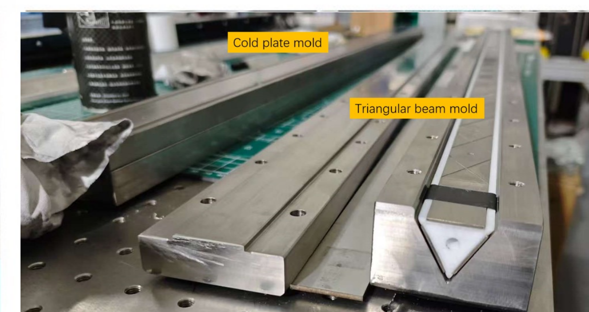


M55J预浸料

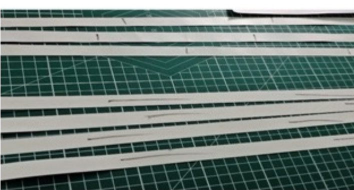
M55J碳纤维丝

碳纤维树脂和脱模剂

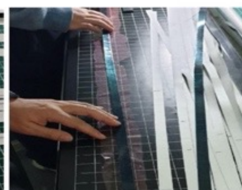
烘箱



设计加工的碳纤维热压磨具



碳纤维预浸料裁剪带



碳纤维预浸料铺层

涂脱模剂

成型样样件

Latest engineering prototypes designed and fabricated by the team

Mechanical Design and Fabrication R&D: Manuscript Under Preparation for Submission

Design, fabrication and mechanical testing of a triangular carbon fiber truss beam for the CEPC inner tracker

X.H. Qian*, J. Wang, Y.J. Li, J.J. Zhang, Q. Yan, G. Li, X.P. Jing, X.Y. Ma, S. Xia, Z. Liu, W. He, J.Y. Fu, S.J. Hou

Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China

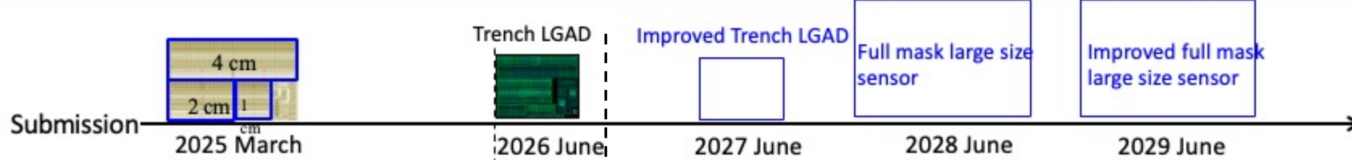
*Corresponding author.

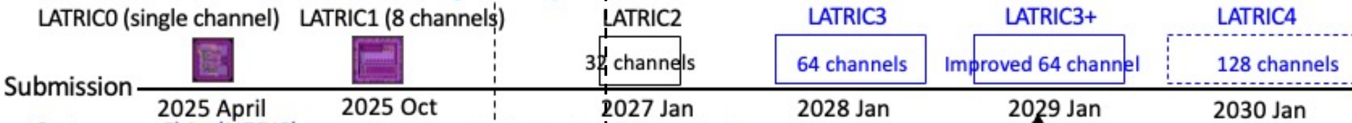
Abstract

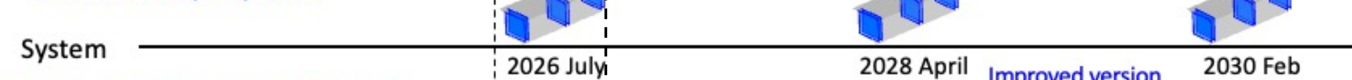
The inner tracker (ITK) of the Circular Electron Positron Collider (CEPC) imposes stringent requirements on mechanical support structures: extremely low material budget, high stiffness, and long-term stability under radiation. This paper presents the complete development of a 1000 mm long triangular-section carbon fiber reinforced polymer (CFRP) truss beam for the CEPC-ITK, covering structural design, finite element analysis (FEA), mold design and optimization, fabrication process development, and static mechanical testing. The truss beam consists of three longitudinal main beams made of M40J high-modulus carbon fiber prepreg (layup [0/0/0/90/0/0/0], 7 plies, 0.4 mm thick) and helical secondary beams made of T700 carbon fiber tows (12K, continuous winding). A continuous fiber winding process was developed to overcome the insufficient node bonding strength encountered with the segmented bonding approach; the total winding fiber length is approximately 7 m. The fabricated 1000 mm beams weigh approximately 15 g, corresponding to a linear density of ~15 g/m. Static mechanical tests show a deflection of 37.25 ± 0.96 μm under a 50 g concentrated load with fixed support, with the FEA prediction deviating by only 2.6%. Under a uniformly distributed load of 80 g (simulating the real sensor weight), the deformation is approximately 20 μm. The good agreement between FEA results and measurements under two distinct boundary conditions validates the design methodology and fabrication process. This study provides key verification for the engineering design of lightweight support structures for the CEPC-ITK.

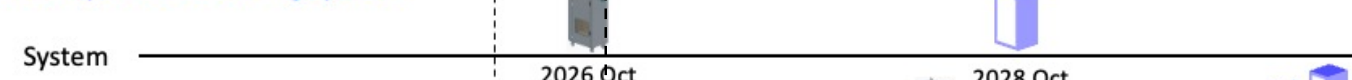
Keywords: CEPC; Inner tracker; Carbon fiber reinforced polymer; Triangular truss beam; Finite element analysis; Lightweight support structure

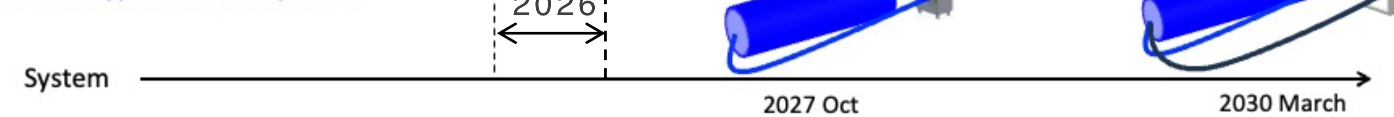
Plan and Others





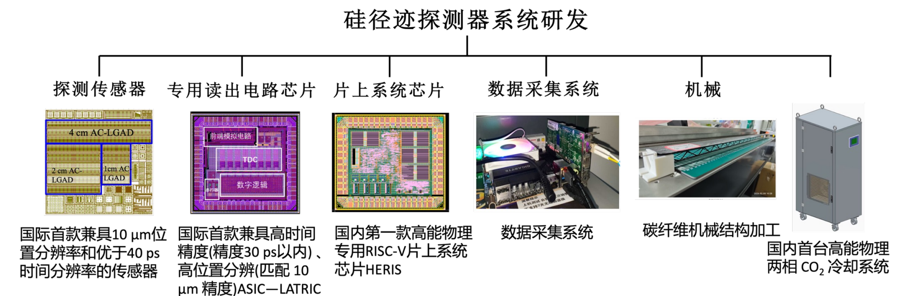






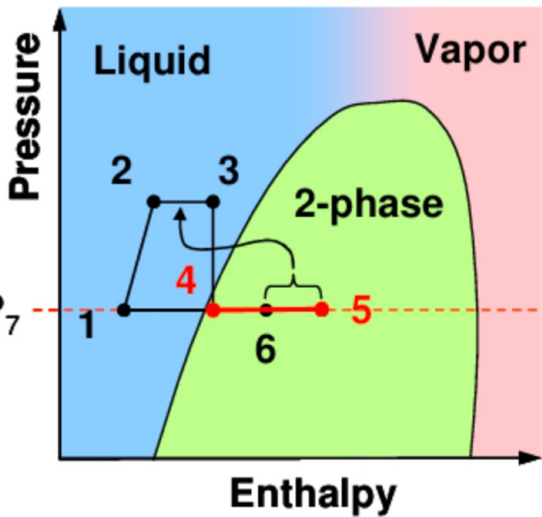
2026 plan: tape-out of trenched LGAD, development of LATRIC2 readout ASIC (32 channels), R&D of HERIS-V2 SoC; beam telescope construction and beam test, and development of two-phase CO_2 cooling system with full system integration tests.

- Team funding support: None; personnel talent program funding only.
- The project aims at engineering-oriented research with a strong focus on silicon tracker development. It establishes an integrated R&D framework covering sensors, dedicated readout electronics, and mechanical and cooling systems.

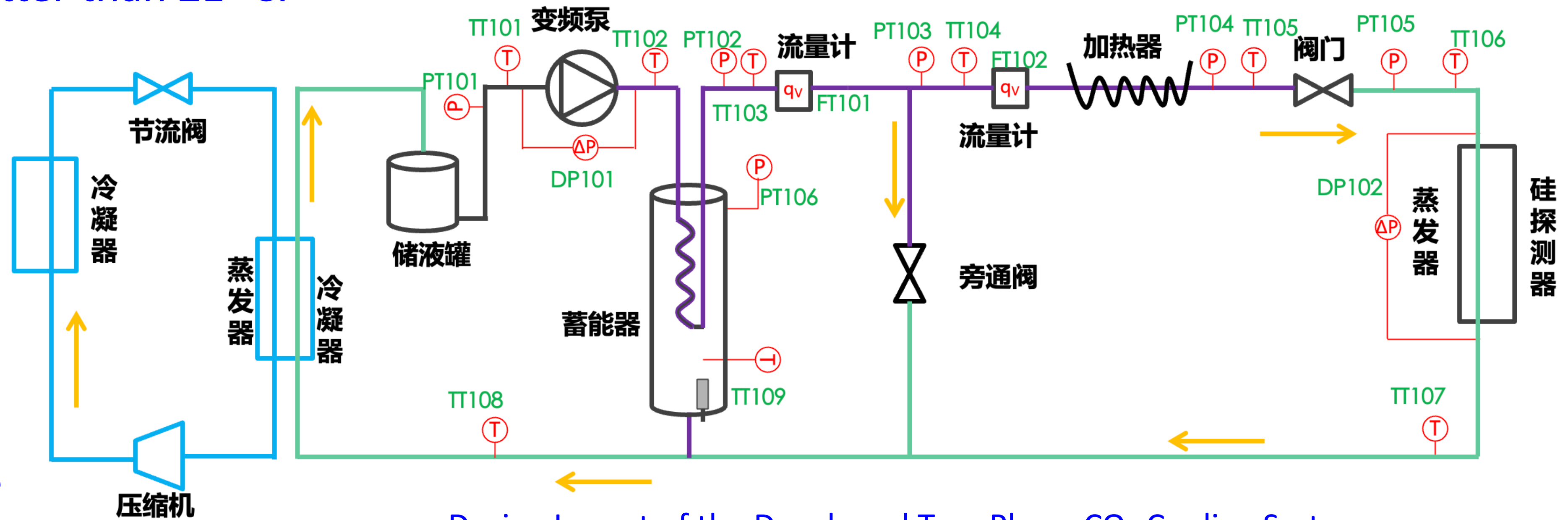


Development of Two-Phase CO_2 Cooling System

We are developing the first two-phase CO_2 cooling system together with TIPC. The integrated system is going be completed in October 2026. The system features a compact and portable design, with a nominal heat load capacity of ~1.2 kW (upgradeable to >2 kW), an operating temperature range from –40 °C to 20 °C, and a temperature stability better than ±1 °C.



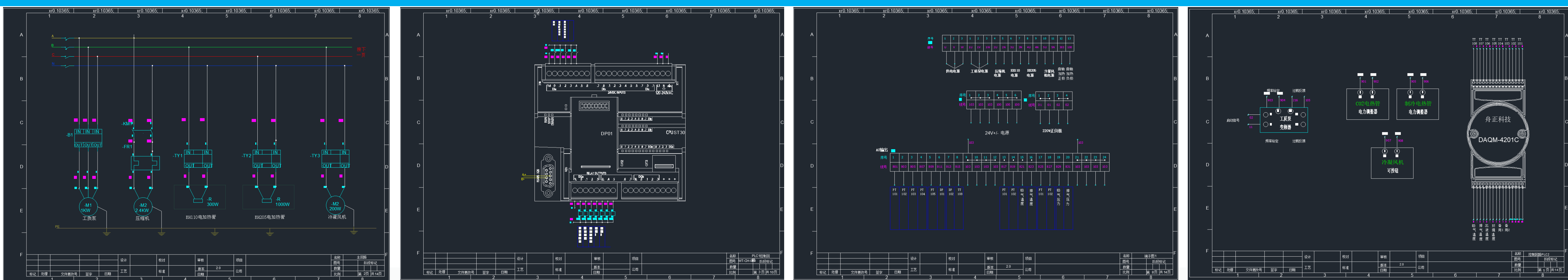
P–h Diagram of the Two-Phase CO_2 Cooling System



Design Layout of the Developed Two-Phase CO_2 Cooling System

The system can be integrated with a variety of thermal load systems, making it suitable for different experimental setups and application requirements. The system features a compact layout with a total weight of approximately 100 kg. It also provides a scalable platform for the development of larger cooling systems.

Design of the CO_2 Cooling System



- System electrical schematic
- System design layout

Compressor

Plate heat exchanger

Expansion valve driver

Filter (R404A)

Sight glass (R404A)

Oil separator

Electronic expansion valve (EEV) driver

Temperature sensor

Cartridge heater

Pressure sensor

Filter (CO_2)

Differential pressure sensor

Flow meter

Refrigerant sight glass for CO_2

Integration of the complete system is ongoing and is scheduled to be completed before October 2026.

高精度皮秒激光TCT测试系统

皮秒激光器

50%

保偏分束器

50%

减光片和聚焦系统

光电二极管

被测器件

AC-LGAD or AC-LGAD+LATRIC

PCB

触发

示波器

被测传感器

激光扫描线

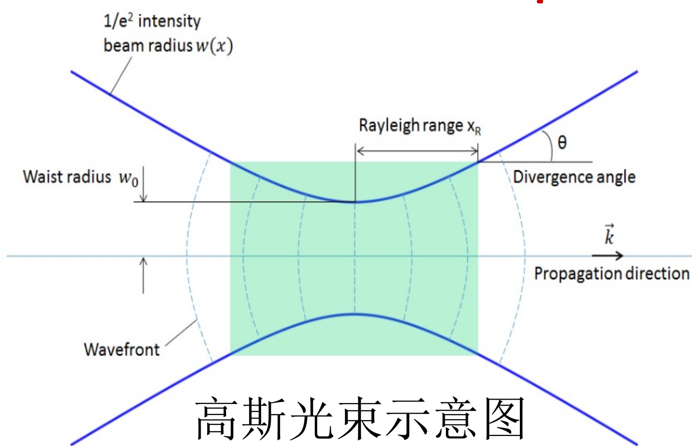
数据分析

为实现度位置分辨率和时间分辨率的高精度表征，**激光光斑需聚焦至微米尺度，要求Z轴以微米精度对焦至焦平面：**

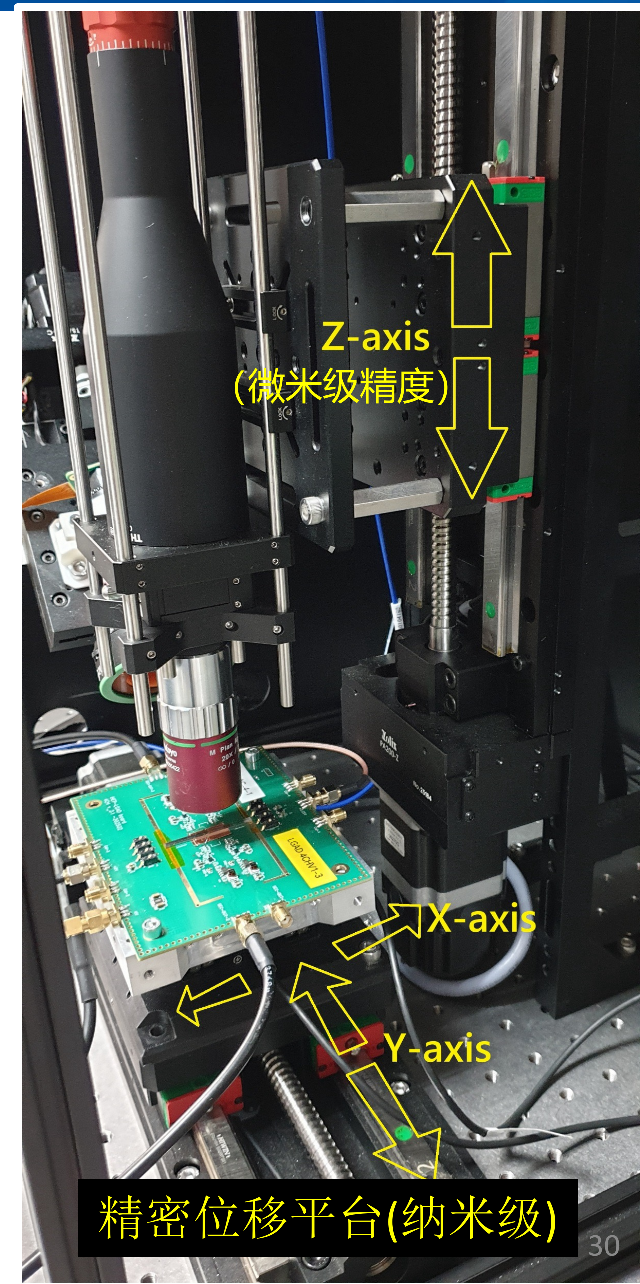
- 实验平台采用Mitutoyo 20X扩束镜（焦距f=10mm、数字孔径N_A=0.42mm）对1064nm激光进行聚焦。根据光学理论，物镜入瞳直径D=2*N_A*f=8.4mm, 对应高斯光束腰部直径

$$\approx \frac{4\lambda f}{\pi D} = \frac{4*1.065\mu m*10mm}{\pi*8.4mm} = 1.62\mu m$$

- 考虑艾里效应，实际光斑约为高斯光束腰部直径两倍，**光斑理论最小值~3.24μm**



高斯光束示意图



精密位移平台(纳米级)