ALICE

课题三：ALICE探测器升级

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课题承担单位：华中师范大学
课题参与单位：中国原子能科学研究院

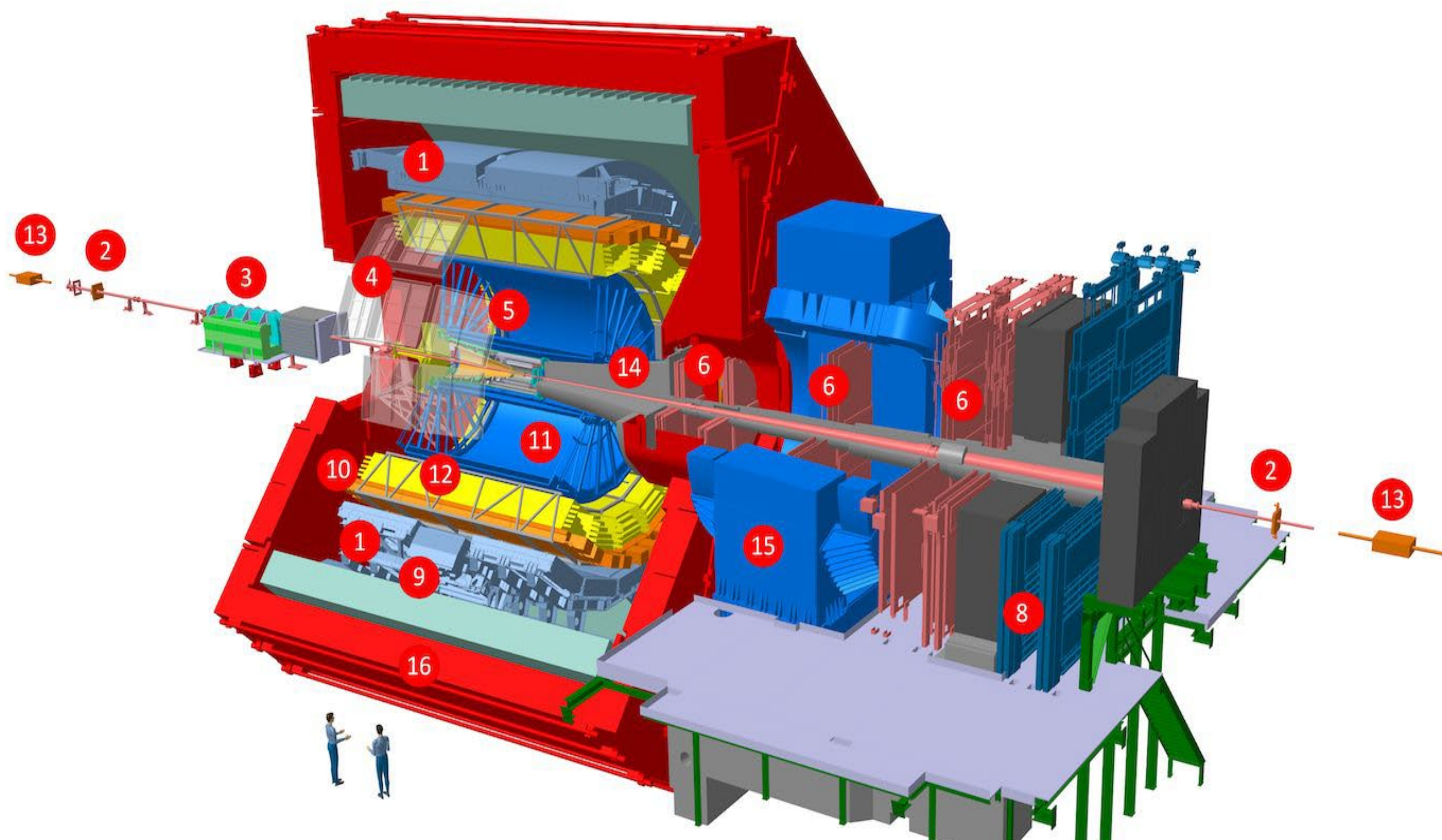
汇报内容

- 研究内容、考核指标、研究进度
- 课题研究的主要进展
  - ITS3硅像素芯片
  - FoCal硅像素层
  - FoCal读出电子学系统（见客守龙的报告）
- 存在的问题
- 总结

升级后的ALICE探测器（~~2029~~2030年）

ALICE

LS3 （~~2026-2028~~）期间
2026.7-2030.6



1 **EMCAL |** Electromagnetic Calorimeter

2 **FIT |** Fast Interaction Trigger

3 **FoCal |** Forward Calorimeter　　新增

4 **HMPID|** High Momentum Particle Identification Detector

5 **ITS|** Inner Tracking System　　更新

6 **MCH|** Muon Tracking Chambers

7 **MFT|** Muon Forward Tracker

8 **MID|** Muon Identifier

9 **PHOS/CPV|** Photon Spectrometer

10 **TOF|** Time Of Flight

11 **TPC|** Time Projection Chamber

12 **TRD|** Transition Radiation Detector

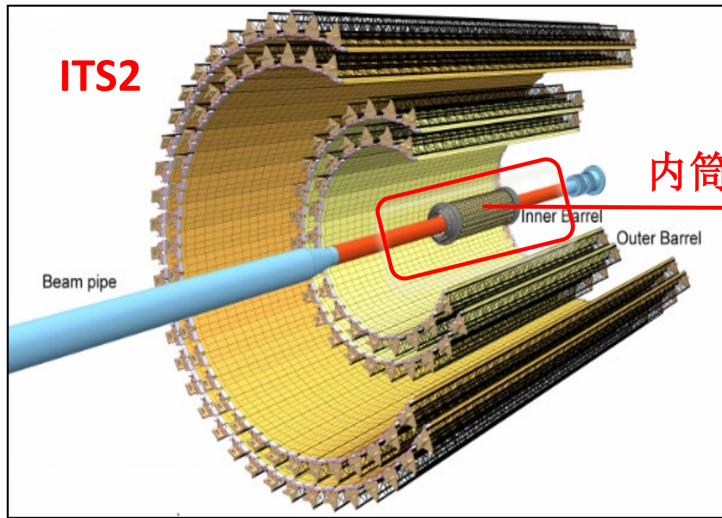
13 **ZDC|** Zero Degree Calorimeter

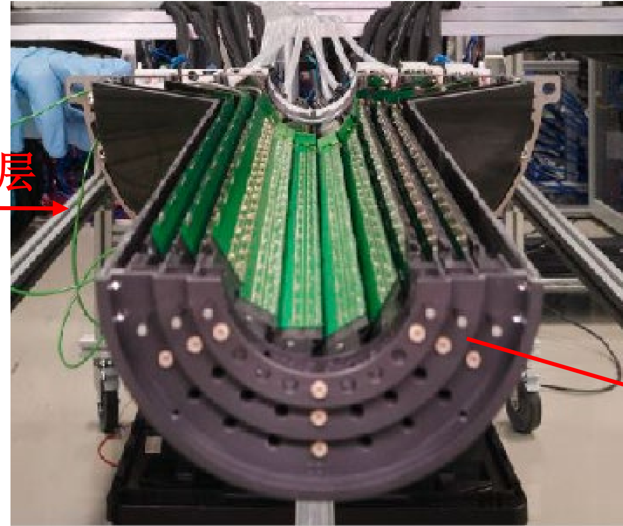
14 **Absorber**

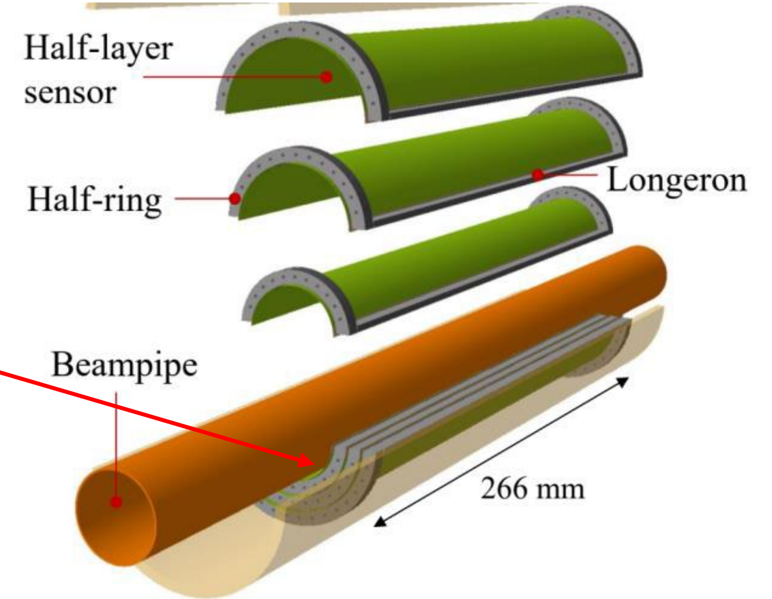
15 **Dipole Magnet**

16 **L3 Magnet**

ITS3







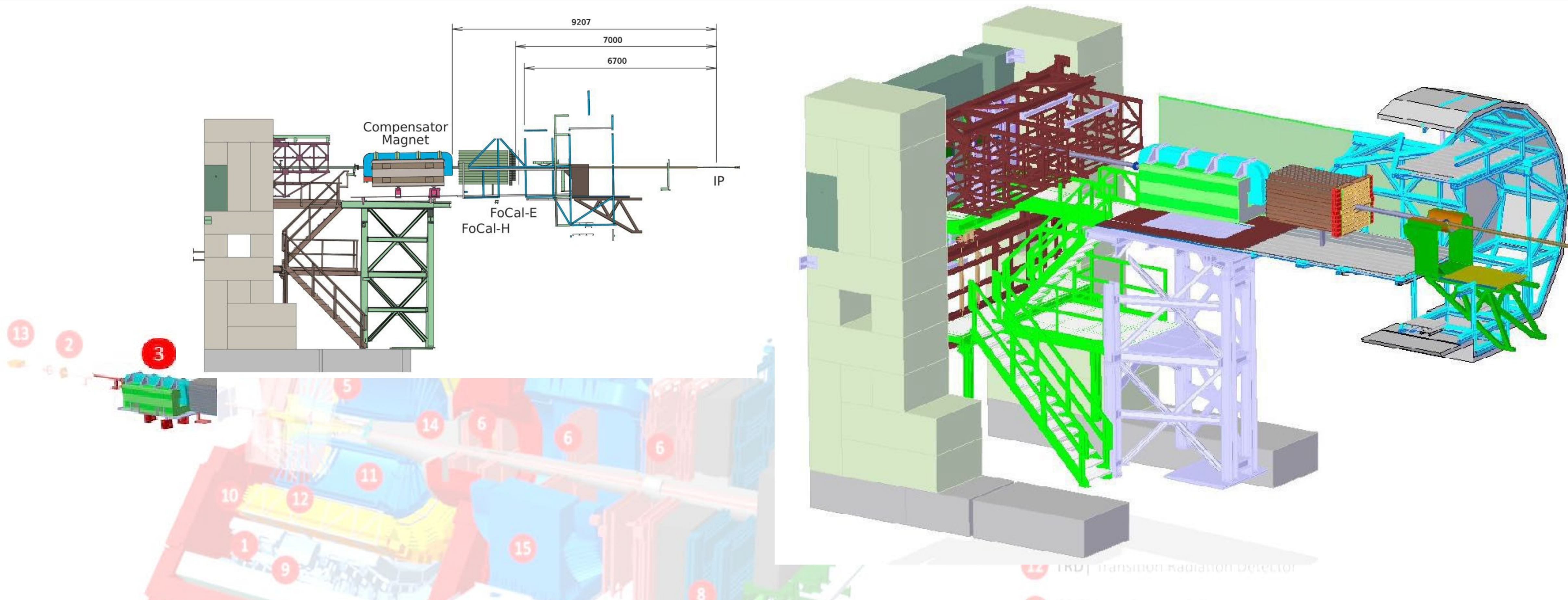
	ITS2	ITS3
到碰撞点的径向距离 （mm）	22	19
最内层辐射长度（%X_0）	~0.35	~0.09
像素大小 （μm²）	30×30	*O*(~~15×15~~22.8 ×20.8)
芯片大小 （cm²）	1.5×3.0	O(90×280)
芯片厚度 （μm）	50	50

整个探测器由6片大面积超薄传感器芯片组成

- 非常小的探测器材料辐射长度
- 非常均匀的材料分布，减小系统误差
- 更细的束流管，探测器最内层半径更小

- 会极大地提升在重离子碰撞中测量低横动量粲强子和底强子以及低质量双电子的能力

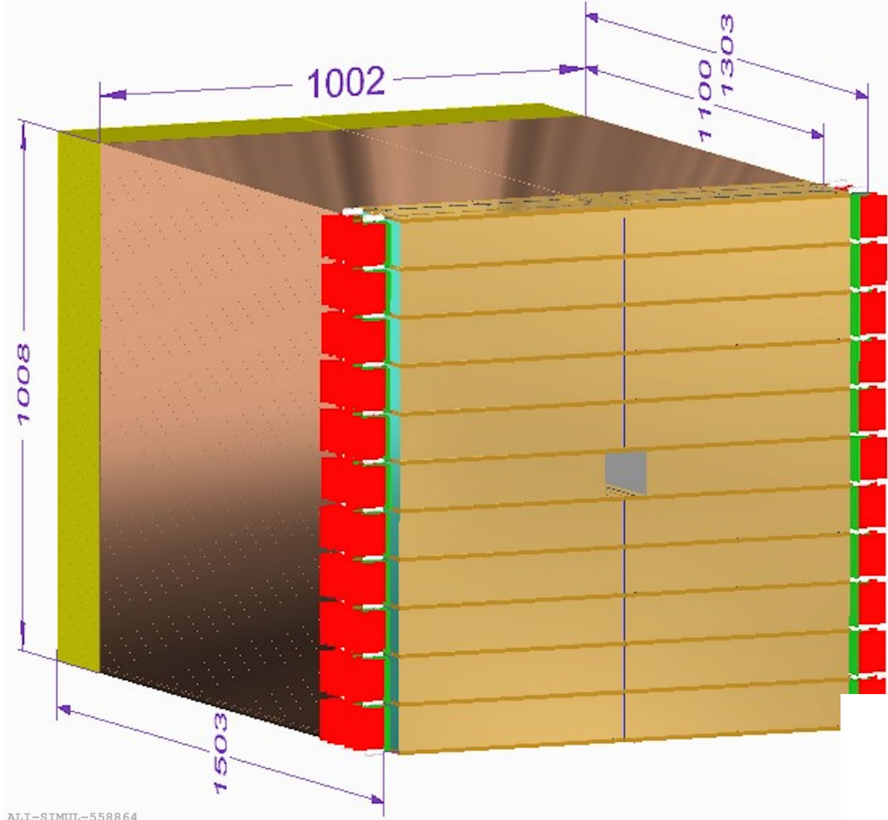
Forward Calorimeter (FoCal)



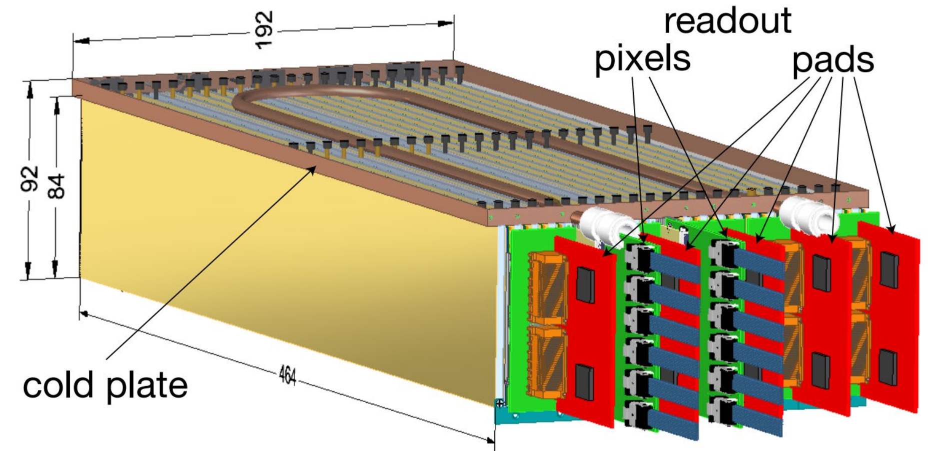
- 离碰撞点的距离为7米
- 覆盖赝快度：3.4 - 5.8

- 小 x 物理

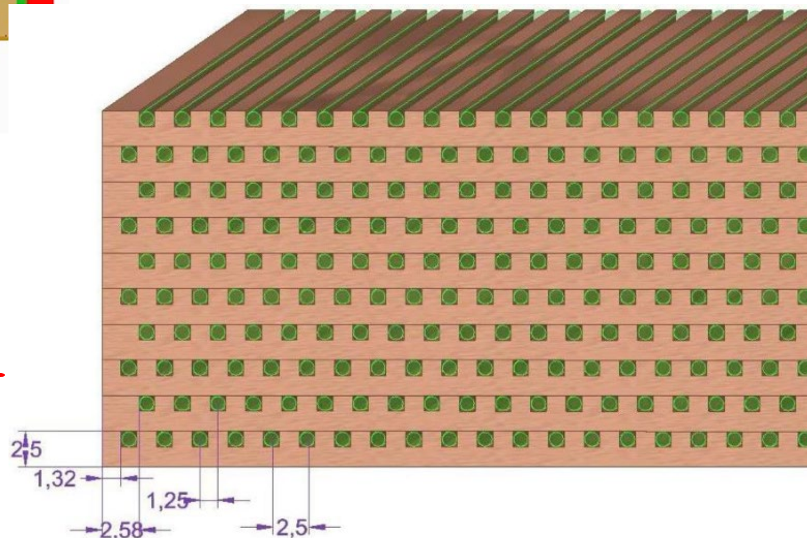
FoCal探测器的构造



- FoCal-E: 18层粒度为1×1 cm²硅片+2层硅像素层取样型**电磁量能器**



共含22个FoCal-E模块



- FoCal-H: 铜质沟槽板+闪烁光纤意大利面型**强子量能器**

- Hamamatsu S14160 SiPM (6 mm × 6 mm) 读出
- 每个SiPM对应16根（1.6 cm × 1.6 cm）

课题研究内容

ALICE

- 合作研发晶圆尺寸的超薄硅像素芯片
  - 与CERN合作，利用拼接缝合技术，研发晶圆尺寸的超薄硅像素芯片
  - 参与芯片设计、模拟验证和测试等工作
- FoCal探测器的硅像素层研制
  - 与挪威卑尔根大学等单位合作，研制出FoCal探测器的硅像素层及其读出电子学系统
  - 参与束流测试，研究硅像素层模块的性能
  - 通过探测器模拟，优化FoCal的构造和像素层的位置
  - 设计开发探测器读出单元，结合系统模拟，优化固件架构设计，提高探测器性能
  - 基于束流测试结果，优化MC模拟参数，研究探测器物理性能，建立分析框架

考核指标

课题目标[1]	预期成果				考核指标[2]				考核方式（方法）及评价手段[4]
	预期成果名称			预期成果类型	指标名称	立项时已有指标值/状态	中期指标值/状态[3]	完成时指标值/状态	
（限 500 字以内。） 参与研发用于 ALICE 第三代硅像素探测器的晶圆尺寸硅像素芯片，掌握其研发关键技术；完成 FoCal 探测器的硅像素层的研制任务，掌握研制基于硅像素芯片的高粒度量能器及其读出电子学的关键技术。发表论文 1-2 篇；培养研究生 2-3 名。	主要成果	1	合作研发出大面积硅像素芯片	☐新理论 ☐新原理 ☐新产品 ☐新技术 ☐新方法 ■关键部件 ☐数据库 ☐软件 ☐应用解决方案 ☐实验装置/系统 ☐临床指南/规范 ☐工程工艺 ☐标准 ☐论文 ☐发明专利 ☐其他______	指标 1.1 芯片技术指标-面积、功耗等	无	芯片面积达 90 mm x 140 mm	芯片面积达 90 mm×140 mm，像素大小约 15 um×15 um，功耗低至 20 mW/cm^2	合作组安排测试，提供测试结果
		2	合作研制出 FoCal 硅像素层模块及其读出电路板	☐新理论 ☐新原理 ☐新产品 ☐新技术 ☐新方法 ■关键部件 ☐数据库 ☐软件 ☐应用解决方案 ■实验装置/系统 ☐临床指南/规范 ☐工程工艺 ☐标准 ☐论文 ☐发明专利 ☐其他______	指标 2.1 FoCal 技术指标-位置分辨本领	～10 mm	样机位置分辨率～5 mm	～5 mm	合作组安排测试，提供测试结果
	其他成果								

进度安排

任务名称

2022-10-01 Q4 | 2023-01-01 Q1 Q2 Q3 Q4 | 2024-01-01 Q1 Q2 Q3 Q4 | 2025-01-01 Q1 Q2 Q3 Q4 | 2026-01-01 Q1 Q2 Q3 Q4 | 2027-01-01 Q1 Q2 Q3

- 1) 大面积硅像素芯片研发
  - 模拟、数字功能芯片验证
  - 工程批1期（ER1）设计、模拟验证与提交
  - ER1单片缝合芯片流片
  - ER1单片缝合芯片性能测试
  - 工程批2期(ER2)全尺寸传感器芯片设计、模拟验证和提交
  - ER2全尺寸传感器芯片性能测试
  - 工程批3 (ER 3)期全功能晶圆尺寸传感器芯片设计和模拟验证
  - ER3全功能晶圆尺寸传感器芯片测试
  - 晶圆尺寸超薄硅像素芯片工程版定型
- 2) FoCal探测器硅像素层研制
  - 研制FPC、研制工装夹具
  - 研制HIC和String模块样机
  - 研制硅像素层样机
  - 硅像素层模块预生产
  - 束流测试
  - 硅像素层模块定型
  - 硅像素层模块量产
  - FoCal探测器安装和调试

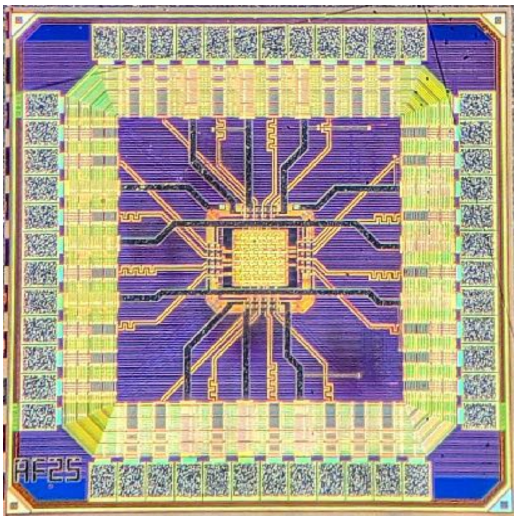
- 模拟、数字功能验证（√）
- ER1单片缝合芯片流片 （√）
- ER1单片缝合芯片性能测试（√）
- ER2全尺寸芯片设计、模拟验证和提交（√）
- ER2全尺寸芯片性能测试（进行中）

- 研制FPC（√）、研制工装夹具（√）
- 研制String模块样机（√）
- 研制硅像素层模块样机（√）
- 参与样机束流测试（√）
- FoCal硅像素层模块量产（准备中）

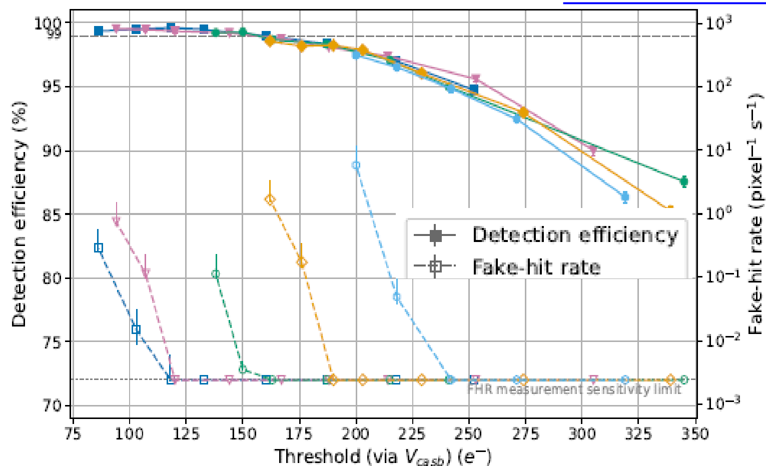
ITS3芯片研发：模拟、数字功能验证

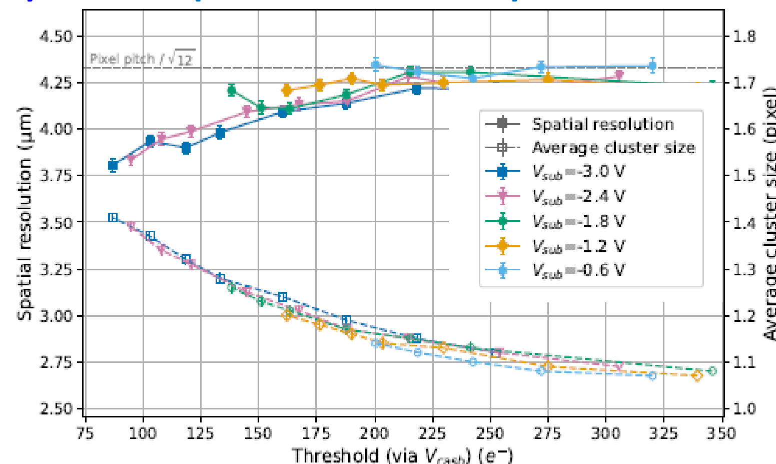
NIMA 1056 (2023) 168589 (arXiv:2212.08621)

APTS



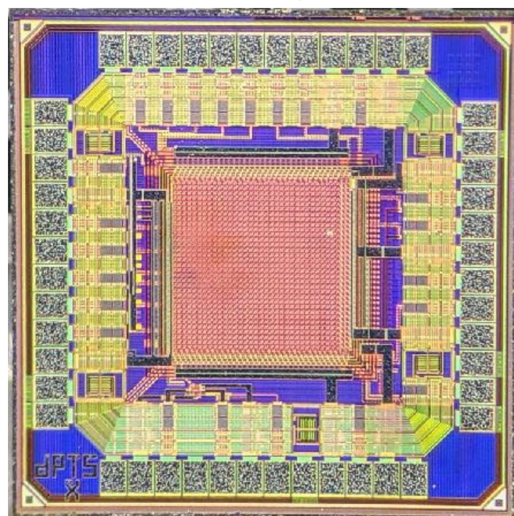
Matrix: 6x6 pixels
Readout: direct analog readout of central 4x4
Pitch: 10, 15, 20, 25 µm
Total: 34 dies



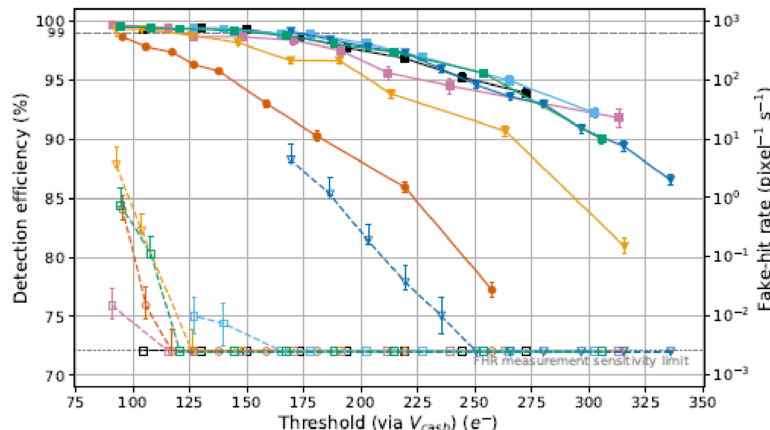


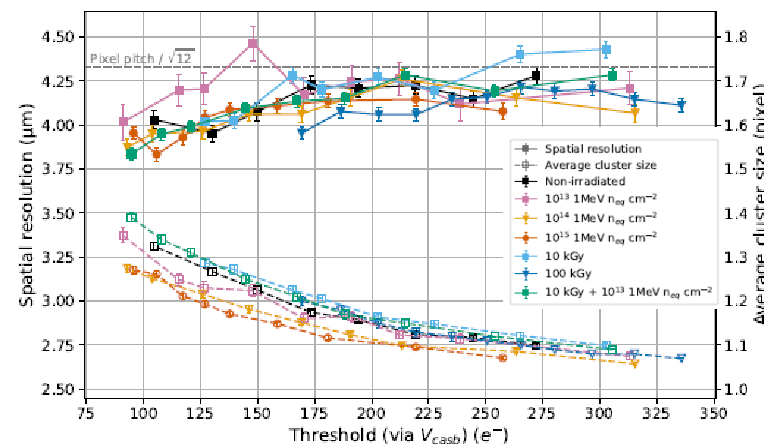
Sensor irradiated to a dose of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} at different $V_{sub} = V_{pwell}$.

DPTS



Matrix: 32x32 pixels
Readout: async. digital with ToT
Pitch: 15 µm
Total: 3 dies

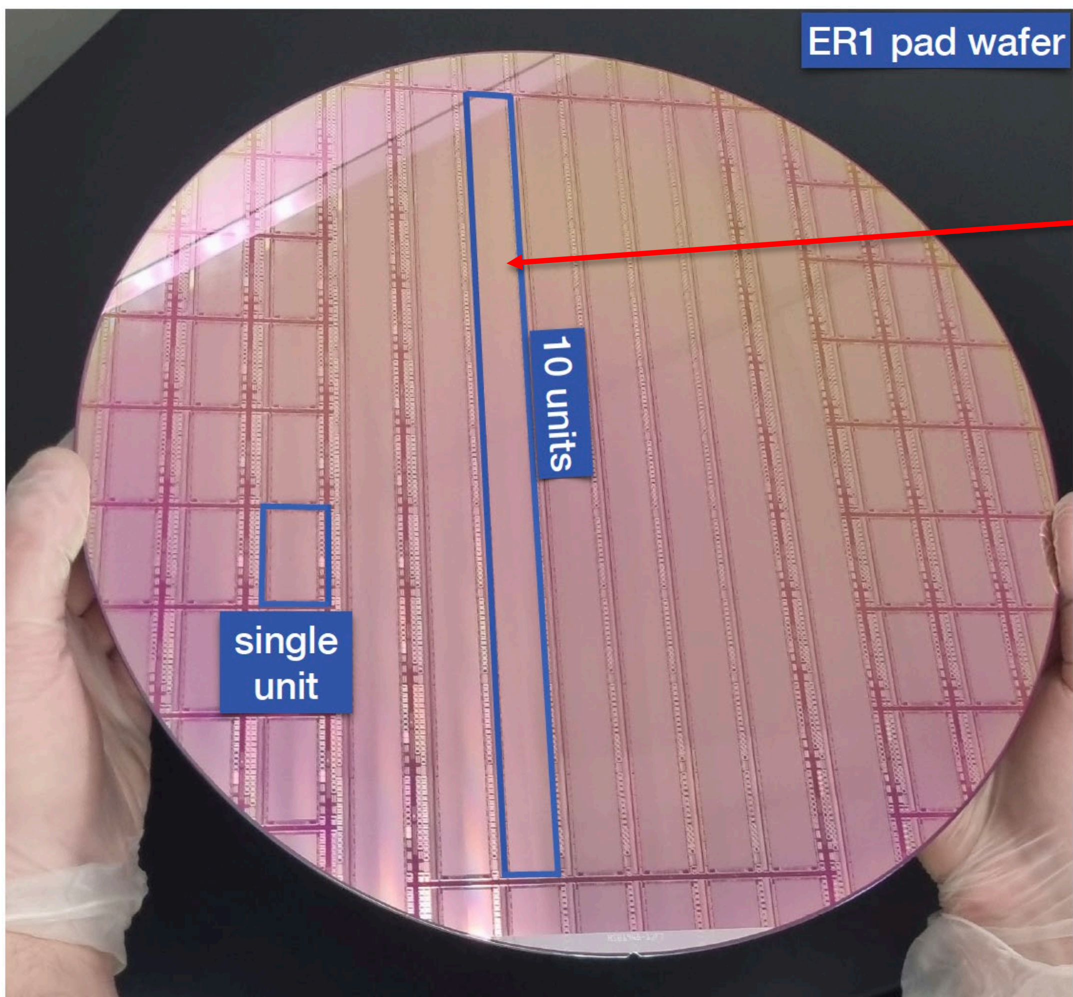


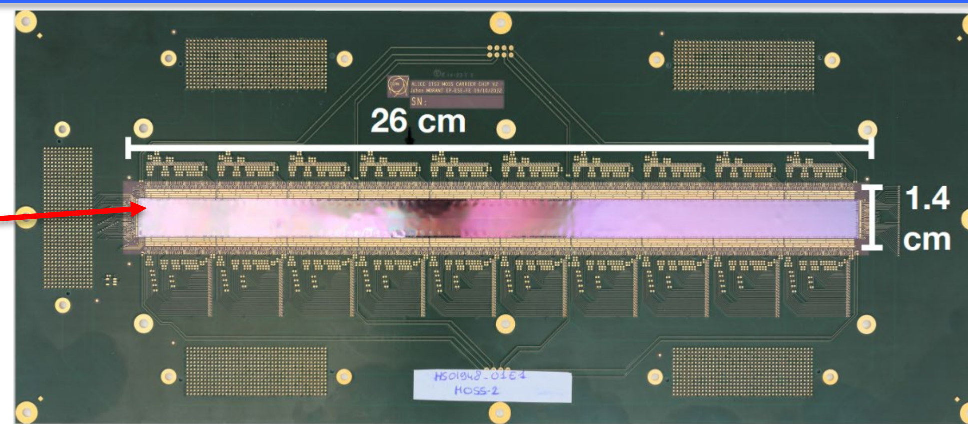


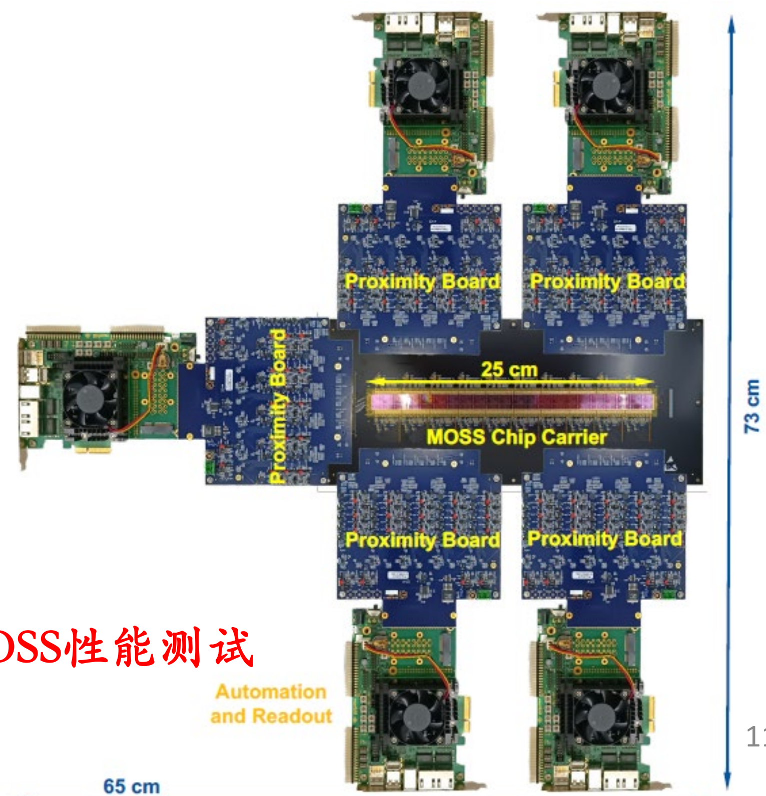
Sensors irradiated to different levels.

验证了基于65 nm工艺生产的芯片的探测器效率、位置分辨、抗辐照本领等性能指标满足ITS3要求

ER1单片缝合芯片MOSS性能测试





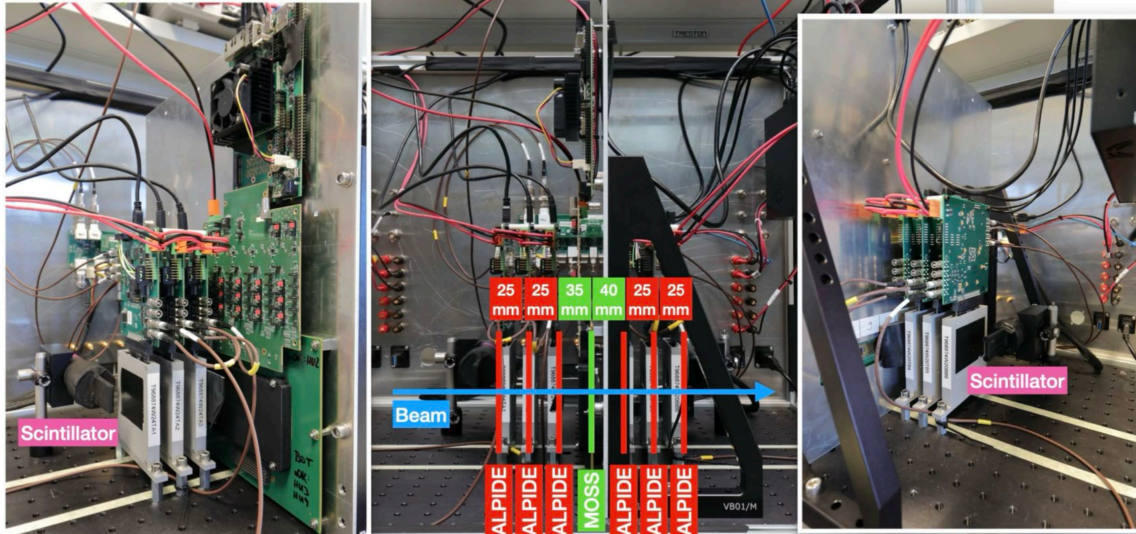


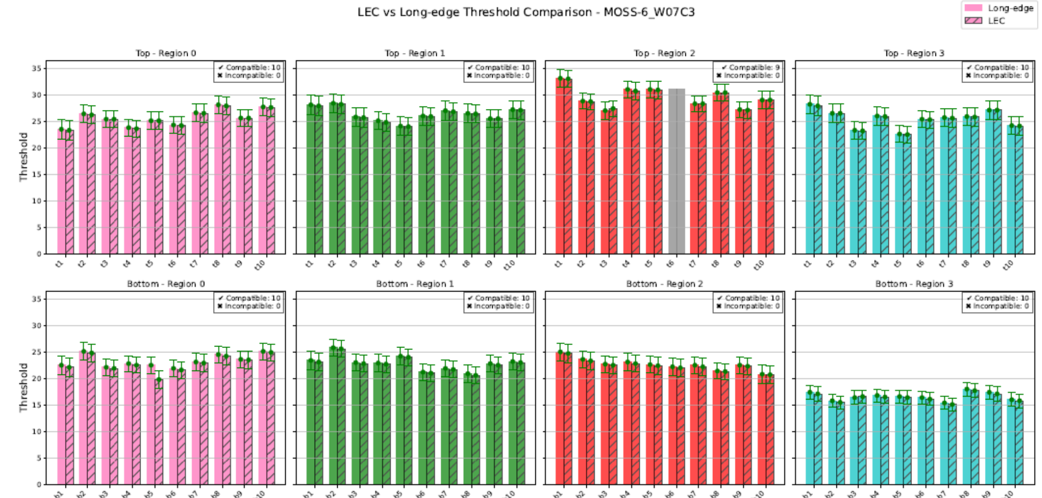
邓文静参与MOSS芯片的设计

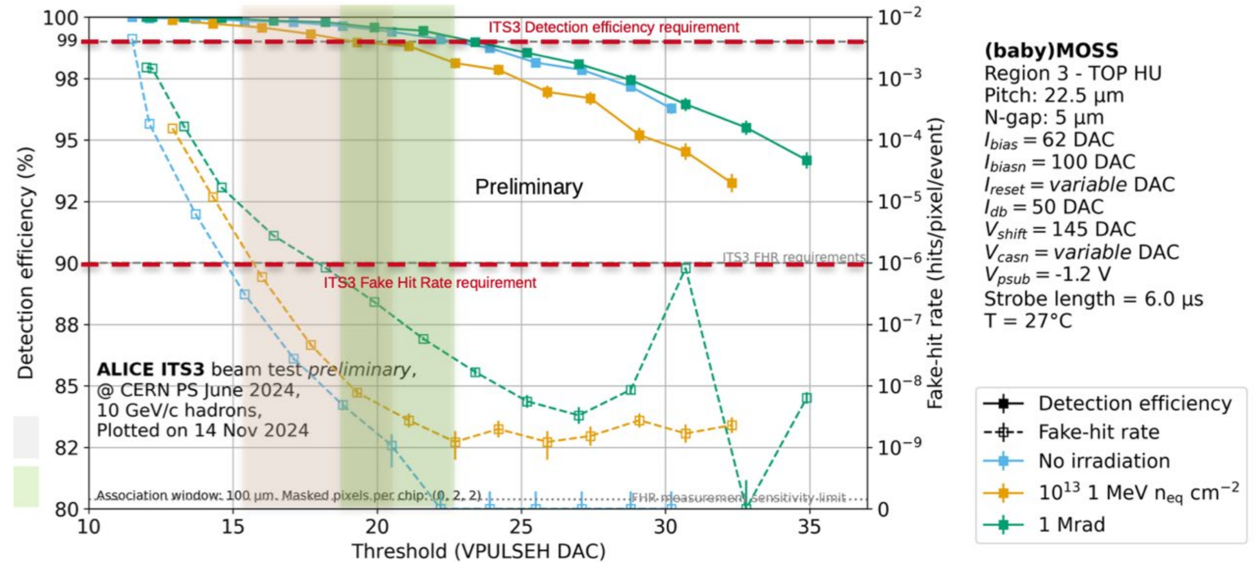
王淳正、赵子俊参与MOSS性能测试

MOSS芯片性能测试

- 实验室测试
  - ✓ 阻抗测试
  - ✓ 逐步上电-稳定性测试
  - ✓ 阻抗再测量
  - ✓ 成套功能测试
    - 供电，寄存器，位移寄存器，数模转换器，阈值和假击中率扫描
- 束流测试
  - ✓ 探测效率
  - ✓ 位置分辨率
  - ✓ 抗辐照能力

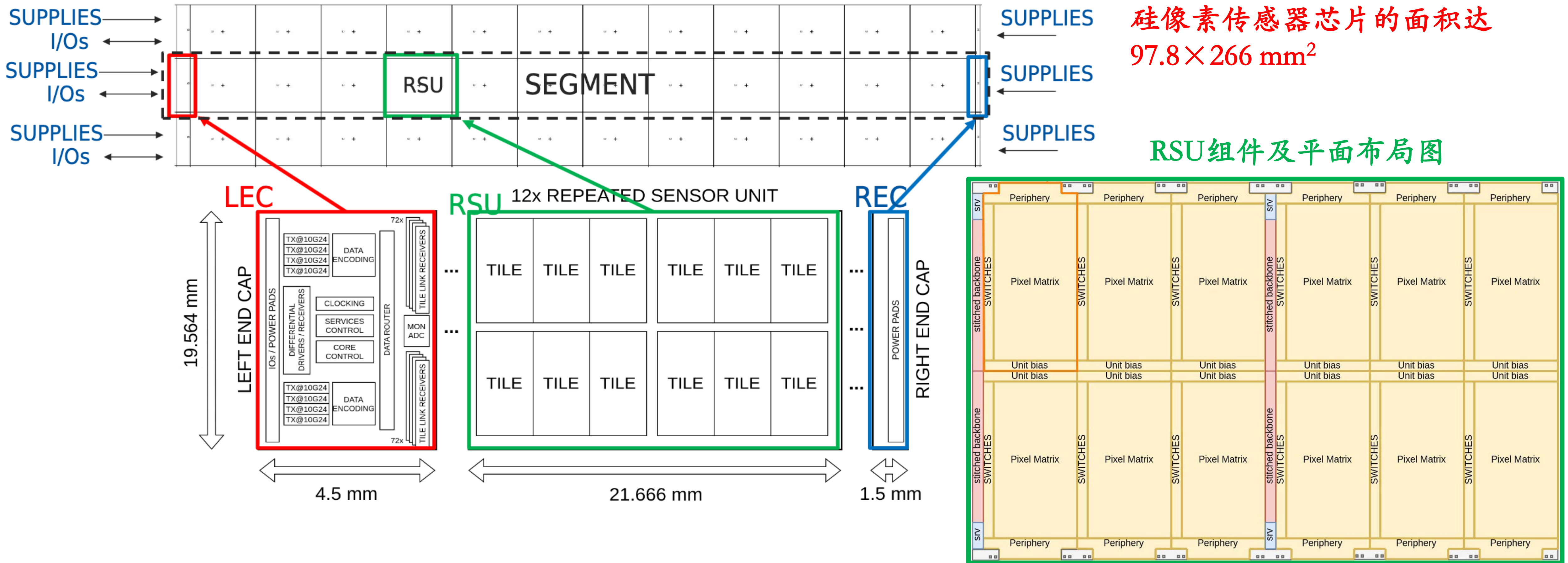






验证了MOSS芯片的性能符合设计预期，满足ITS3的需求

ER2芯片：MOSAIX总体结构



硅像素传感器芯片的面积达 $97.8\times266\ \mathrm{mm}^2$

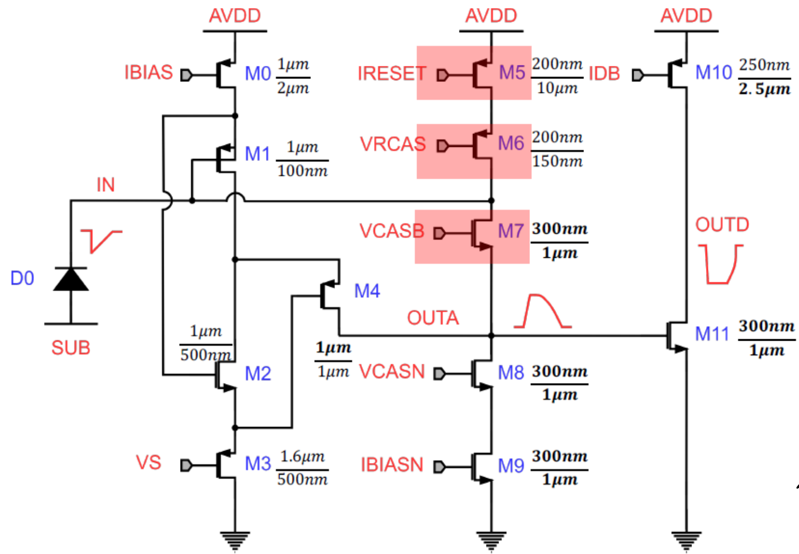
每个MOSAIX段由12各重复传感器单元(RSU)组成，每个RSU含12个瓦片 （TILE）

一个瓦片占L0层的1/864=0.116%

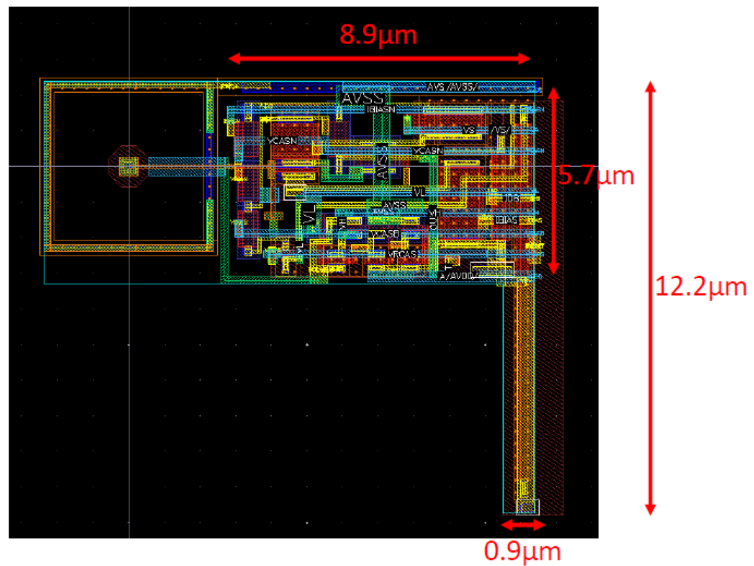
每个像素矩阵TILE分配独立的电源开关和外围传输电路，开关模块占用1个像素列约20微米，由四组的接骨架和标识对称排列构成

全乔木参与MOSAIX芯片的设计与模拟验证

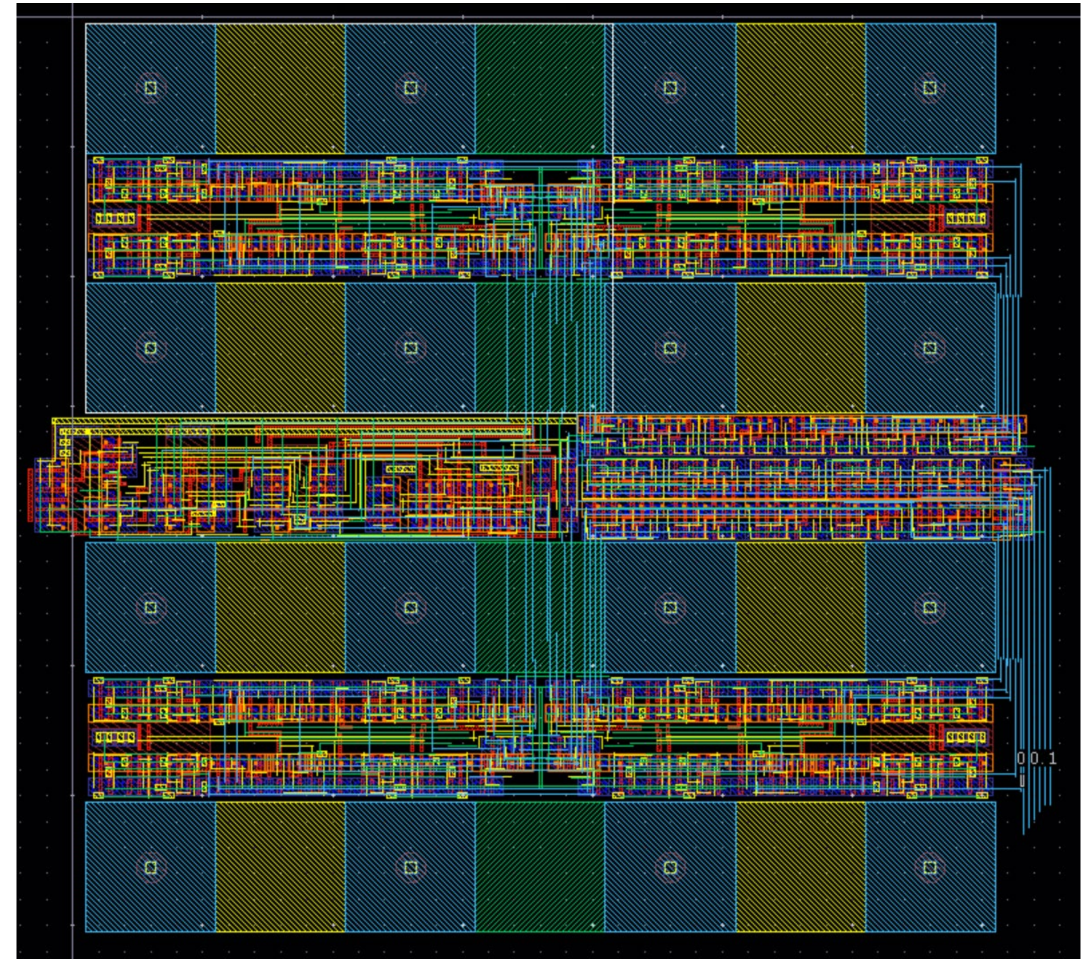
MOSAIX前端



原理图

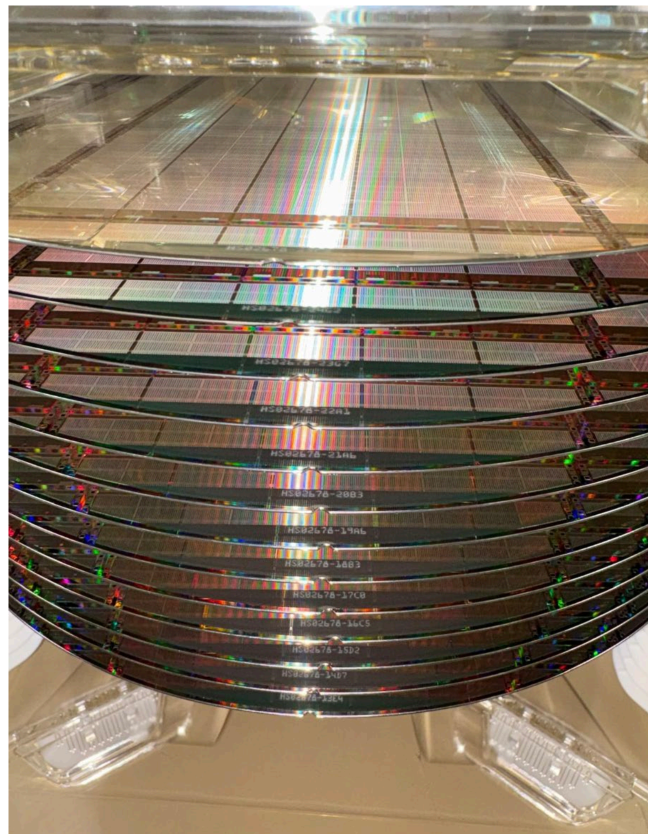


版图

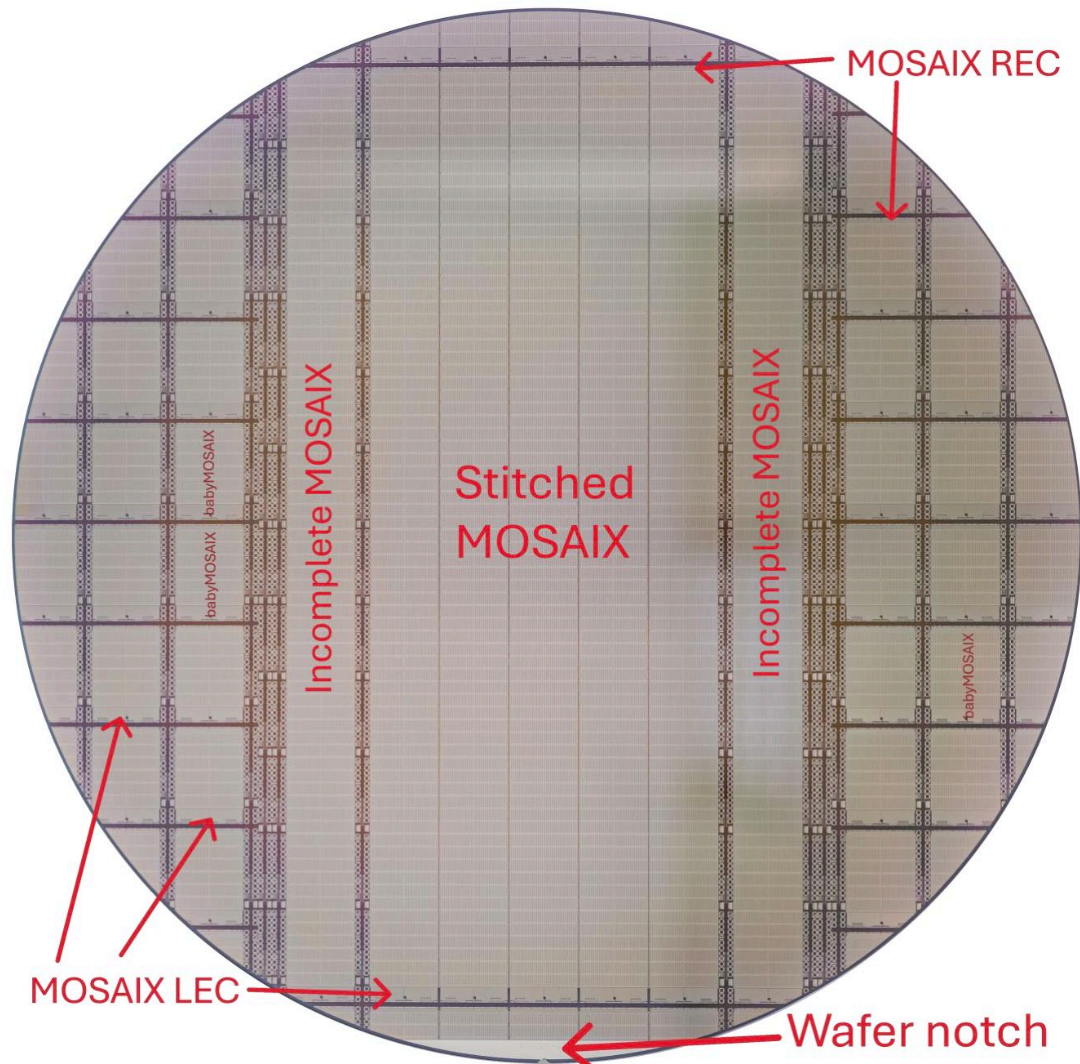


数字前端读出结构布局布线

ER2芯片现状



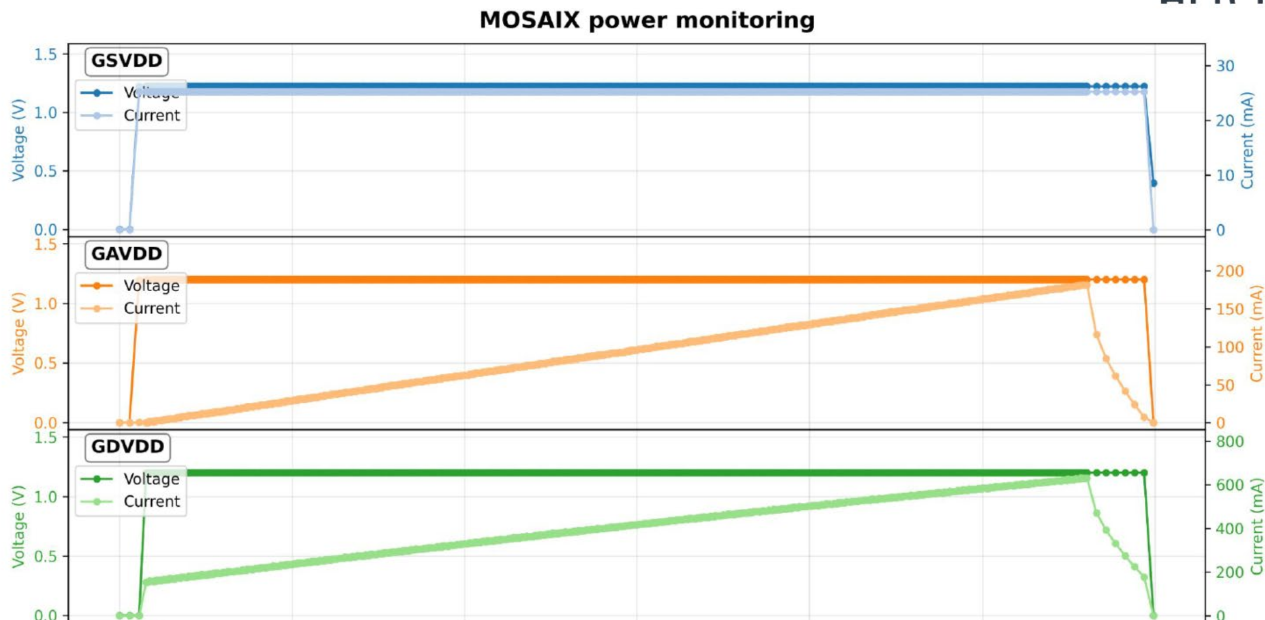
36片晶圆



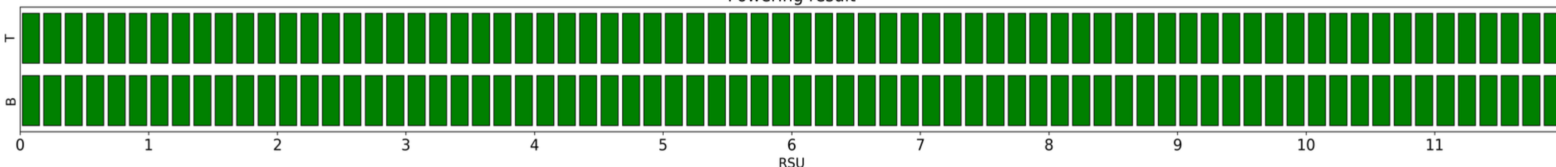
- 2025年7月份提交流片
- 二月份开始进行芯片减薄和切割
- 首先进行探针台测试
- 首批MOSAIX于三月中旬交付，并逐步进行测试
- 首批baby-MOSAIX于四月中旬交付，并逐步进行测试
- 测试系统软件（王淳正开发）已在实验室和探针台系统上完成安装与调试

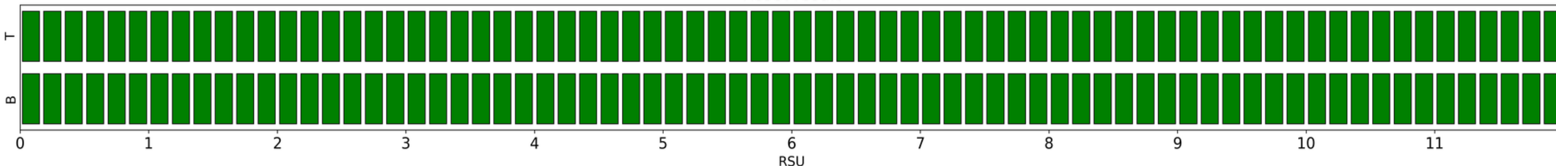
ER2芯片测试现状

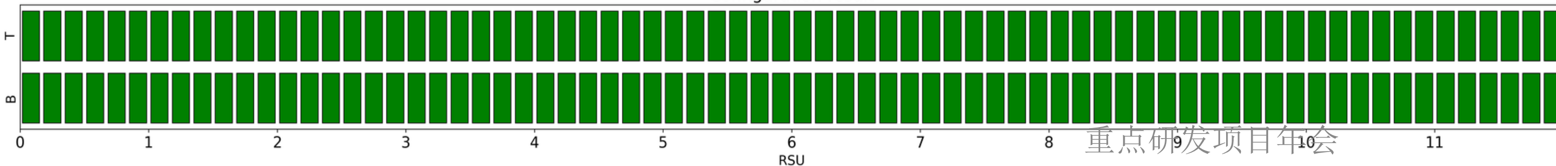
- ✓ 所有瓦片能同时供电并完成全面配置
- ✓ 慢控稳定
- ✓ 模拟监控总线工作正常
- ✓ ADC工作正常（正进行详细表征）
- ✓ DAC工作正常
- ✓ 片上数据传输链路工作正常
- ✓ 模拟和数字前端工作正常
- ✓ 阈值扫描进行之中



MOSAIX test results map







静态功耗(PSUB = 0 V)

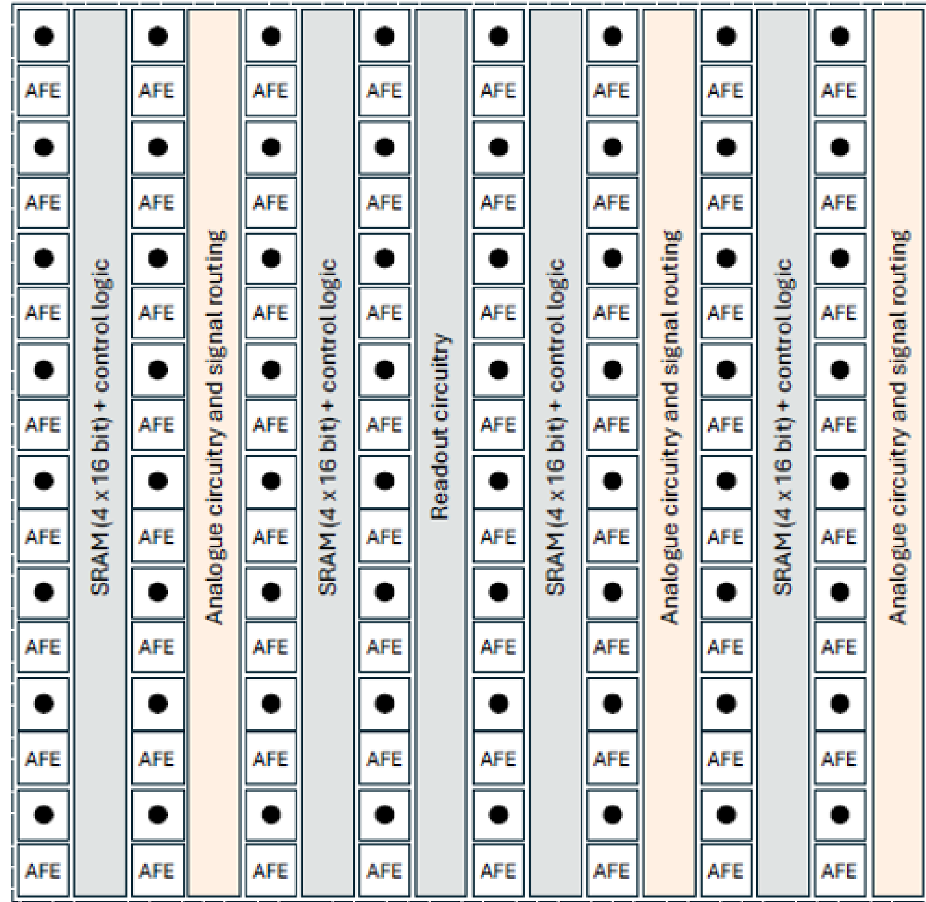
- GSVDD: 25 mA
- GAVDD: 180 mA
- GDVDD: 630 mA

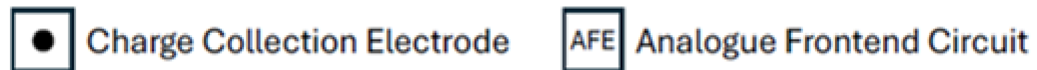
功耗密度：19.7 mW/cm^2

- 施加反向偏压、电荷注入和不同时钟频率下的功耗的测试进行中

周紫轩、赵子俊参与芯片表征

小像素芯片的研发





间距为10微米的像素Pixel Macro

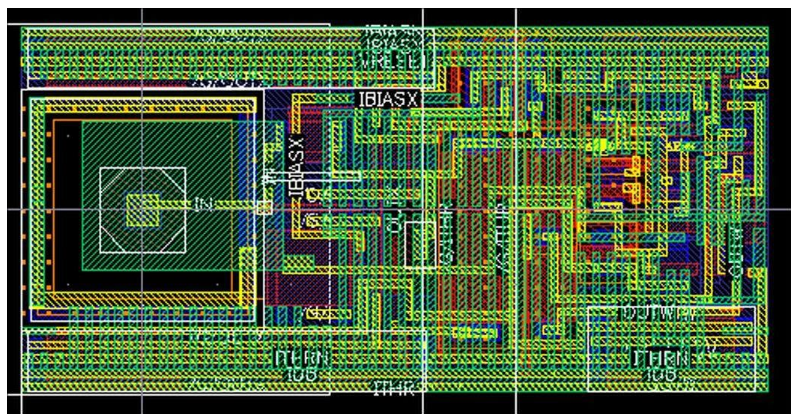
在10 μm版本的像素单元中，面积分配如下：

- 模拟部分：电极与模拟前端（AFE）占据约50%的面积。
- 数字/存储部分：剩余空间的50%用于双列合并的SRAM和控制逻辑（即像素面积的25%）。保留总面积的25%用于后续的模拟控制以及读出电路。

核心挑战：需在仅占总面积约25%的空间内，集成控制逻辑、存储阵列及控制电路

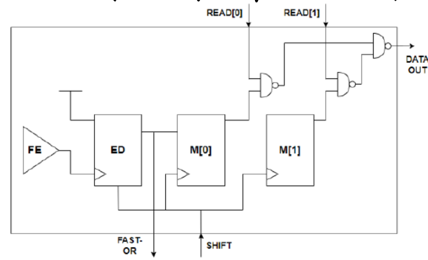
模拟前端和读出方案的验证与优化

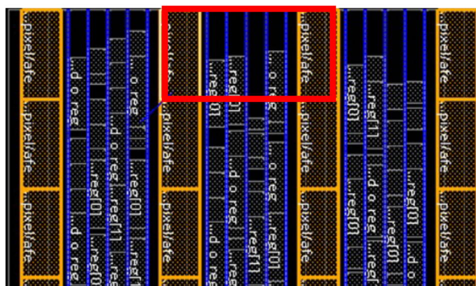
基于Corentin和Gabriele共同开发的Python仿真自动化脚本框架，实现网表自动生成与批量仿真，可评估功耗、阈值、噪声、mismatch、ToT、ToA、时间分辨率等多项前端指标。采用全局优化（粗粒度大范围搜索）+局部优化（以全局最优点为起点的精细收敛）两阶段策略；按参数维度分为小优化（仅调偏置电流）与大优化（同时优化电流+晶体管尺寸）。



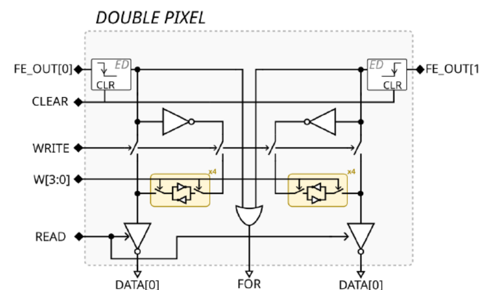
模拟前端版图

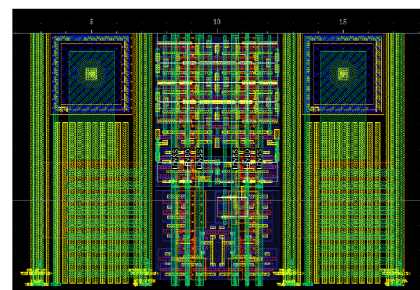
SIPO移位寄存器方案（标准单元流）



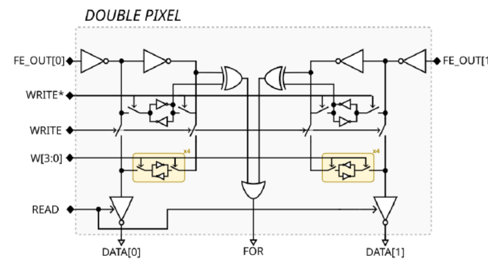


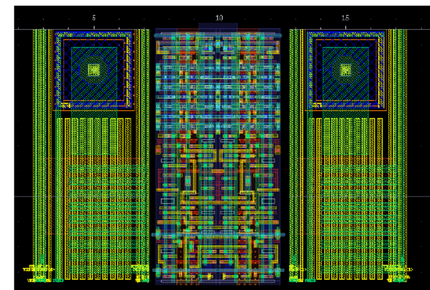
SRAM读出方案





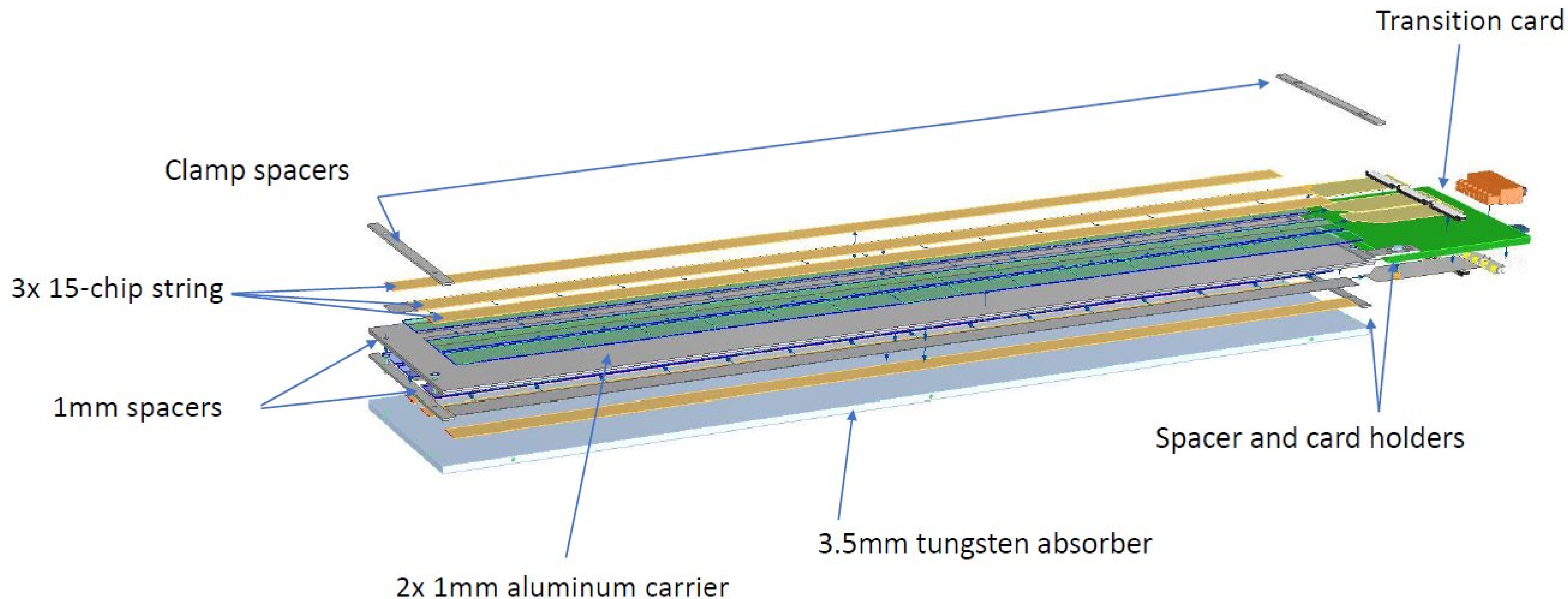
XOR双像素方案





对比全定制的方案二和方案三，像素内存储采用串入并出移位寄存器（SIPO/SR）替代 SRAM，无需写地址逻辑，同时可随时读取，外围控制电路更加精简。基于标准单元全数字实现，RTL到后布线仅需2—3小时，可直接复用成熟的数字设计流程，无需R&D投入，便于快速迭代和系统集成研究。是三种方案中目前唯一完成RTL+门级网表功能验证（11项测试全通过）、完成布局布线（无核心区DRC违规）、完成PixESL系统级命中效率仿真的方案。

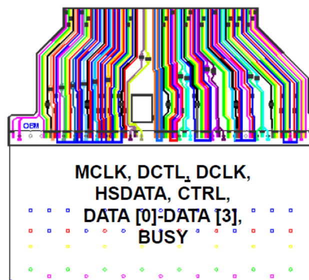
FoCal硅像素层的结构

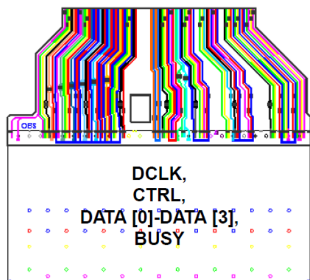


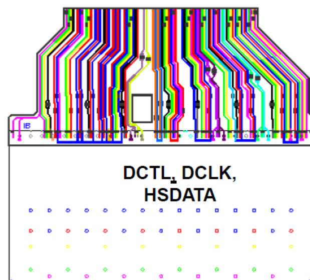
Total thickness = 3.5 (absorber) + 1.0 (spacer) + 1.0 (carrier) + 1.0 (carrier) + 1.0 (spacer) + 1.0 (spacer) = **8.5mm**

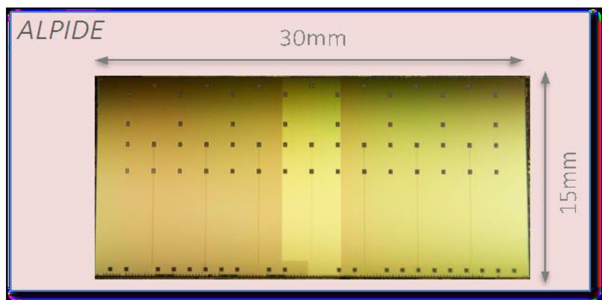
FoCal探测器硅像素层制作流程

3 types of chip-cables



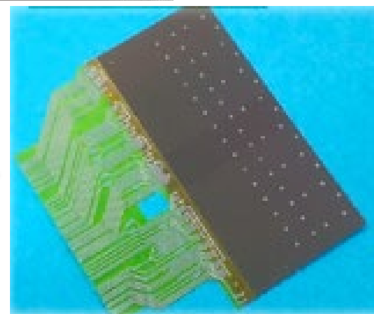


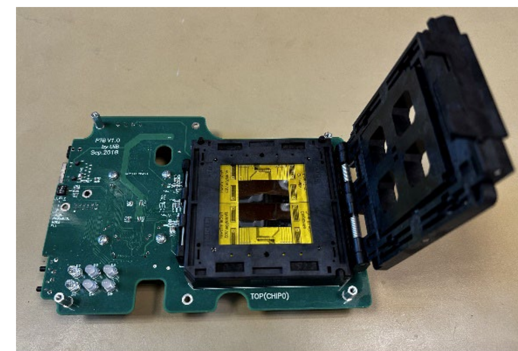




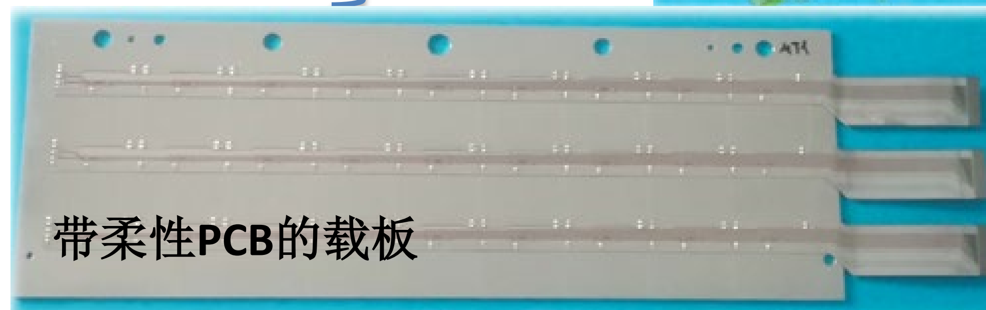
单芯片组装夹具

SpTAB





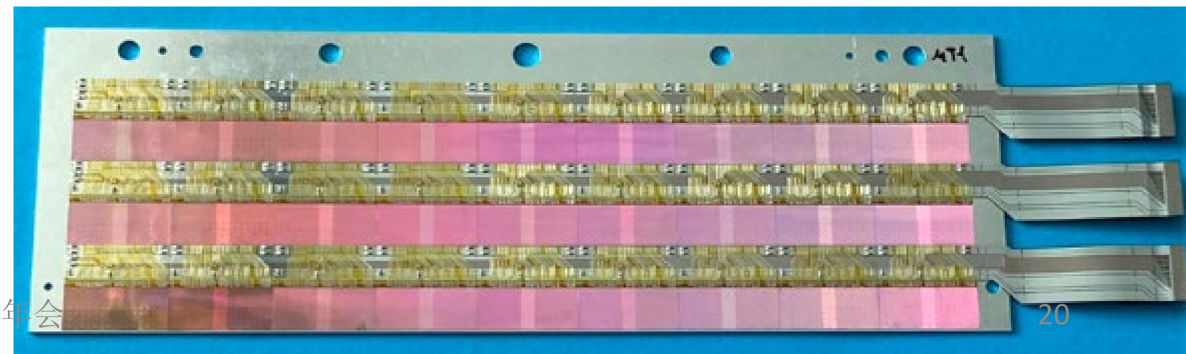
功能测试盒



带柔性PCB的载板

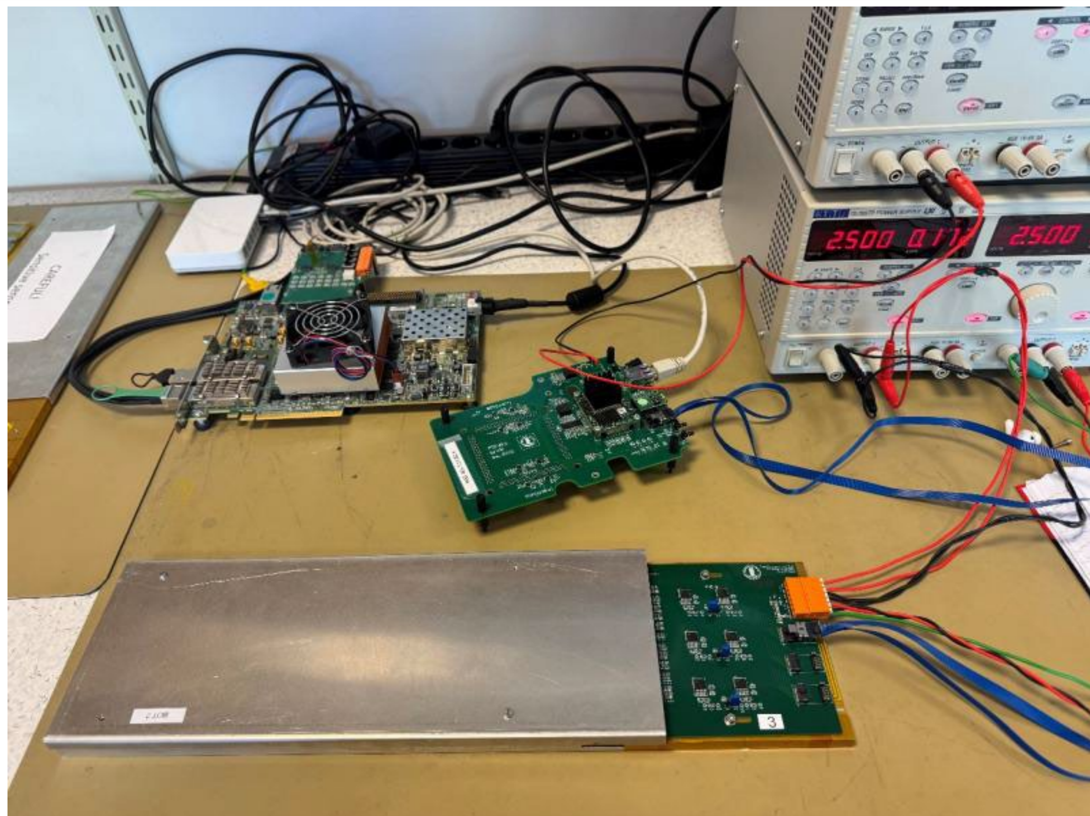
SpTAB

硅像素层模块组装夹具



硅像素层模块实验室测试系统的搭建

ALICE



测试清单:

- 上电(AVDD, DVDD)
- 寄存器
- 高速传输链路
- FIFO
- 模拟电路扫描
- 数字电路扫描
- 阈值扫描
- ……

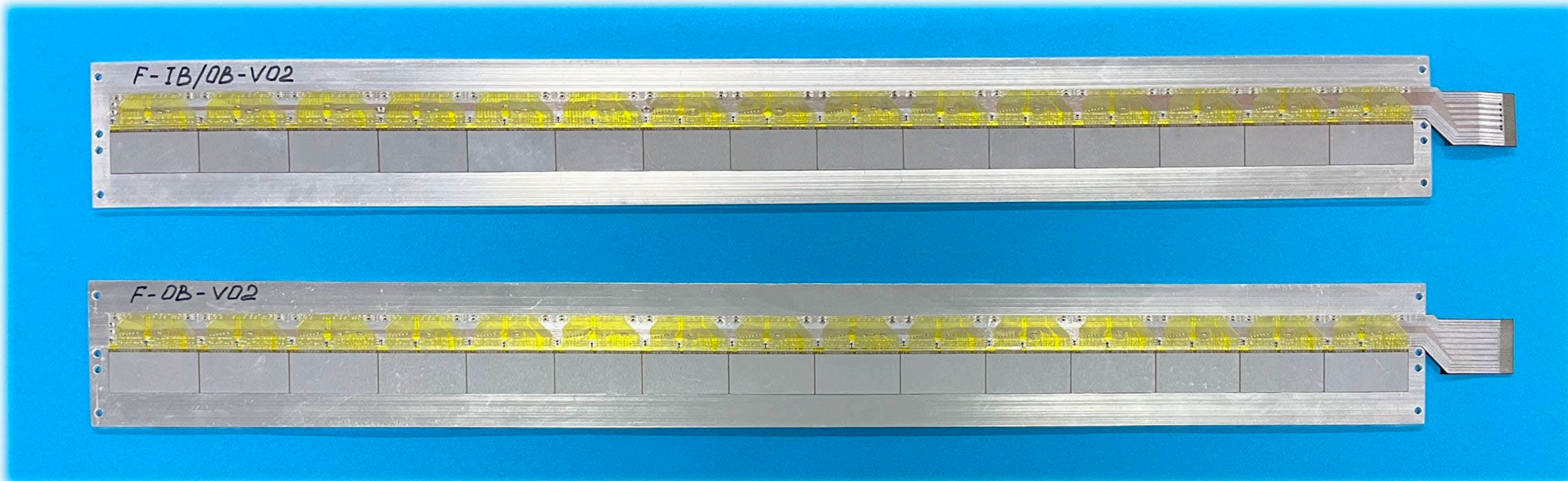
3 × 9 IB芯片串

易杰在卑尔根大学参与硅像素层测试系统的搭建

- ✓ 开发测试代码
- ✓ 建立质控标准

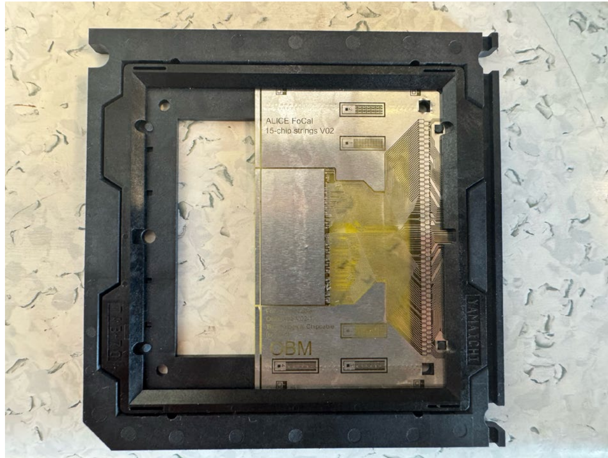
15个ALPIDE芯片串

ALICE

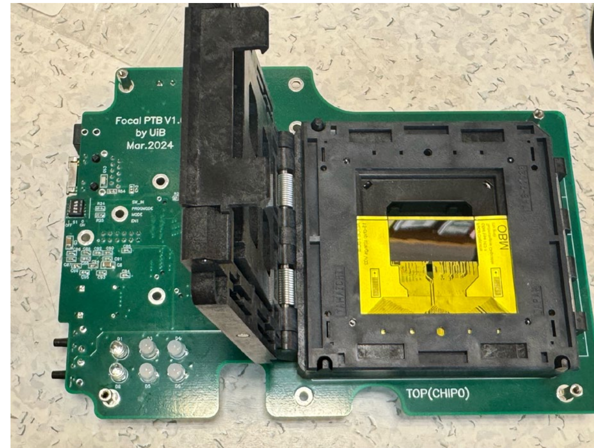


- 已组装了15芯片串原型（V02）以及测试芯片组件（OBM、OBS和IB），用于对FoCal PTB进行最终调试，并验证用于量产的测试程序

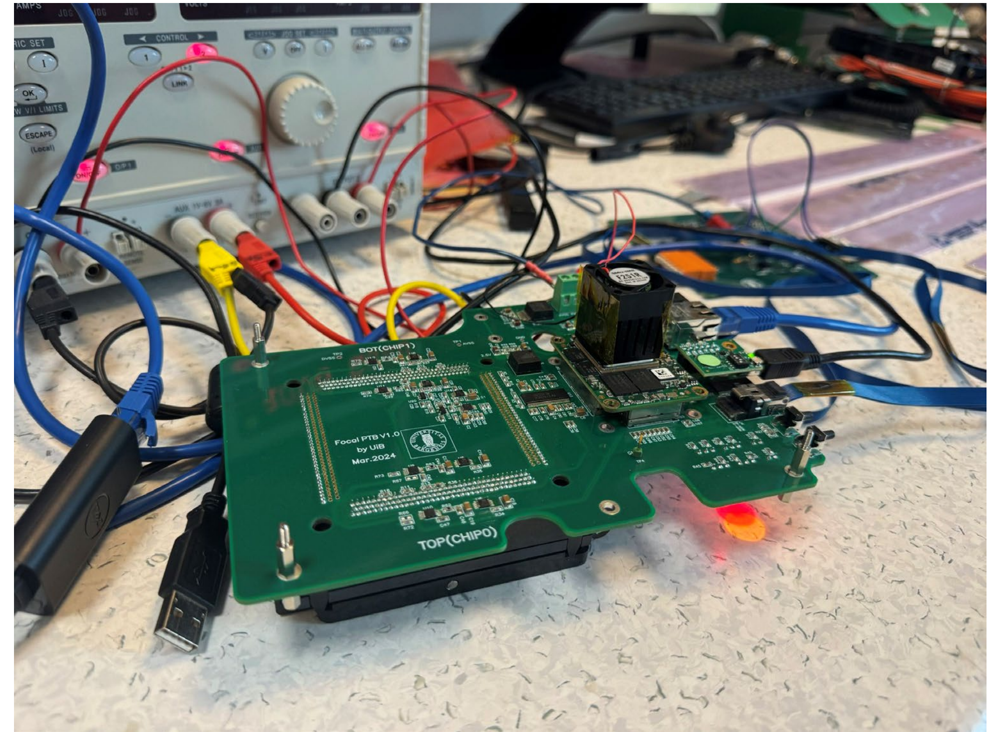
硅像素层模块测试系统及其软件开发进展



绑定到chipcable上的ALPIDE



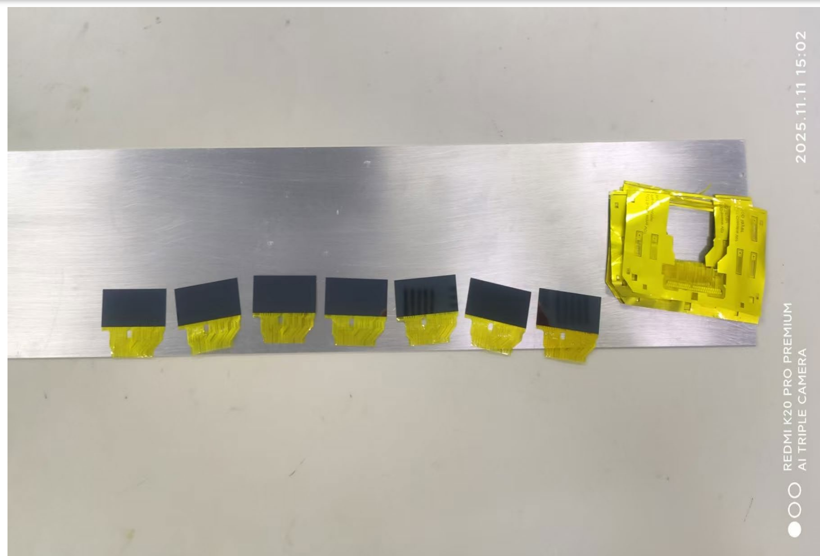
功能测试盒（PTB）



- 已搭建一个基于FoCal PTB的，用于测试15个ALPIDE（IB/OB）芯片串的测试系统
- 通过PTB能够与串上的ALPIDE芯片进行通信
- 基于Python开发了一个全新架构的测试软件
- 测试软件能够通过FoCal PTB向串上的ALPIDE的寄存器发送读写指令，并采集测试结果

硅像素层模块量产准备情况

ALICE



- 已确定将 ALPIDE 装配到芯片线缆的流程
- 将带有芯片的芯片电缆装配到载板上的柔性电路板的步骤尚待验证

- 一块多层铝质柔性印制电路板和多个不同类型的chip-cables已从卑尔根大学寄往我校，用于进一步测试组装流程
- 拟于10月份在芬兰赫尔辛基开硅像素模块组装交流会
- 拟于10月底开始量产

存在的问题

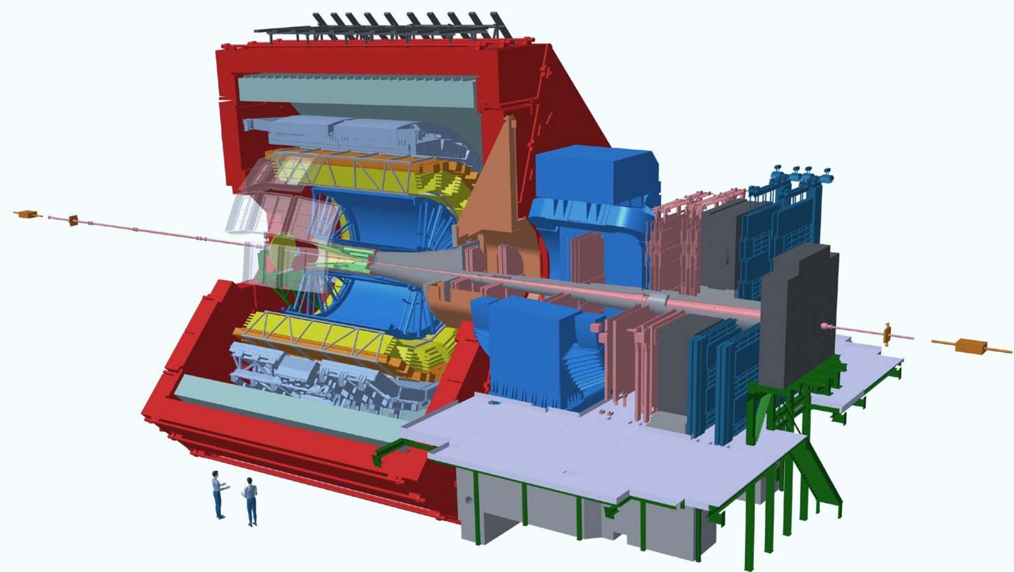
- “俄-乌冲突”导致乌克兰LTU延迟交付铝基柔性电路板。（6月18日获悉其一位骨干被应征入伍，对项目的影响尚在评估之中）
- LHC运行计划发生了改变，第三次长停机（LS3）调整为2026年7月-2030年6月，致使ALICE升级项目的时间线有所调整。
- 美国DOE和NSF决定不支持ALICE FoCal项目
- 印度FoCal项目经费尚未到位
- 钨粉(日本承担的钨板的生产任务)价格上涨近3倍
- FoCal探测器面临缩小几何接受度
- ALICE合作组已对用于ALICE 第三代硅像素探测器的晶圆尺寸硅像素芯片的技术指标进行了调整。我们已于2025年12月份提交了考核指标变更的申请，但尚未得到批复。

总结

- 课题组按计划在实施承担的ALICE在LS3期间的升级任务
  - ✓ 参与研发了ITS3晶圆级超薄柔性硅像素芯片，正参与ER2芯片的表征测试
  - ✓ 参与研制的FoCal探测器硅像素层样机的双光子位置分辨已达到mm量级，已为硅像素层模块量产做好了准备
- 课题组已开展的相关工作
  - ✓ 参与完成了模拟、数字测试芯片和ER1 MOSS芯片性能表征，结果已经发表在NIMA上
  - ✓ 参与完成了ER2 MOSAIX芯片设计和模拟验证
  - ✓ 已研制出单ALPIDE芯片工装夹具和硅像素层的工装夹具
  - ✓ 参与研制了硅像素层模块样机及其实验室和束流测试
  - ✓ 合作完成了读出单元PCB已最终确定，等待生产
  - ✓ 负责分析了硅像素层束流测试数据，结果已经发表在JINST上
  - ✓ 对硅像素层读出系统进行了系统模拟，结果被包含在TDR之中，并发表在NIMA上
  - ✓ 参与向O^2中移植探测器模拟软件，研究了簇团重建方法，分析了中性π介子的重建效率

谢谢各位专家的指导!

课题简介



- ALICE是LHC上唯一致力于重离子碰撞物理的大科学装置。
- 研究夸克-胶子等离子体（QGP）的性质及其演化规律，以深入理解由量子色动力学（QCD）主导的多粒子系统的特性，认识早期宇宙及其演化规律。

ALICE

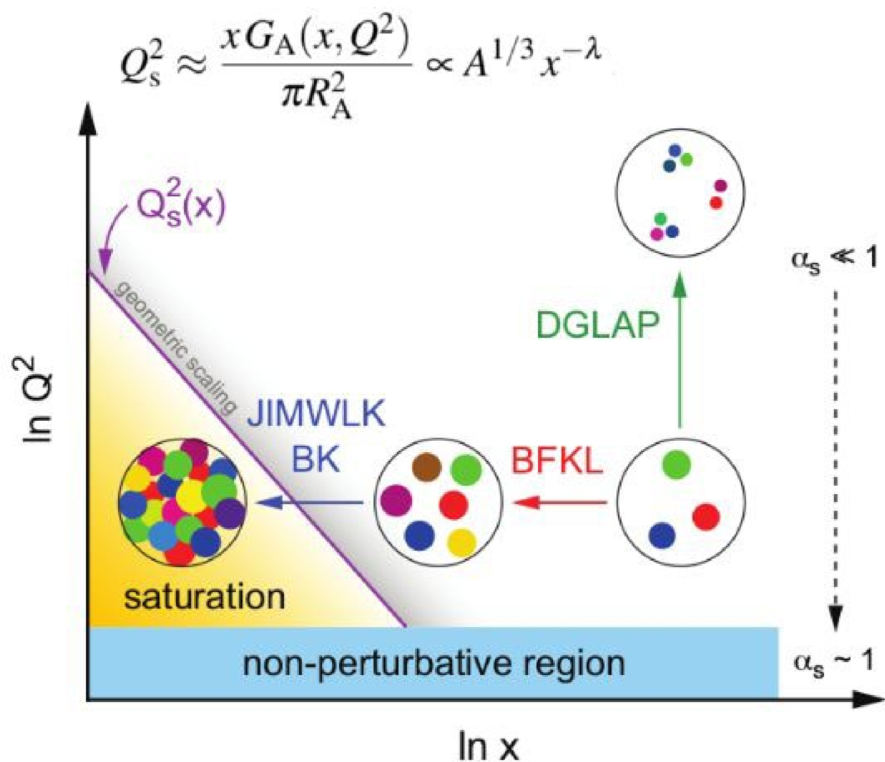
~40个国家，~172个大学和研究机构，~2000名科学家和工程技术人员

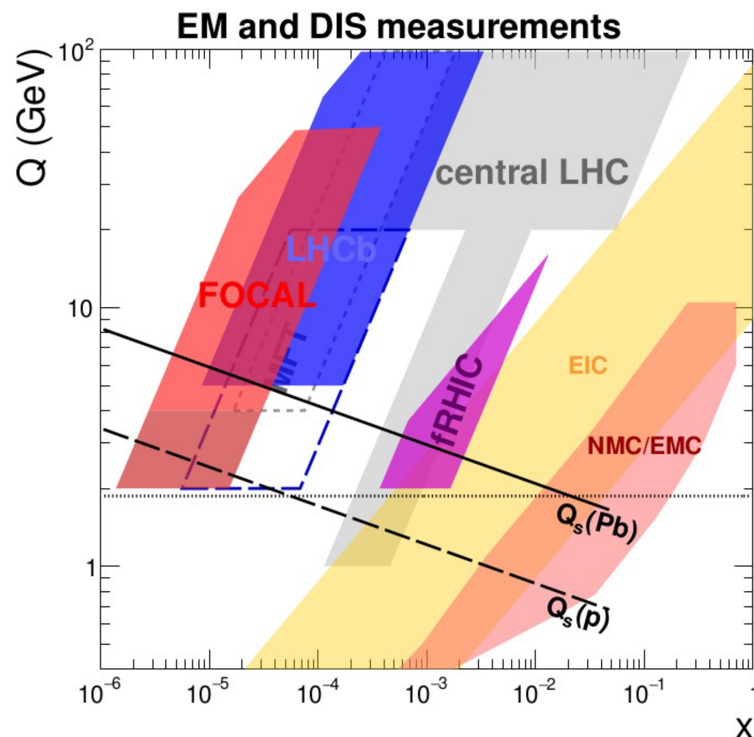
探测器建造费用：　200 M 瑞郎

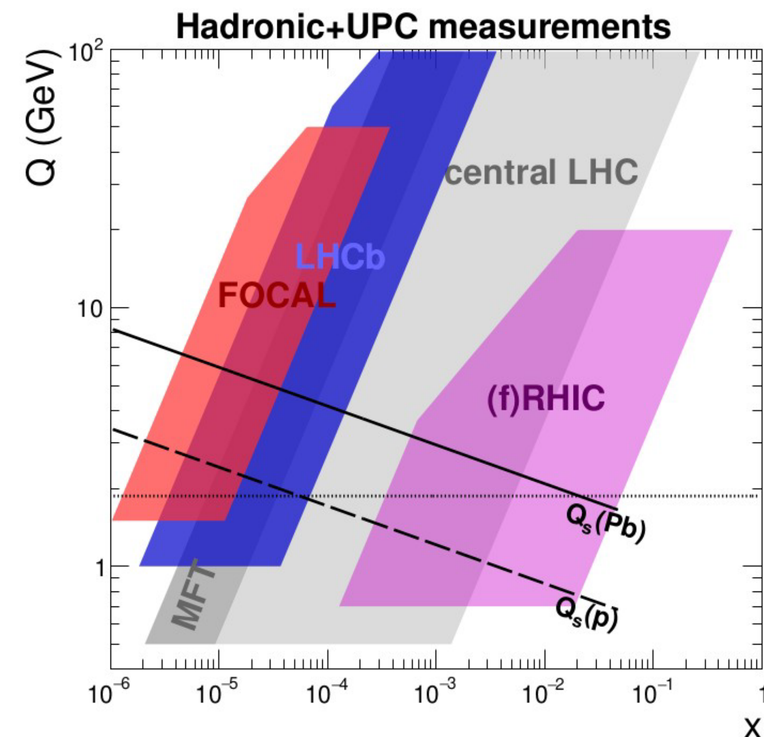
本次升级总经费：18 M 瑞郎

→ 中国组预期贡献：~2.8 %

FoCal的物理目标







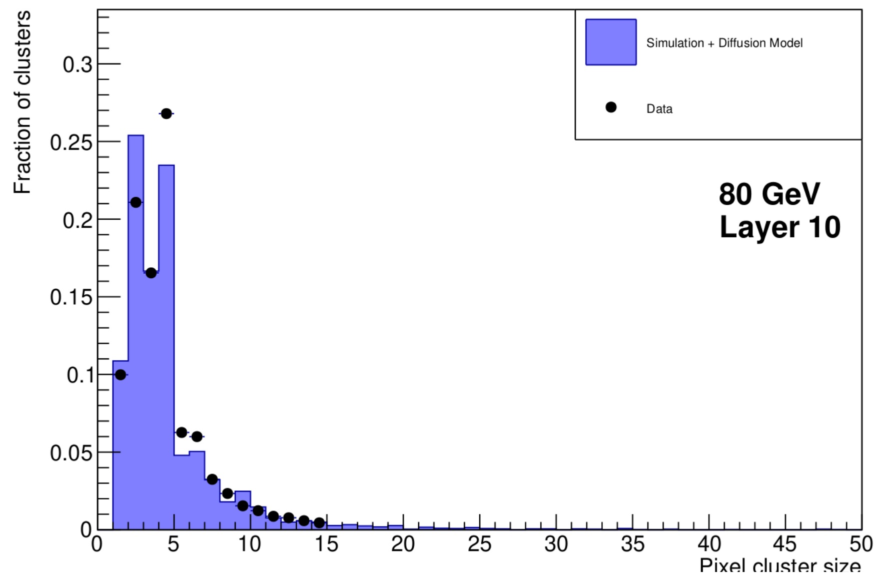
- FoCal将拓展Q-x探测区域，x低至10^{-6}，Q达4 GeV→测量质子-质子碰撞中前向快度区直接光子的横动量谱
- 研究小x物理及QCD非线性动力学→测量π^0-π^0和γ-π^0方位角关联

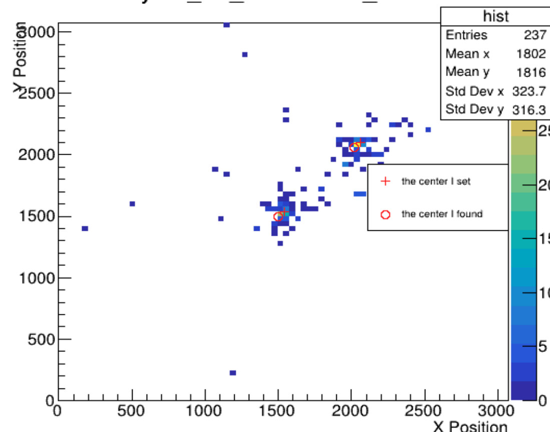
FoCal强子量能器读出电子学系统

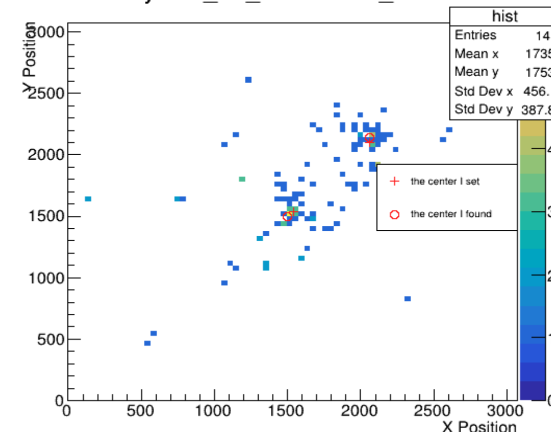
ALICE

- ✓ 参与了基于HGCROC芯片的读出电子学系统的搭建。
- ✓ 参与了2024 年在SPS H4进行的束流测试，负责开发了读出软件系统，并主导了测试数据分析。
- ✓ 对基于 H2GCROC 芯片的电子学读出系统进行性能评估。
  - ✓ 在最小增益下，系统在 60 – 300 GeV 能量扫描中有良好的响应线性。
  - ✓ 能量分辨率为 $(1.34 \pm 0.3)/\sqrt{E} \oplus (0.06 \pm 0.02)$，与 2023 年使用商业读出系统获得的分辨率相当。

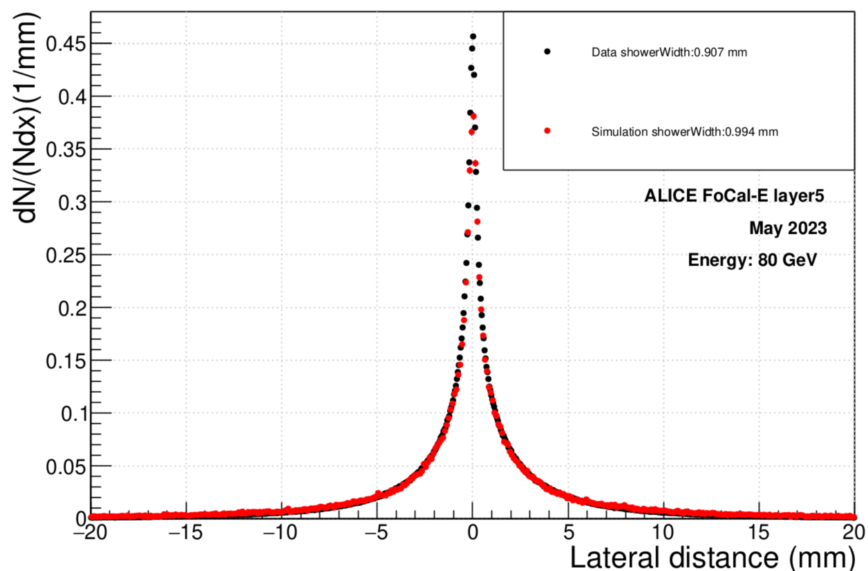
探测器GEANT4模拟



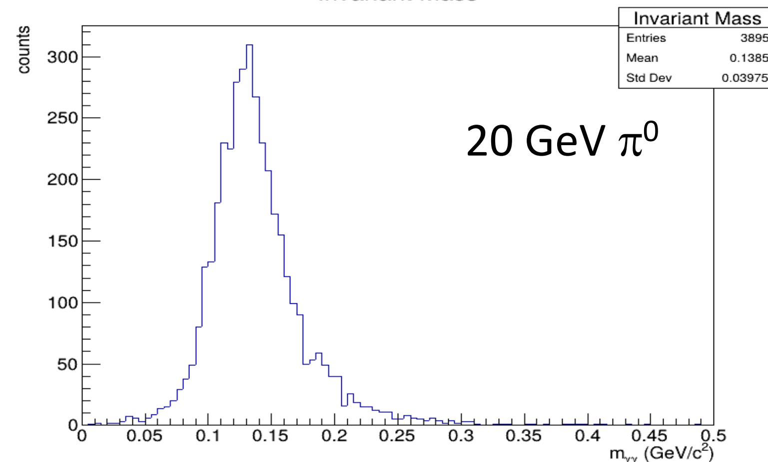




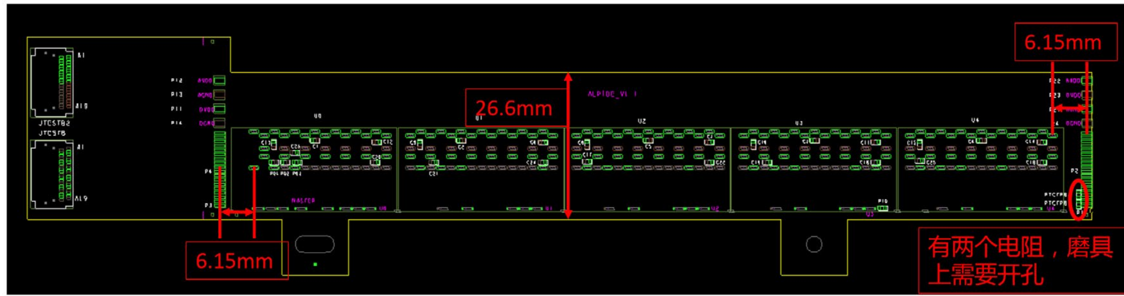
- 用像素层确定PAD层簇射的中心位置
- 基于簇射的径向分布，分解有交叠的簇团
- 将源于同一粒子的各层簇团能量相加
- 计算双簇团的不变质量

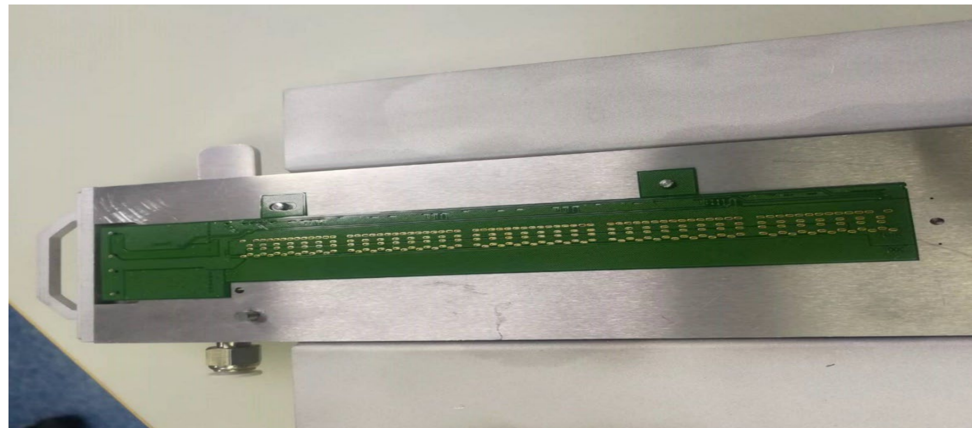


引入扩散效应，模拟数据能够比较好地符合束流测试结果



FoCal硅像素层研制进展: FPC、 夹具研制

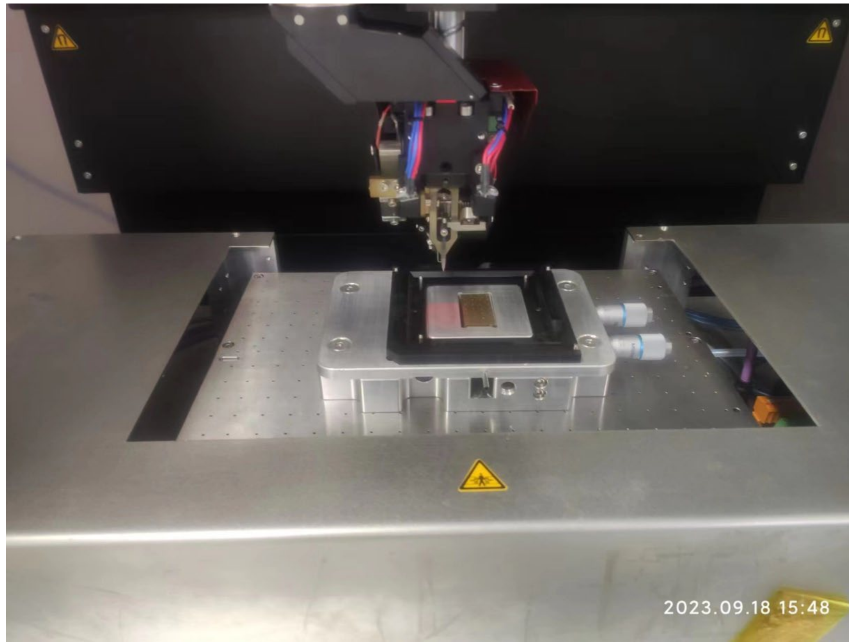




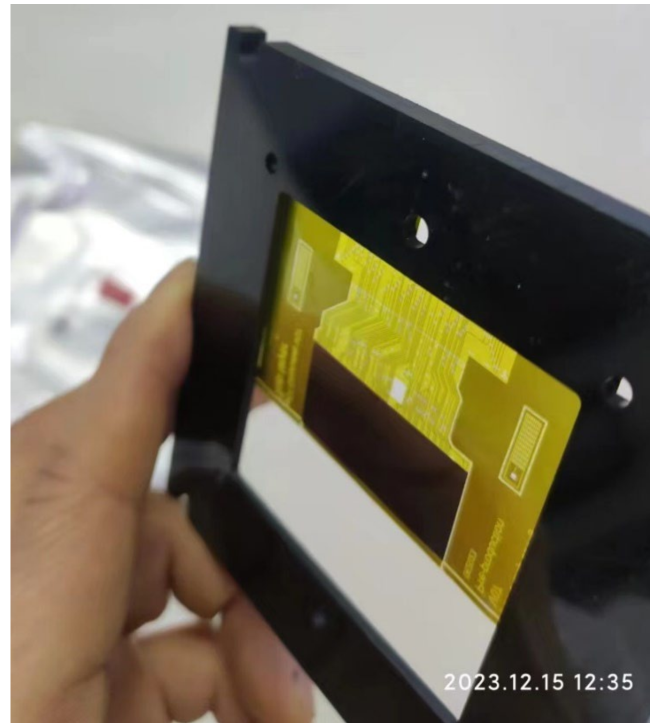
FPC gripper

- R&D on HIC as backup solution is ended as chips have to be returned to CERN by the end of March,2023
- We are suggested to join the effort on string-based pixel layer R&D and production.

FoCal硅像素层研制进展: ALPIDE2Chipcable

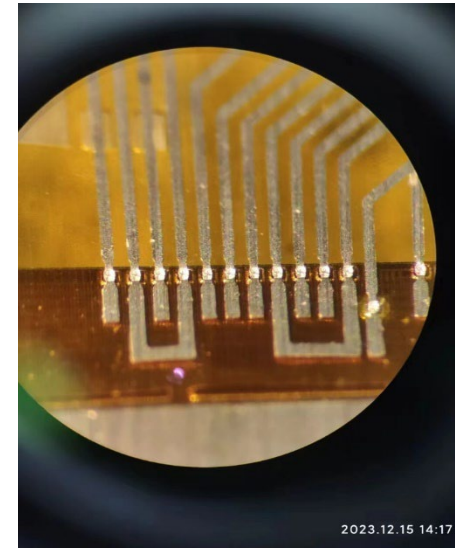


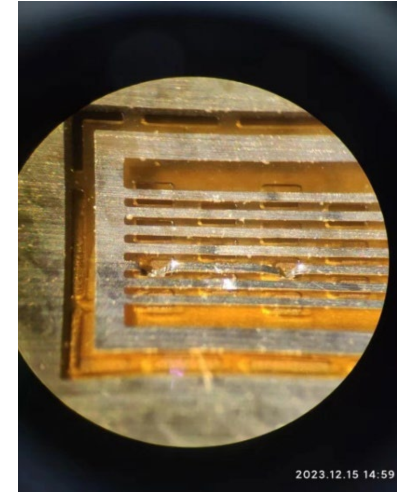
为放置单芯片组装夹具，绑线机平台需调低 2 cm

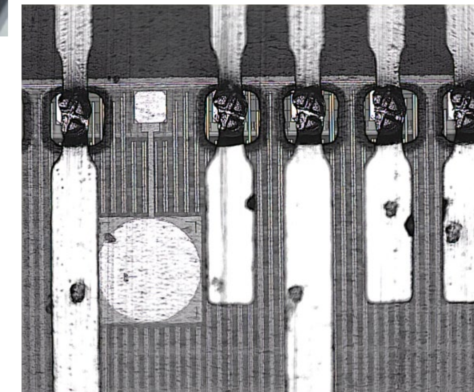


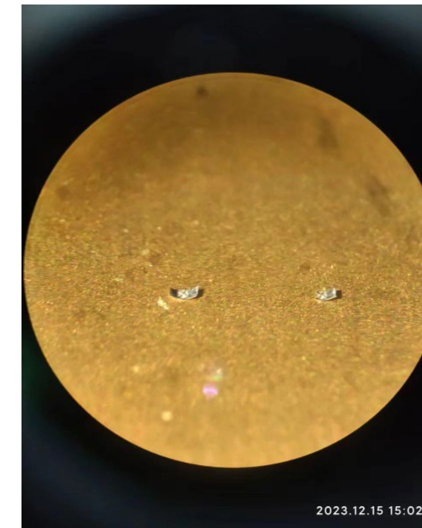
ALPIDE绑定到chip-cable

显微镜下检查绑定效果



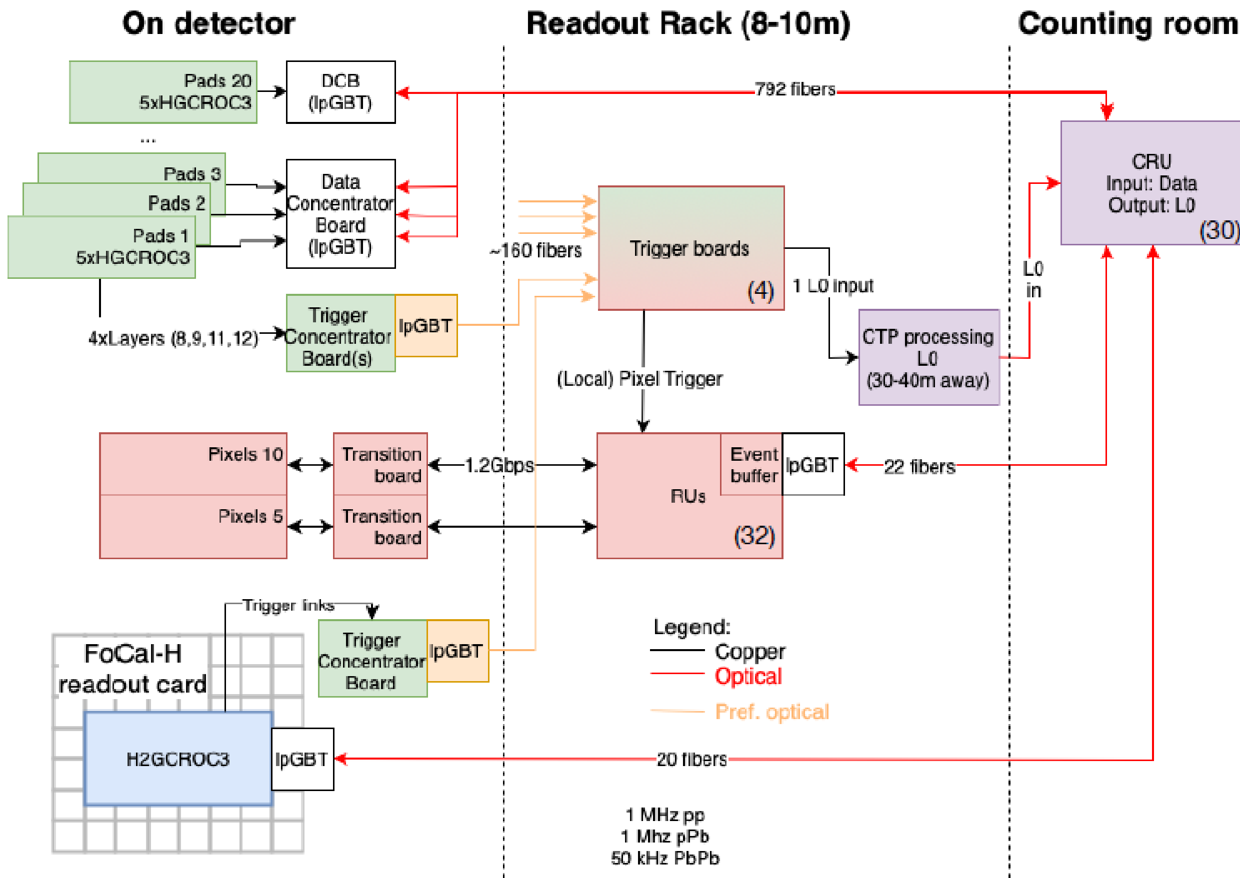




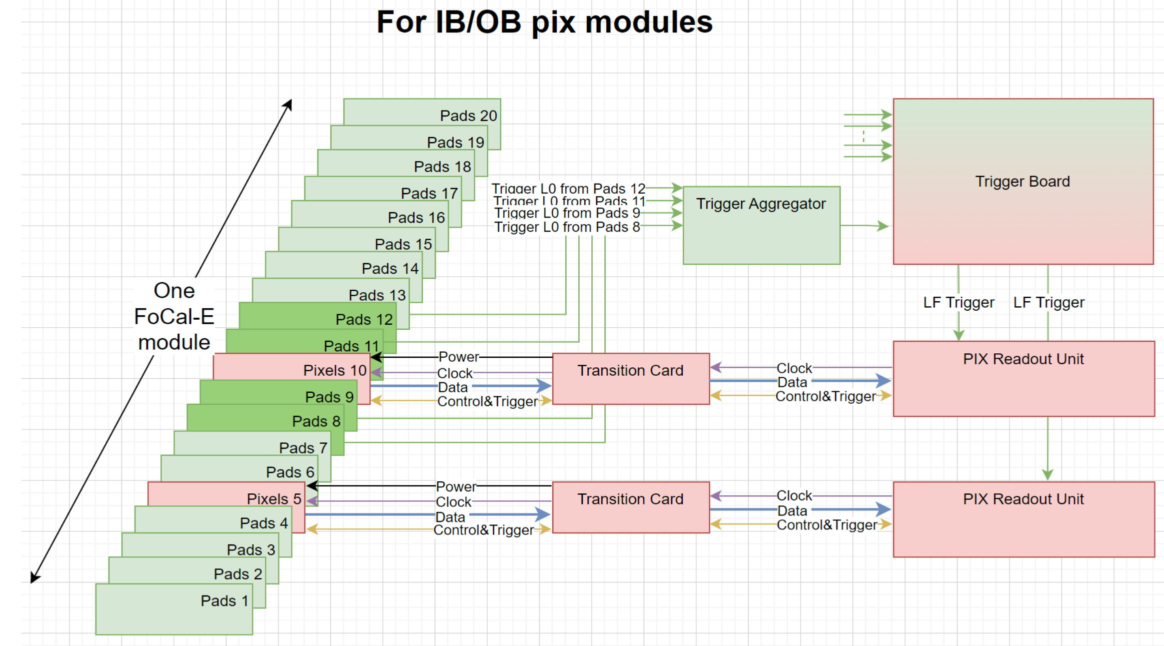


剥离测试

FoCal探测器硅像素层读出电子学系统



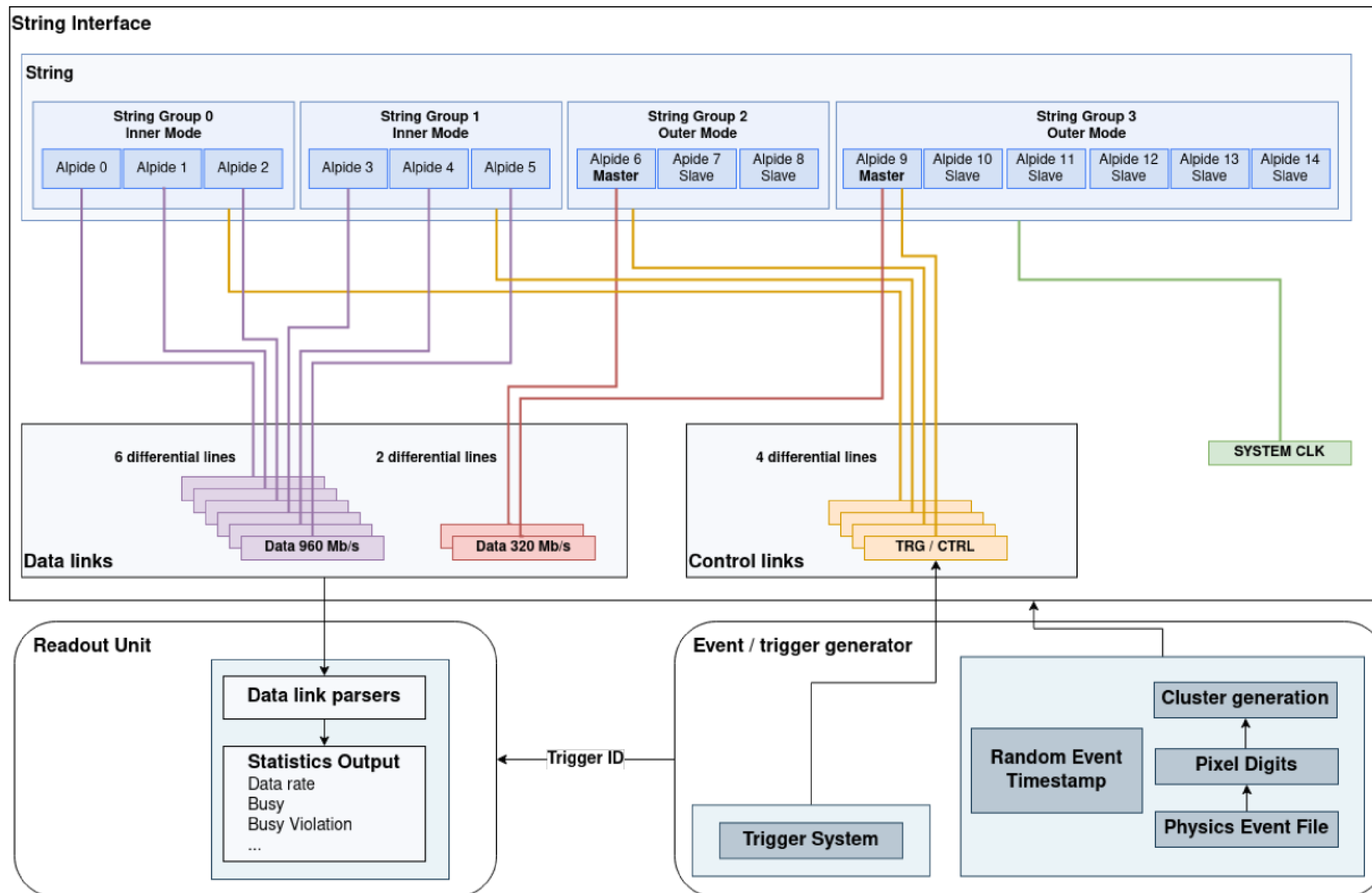
FoCal读出系统



硅像素层读出系统

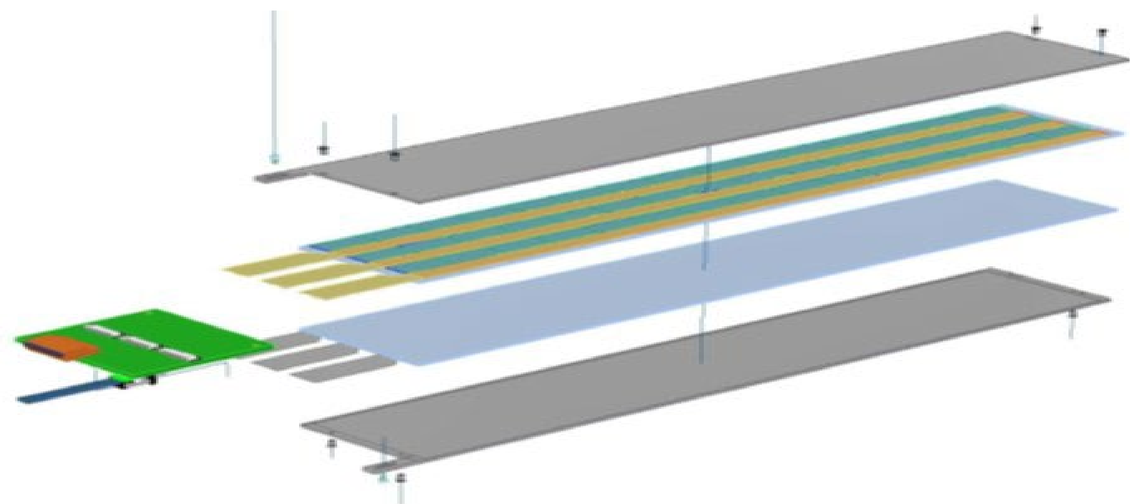
- 将合作研制硅像素层读出单元

SystemC模拟框架

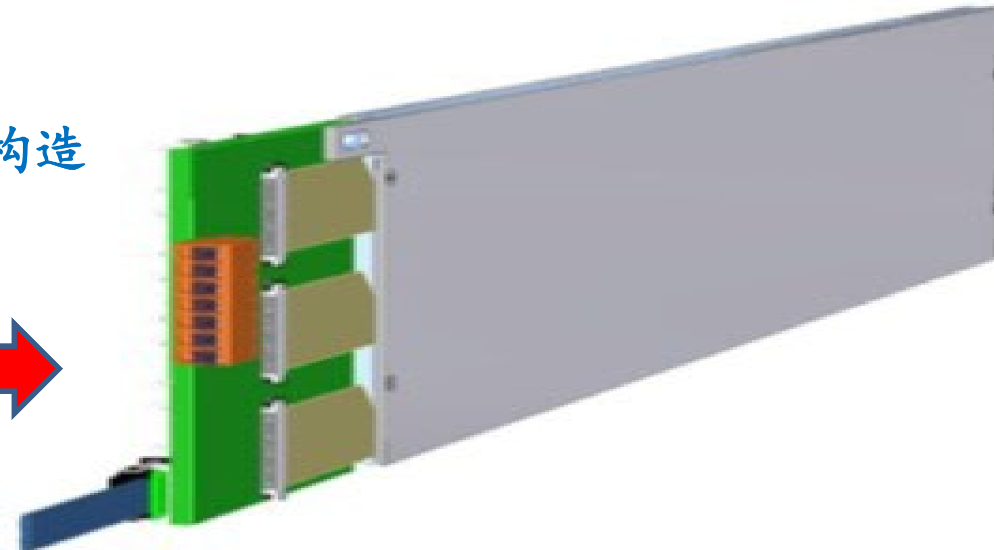


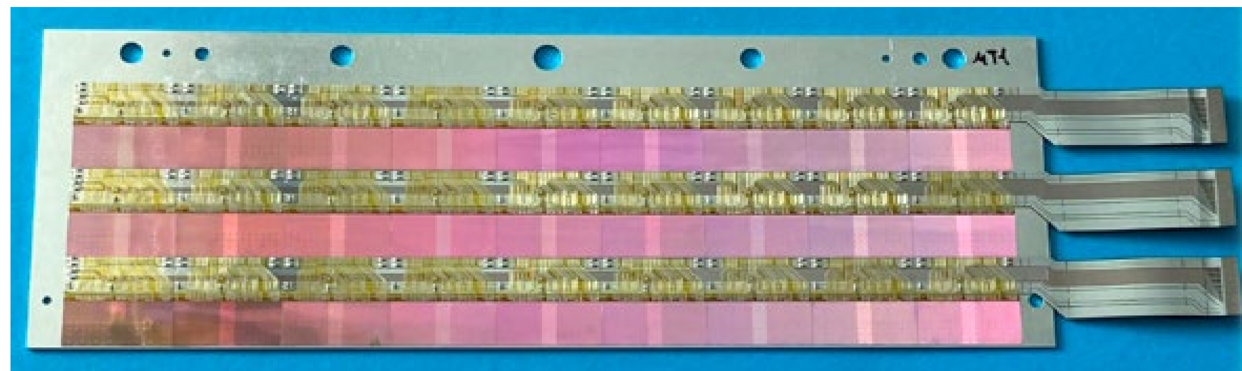
- 通过系统模拟，优化FoCal的构造和像素层的位置，在实现有效分离高能π^0衰变光子的同时，减小读出带宽和读出死（忙）时间。

FoCal探测器硅像素层的研制

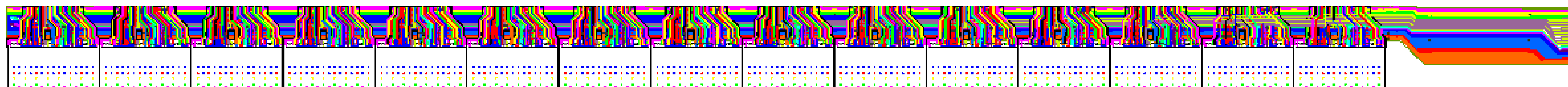


硅像素层构造





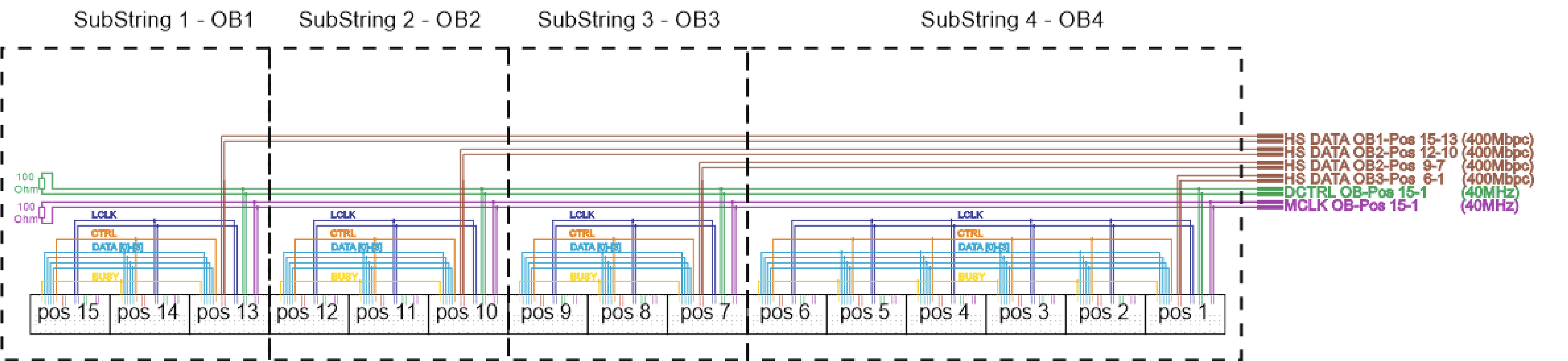
- 每个模块含 2 × 3 个长条，每个长条由15 个ALPIDE芯片及其读出柔性电路组成
- 每个模块含90个 ALPIDE芯片
- FoCal共44 个像素层模块, 需要3960个ALPIDE芯片



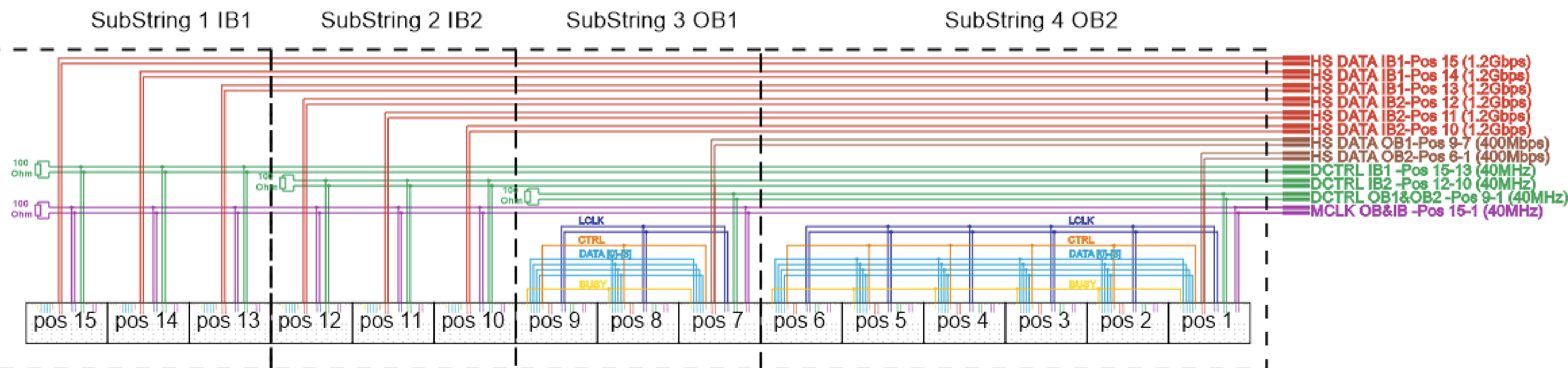
由15个ALPIDE组成的长条

FoCal硅像素层研制进展: String研制

Schematic diagram of strings



OB string



IB/OB string

- 1个由IB/OB ALPIDE芯片构成的模块 含6个长条 → 1个RU:
  - 36 IB chips @ 960 Mbps
  - 12 OB 主芯片 @ 320 Mbps

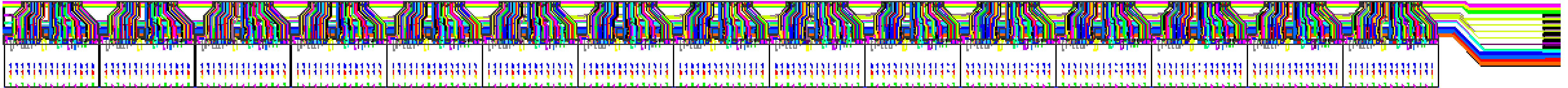
  带宽: 38.4 Gbps
- 3 个由OB ALPIDE 芯片构成的模块 → 1个RU:
  - 每个模块含24个OB主芯片
  - → 72 个OB 主芯片 @ 320 Mbps

  带宽: 23.4 Gbps

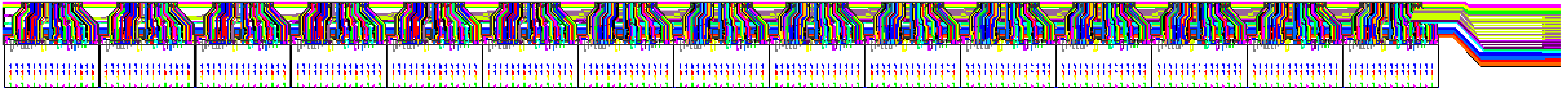
FoCal硅像素层研制进展: String研制

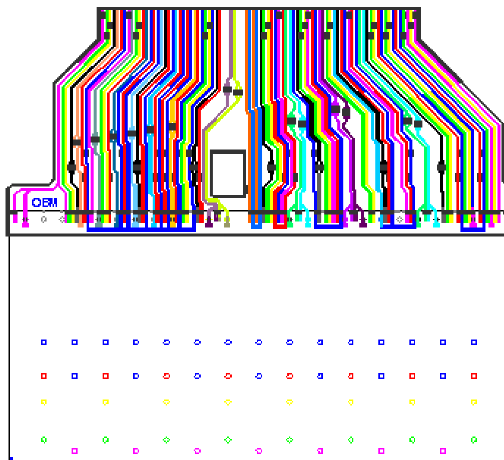
Layout of the strings

IB/OB string

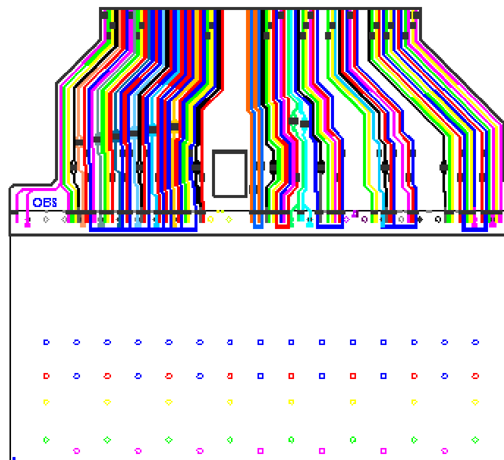


OB string

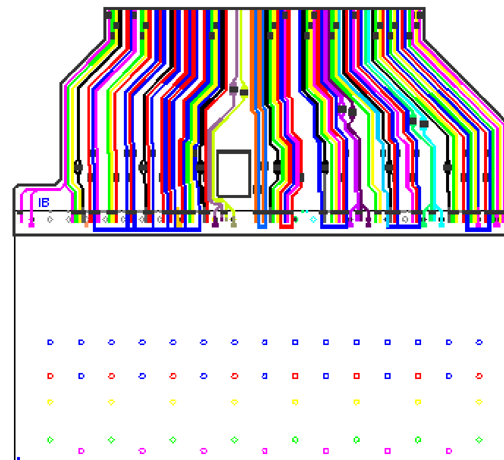




OB-M



OB-S



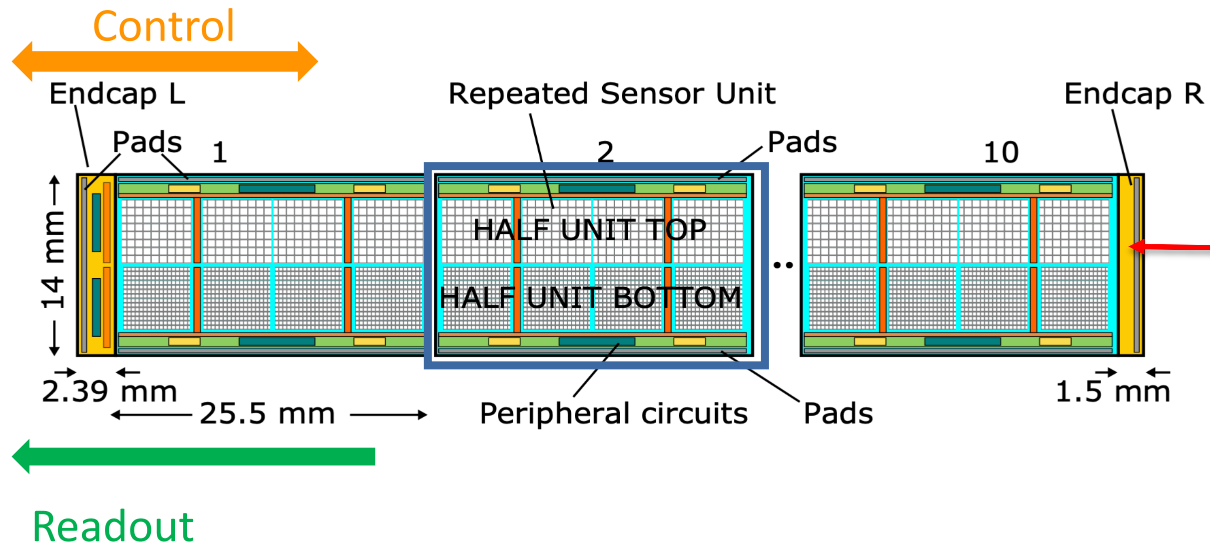
IB

Three different types of chip-cables are designed as similar as possible

ER1 MAPS Chip

Aim at learning and proving **stitching**, submitted in December 2022

Two wafer scale stitched sensor chips (MOSS, MOST)



	Pixel matrix	Pixel size
Matrices on the top	256 × 256	22.5 μm
Matrices on the bottom	320 × 320	18 μm

MOSS (1 of 6)

MOST (1 of 6)

300 mm wafer

MOST: 2.5 mm × 259 mm, 0.9 Mpixels (18 × 18 μm²),

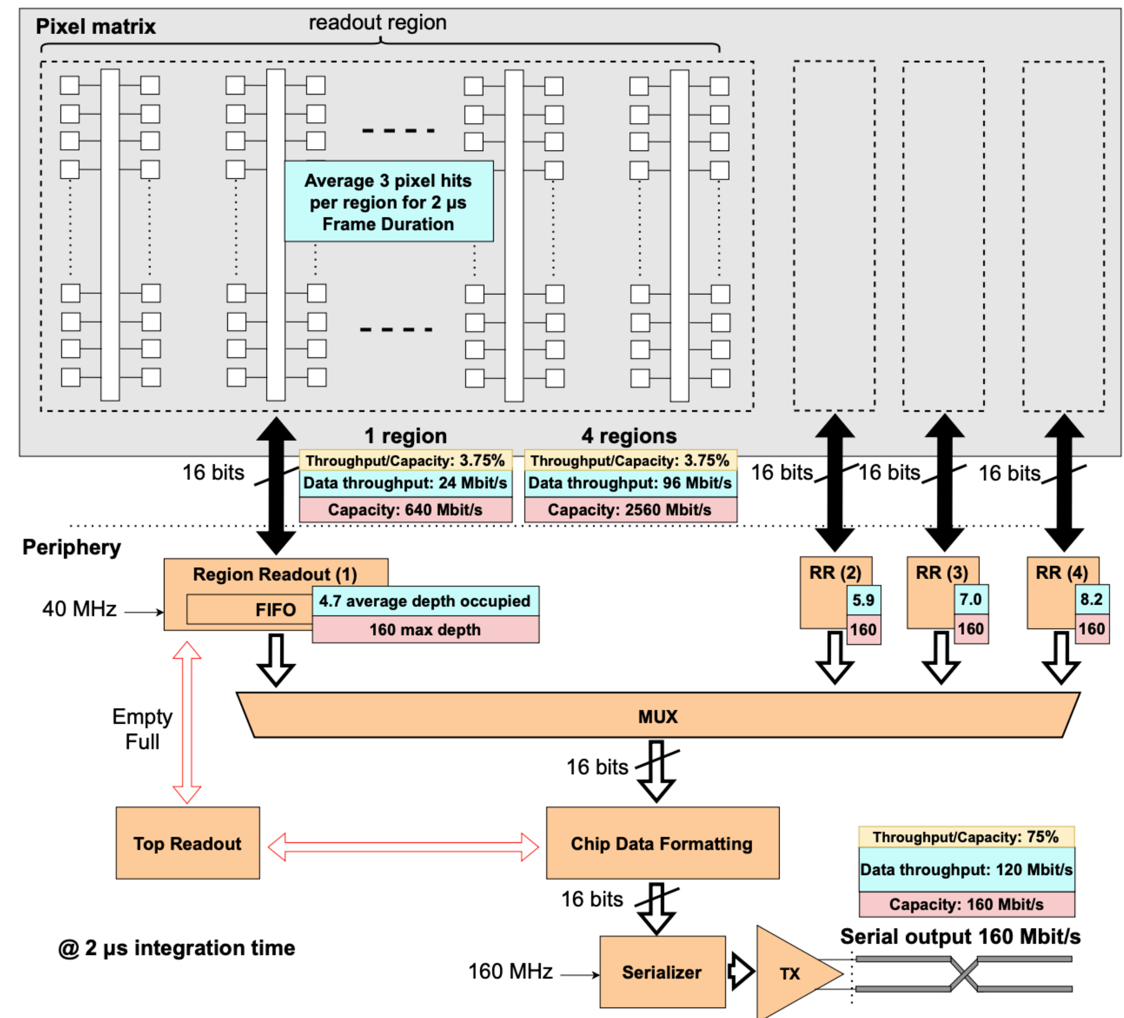
The MOSS chip contains 20 half units and 6.72 million pixels.

ER2芯片设计：ASIC框图

设计指标

Simulation parameters	Value	Unit	Conditions
Particle Rates			
Pb-Pb Interaction Rate	164	kHz	Safety factor 2
Particle flux (Hadronic)	2.55	$\mathrm{MHz\,cm^{-2}}$	z=0 cm, all centralities.
Particle flux (QED)	3.20	$\mathrm{MHz\,cm^{-2}}$	z=0 cm.
Total particle flux	5.75	$\mathrm{MHz\,cm^{-2}}$	z=0 cm, all centralities.
Geometry, timing, encoding, data transfer capacity			
Pixel dimensions	20.8×22.8	$\mu\mathrm{m} \times \mu\mathrm{m}$	
Tile pixel array size	442×156		
Pixels per Tile	68952		
Sensitive Area of the tile	0.328	$\mathrm{cm^2}$	
Tiles per segment	144		
Readout regions per tile	3 or 4		
Frame Interval Duration (FD)	2 or 5	µs	
Minimum average cluster size	2.1		$\Delta z = 0$ cm, Fig. 3.43.
Pixel hit encoding time	25	ns	
Bits per pixel hit	16	bit	
Capacity of tile link	160	$\mathrm{Mbit\,s^{-1}}$	
Aggregated capacity (Segment)	23.04	$\mathrm{Gbit\,s^{-1}}$	
Simulation results			
Average pixel occupancy	$< 2.0 \times 10^{-4}$		z=0 cm.
Average pixel occupancy	$< 5.0 \times 10^{-4}$		z=0 cm, FD=5 µs.
Data throughput	120	$\mathrm{Mbit\,s^{-1}\,Tile^{-1}}$	z=0 cm.
Data throughput	15.55	$\mathrm{Gbit\,s^{-1}\,Segment^{-1}}$	
Data throughput per unit area	365	$\mathrm{Mbit\,s^{-1}\,cm^{-2}}$	z=0 cm.
Data throughput per unit area	329	$\mathrm{Mbit\,s^{-1}\,cm^{-2}}$	Average over z.
Data throughput per link	2.58	$\mathrm{Gbit\,s^{-1}}$	
Incomplete event probability	$< 6 \times 10^{-5}$		Layer 0 segment.
Incomplete event probability	$< 2 \times 10^{-4}$		Full layer 0.

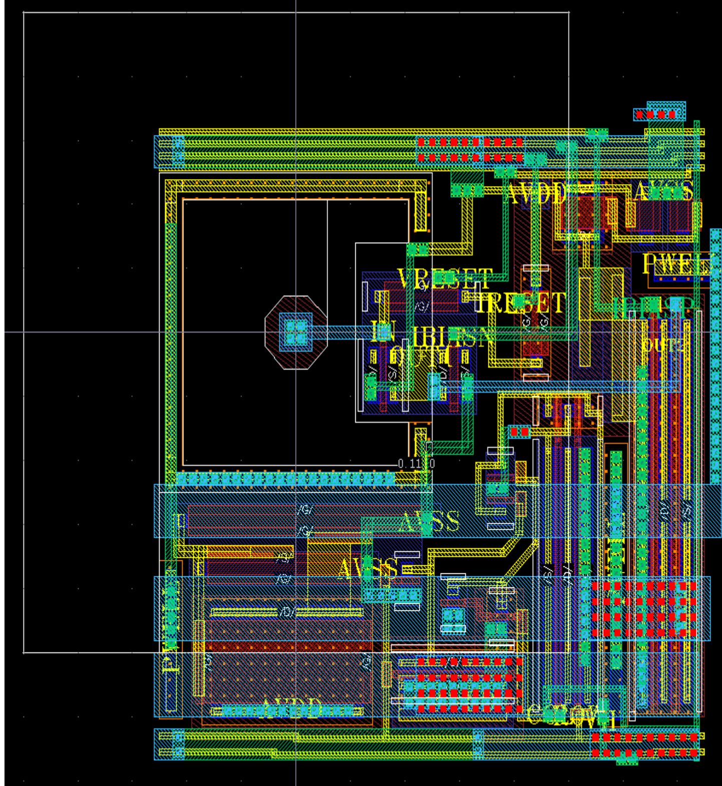
One tile (total 6) of the half of one repeated sensor unit (total 12)



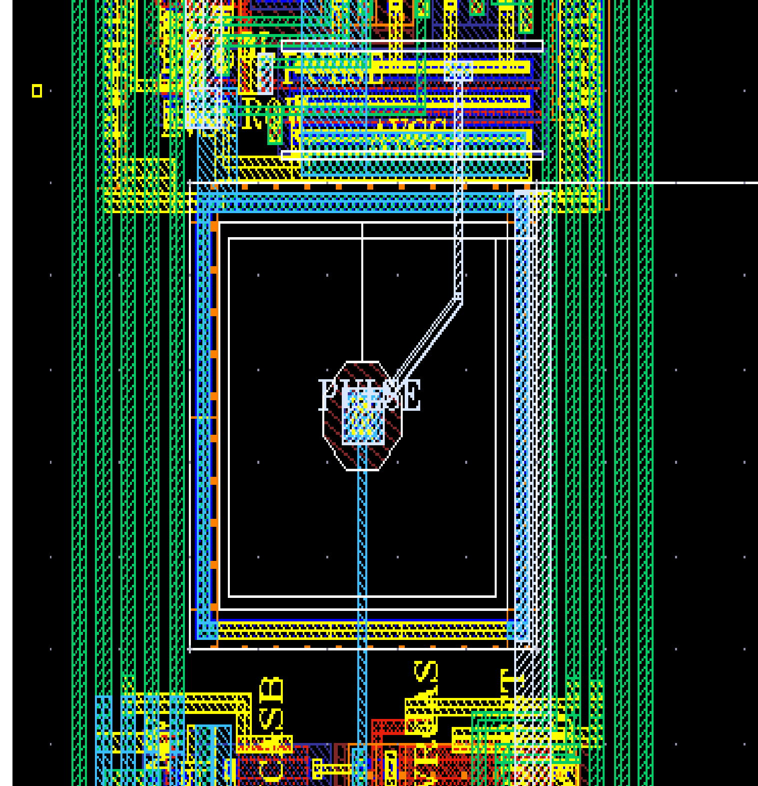
ER2芯片设计：功能优化

ALICE

- Reduce the input capacitance while balance current leakage



APTS

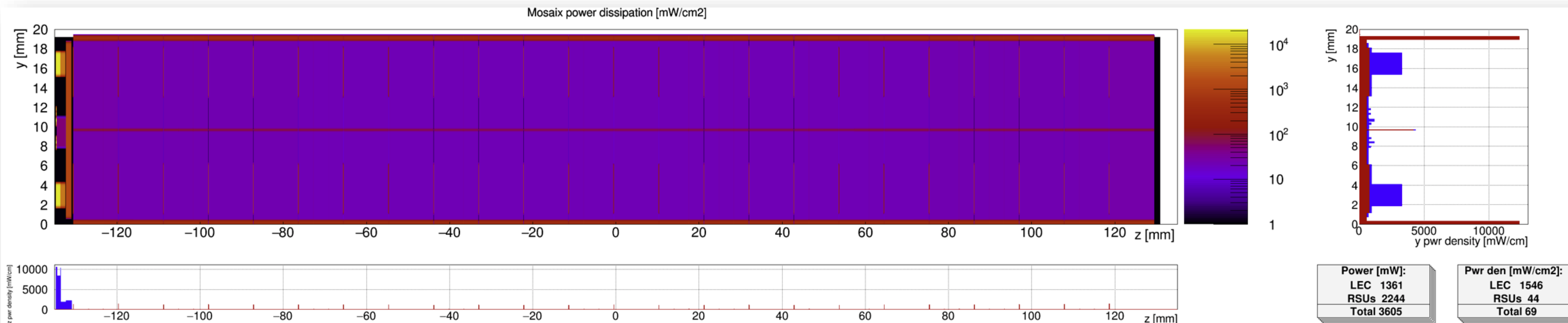


DPTS

- The length of the metal lines at the input terminal has a negligible impact on its own capacitance, approximately from 0.01 to 0.05fF.
- Concerning coupling capacitance, shortening the metal lines significantly reduces the coupling capacitance between the input terminal and the substrate PWELL, while changes in other areas are minor.
- Optimizing the layout of power lines and isolation rings can reduce some coupling capacitance.
- Additionally, removing the PULSE covering the M4 metal portion on the input terminal can decrease the coupling capacitance by approximately 0.1fF.

MOSAIX模拟验证

- MOSAIX的连线、设计规则检查、电气规则检查、天线效应检查、静电放电、高低压设计检查等物理验证与可靠性检查均已通过。
- 其余可能的设计规则检查（DRC）缺陷由代工厂进行审查。
- 对 MOSAIX 供电瞬态的模拟进行了全面的审核确认，以确保各种可能的改进随时都能为批量生产做好准备。



功率仿真分析

MOSAIX功耗模拟结果

RSU CONSUMPTION [mA] (19.564mm x 21.666mm) @ 160MHz

	TYP				MAX			
	GAVDD		GDVDD		GAVDD		GDVDD	
	Static	Dynamic	Static	Dynamic	Static	Dynamic	Static	Dynamic
12 TILES	28.42	0.00	11.72	63.22	44.97	0.00	35.21	69.22
SBB buffers			6.34	5.95			6.34	5.95
TOTAL	28.42	0.00	18.06	69.17	44.97	0.00	41.55	75.17
	28.42		87.23		44.97		116.72	
Total current [mA]	115.7				161.7			
Total power den[mW/cm2]	32.7				45.8			

RSU CONSUMPTION [mA] (19.564mm x 21.666mm) @ 80MHz

	TYP				MAX			
	GAVDD		GDVDD		GAVDD		GDVDD	
	Static	Dynamic	Static	Dynamic	Static	Dynamic	Static	Dynamic
12 TILES	28.42	0.00	11.72	32.72	44.97	0.00	35.21	35.72
SBB buffers			6.34	2.97			6.34	2.97
TOTAL	28.42	0.00	18.06	35.70	44.97	0.00	41.55	38.70
	28.42		53.76		44.97		80.25	
Total current [mA]	82.2				125.2			
Total power den[mW/cm2]	23.3				35.5			

RSU CONSUMPTION [mA] (19.564mm x 21.666mm) @ 40MHz

	TYP				MAX			
	GAVDD		GDVDD		GAVDD		GDVDD	
	Static	Dynamic	Static	Dynamic	Static	Dynamic	Static	Dynamic
12 TILES	28.42	0.00	11.72	17.47	44.97	0.00	35.21	18.97
SBB buffers			6.34	1.49			6.34	1.49
TOTAL	28.42	0.00	18.06	18.96	44.97	0.00	41.55	20.46
	28.42		37.02		44.97		62.01	
Total current [mA]	65.4				107.0			
Total power den[mW/cm2]	18.5				30.3			

RSU CONSUMPTION [mA] (19.564mm x 21.666mm) @ 20MHz

	TYP				MAX			
	GAVDD		GDVDD		GAVDD		GDVDD	
	Static	Dynamic	Static	Dynamic	Static	Dynamic	Static	Dynamic
12 TILES	28.42	0.00	11.72	9.85	44.97	0.00	35.21	10.60
SBB buffers			6.34	0.74			6.34	0.74
TOTAL	28.42	0.00	18.06	10.59	44.97	0.00	41.55	11.34
	28.42		28.65		44.97		52.89	
Total current [mA]	57.1				97.9			
Total power den[mW/cm2]	16.2				27.7			

RSU power density

Clk [MHz]	Power density [mW/cm2]			
	TYP		MAX	
	Nominal Ibias	Reduced Ibias	Nominal Ibias	Reduced Ibias
20	16.2	14.5	27.7	24.8
40	18.5	16.8	30.3	27.4
80	23.3	21.6	35.5	32.6
160	32.7	31	45.8	42.9

*) Reduced Ibias – 25% lower analog front-end consumption

ER2芯片测试计划

Task Name	Duration	Start	Finish	Predec
ITS3_11122025_v1	4362.1 day:	Thu 6/1/23	Mon 2/20/40	
Sensor ASIC	810 days?	Thu 6/1/23	Wed 7/8/26	
ER1 produced	0 days	Sat 7/1/23	Sat 7/1/23	
ER1 functional verification	494 days	Sat 7/1/23	Thu 5/22/25	
ER2 Specification review	0 days	Thu 6/1/23	Thu 6/1/23	
ER2 Design	23 mons	Thu 6/1/23	Wed 3/5/25	51
ER2 tapeout verification	4 mons	Thu 3/6/25	Wed 6/25/25	52
ER2 tapeout	0 days	Wed 6/25/25	Wed 6/25/25	53
ER2 production	8.5 mons	Thu 6/26/25	Wed 2/18/26	54
ER2 post processing	2 mons	Thu 2/19/26	Wed 4/15/26	55
ER2 babyMOSAIX delivered	0 days	Wed 4/15/26	Wed 4/15/26	56
ER2 full MOSAIX delivered	0 days	Thu 3/19/26	Thu 3/19/26	56FS-2
ER2 functional verification and performance for ER3	100 days?	Thu 2/19/26	Wed 7/8/26	
GWT-PSI chiplet testing NIKHEF Utrecht	3 mons	Thu 4/16/26	Wed 7/8/26	57
Wafer probing	25 days?	Thu 2/19/26	Wed 3/25/26	
	5 days	Thu 2/19/26	Wed 2/25/26	55
Impedance and power ramp	20 days	Thu 2/26/26	Wed 3/25/26	62
functional testing low speed interfaces	1 day?	Thu 3/5/26	Thu 3/5/26	63SS+!
functional testing high speed link testing				
babyMOSAIX	25 days	Thu 4/16/26	Wed 5/20/26	
Inspection	5 days	Thu 4/16/26	Wed 4/22/26	57
bonding	10 days	Thu 4/23/26	Wed 5/6/26	67
Impedance	10 days	Thu 5/7/26	Wed 5/20/26	68
functional tests (registers, digital, analog, THR, FHR)	10 days	Thu 5/21/26	Wed 6/3/26	69
sensor performance (lab, test beams)	0 days	Wed 5/20/26	Wed 5/20/26	69SS+:
split 6				
irradiation	35 days	Thu 4/23/26	Wed 6/10/26	
TID	5 days	Thu 6/4/26	Wed 6/10/26	71SS+:
NIEL (incl sending, reception, bondlab)	30 days	Thu 4/23/26	Wed 6/3/26	67
Irradiation testing (NIEL,TID, SEE)	220 days	Thu 1/8/26	Wed 11/11/26	
TID sensors performance tests	5 mons	Thu 6/11/26	Wed 10/28/26	76
NIEL sensors functional tests	5 days	Thu 6/18/26	Wed 6/24/26	77FS+:
NIEL sensors irradiation performance tests	5 mons	Thu 6/25/26	Wed 11/11/26	80
SEU	107 days	Thu 1/8/26	Fri 6/5/26	71SS+:
System preparation	4 mons	Thu 1/8/26	Wed 4/29/26	
SEU tests at NPI	5 days	Mon 6/1/26	Fri 6/5/26	83
SEL	137 days	Thu 1/8/26	Fri 7/17/26	71
system preparation	6 mons	Thu 1/8/26	Wed 6/24/26	
HIF tests	5 days	Mon 7/13/26	Fri 7/17/26	86
MOSAIX	35 days	Thu 3/19/26	Wed 5/6/26	
Inspection	5 days	Thu 3/19/26	Wed 3/25/26	58
bonding	10 days	Thu 3/26/26	Wed 4/8/26	89
impedance	20 days	Thu 4/9/26	Wed 5/6/26	90
yield studies	6 mons	Thu 4/23/26	Wed 10/7/26	91SS+:
functional tests (registers, digital, analog, THR, FHR)	1 mon	Thu 4/23/26	Wed 5/20/26	91SS+:
sensor performance (lab, test beams)	6 mons	Thu 5/21/26	Wed 11/4/26	94
Test beams	100 days	Wed 3/25/26	Tue 8/11/26	
TB_2026 CERN	100 days	Wed 3/25/26	Tue 8/11/26	
TB1	1 wk	Wed 3/25/26	Tue 3/31/26	
TB2	1 wk	Wed 5/13/26	Tue 5/19/26	
TB3	1 wk	Wed 6/24/26	Tue 6/30/26	
TB4	1 wk	Wed 7/15/26	Tue 7/21/26	
TB5	1 wk	Wed 8/5/26	Tue 8/11/26	
ER2 experience gaining after ER3	11 mons	Thu 7/9/26	Wed 5/12/27	59

Qtr 4, 2025: Oct, Nov, Dec | Qtr 1, 2026: Jan, Feb, Mar | Qtr 2, 2026: Apr, May, Jun | Qtr 3, 2026: Jul, Aug, Sep | Qtr 4, 2026: Oct, Nov, Dec

Thinning and dicing starts

First MOSAIX

First babyMOSAIX

3/19

5/20

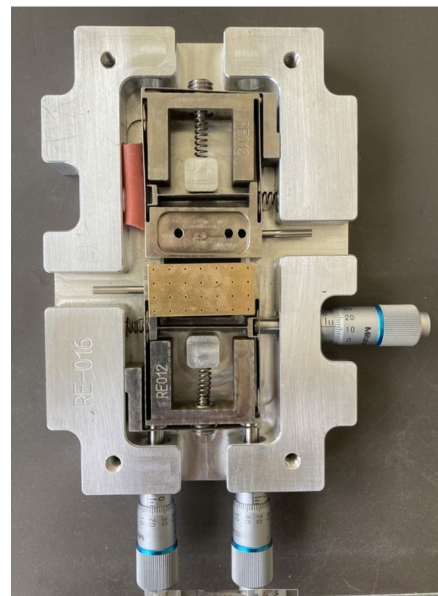
5 weeks of actual beam time

CERN 2026 Test Beams

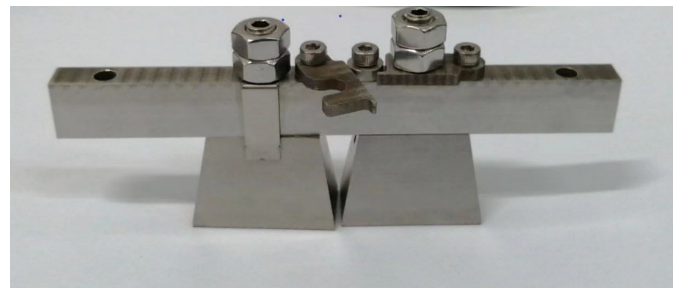
ELSA, Frascati, Jlab (tbc)

FoCal硅像素层研制进展: 组装夹具研制

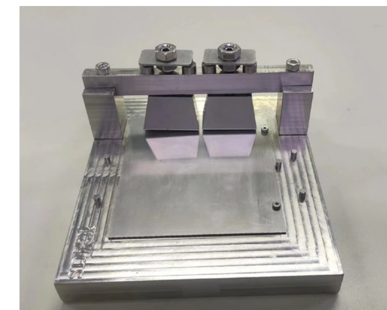
单芯片组装夹具研制



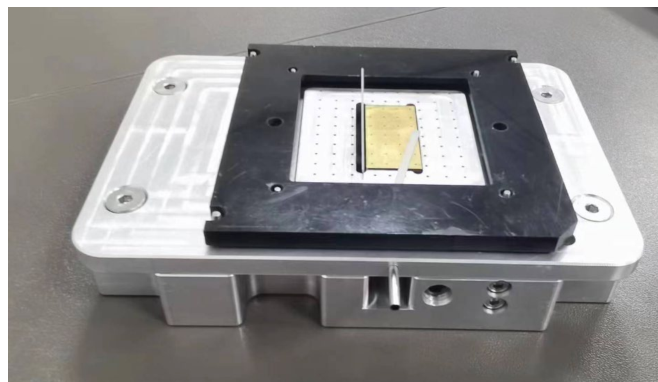
硅像素层模块组装夹具研制



在2023年底生产的第一次夹具测试样（含两种结构）



2024年4月生产的第二个夹具测试样



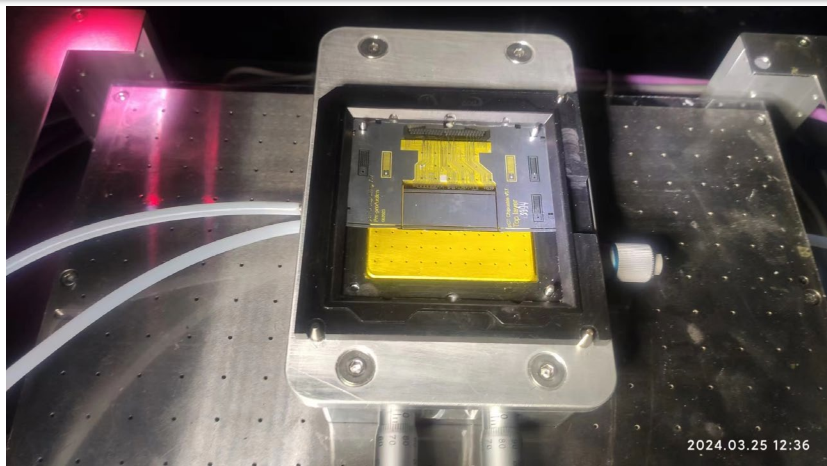
首次加工失败
通过热处理释放应力得以解决

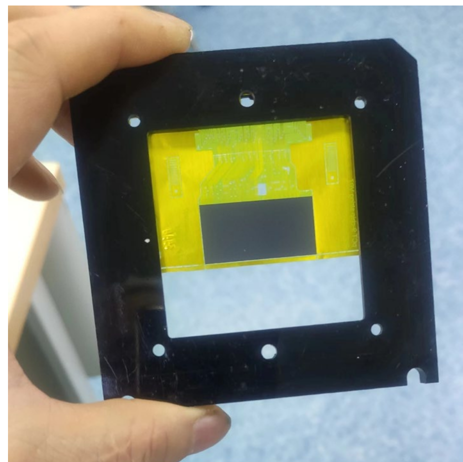
- 2023 年 5 月 带 到 CERN进行验证
- 通过验证后，生产了3套，寄往各实验室
- 真空密闭性检验
- 用千分头进行功能测试

2024年8月生产的最终的组装夹具
2024年11月底寄到挪威奥斯陆

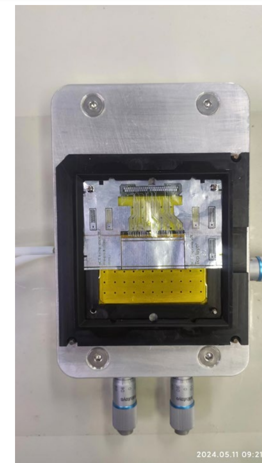
FoCal硅像素层研制进展: 组装流程测试

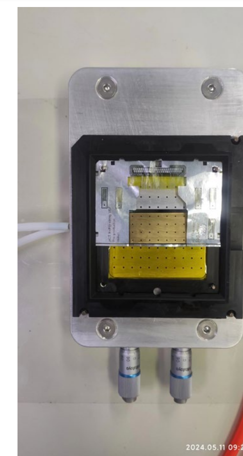
ALICE



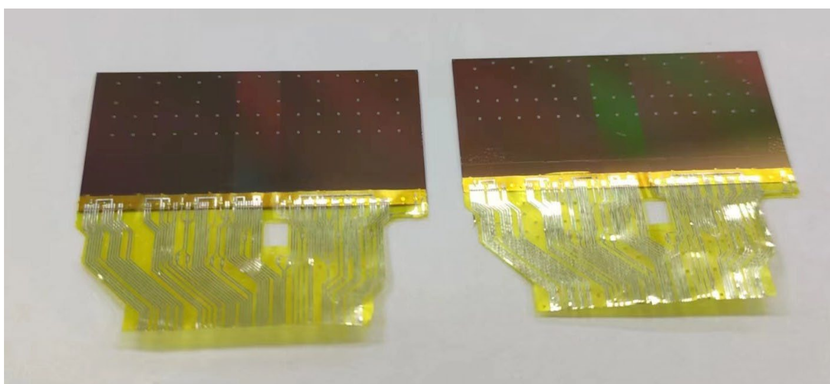


用F&K Delvotec G5 64000绑线机实现 SpTAB绑定

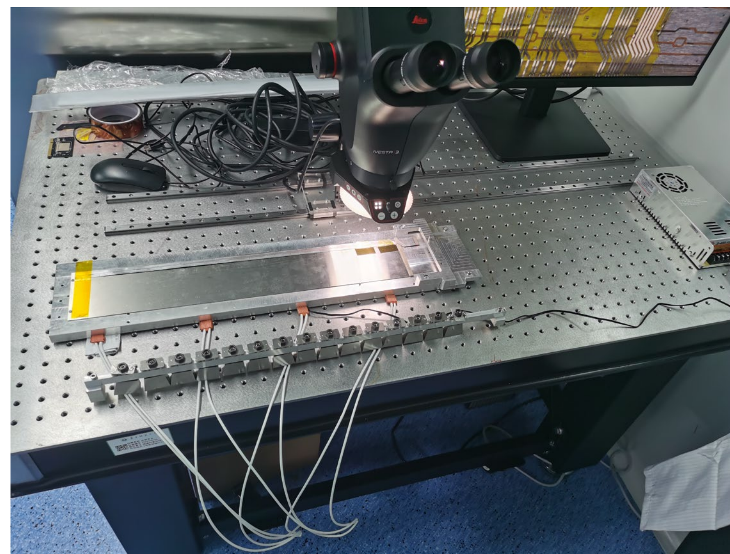


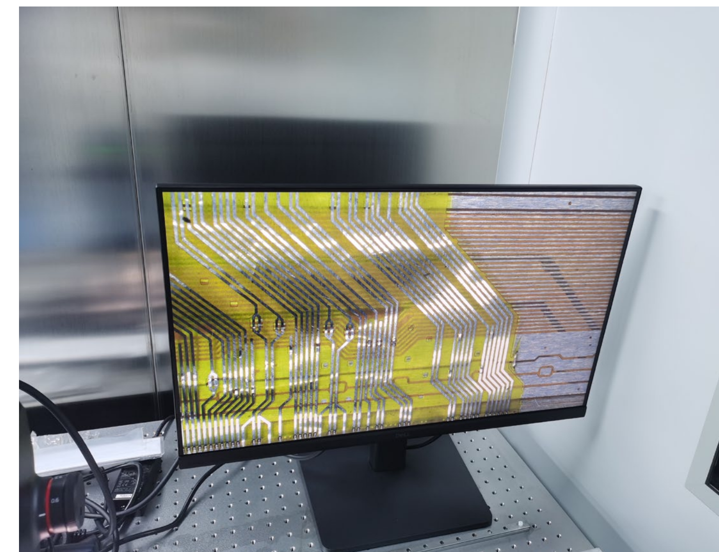


用手术刀裁下待组装部分



裁下的待组装部分





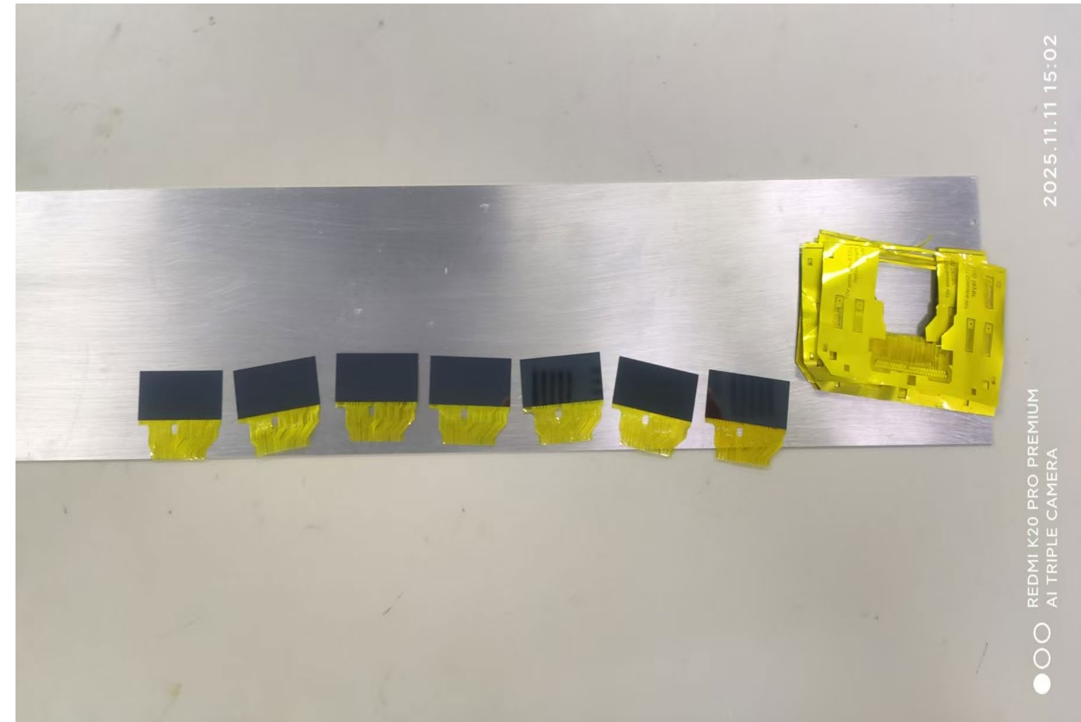
用工装夹具在带柔性条的载板上摆放待组装的芯片

Preparation for mass production (I)

ALICE

Steps of assembling ALPIDE to chipcable established

1. Placing chipcable in plastic frame, blowing chipcable by air
2. Placing chip on jig
3. Applying glue on chip
4. Placing framed chipcable on jig
5. Aligning chipcable with chip (using screws of the jig)
6. Moving jig under bonder
7. SpTABing chipcable to chip
8. Moving back jig from bonder
9. Visual inspection
10. Placing chip assembly on flat surface
11. Placing weight above the chip from chipcable side
12. Curing glue ~1-1,5h at room temperature
13. Preliminary functional test (PTB)
14. Protecting SpTAB joints by glue
15. Final functional test (PTB)
16. Cutting-out work area of chip assembly



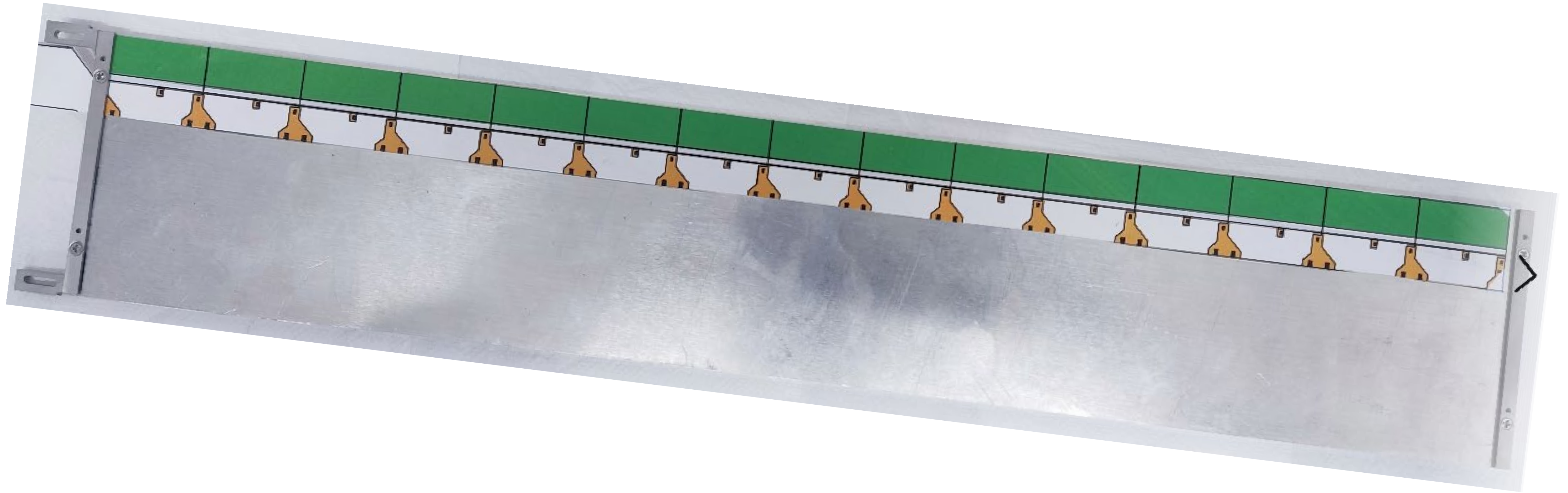
Preparation for mass production (II)

Steps of assembling chipcable with chip to flex on carrier

1. Applying glue on the carrier
2. Applying glue on the flex
3. Placing chip on carrier
4. Aligning chip
5. Placing chip assembly on flat surface
6. Placing weight above the chipcable (above the chip and flex)
7. Precuring glue ~20-30min at room temperature
8. Visual inspection (aligning)
9. SpTABing chipcable to flex
10. Preliminary functional test (PTB)
11. Final curing ~1h at room temperature
12. Protecting SpTAB joints by glue
13. Curing ~2h at room temperature
14. Final functional test (PTB)
15. Visualinspection

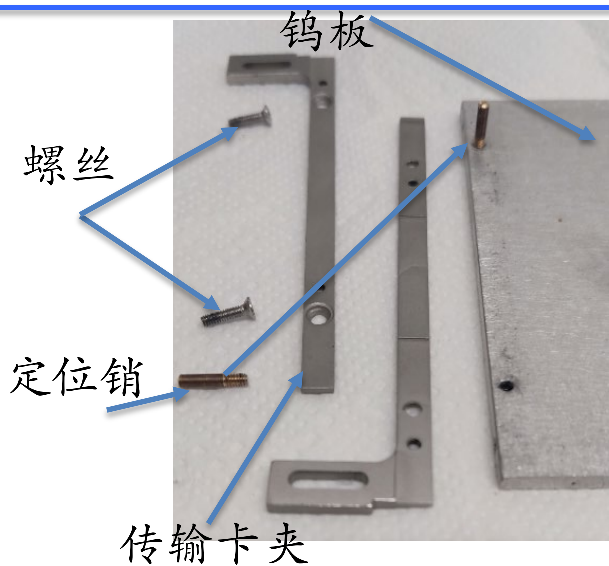
- Waiting for flex on carrier delivered from Ukraine
- Waiting for PTB delivered from Bergen
  - Some issue with firmware to be fixed

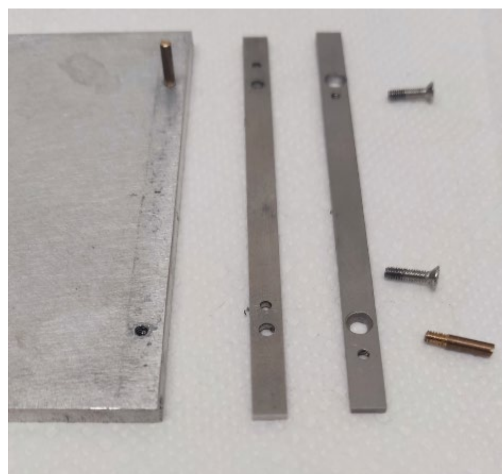
硅像素层模块机械实体样生产



- 生产了两套模块实体样组件
- 一套是铝合金的，一套是不锈钢的

硅像素层模块机械件组装流程





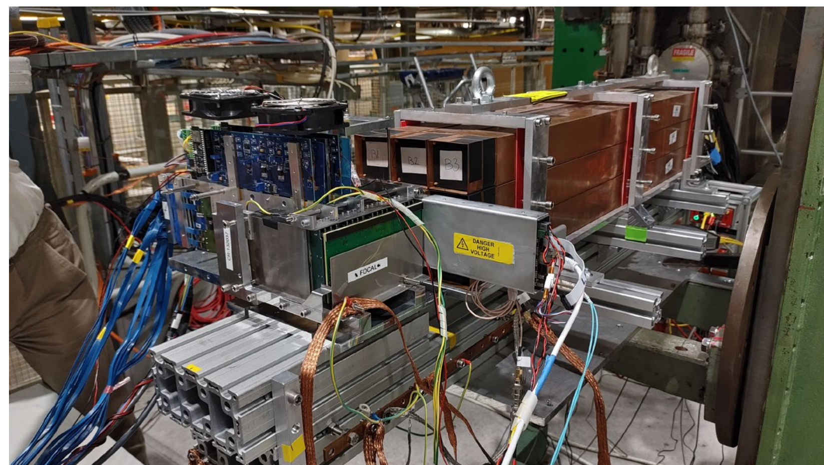
所有部件

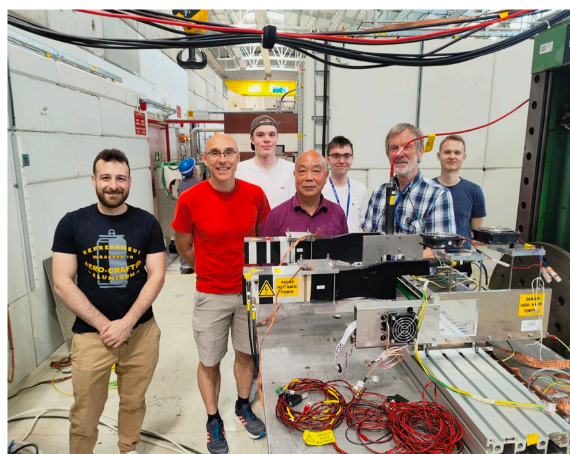
安装垫片

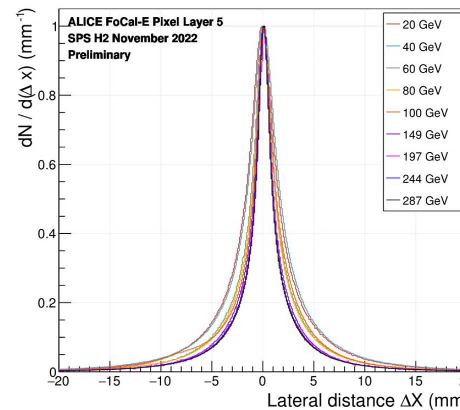
安装两个载板
和顶部垫片

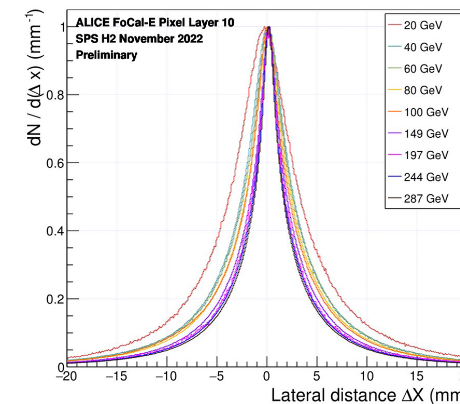
固定所有部件，定位销
用于组装下一个模块

FoCal硅像素层研制进展: 束流测试及其数据分析

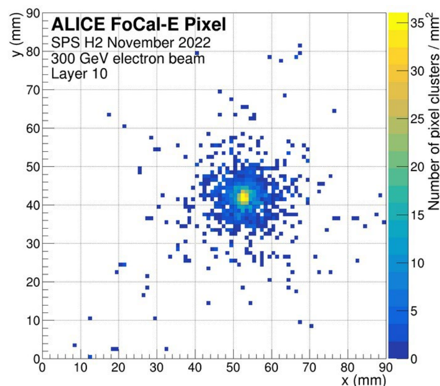


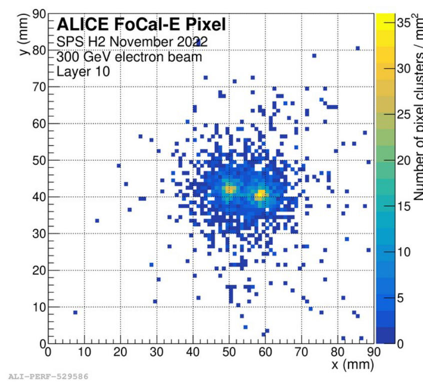


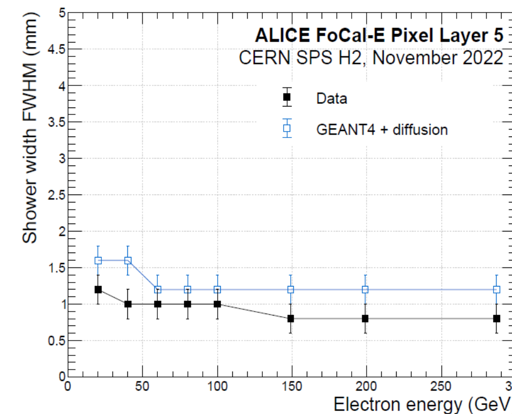




JINST 19 （2024）P07006 arXiv:[2311.07413](https://arxiv.org/abs/2311.07413)







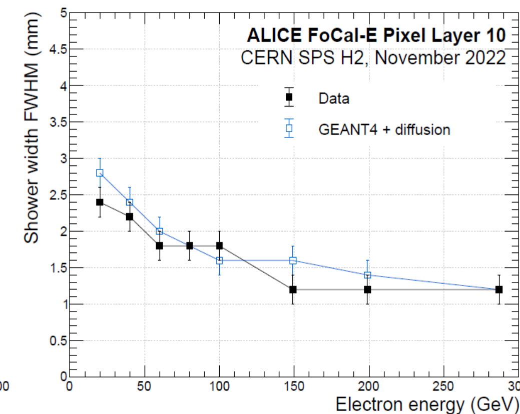


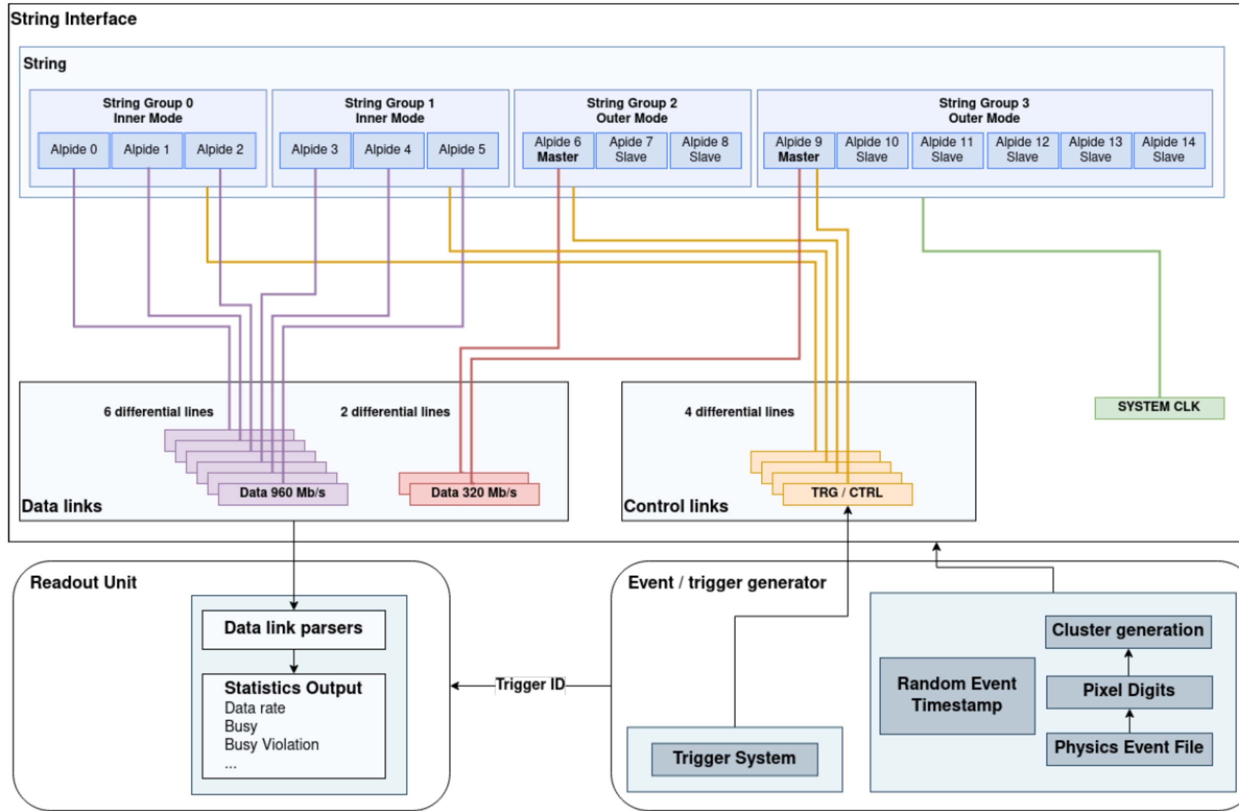
Figure 33. Measured and simulated FWHM for layer 5 (left panel) and 10 (right panel) versus electron energy. The error bars represent an uncertainty of 0.2 mm.

- 何柳参与了2022年9月份的束流测试
- 易杰和周老师参与了2023年6月份的束流测试
- 何柳负责分析了硅像素层束流测试数据，结果已发表在JINST上

- 簇射横向分布半高宽度可达1 mm 左右，达到中期考核指标

SystemC 模拟

易杰负责完善了SystemC 模拟框架



- SystemC 模拟结果已经包含在2024年3月批准的技术设计报告TDR中.

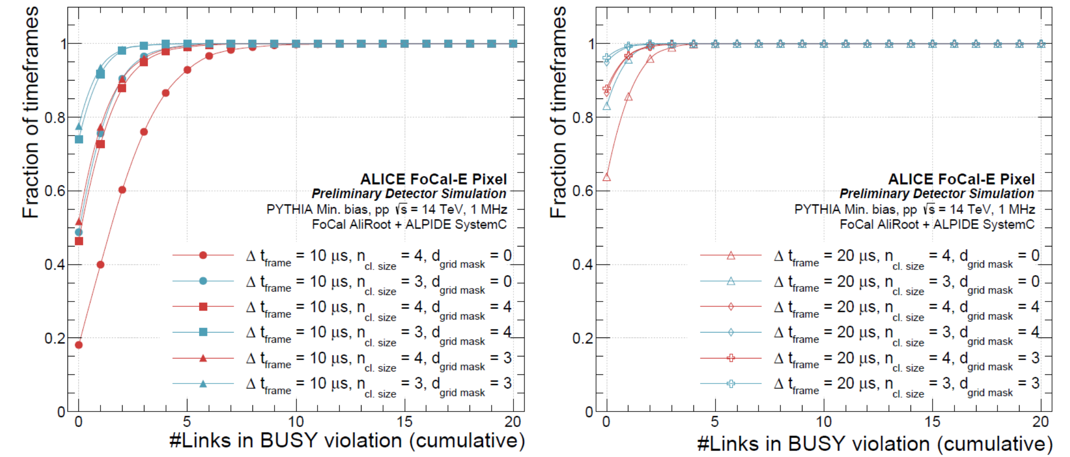
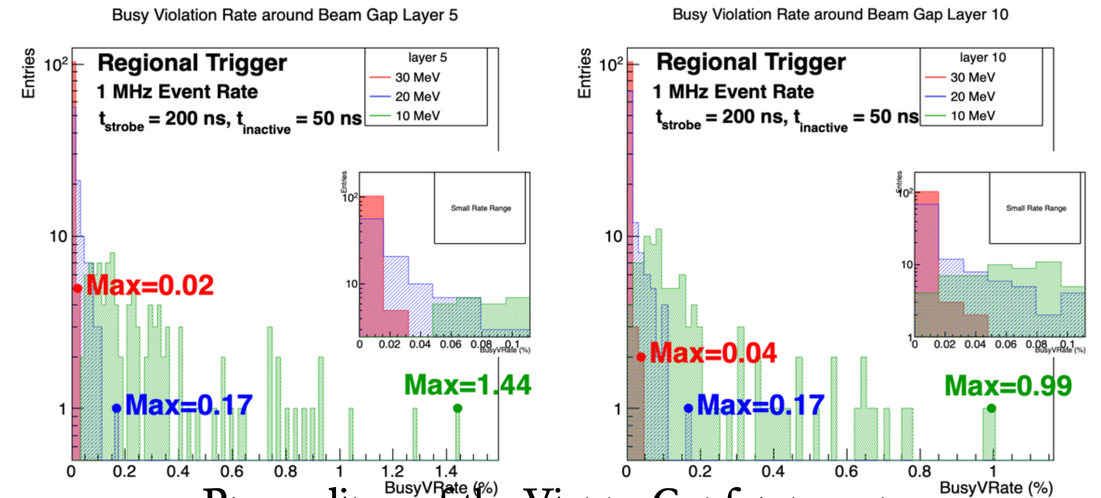
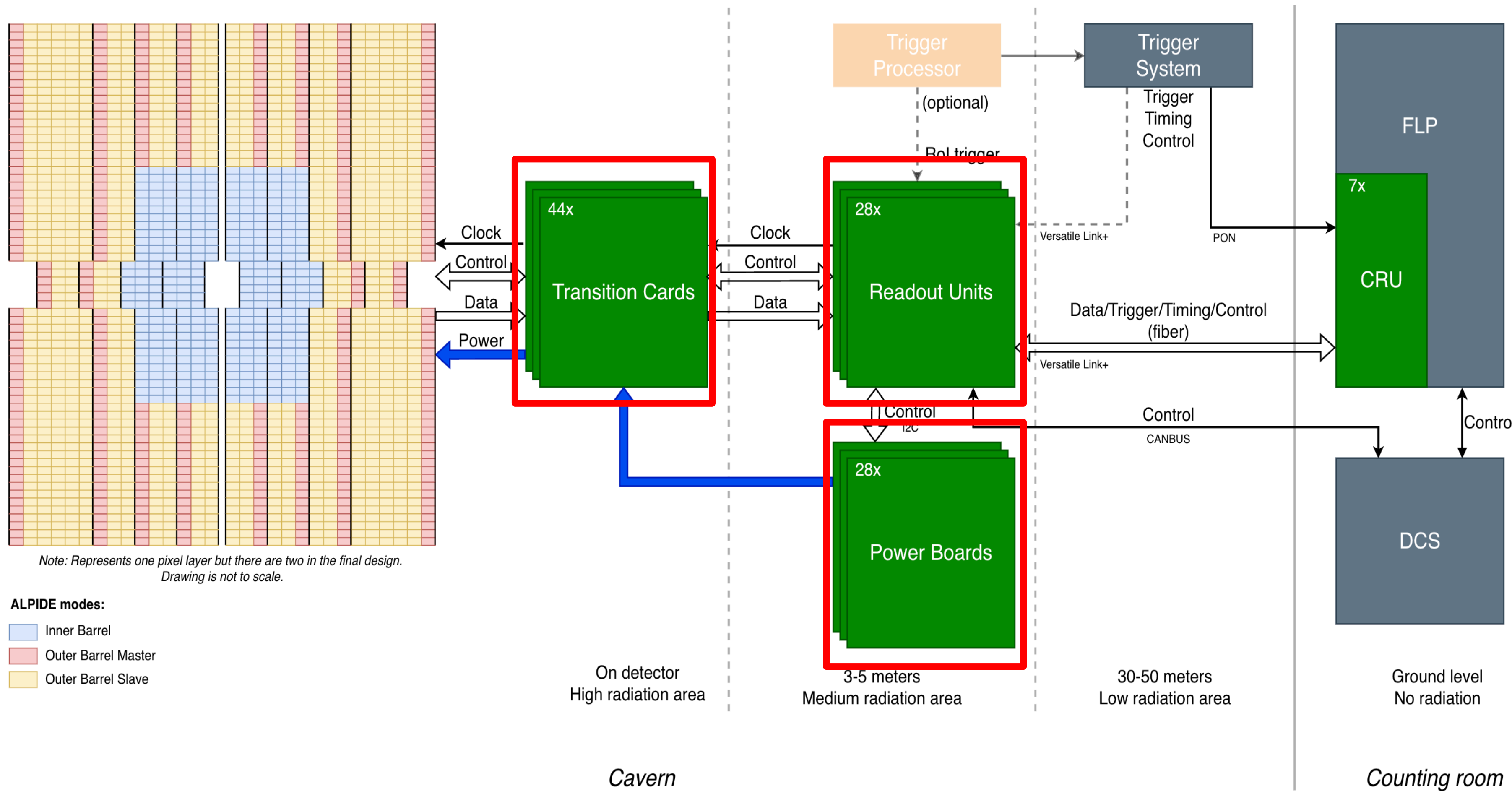


Fig. A.19: Fraction of frames with the cumulative number of links in BUSY violation for pp collisions, i. e. #Links with grid mask of $d_{\text{grid mask}} = 4$ and $d_{\text{grid mask}} = 3$, with two different timeframe lengths $\Delta t_{\text{frame}} = 10\,\mu\text{s}$ (left) and $\Delta t_{\text{frame}} = 20\,\mu\text{s}$ (right). The cumulative curves show the probability to encounter a timeframe with a maximum of #Links in BUSY violations.



Proceedings of the Vienna Conference on Instrumentation 2025

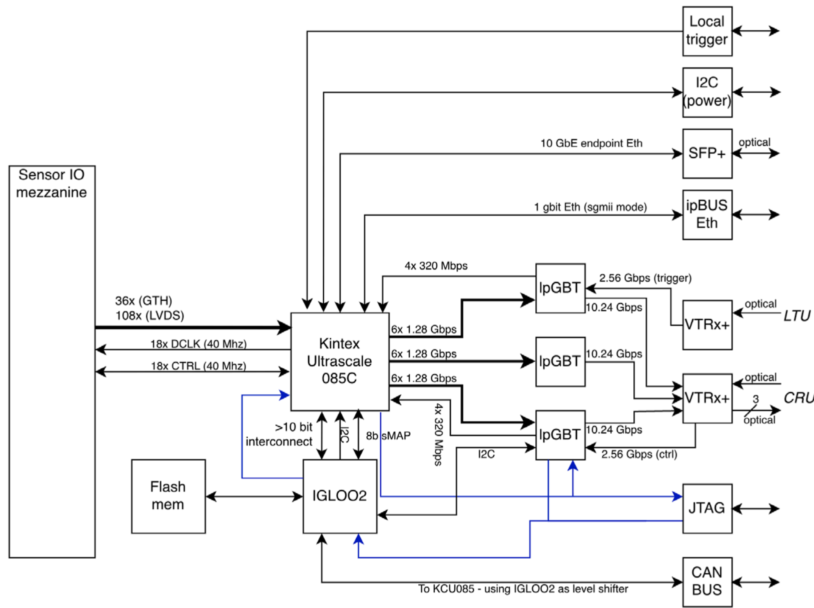
硅像素层读出电子学系统



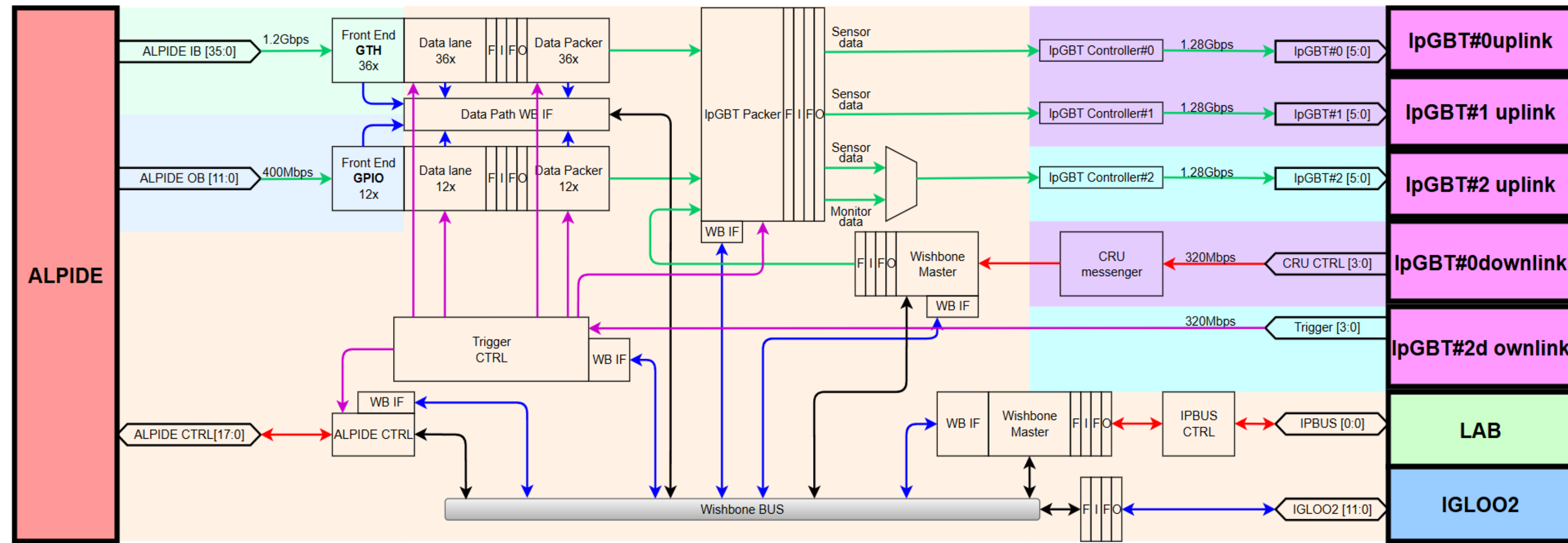
- ✓ 参加像素层读出系统设计
- ✓ 负责像素层读出单元主FPGA固件开发
- ✓ 负责转接板，背板设计与生产
- ✓ 参加电源板设计，负责电源板生产

硅像素层读出单元（RU）

ALICE



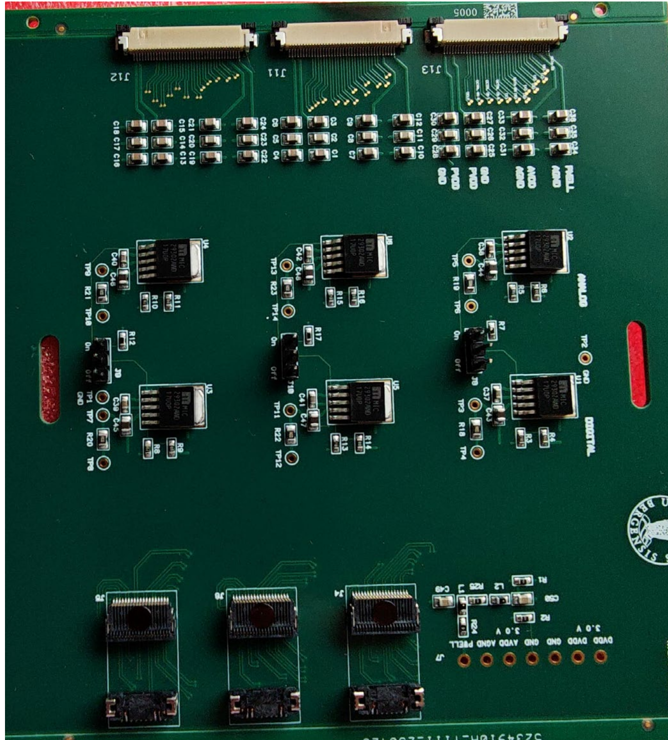
读出单元框图



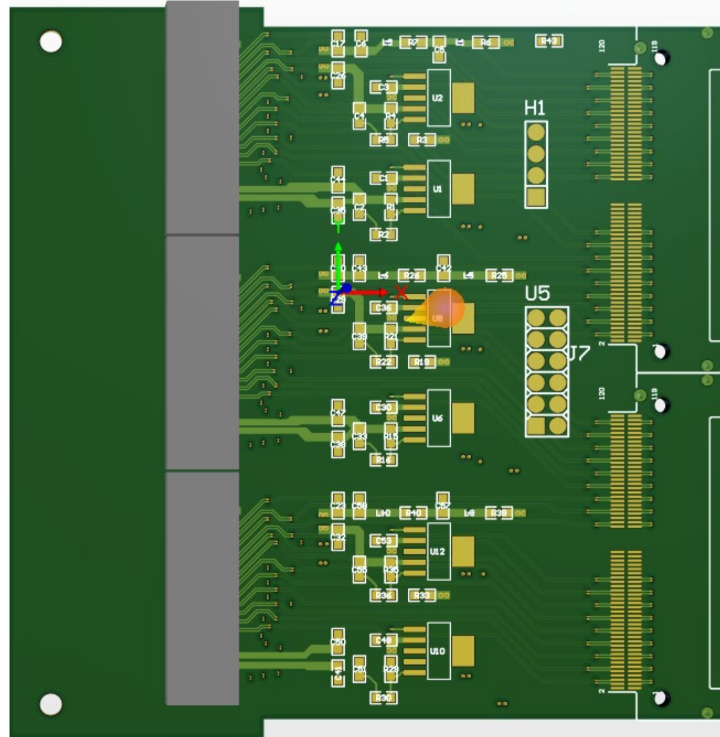
主FPGA固件逻辑模块图

- ✓ 参与了读出单元器件选型，功能定义，系统设计
- ✓ 确定主、辅FPGA，和数据传输链路（采用lpGBT和VTRX+）
- ✓ 参与了HPIO数据链路测试，HPIO-lpGBT-VTRX+测试
- ✓ 完成了主FPGA功能定义，模块划分，资源、功耗估计以及第一版测试固件设计
- ✓ 提出了三种lpGBT数据打包方案，正在进行数据传输效率模拟

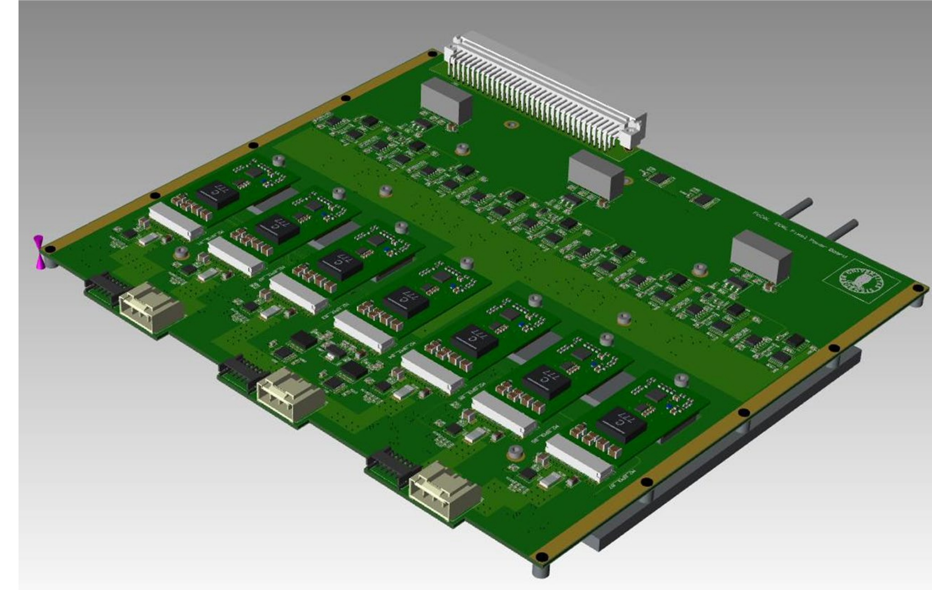
硅像素层读出电子学设计与生产



转接板测试板



FoCal转接板



FoCal电源板

- ✓ 设计了转接板测试板，五月份在国内生产后送至卑尔根大学进行测试
- ✓ 完成了转接板原理图和layout设计，等待检查和在中国生产
- ✓ 参与了电源板设计，等待最终检查和在中国生产

技术指标调整发言人证明信

ALICE Collaboration
https://alice-collaboration.web.cern.ch

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Email: marco.van.leeuwen@cern.ch

Our reference: ALICE/MvL/mk/06-11-2024/093

Geneva, 6 November 2024

The CCNU group is participating the design and characterization of the ITS3 sensors with 3 students who are stationed at CERN to work together with the design and characterization teams. The goal of the final design is to design a large-scale stitched pixel sensors with integrated readout circuits. Based on the R&D experience and the requirements of the geometry of the final detector, the final design will use a pixel size of 20.8 μm x 22.8 μm, which is expected to give a space point resolution of better than 5 μm and a power density below 50 mW/cm^2. While the pixel size is slightly larger than the goal that was originally formulated

A key design goal is that the detector can be air cooled, in order to keep the material budget in the active area to a minimum. R&D on mechanical integration and air cooling solutions has demonstrated that the detector can cooled effectively with (average) power density up to about 50 mW/cm^2 over the full sensor area. The project is now moving towards the final design phase.

The CCNU group is participating the design and characterization of the ITS3 sensors with 3 students who are stationed at CERN to work together with the design and characterization teams. The goal of the final design is to design a large-scale stitched pixel sensors with integrated readout circuits. Based on the R&D experience and the requirements of the geometry of the final detector, the final design will use a pixel size of 20.8 μm x 22.8 μm, which is expected to give a space point resolution of better than 5 μm and a power density below 50 mW/cm^2. While the pixel size is slightly larger than the goal that was originally formulated

in the Letter of Intent, the impact on the overall performance was evaluated to be very small. A more detailed discussion can be found in the Technical Design Report (ALICE-TDR-021).

The design of the final prototype sensor is progressing well and we expect to submit the design for production in 2025. ALICE and the ITS3 project welcome the contributions of the CCNU group to the design and testing of prototypes and look forward to the continued collaboration in the coming years.

Yours sincerely,

Dr. Marco van Leeuwen
ALICE collaboration Spokesperson