

Development of MAPS Sensors for the LHCb Upgrade II Upstream Tracker

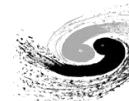
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Institute of High Energy Physics, CAS (IHEP)

on behalf of the **COFFEE** collaboration & the LHCb UP team

The 12th China LHC Physics Conference (CLHCP2026), Wuhan

The LHCb Upgrade II



中国科学院高能物理研究所
Institute of High Energy Physics, CAS



Upstream Pixel

UT → UP

- MAPS detector

Upgrade I (Run 3, 4)

$$\mathcal{L}_{\text{peak}} \sim 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$$

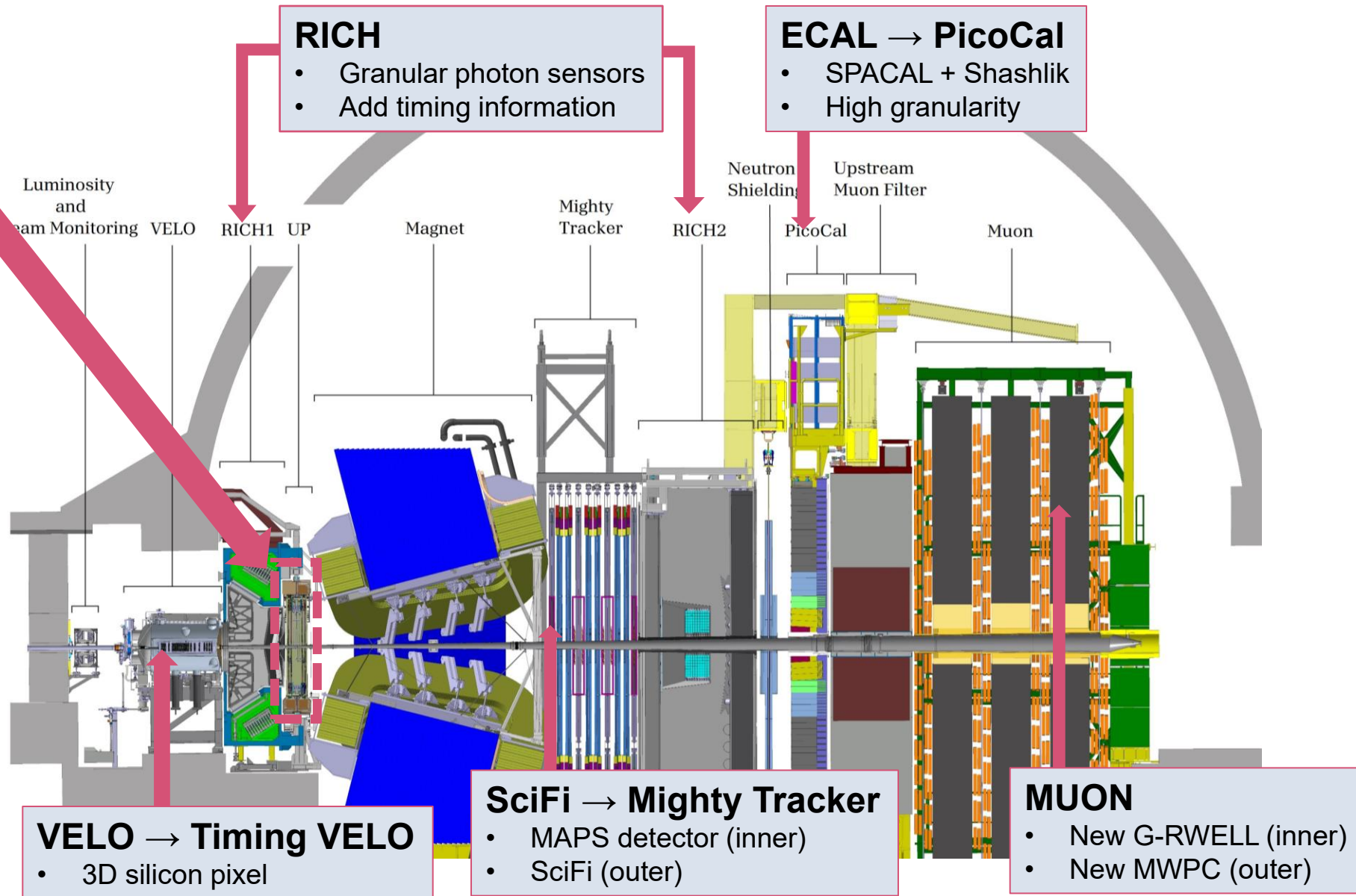
$$\mathcal{L}_{\text{int}} \sim 50 \text{ fb}^{-1}$$



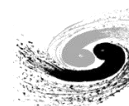
Upgrade II (Run 5)

$$\mathcal{L}_{\text{peak}} \sim 1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$$

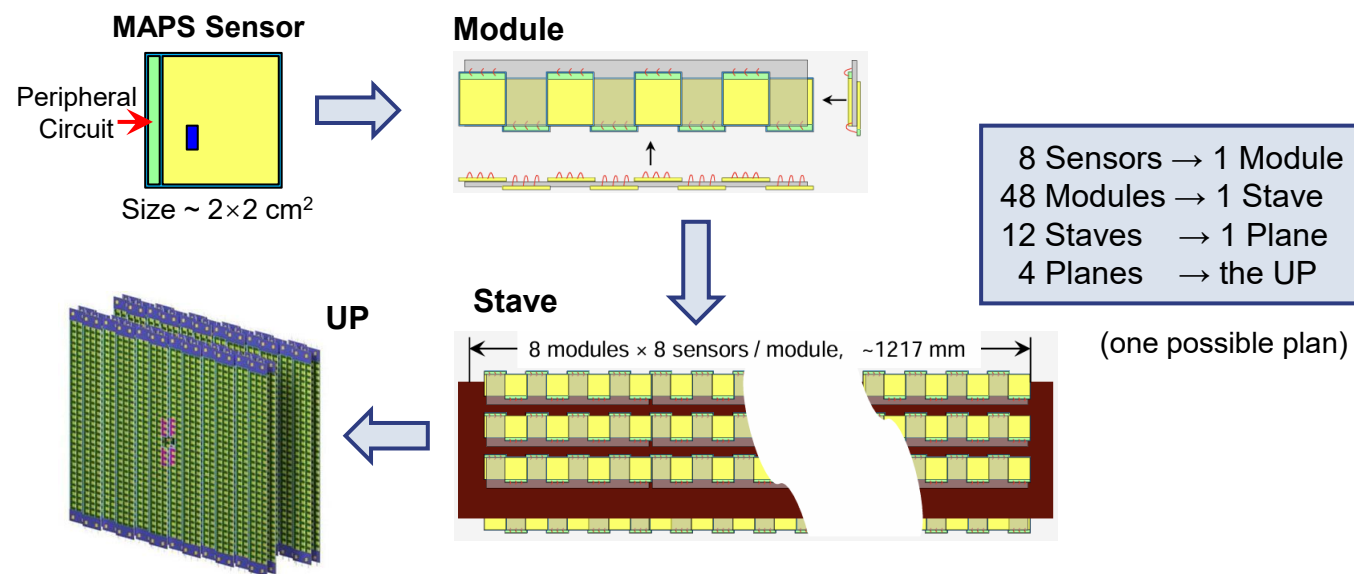
$$\mathcal{L}_{\text{int}} \sim 300 \text{ fb}^{-1}$$



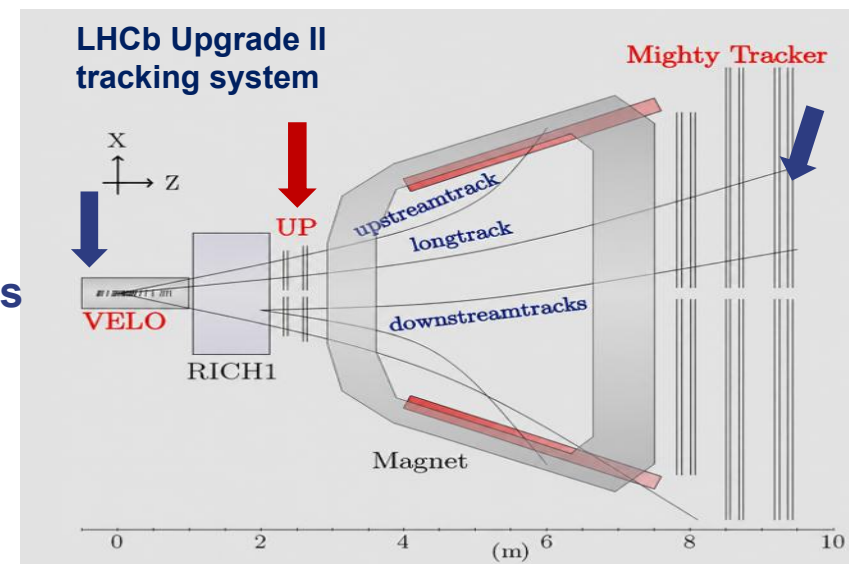
UP Detector Layout



- UP is the middle component of LHCb tracking system
 - crucial for **suppressing ghost tracks**
 - crucial for **improving track momentum resolution**
 - crucial for **reconstruction efficiency of tracks from long-lived particles**
- UP module prototyping: detailed in next [Zhijie's talk](#)



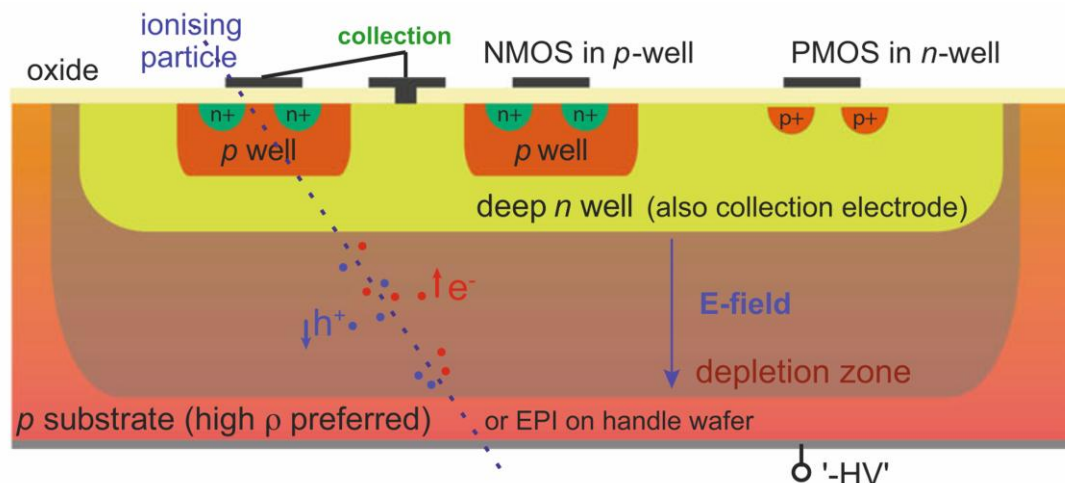
- serial powering: detailed in [Tianyu's talk](#)
- electronics: detailed in [Hanbing's talk](#)
- cooling: detailed in [Tiange's talk](#)



Parameter	UP specification
spatial resolution	$\sim 10 \mu\text{m}$
time resolution	3 to 5 ns
max. hit rate	91.2 MHz/cm^2
substrate thickness	100 to $200 \mu\text{m}$
in-time efficiency	$> 99\%$ within 25 ns
transmission rate	N links of 1.28 Gbit/s ($N \leq 7$)
NIEL	$3 \times 10^{15} n_{\text{eq}}/\text{cm}^2$
TID	190 MRad
power consumption	$\leq 200 \text{ mW/cm}^2$

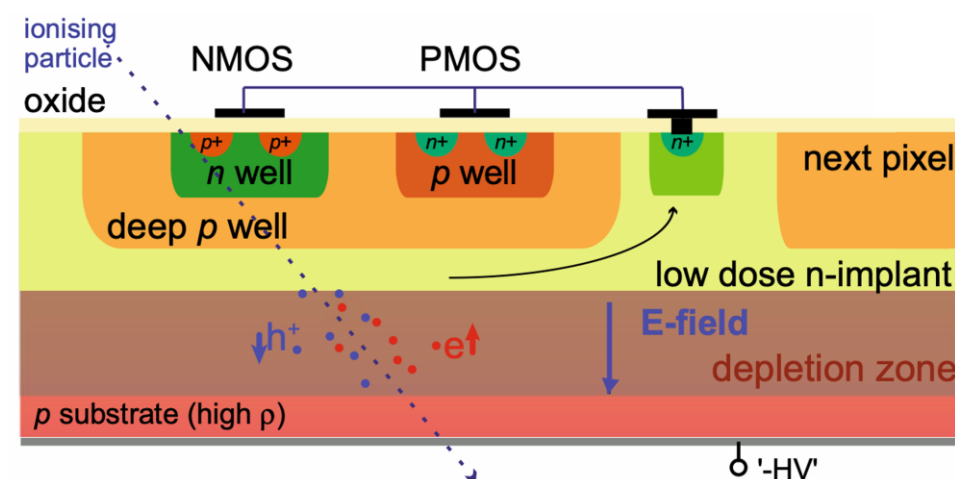
solution: MAPS-based sensors

large electrode MAPS in HV-CMOS technology



- Front-end **inside** collection electrode
- **Intrinsic high radiation tolerance**
- High breakdown voltage & **large depletion zone**
 - more electron-hole pairs
 - faster charge collection
- High sensor capacitance
 - Higher noise & power consumption

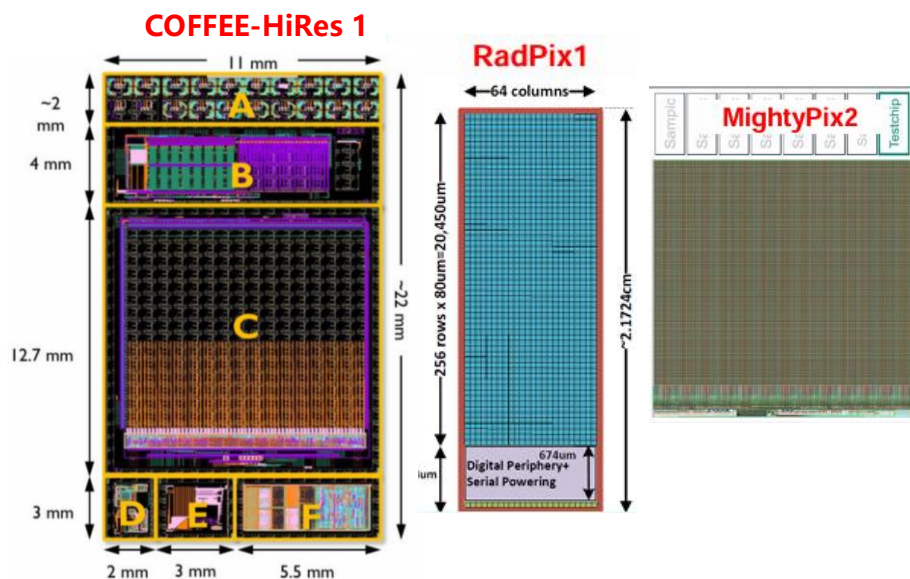
small electrode MAPS in CMOS technology



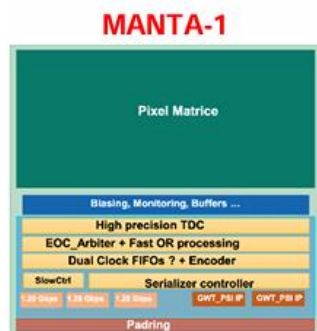
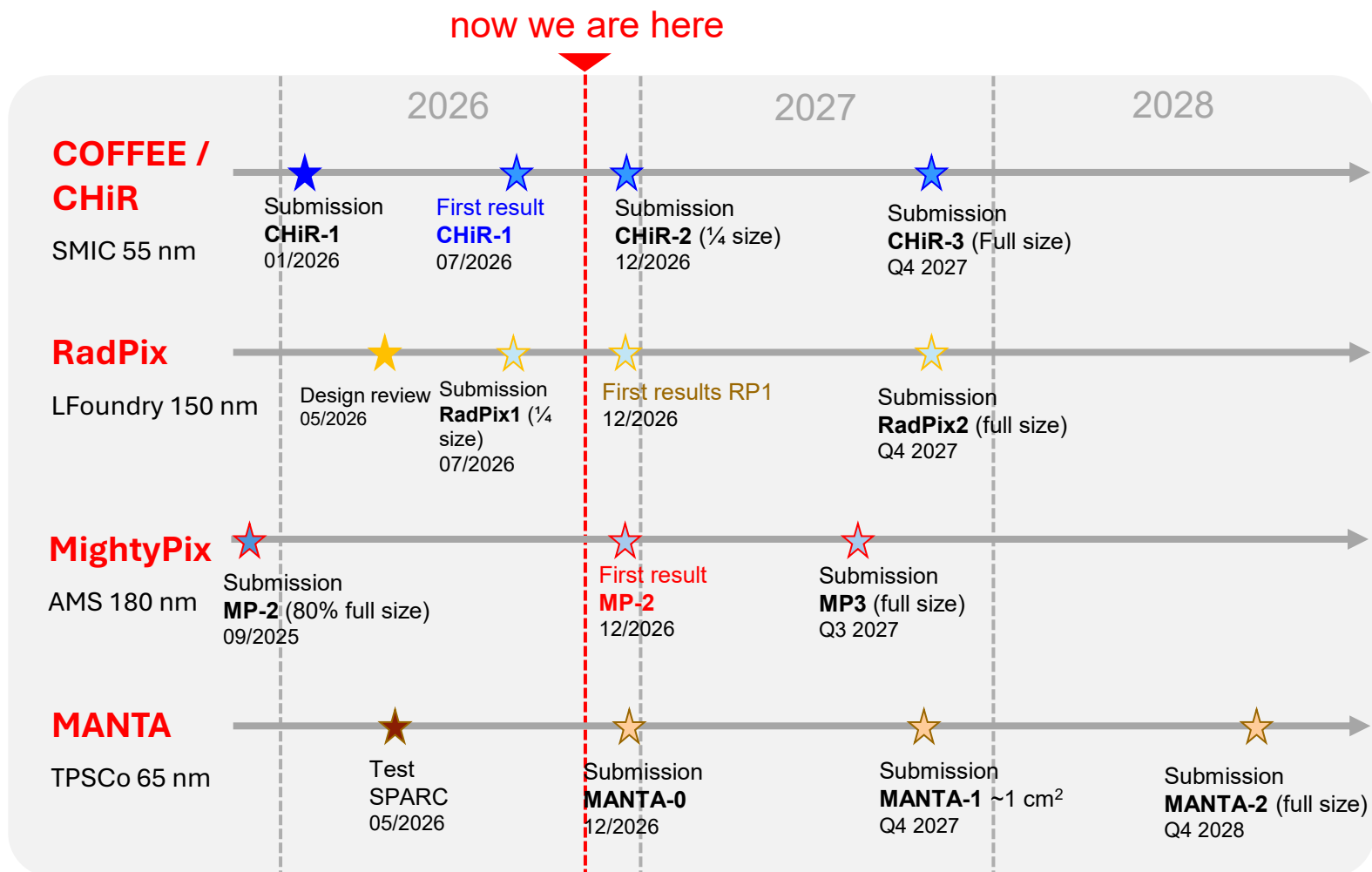
- Front-end **outside** collection electrode
- Radiation tolerance relies on process modification
- Low breakdown voltage & limited depletion zone
 - limited electron-hole pairs
 - limited charge collection speed
- **Low sensor capacitance**
 - Lower noise & power consumption

Candidates of UP MAPS sensor

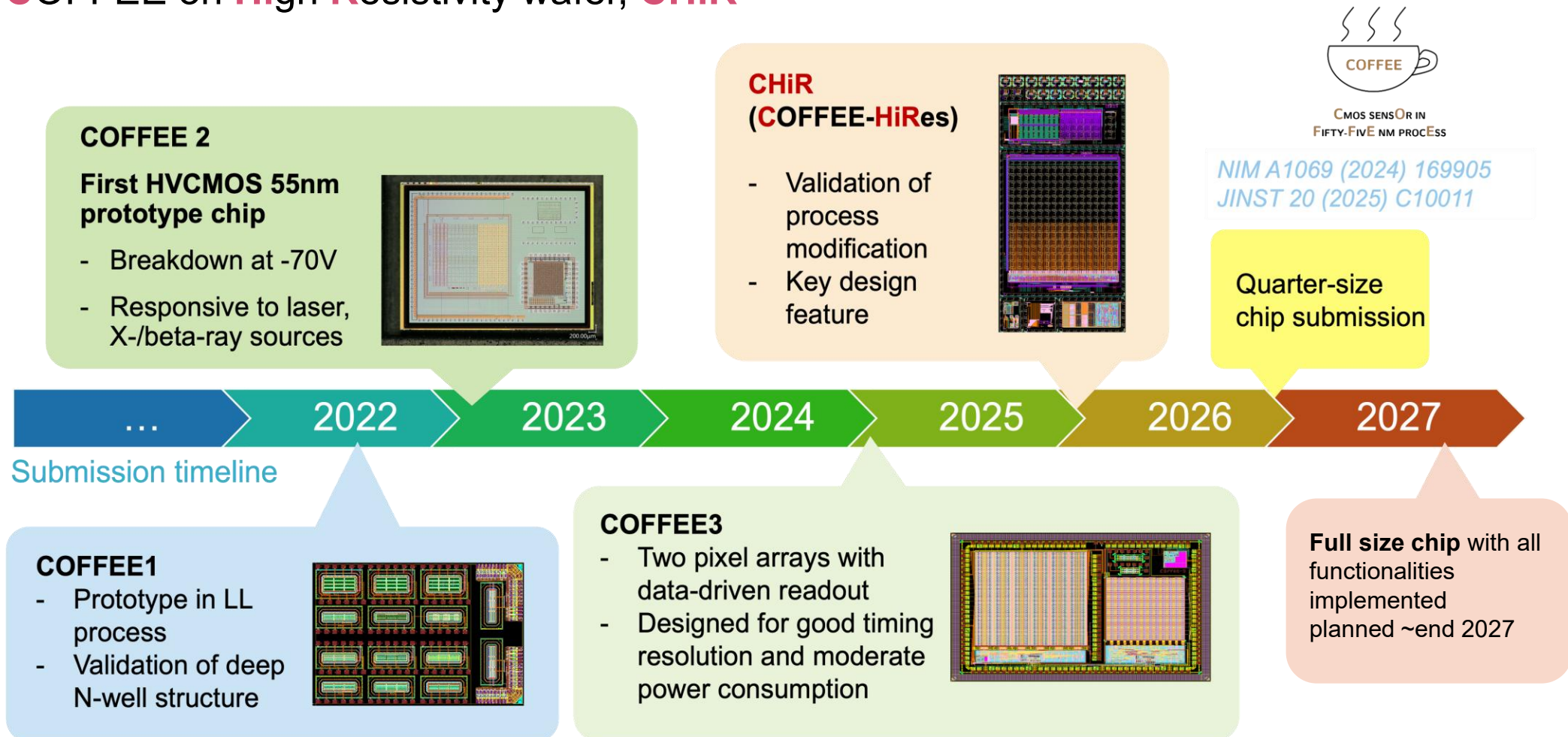
- investigating **HV-CMOS** technology:



- alternative **CMOS** technology:



- ❑ CMOS sensOr in Fifty-FivE nm procEss, **COFFEE**
- ❑ COFFEE on HiGh Resistivity wafer, **CHiR**



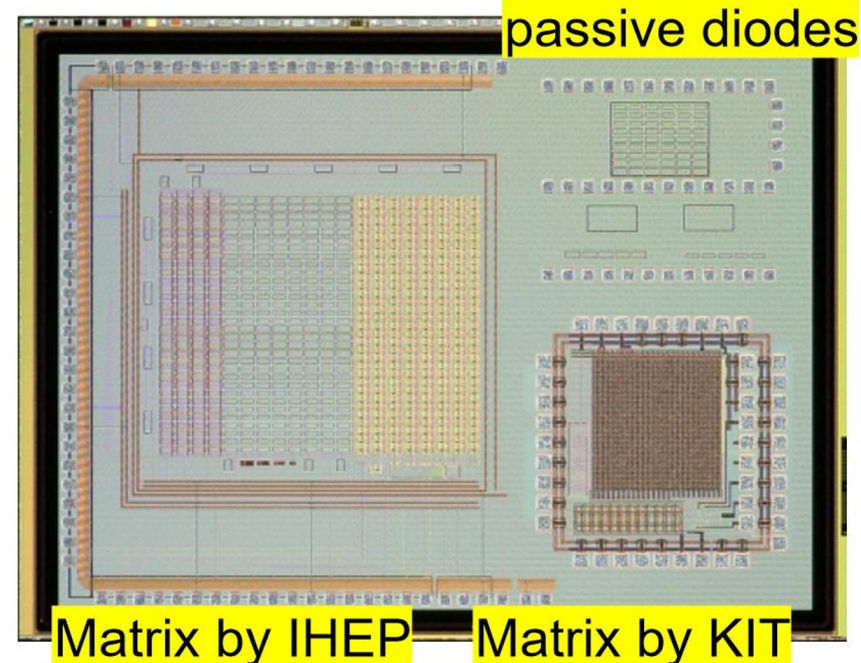
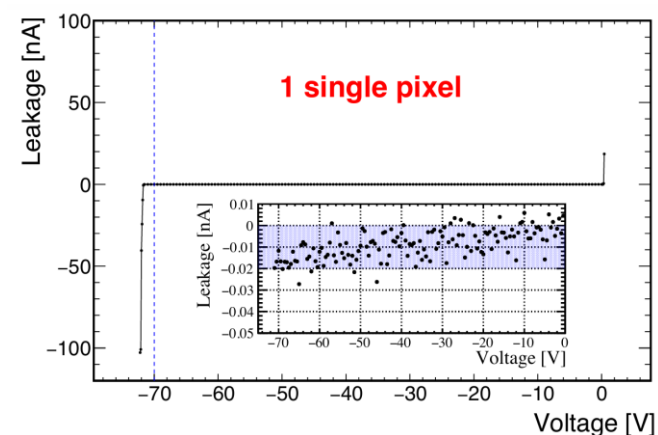
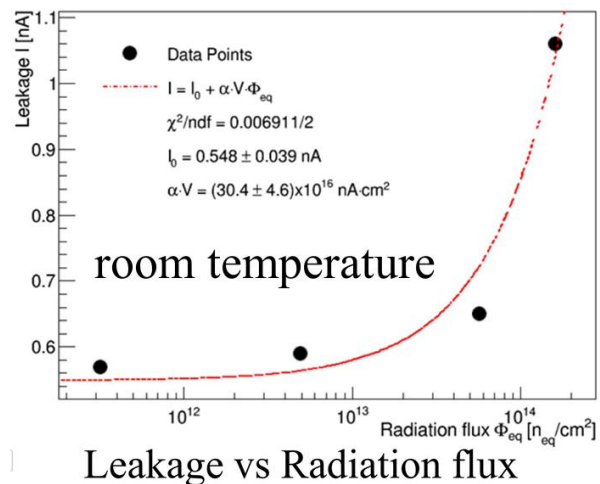
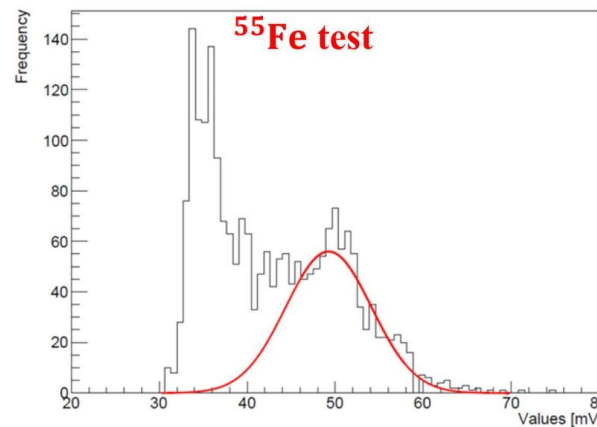
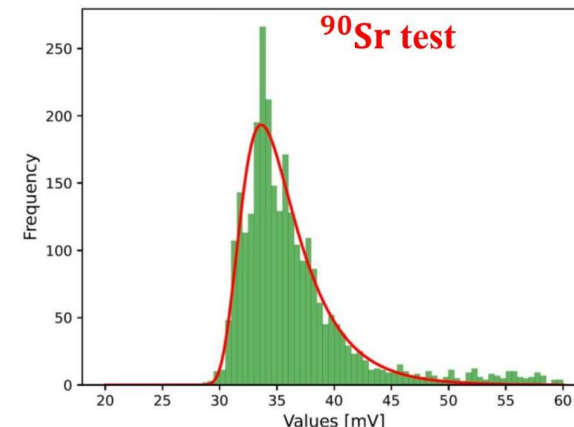
□ COFFEE2: prototype with analogue frontend

- passive diodes for sensor characterizing
- R&D for pixel electrode structure, in-pixel amplifier & comparator

□ Many results from COFFEE2

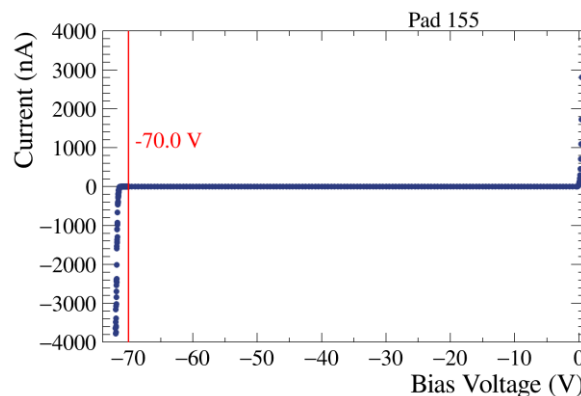
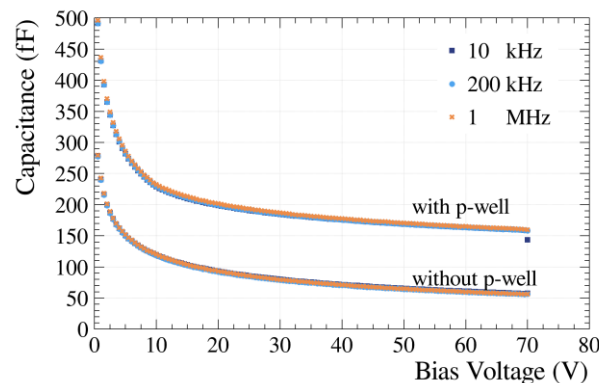
- IV / CV performance on 10 $\Omega \cdot \text{cm}$ wafer
- irradiation tolerance on sensor study @CSNS 80 MeV proton beam
- response to radiation source ^{55}Fe , ^{90}Sr

[CLHCP2025](#)



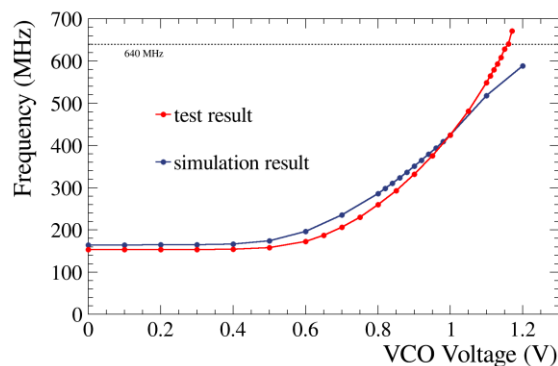
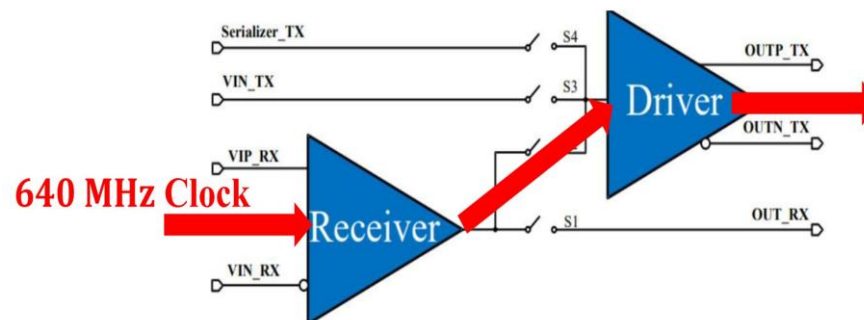
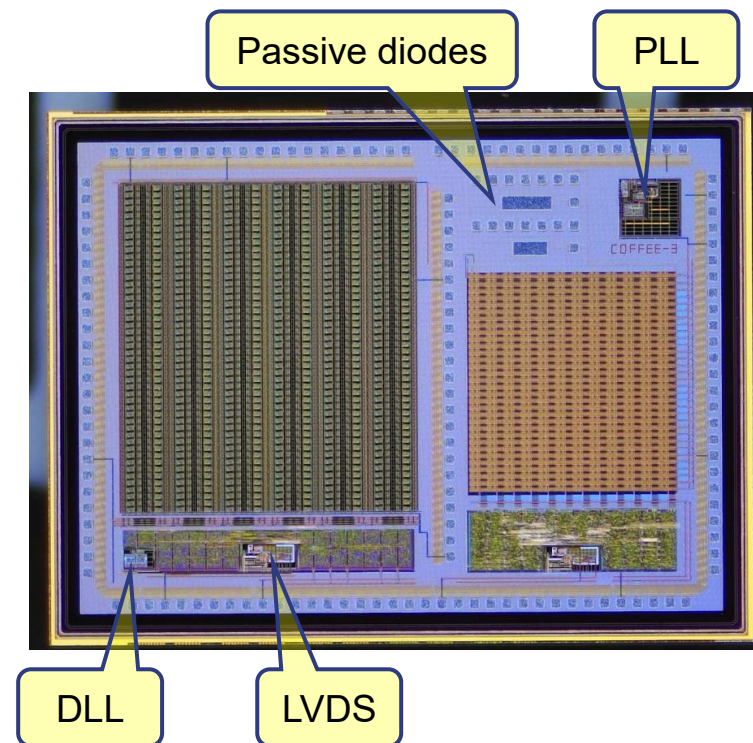
Passive diodes

- IV: breakdown at **-70V**, expected for low-res ($10 \Omega \cdot \text{cm}$) wafer
- CV: Single pixel **$\sim 50 \text{ fF}$** at -70V. Higher capacity with circuits (P-well)



PLL (Phase Locked Loop), DLL (Delay Locked Loop), LVDS

- works up to **$> 640 \text{ MHz}$** as designed.

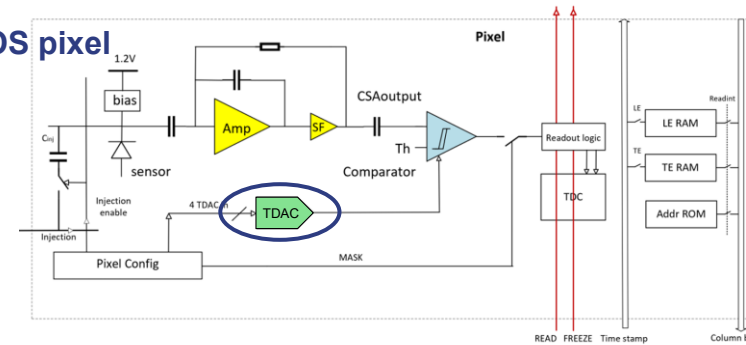
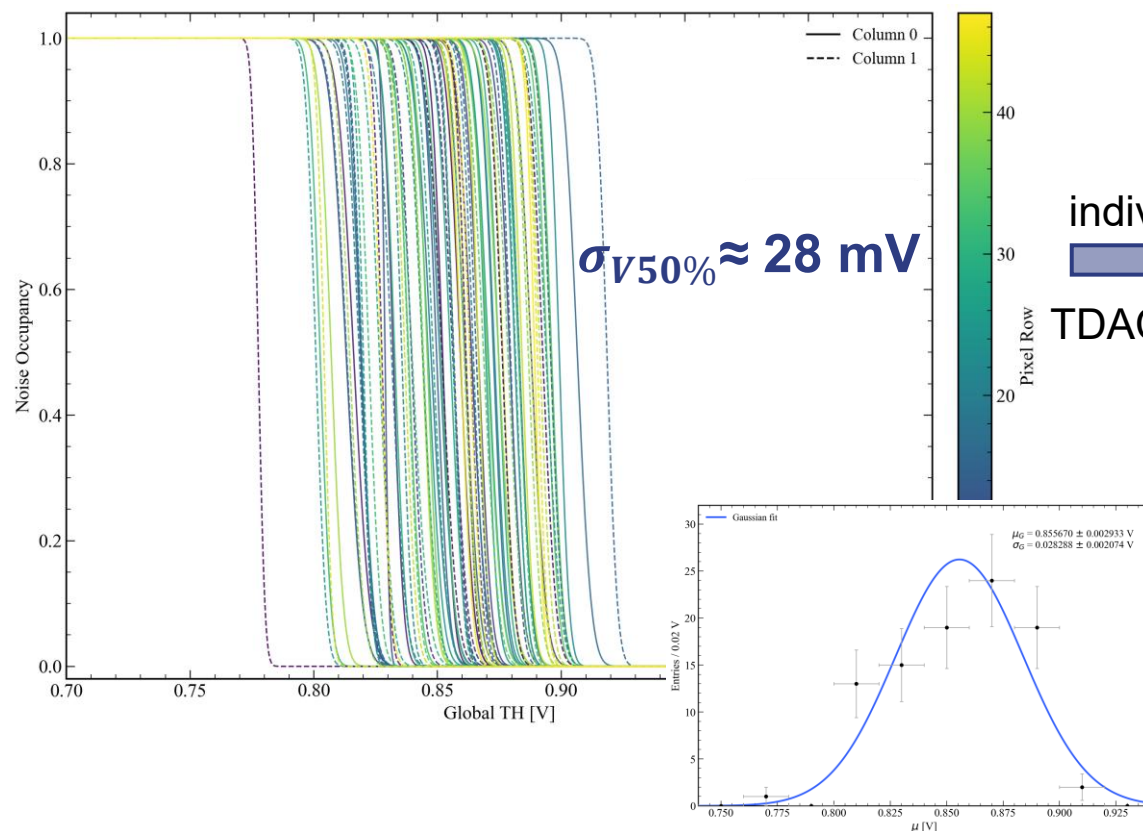
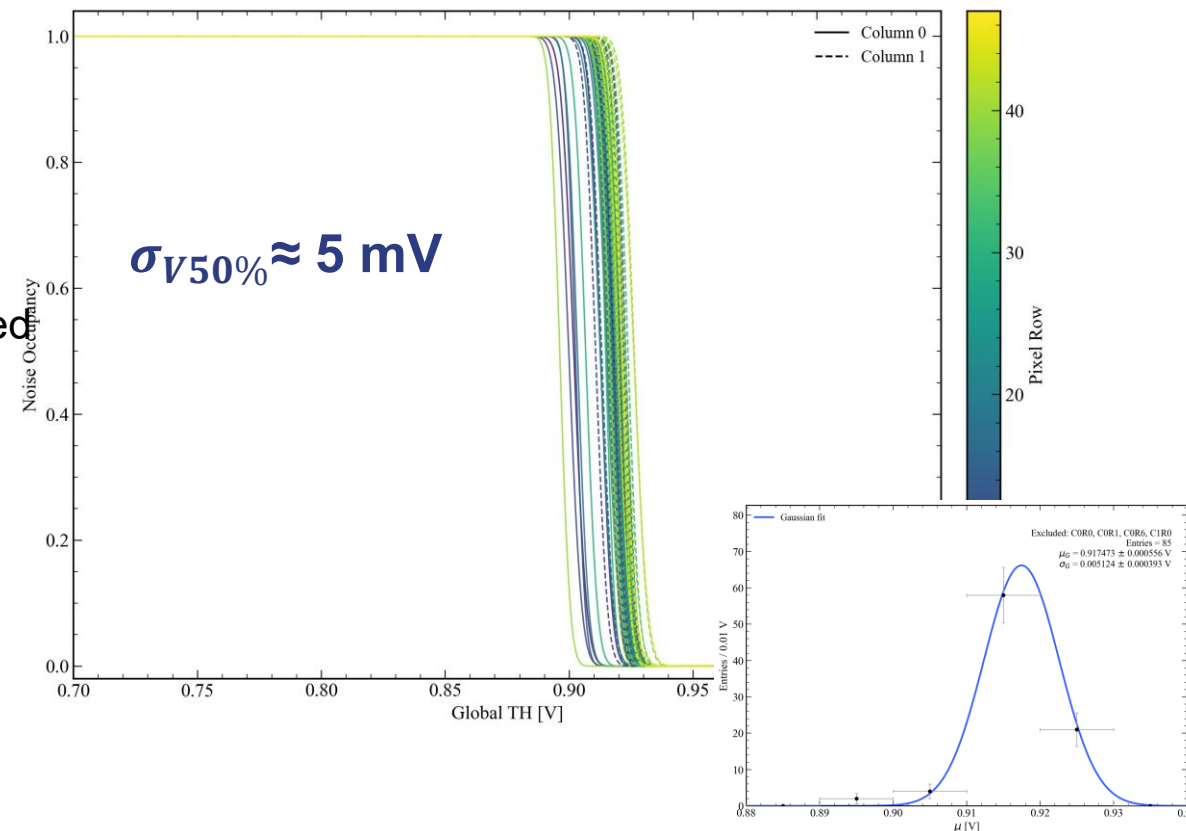


[more in CLHCP2025](#)

□ In-pixel 4-bit TDAC (Trim DAC) validated on noise rate

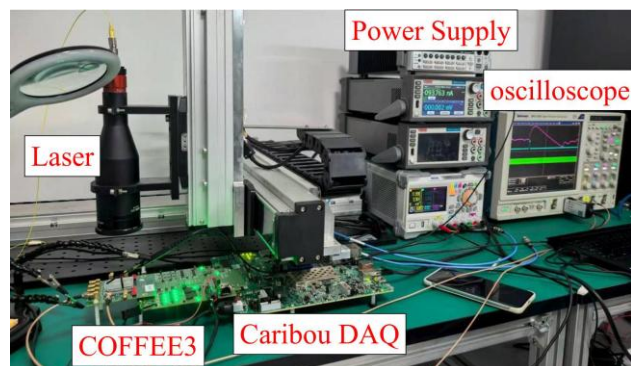
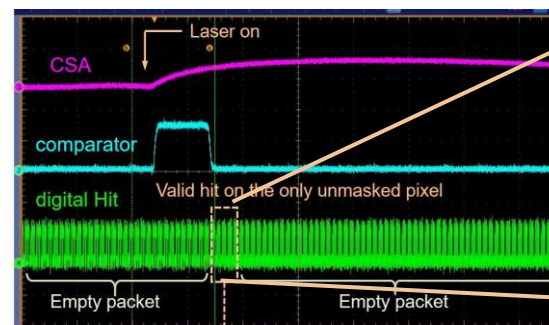
- global threshold potential + TDAC = effective threshold

a CMOS pixel



□ Full readout chain validated using laser (CMOS matrix)

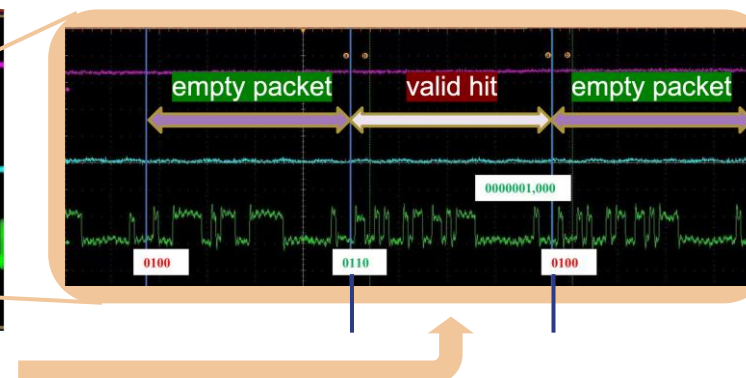
- sensing diode → in-pixel circuitry (CSA/comparator/TDC → local dataframe) → EoC serializer



A valid transmission packet corresponding to a hit

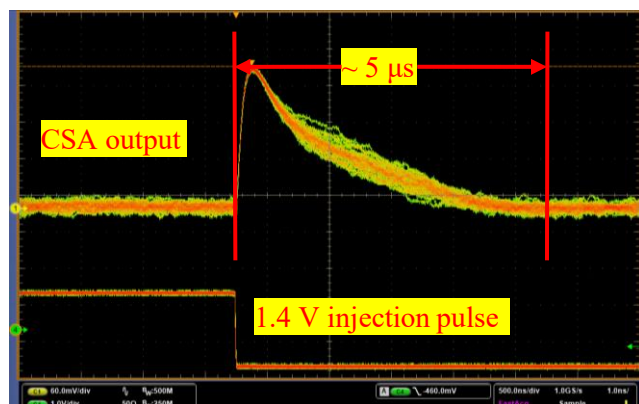
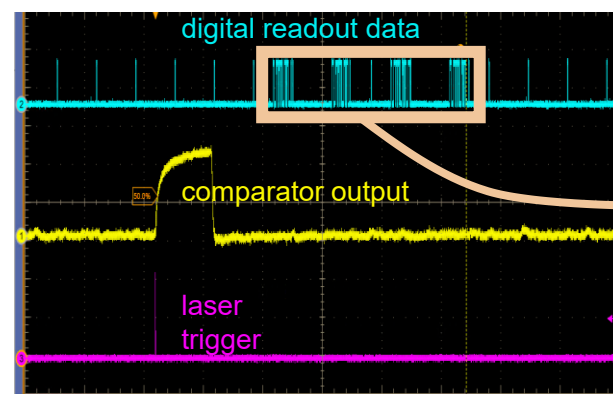
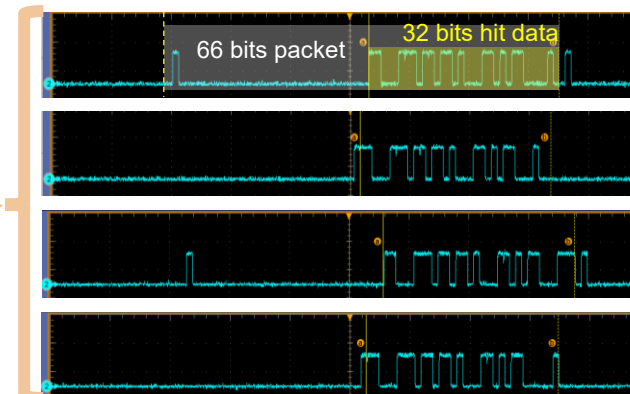
Correct row & column address

4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	8 bit
header	CHIP_ID	IE_count	TE_count	IE_time	TE_time	Addr_row	Addr_col
0 1 1 0	0 1 0 1	0 0 0 1	0 1 1 0	0 1 1 0	0 0 0 0	0 0 0 0 0 0 0 1	0 0 0 0

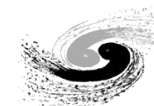


□ Full readout chain validated using laser (NMOS matrix)

- sensing diode → in-pixel circuitry (CSA/comparator) → EoC encoder (comparator/TDC) → EoC serializer



COFFEE3 Performances: testbeam

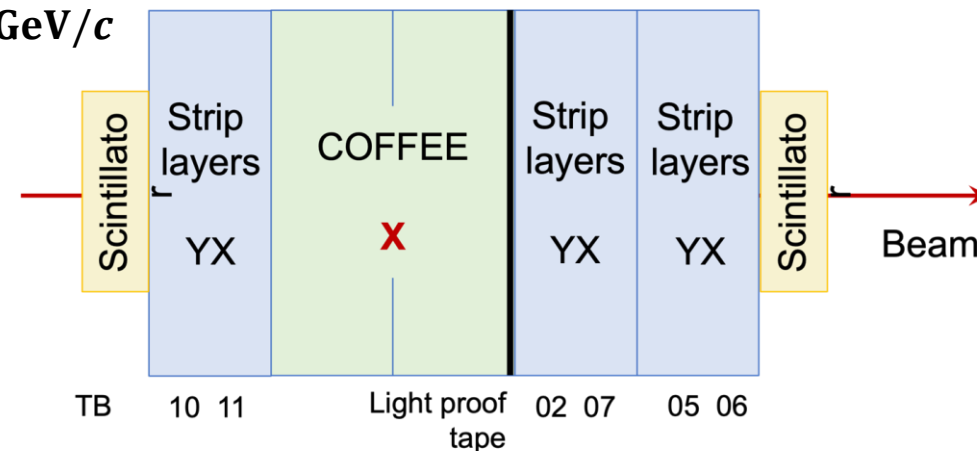


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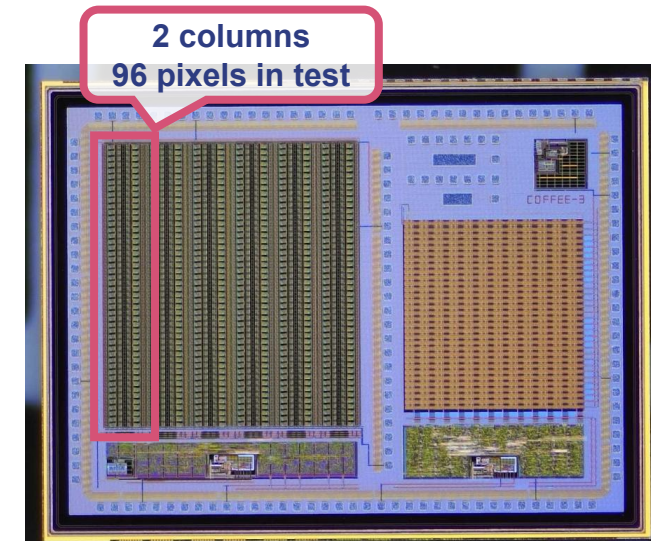


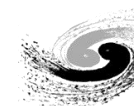
□ May & July 2026 @ CERN SPS, mixed hadron beam ~ 180 GeV/c

- silicon strip telescope + single chip test-board
- scintillator trigger



beam monitor + COFFEE3





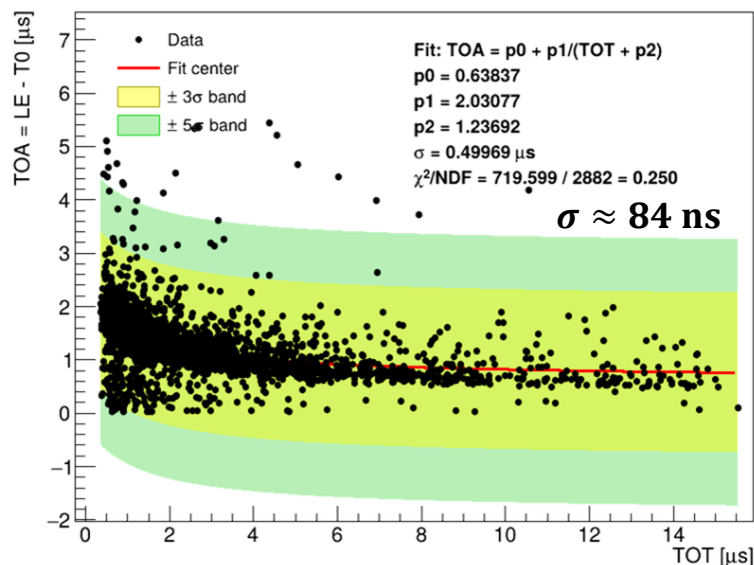
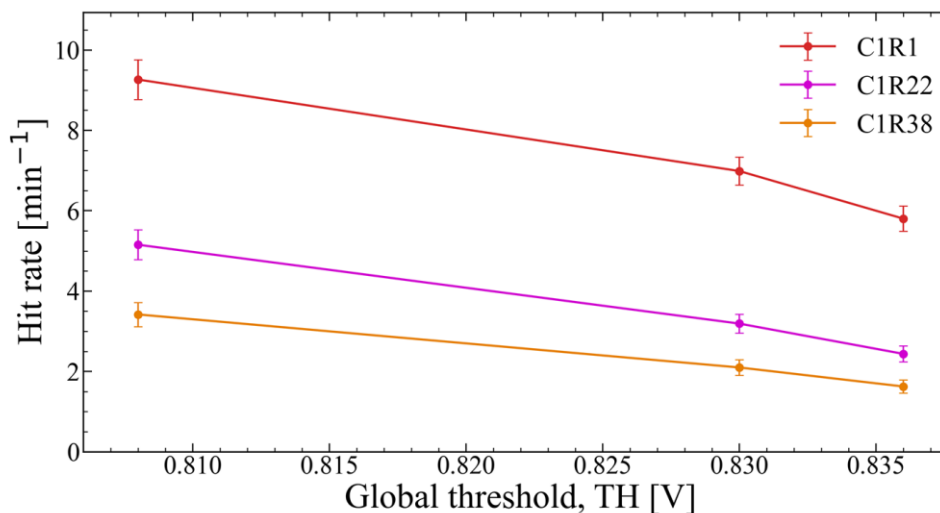
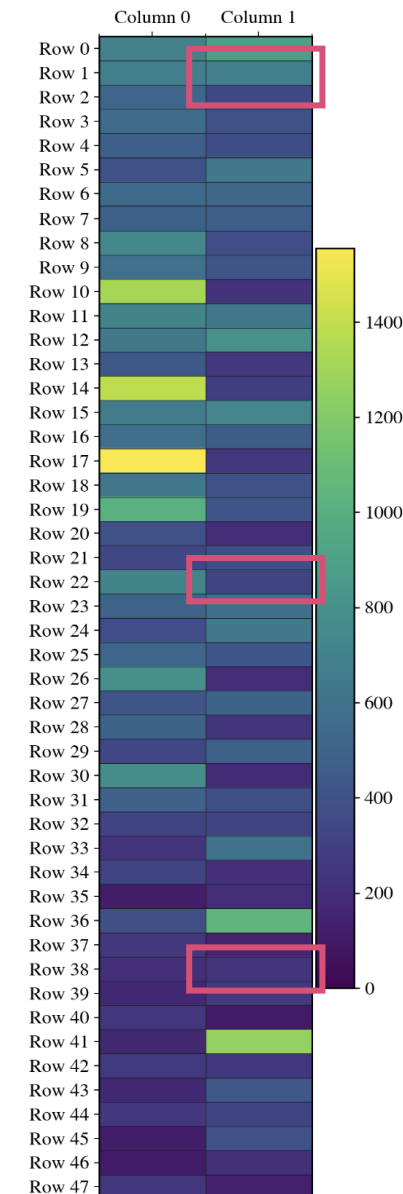
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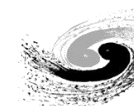
□ Hitmap

- despite the noise, all pixels have their readouts to beam events
- global threshold for comparator works well under beam

□ Timewalk & timing resolution

- timewalk effect estimated by scintillator trigger.





□ May & July 2026 @ CERN SPS, mixed hadron beam ~ 180 GeV/c

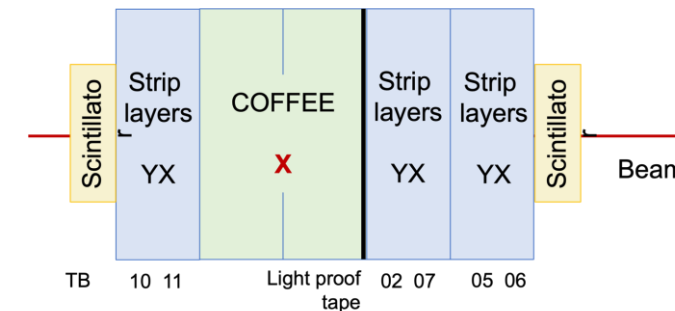
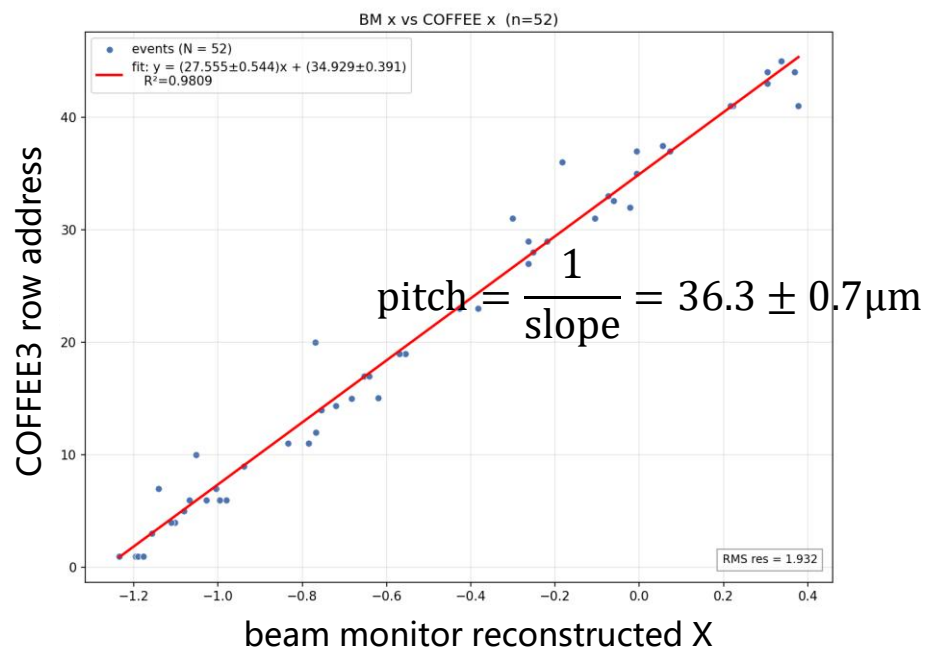
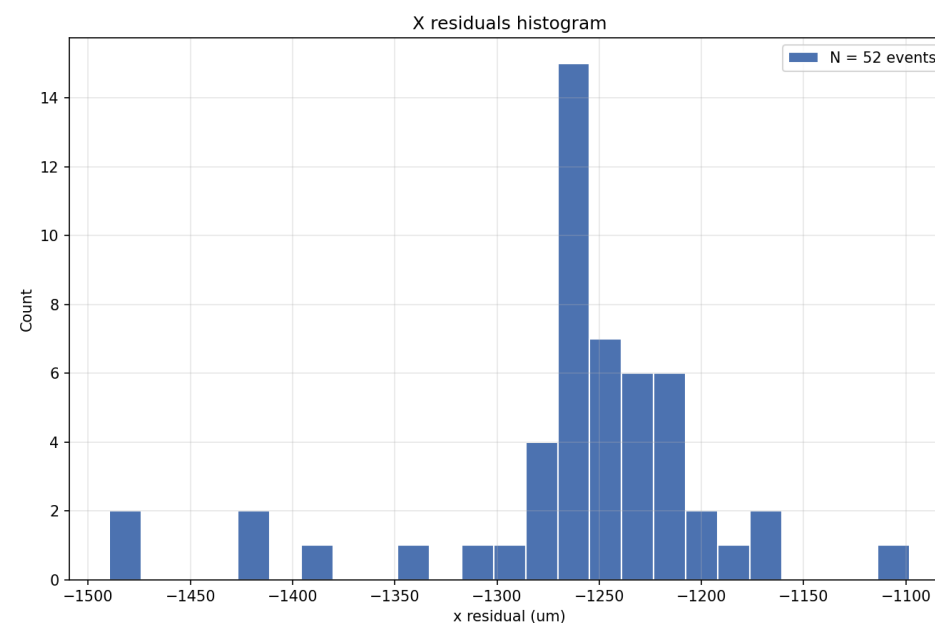
□ Tracking & positioning resolution

- row-direction pitch verified using aligned events with beam monitor



consistent with manufacturing scale $40 \times 0.9 = 36 \mu\text{m}$

- spatial resolution to be estimated with track reconstruction from beam monitor...



High resistivity wafer is expected for improved sensor performance... **CHiR**

□ Limitations on COFFEE2/3

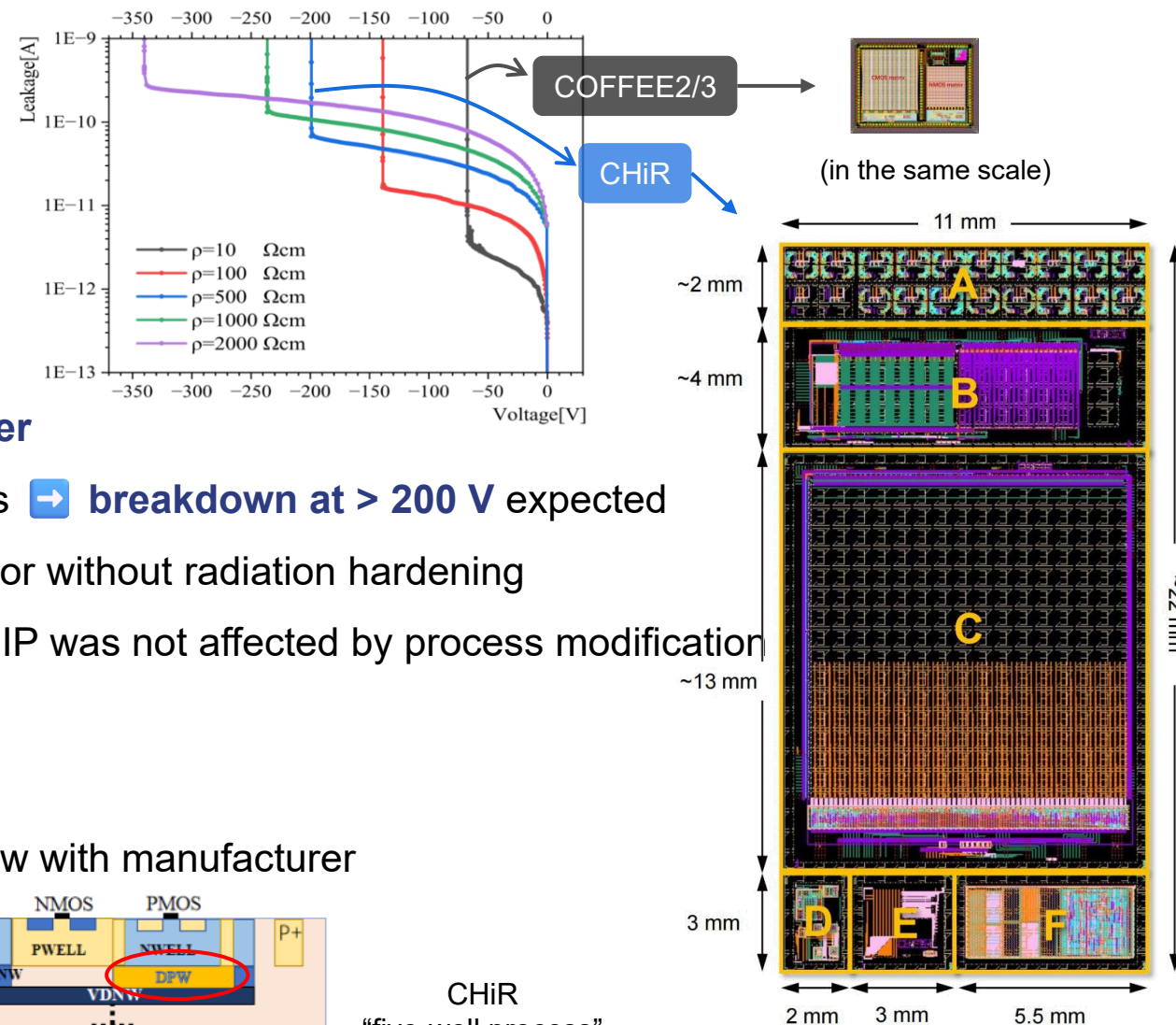
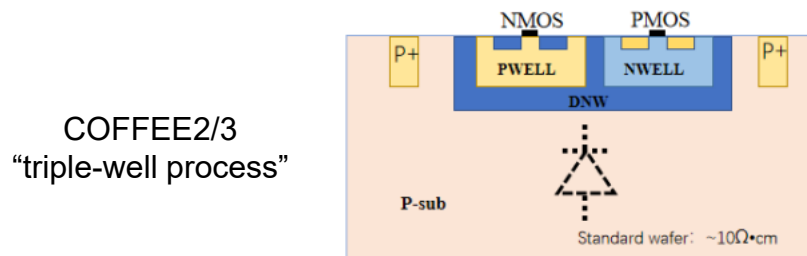
- sensor breakdown voltage not enough
- cross-talk between sensor (deep-n) and PMOS circuit

□ CHiR (COFFEE-HiRes) design goal

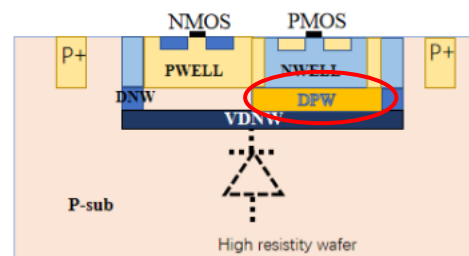
- validate **process modification + high-resistivity wafer**
- 1k / 2k / 4k $\Omega \cdot \text{cm}$ wafer available from two manufactures → **breakdown at > 200 V** expected
- Radiation effects of simple components (e.g. MOS) with or without radiation hardening
- implementation of “**five-well process**” to validate basic IP was not affected by process modification

□ First MPW submitted in early January 2026

- preliminary samples received, final chips are under review with manufacturer



UP!



❑ Segmentations & key features

❑ Passive sensor validation

- A – passive pixels arrays with different pixel or guard-ring designs

❑ Pixel array

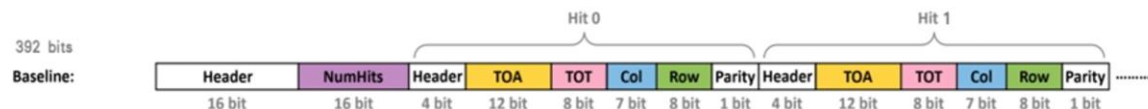
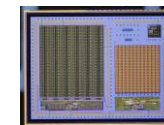
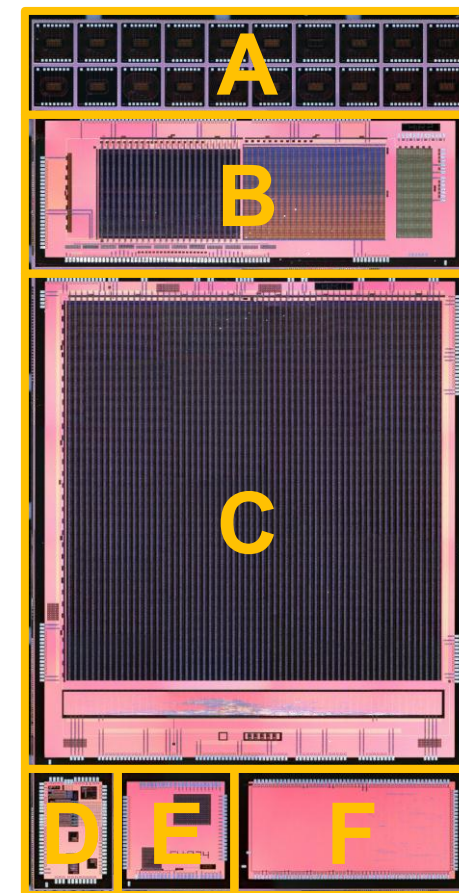
- B – variations of in-pixel analogue front-end designs
- C – large main pixel array
- E – alternative small pixel array, shuntLDO, ...

❑ IP validations

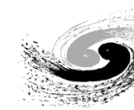
- D – standalone PLL, DLL, LVDS, ...
- F – digital modules for exclusive TID and SEE studies

❑ Pixel digital readout data word

- 12-bit time of arrival (TOA)
- 8-bit time over threshold (TOT)



❑ Testing is on-going...



□ R&D of MAPS sensors aiming to UP requirements: HV-CMOS & CMOS

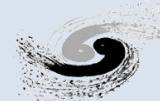
□ COFFEE / CHiR lead by IHEP

- encouraging results from COFFEE2/3
- production of CHiR with **process modification** and high-R wafer almost done
- full-size chip submission planned in 2027

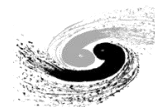
□ More MAPS candidates are well developing



Thank you for your attention!



Thank you for your attention!

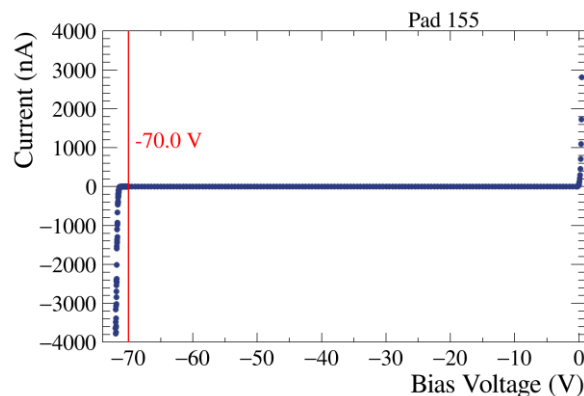
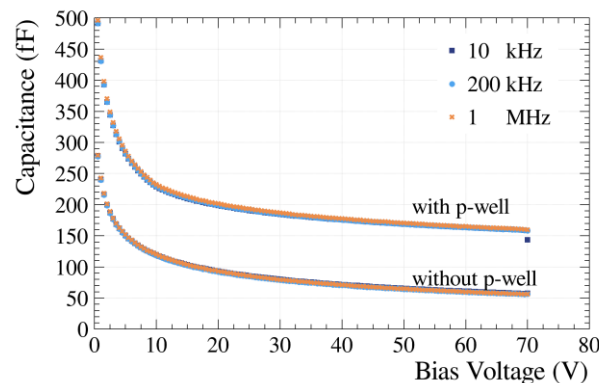


https://indico.cern.ch/event/1632728/contributions/6872615/attachments/3200969/5698418/UPDataFormat_20260109.pdf

[LHCb-TDR-026](#)

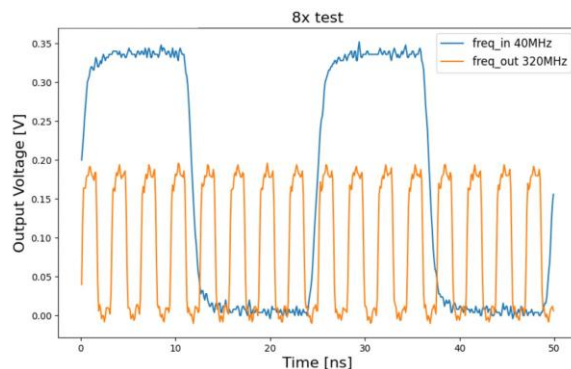
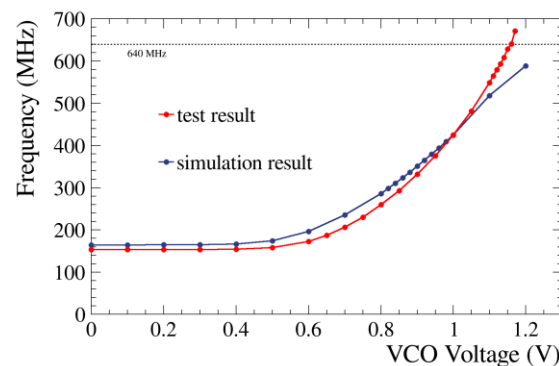
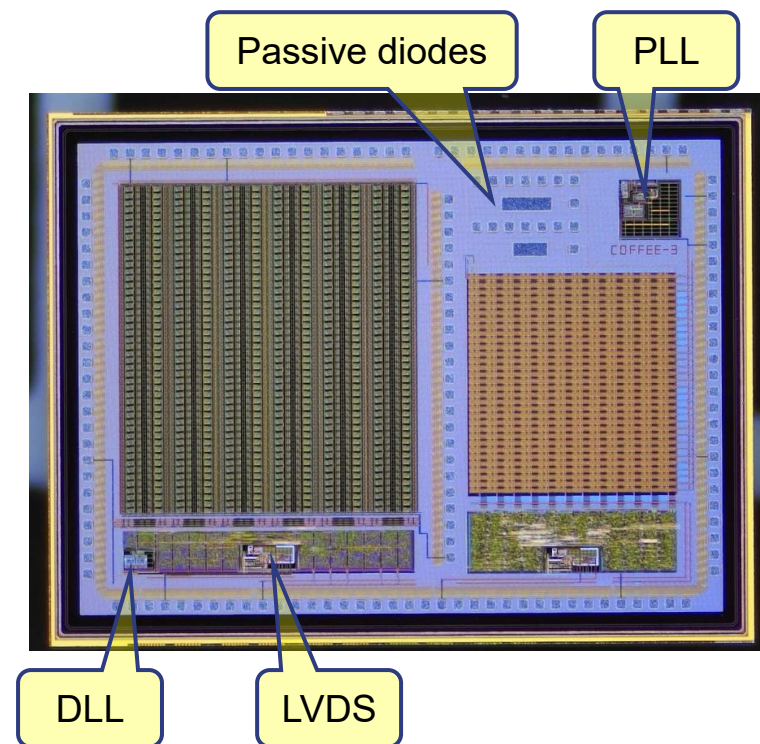
□ Passive diodes

- IV: breakdown at **-70V**, expected for low-res ($10 \Omega \cdot \text{cm}$) wafer
- CV: Single pixel **$\sim 50\text{fF}$** at -70V. Higher capacity with circuits (P-well)



□ PLL (Phase Locked Loop), DLL (Delay Locked Loop), LVDS

- VCO control and frequency multiplication ($\times 4, 8, 16$) works up to **$> 640 \text{ MHz}$**



□ DLL (Delay Locked Loop) for future finer TDC

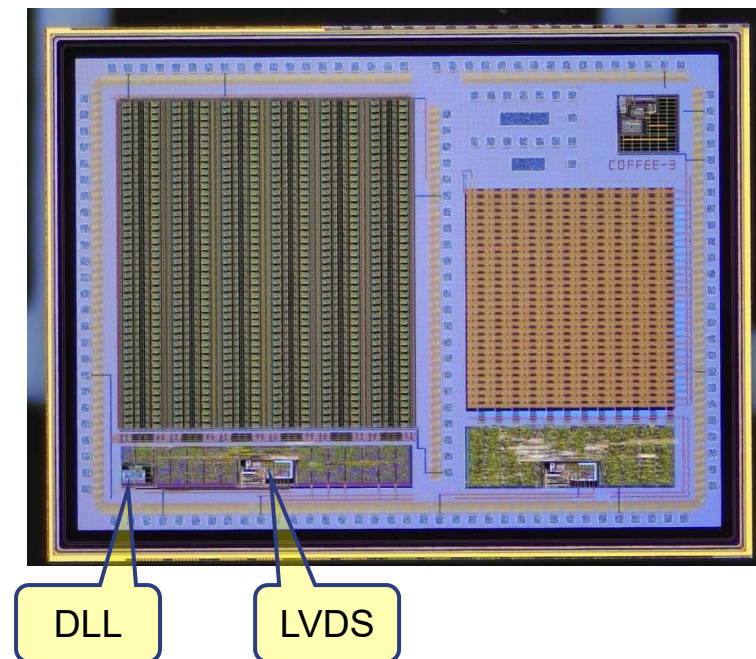
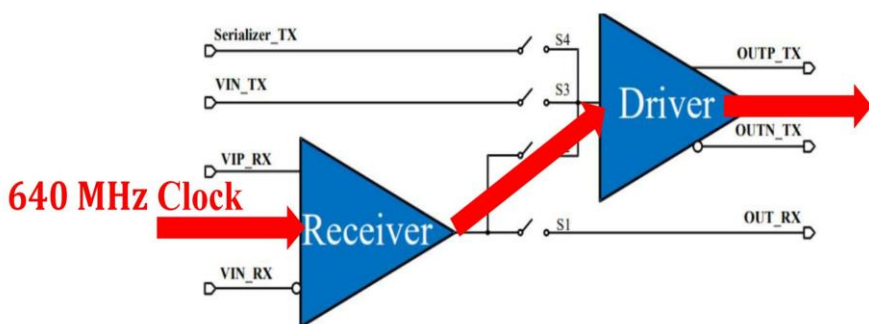
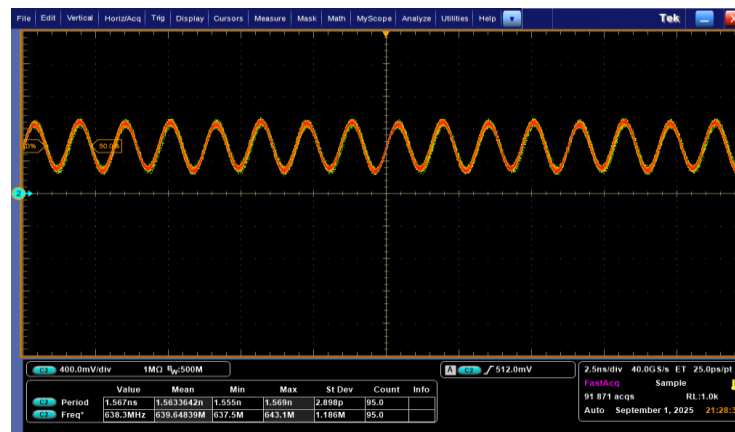
- Delivers clock phase shifted as expected ($\pi/3, 2\pi/3, \dots, 2\pi$)

e.g. DLL-1 v.s. DLL-4
phase shift = π



□ LVDS transceiver

- in-chip main fast clock & high speed data transmission clock

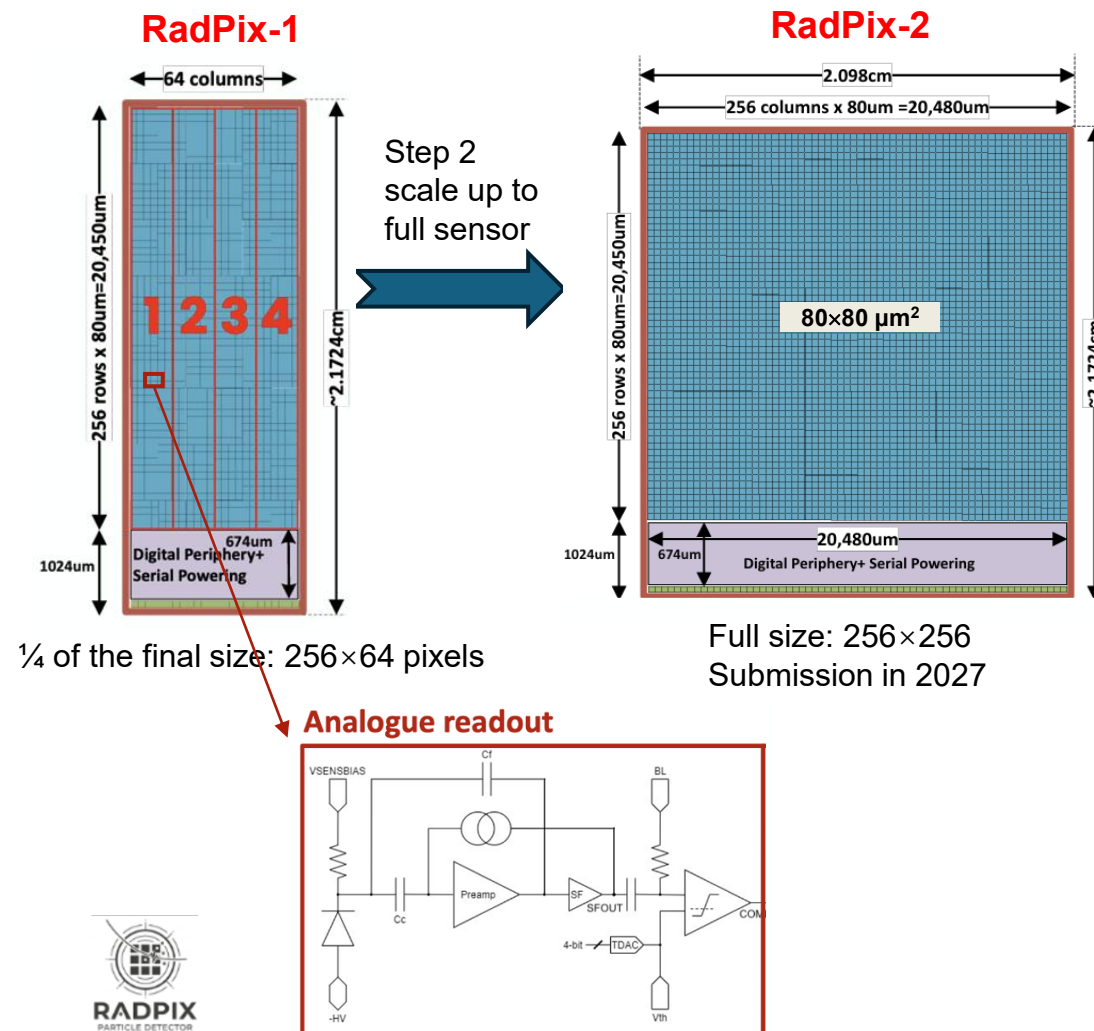


□ RadPix1 (LFoundry 150 nm)

- Aims to UP requirements, also a backup solution for Mighty Pixel Tracker
- DRD3 shared submission in July 2026
- High Resistivity wafer ($> 2\text{k } \Omega \cdot \text{cm}$)
- 4 pixel flavors for analogue readout: PMOS-in, NMOS-in, CMOS-in, Trans-impedance
- 13-bit TOA, 5-bit TOT

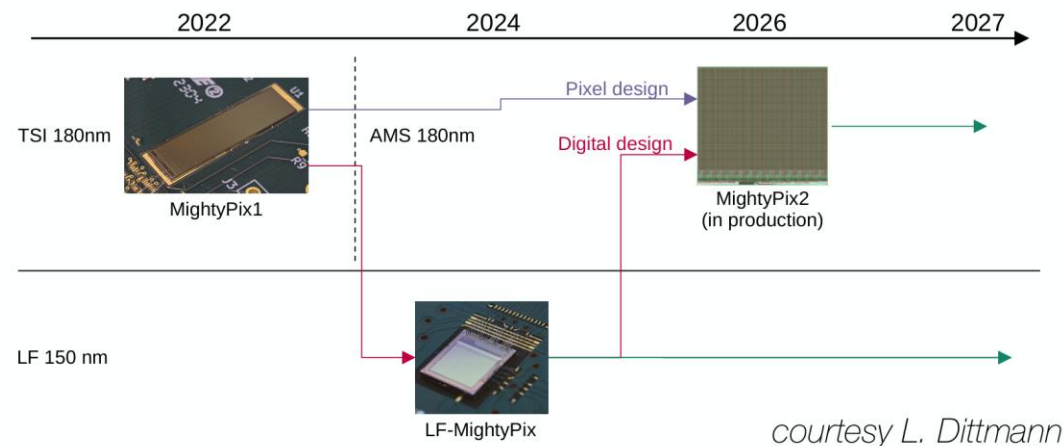
□ Included serial powering and BIG (Bunch crossing ID Grouping) test chip

□ RadPix2 submission expected in Q4 2027

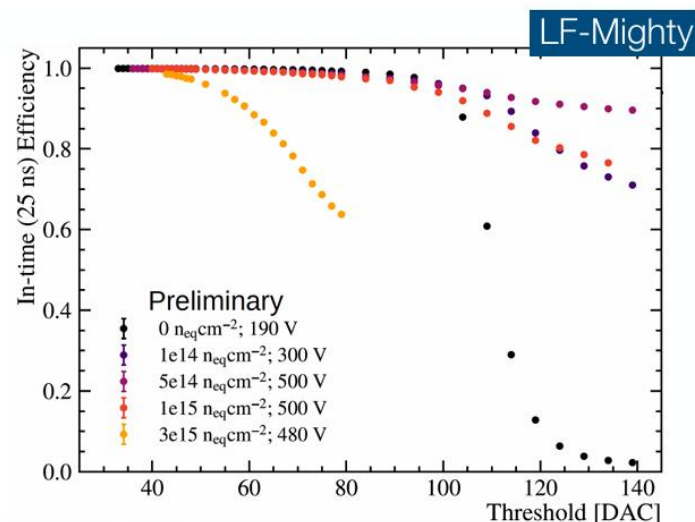


□ MightyPix2 (HV-CMOS AMS 180nm process)

- Solution for MP and outer part of the UP
- Now in production, expected for November 2026
- CSA with NMOS and PMOS-input devices
- Included serial powering
- 12-bit TOA, 4-bit TOT



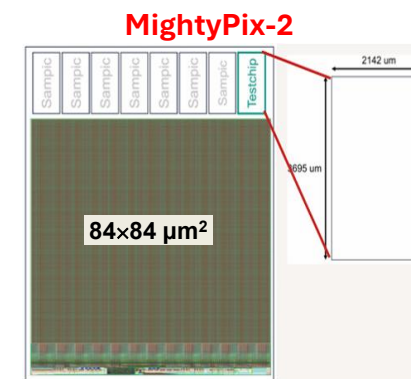
□ Test beams @ DESY on MightyPix1 and LF-MightyPix to test functionalities



MP specs: $5 \times 10^{14} n_{eq}/cm^2$

UP specs: $3 \times 10^{15} n_{eq}/cm^2$

LF-MightyPix: $\varepsilon_{25nm} > 99\%$ @ $1 \times 10^{15} n_{eq}/cm^2$ radiation



<https://mightypix2.docs.cern.ch/>

□ MANTA (CMOS TPSCo 65nm)

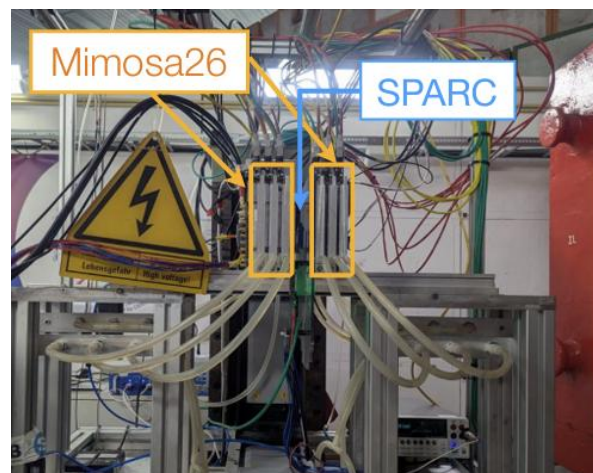
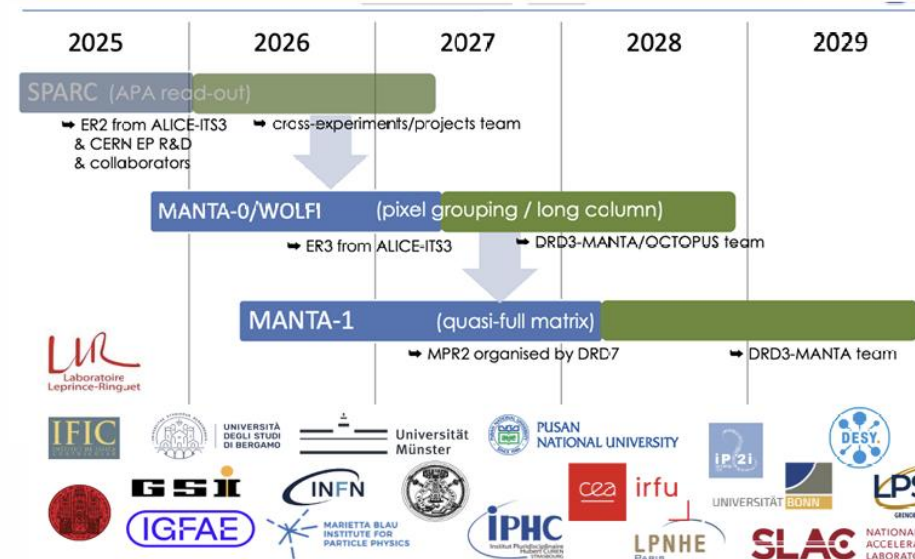
- Aims for a pixel matrix and sensor matching various future trackers
- Based on DPTS pixel arxiv.org/abs/2212.08621

□ SPARC (Prototype Sensor Pixel Asynchronous Readout CMOS)

- prototype of MANTA
- Small chiplet: 32x28 pixel matrix with a pixel pitch of 25x16 μm
- **First Hit map of SPARC in the beam** →

□ Design of MANTA-0:

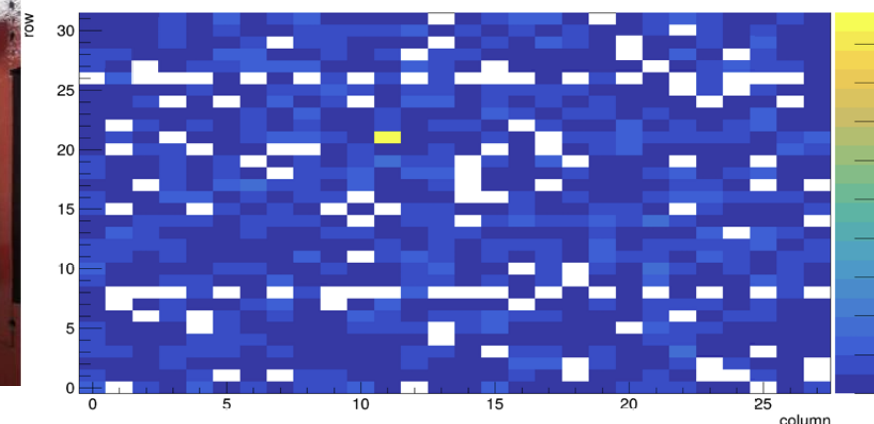
- long pixel column with pixel grouping
- submission foreseen end of 2026

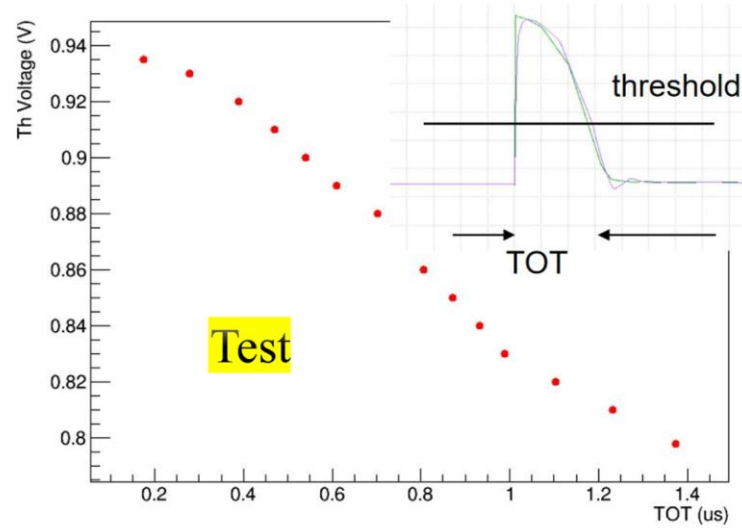


Elisabeth Maria Niel. 9th LHCb Upgrade II workshop

Testbeam @ DESY

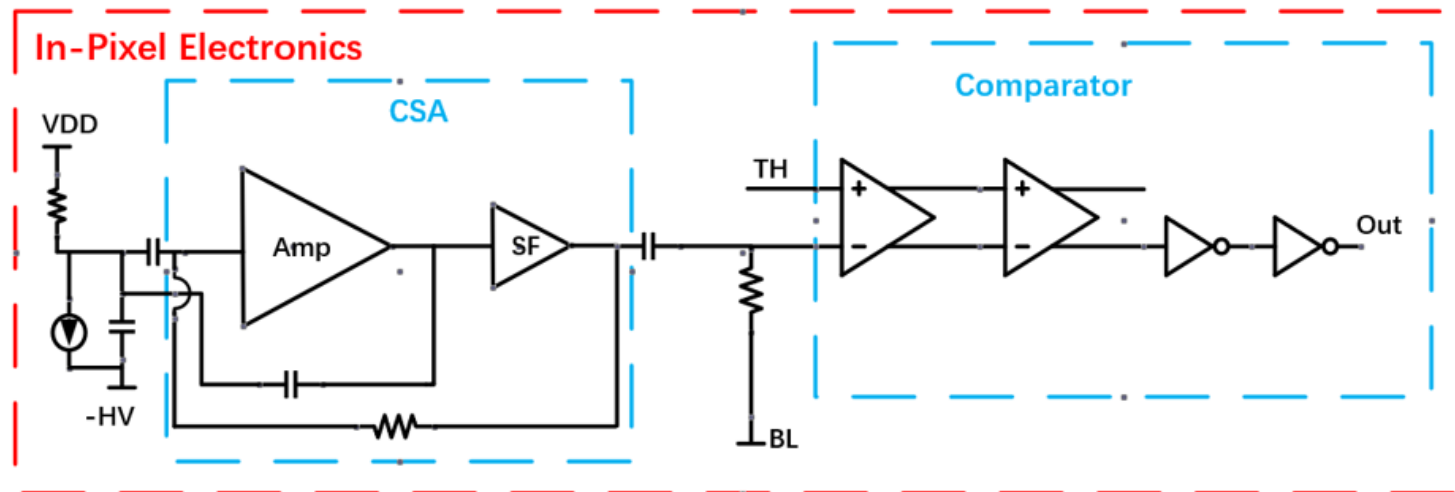
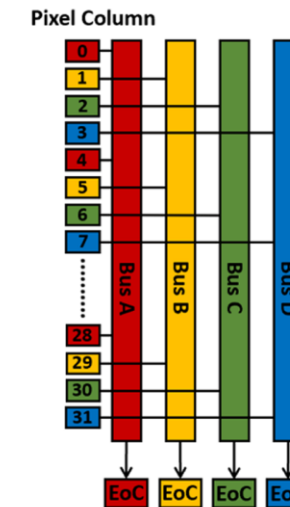
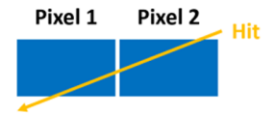
Hit Map



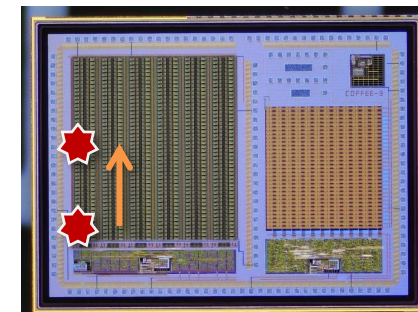
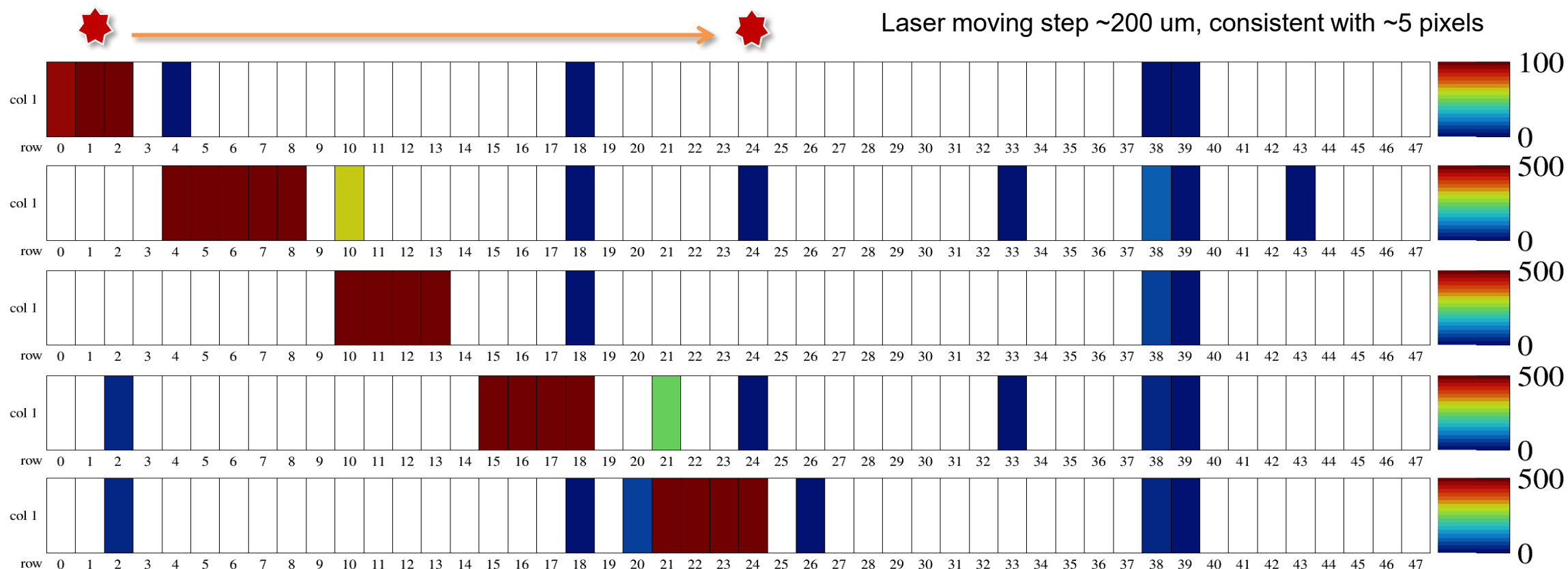


“real” CSA in threshold scanning

NMOS matrix pixel scheme

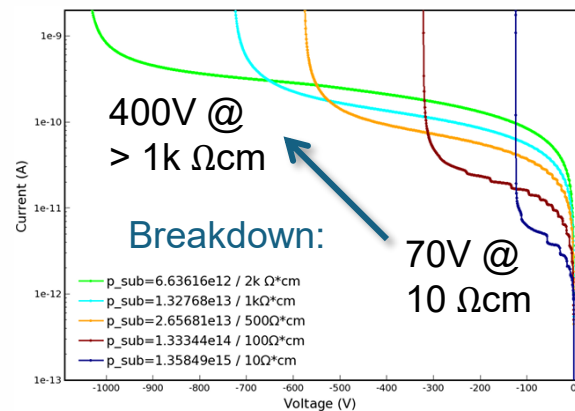
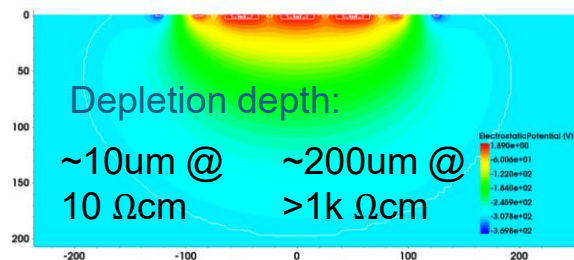
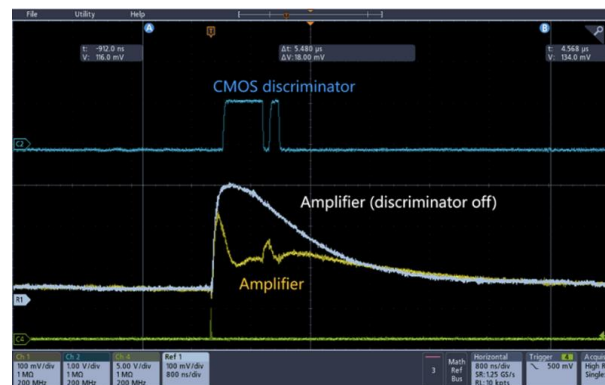


- Readout of **a full column** successful
- Clear response to a laser spot moving along the column



Limitations: breakdown voltage,

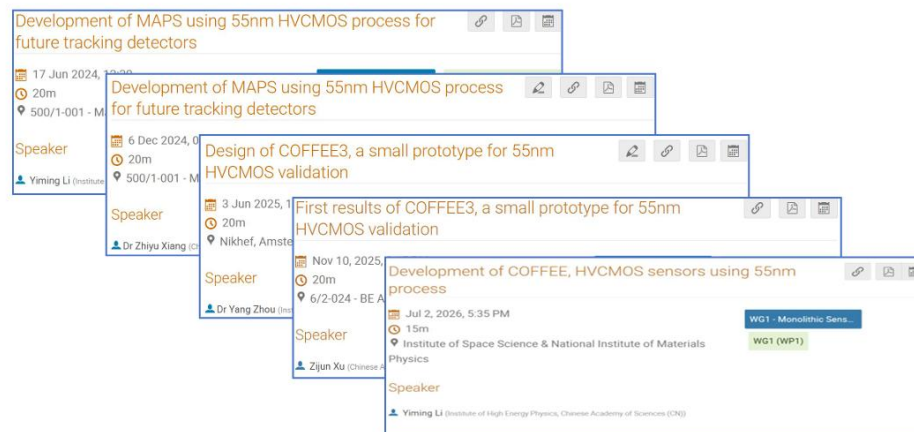
cross-talk



Crosstalk betw sensor & digital circuit @ COFFEE2

HV-CMOS MAPS R&D at IHEP

- IHEP actively involved in CERN DRD3
 - test-beam and irradiation facilities sharing
 - joint serial powering R&D with US/UK/Italy
 - joint aluminum flex R&D with Italy/UK
- Caribou DAQ for MAPS R&D
 - open source hardware/firmware/software
 - FE chip specific carrier board, firmware and software IP blocks by ourself
 - as a user, keep reporting bugs and solutions



<https://caribou-project.docs.cern.ch/>