

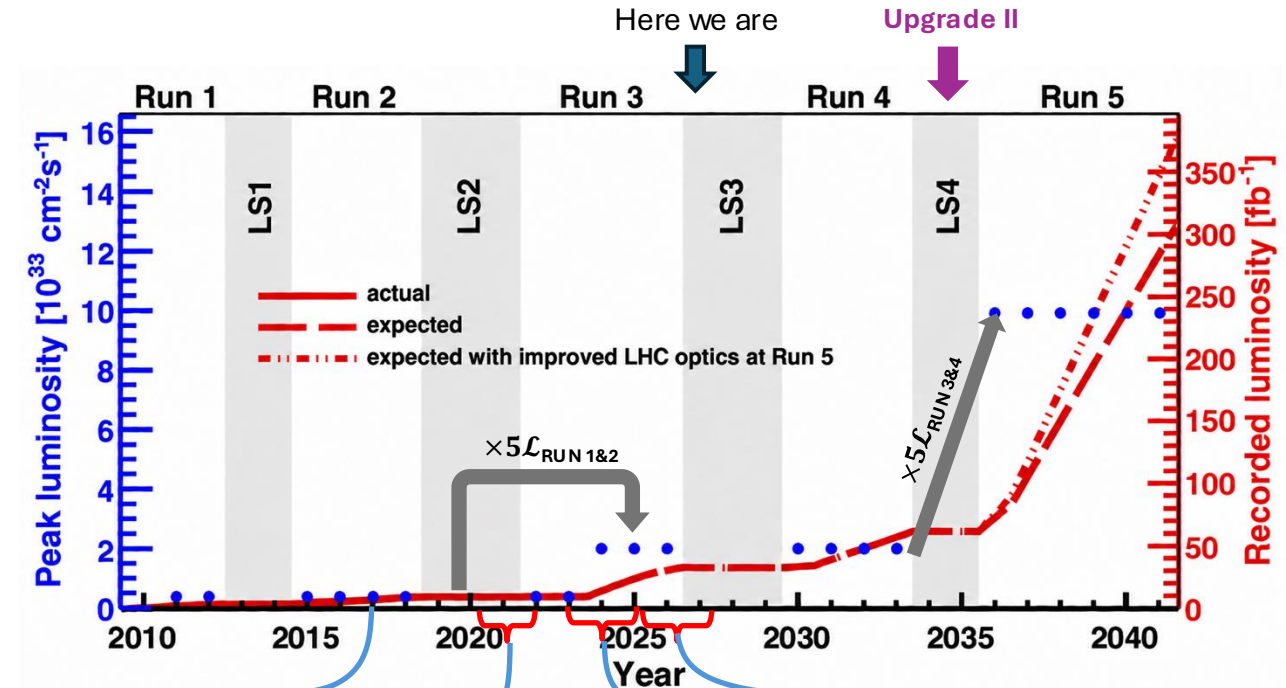
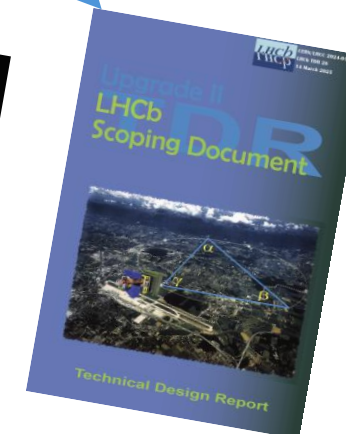
Hybrid-flex and Readout-flex R&D for LHCb UP detector

Hanbing Liu On behalf of UP team

LHCb and Upgrades Overview

- ❖ For further b-physics studies, LHCb plans two successive upgrades.
- **Upgrade I completed by LS2:**
 - ❑ 5× instantaneous luminosity
 - ❑ Full software trigger
- **Upgrade II scheduled at LS4:**
 - ❑ 5× higher instantaneous luminosity, $\sim 300 \text{ fb}^{-1}$ in total
 - ❑ Significant improvement in physics measurement precision is expected

- More details in Yiming's upcoming [talk](#)



LHCb and Upgrade II Overview

❖ Higher luminosity improves the sensitivity of physics measurements, but also brings new challenges

- Data rates
- Radiation levels
- Occupancy
- Ghost rates
- Pile up

New detectors are needed

RICH1, RICH2

- Granular photon sensors
- Add timing information

PicoCal

- SPACAL + Shashlik
- High granularity
- O(10 ps) timing

Muon

- New G-RWELL (inner)
- New MWPC (middle)
- Reused MWPC (outer)

UP (Upstream Pixel tracker)

- MAPS-based silicon pixel detector

- The Upgrade II tracking system will consist of TV, UP, and MT.

Timing VELO

- 3D Silicon Pixel

Magnet

Mighty Tracker

- MAPS pixel (inner)
- SciFi (outer)

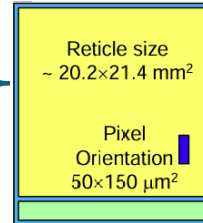
LHCb Upgrade II detector

Peak lumi.	$\sim 1.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
Recorded lumi.	$\sim 300 \text{ fb}^{-1}$
Bunch crossing rate	$\sim 40 \text{ MHz}$

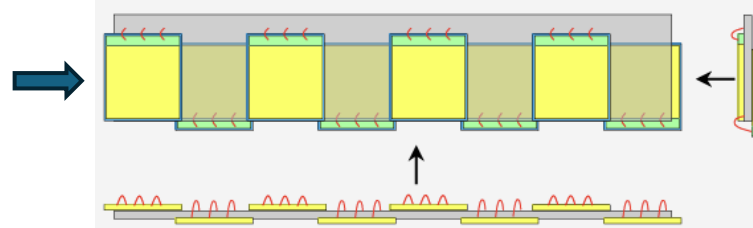
UP Detector Overview

Parameter	UP specification
Spatial resolution	$\sim 10 \mu\text{m}$
Time resolution	3-5 ns
Max. Hit Rate	91.2 MHz/cm ²
NIEL	$3 \times 10^{35} \text{ n}_{\text{eq}}/\text{cm}^2$
TID	187.5 MRad
Power consumption	$\leq 200 \text{ mW}/\text{cm}^2$

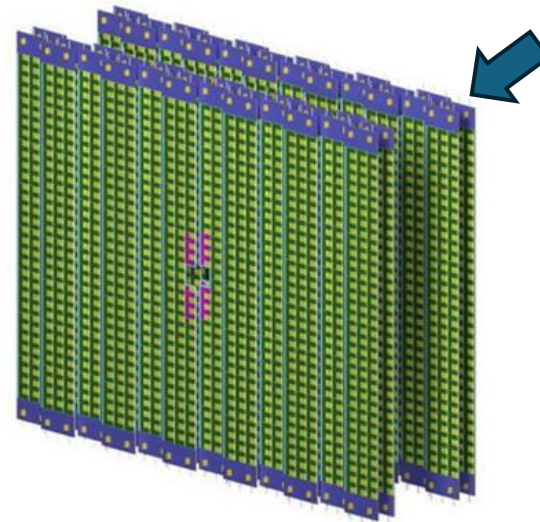
MAPS sensor



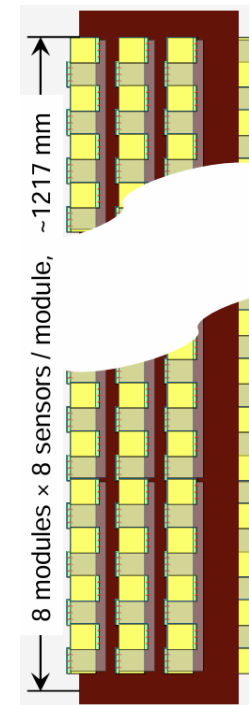
Module



8 Sensors / Module
48 Modules / Stave
12 Staves / Plane
4 Planes / UP



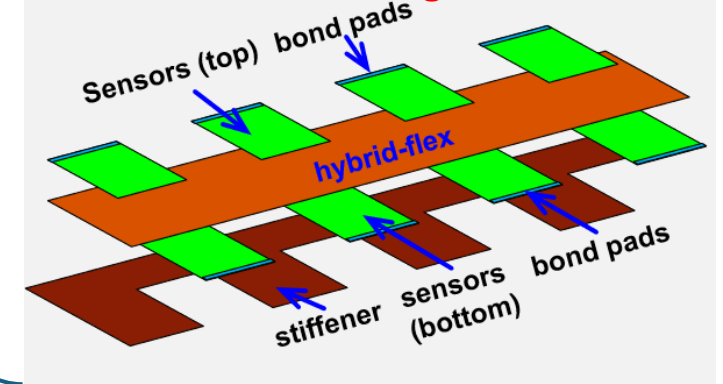
UP



Stave

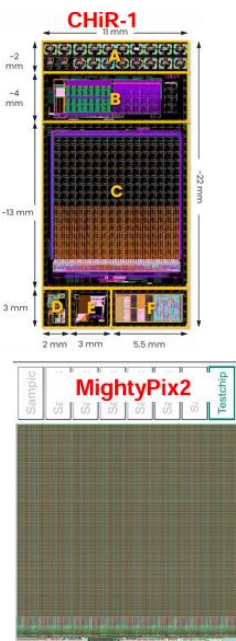
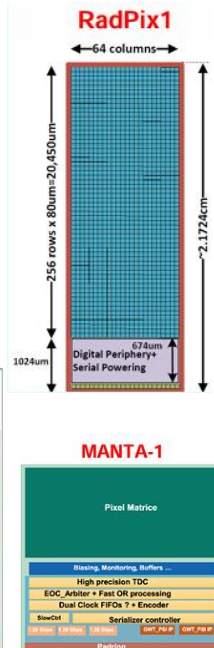
Adapted from UT

no dead area design

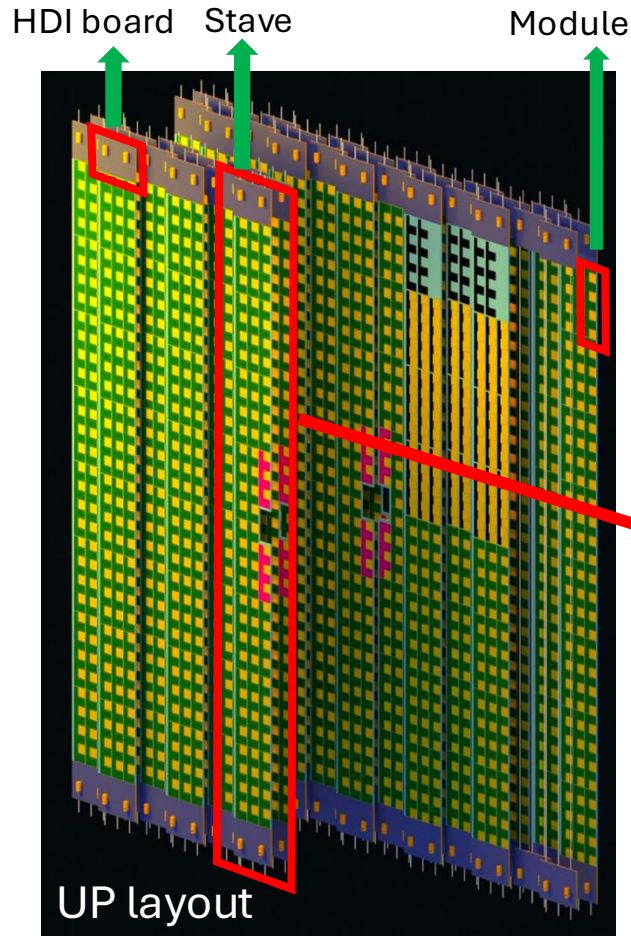


➤ Maybe you are interested in slides:

- [Sensor](#) (Boxin Wang)
- [Prototype](#) (Zhijie Wang)
- [Thermal](#) (Tiange Li)
- [Power](#) (Tianyu Shi)

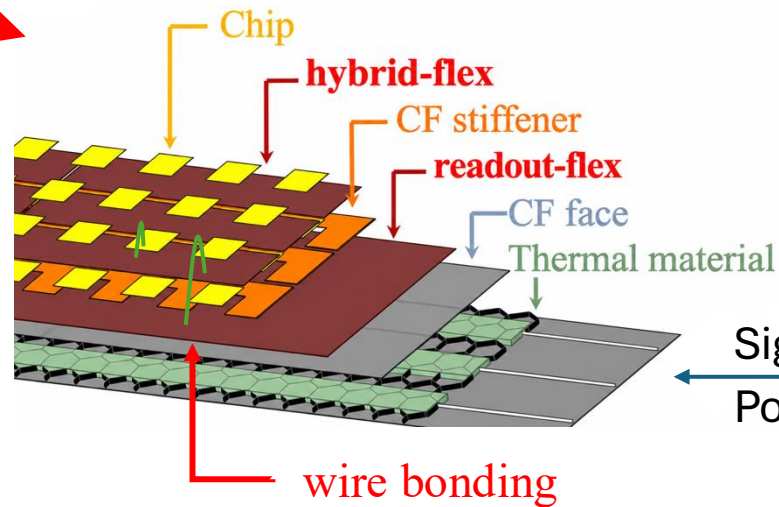


UP Detector Overview

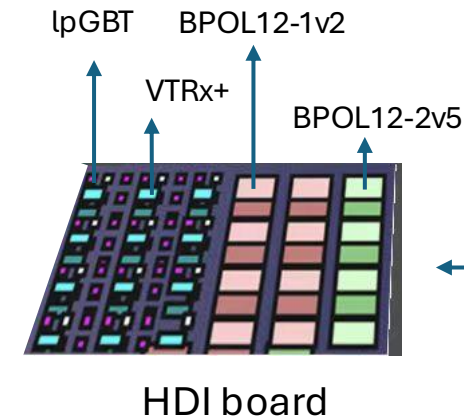


❖ UP Structure:

- Each layer contains staves with modules, chips, and HDI boards.
- **Hybrid-flex** and **readout-flex** provide connection between FE and BE
 - ❑ A critical part of UP
 - ❑ An important factor determining UP performance



Signal
Power



Signal
Power

Backend

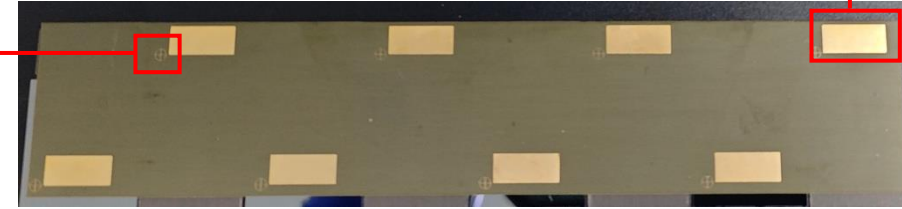
- Readout-flex and Hybrid-flex R&D
 - Mechanics design
 - Thermal validation
 - Electronics
 - Material budget optimization
- Conclusion and prospects

Mechanical Module Prototype

- ❖ Need flex prototypes to validate the module design

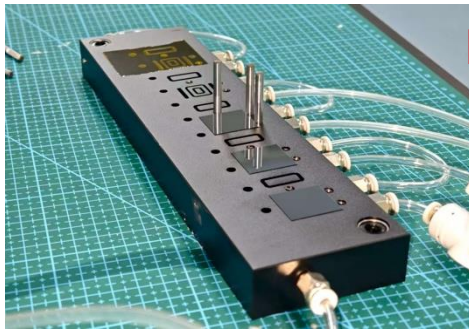
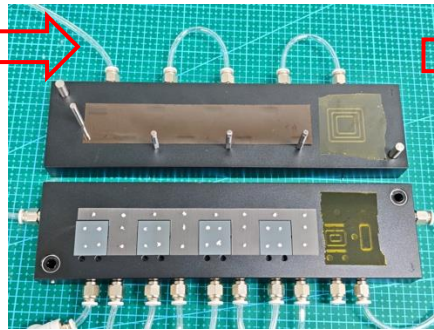
fiducial mark

Wire-bonding pad

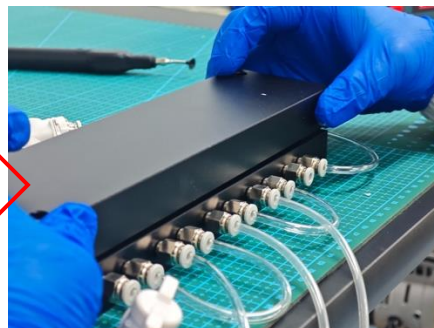
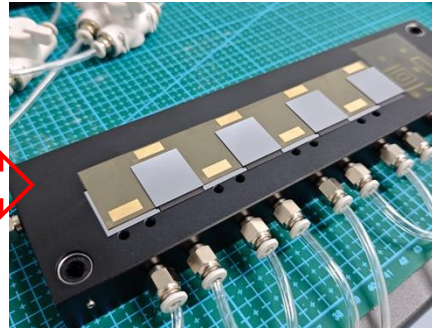
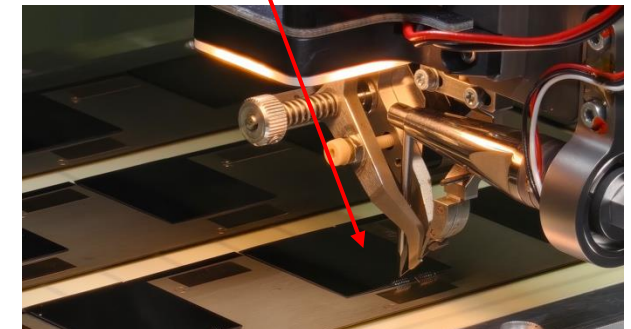


Mechanical hybrid

More details in [Prototype](#) (Zhijie Wang)



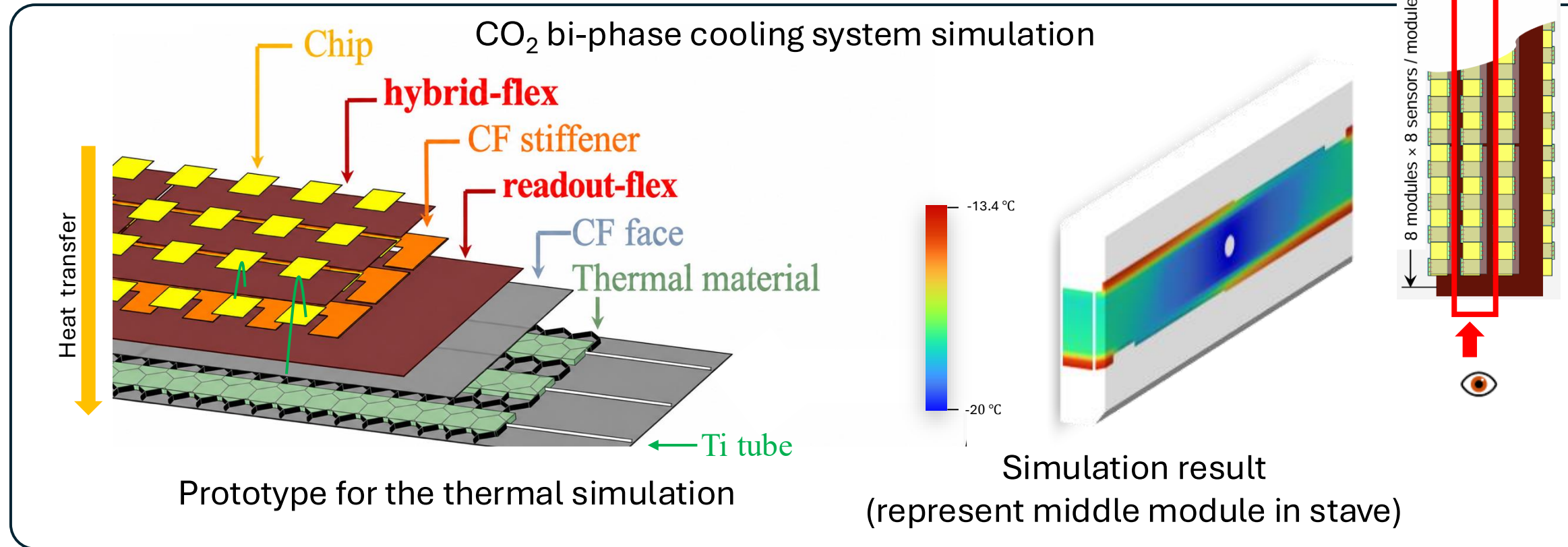
Wire bonding



- ❖ Module design validated with flex prototypes. 

Thermal Validation

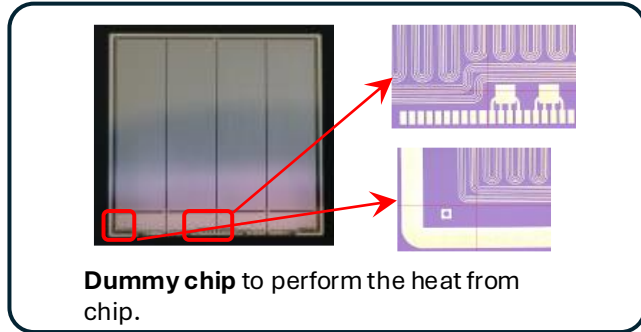
- High heating power from CMOS ($< 200 \text{ mW/cm}^2$)
 - Nominal operation temperature: -20°C
- ➡ Cooling challenge



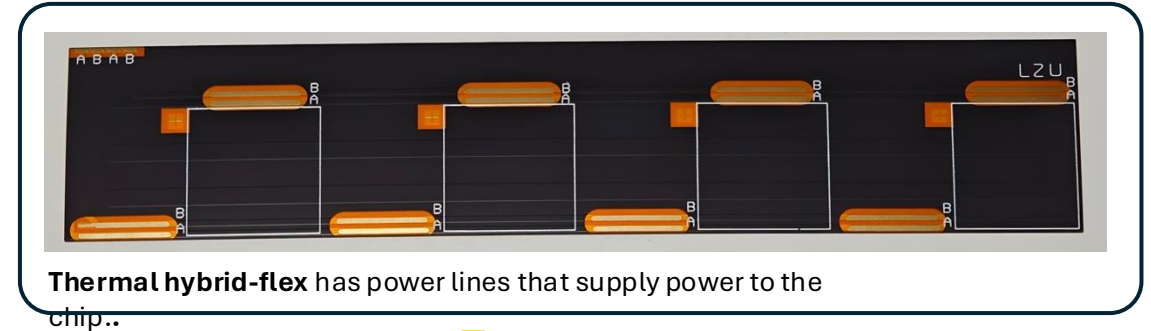
After the simulation ↑, need **thermal prototype** to test the thermal performance.

Thermal Validation

Stave, flex, chip prototype ↓ for thermal test.



Heat
transfer

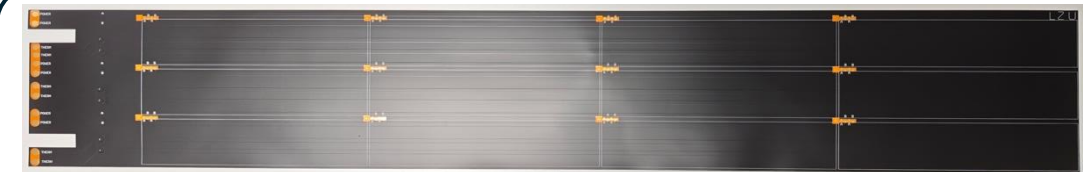


Heat transfer

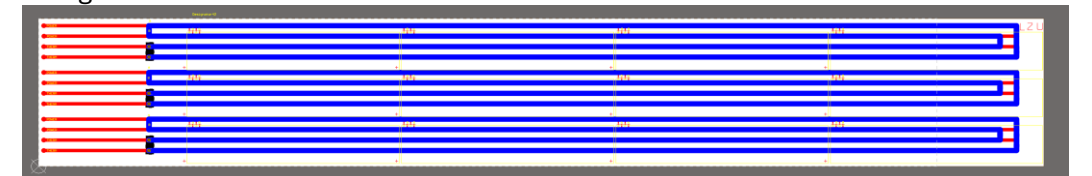


Thermal stave consist with Ti tubes and honeycomb panel, with 2 phase CO₂ in Ti tubes.

Heat
transfer



Thermal readout-flex with power lines and heater. Copper usage is close to the final design.



Thermal area(blue part) is used to simulation the heating from readout-flex and hybrid-flex. The thermal power is 10mW/ cm² (1.2V)

- Design and production have been completed.
- Providing a basis for subsequent thermal tests.
- The thermal performance is close to the final design.

Electronic R&D Overview

❖ The UP electronic readout system require:

➤ **High data rate:**

~ 5 Gb/s for chips near beam pipe

➤ **Signal integrity:**

With **1.28 Gb/s** and **70 cm length**

➤ **High granularity:**

Spatial resolution $\sim 10\mu m$

➤ **Low material budget**

❖ Bring challenge for flex:

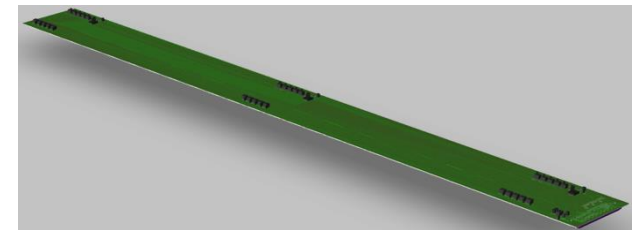
➤ **Impedance match**

➤ **Crosstalk**

➤ **PCB layout**



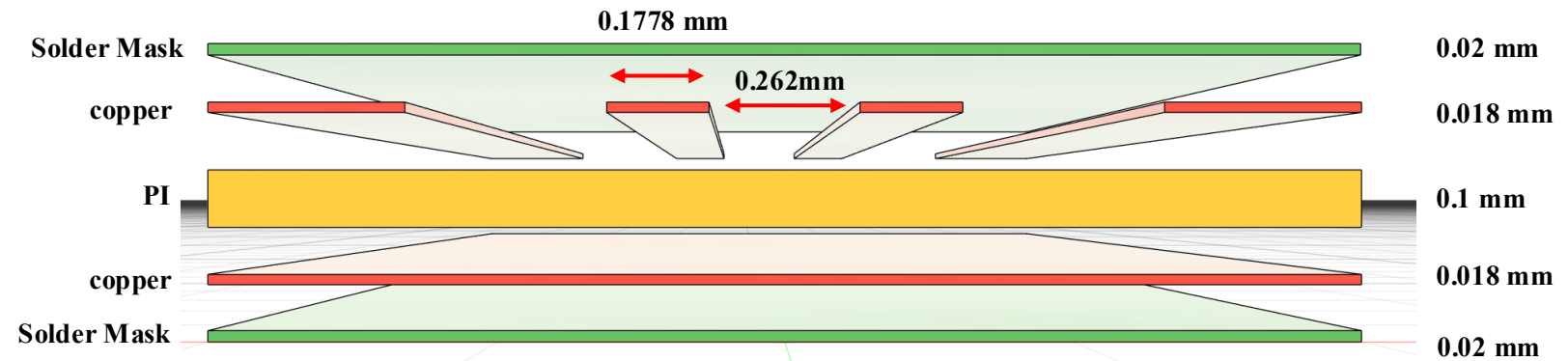
Crosstalk check



Serial or parallel powering power check

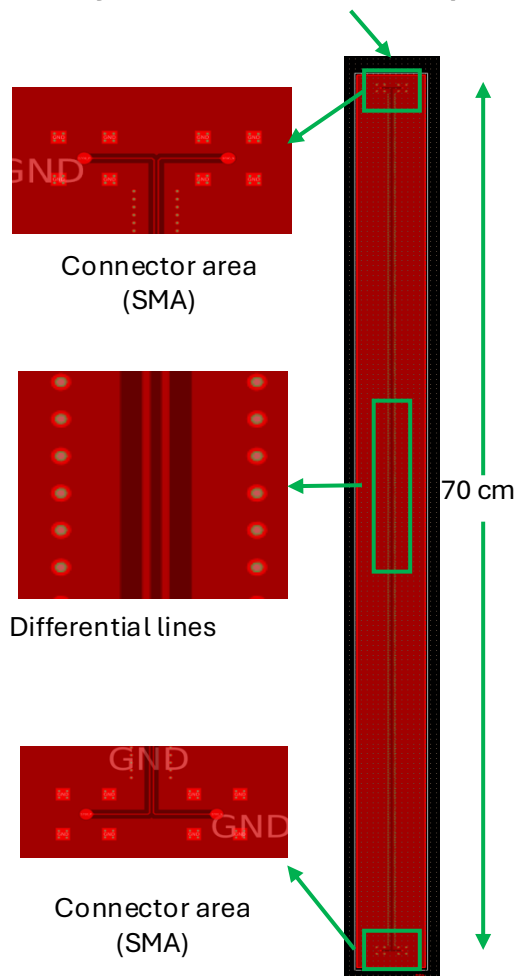
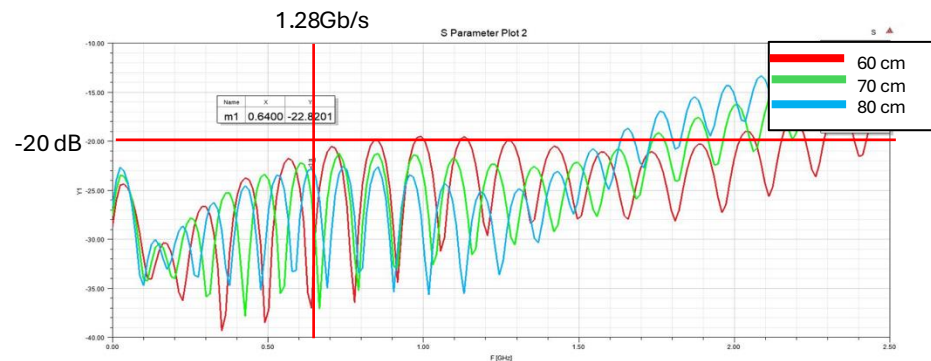
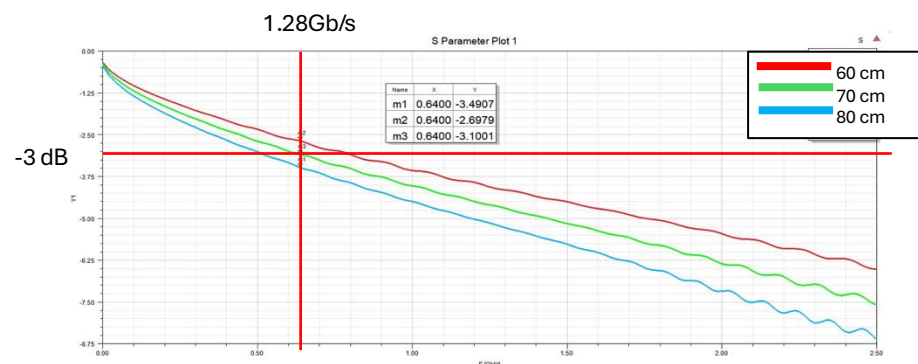
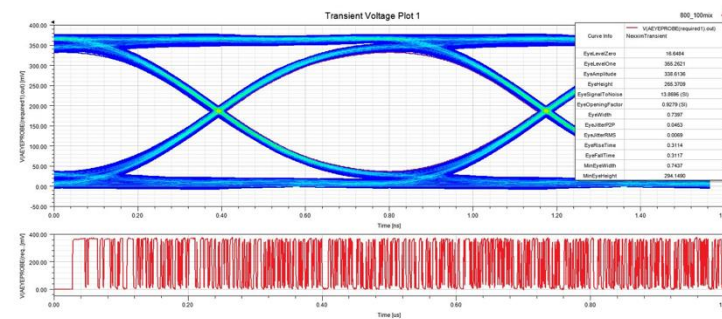
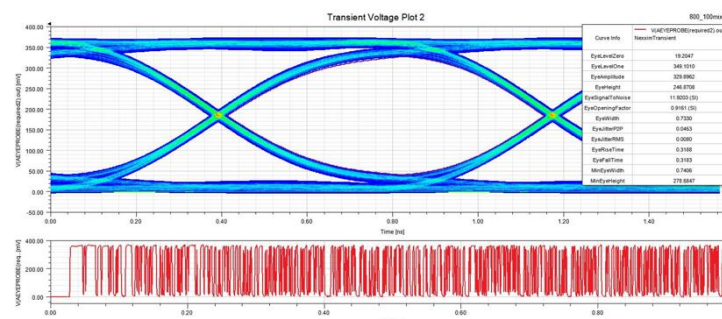
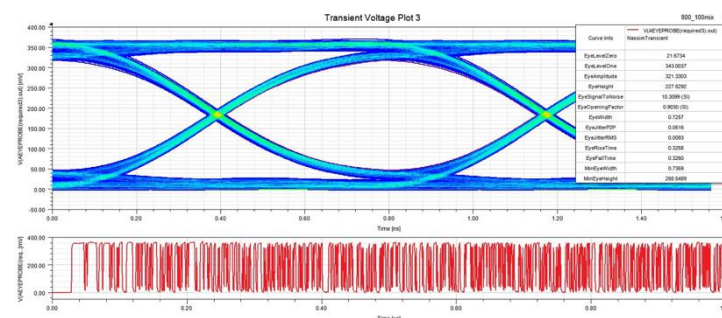
Electronic R&D – Impedance Match

- The signal integrity in 70 cm, 1.28 Gb/s require:
 - A group of reliable traces parameters
 - Impedance match is not enough
 - S-parameters measurement is more reliable
- Strategy:
 - Trace parameters based on the production capacity
 - Simulation
 - Prototype test



Trace Parameters - Simulation

Only one differential pair

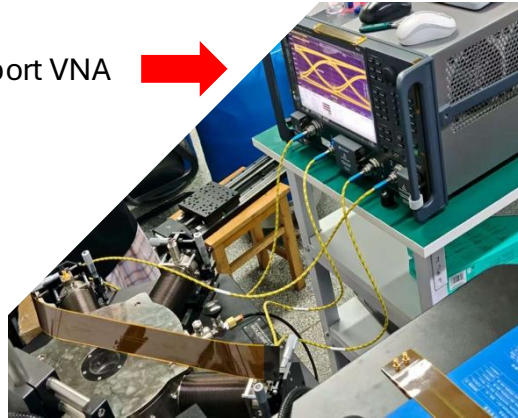


Trace parameters can fit all the signal integrity requirements we need in simulation.

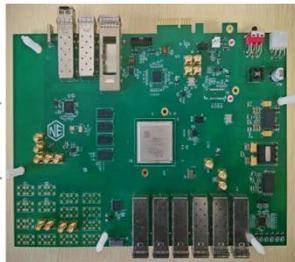
Trace Parameters – Prototype Test



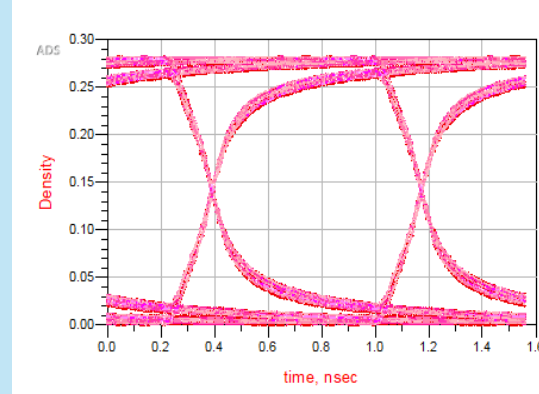
4 port VNA



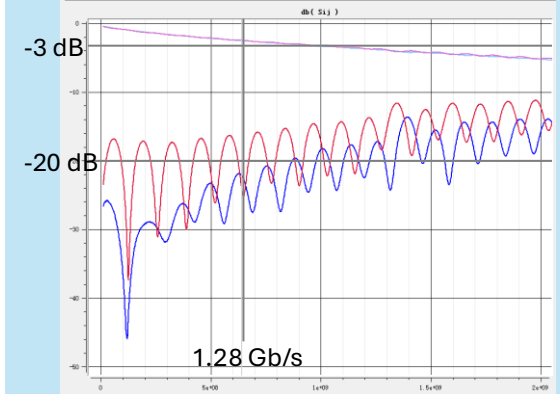
Insertion and return loss test



Bit error rate test



Eye diagram



Insertion & return loss

Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
				<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit
1.280 Gbps	3.567E14	0E0	2.803E-15	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit

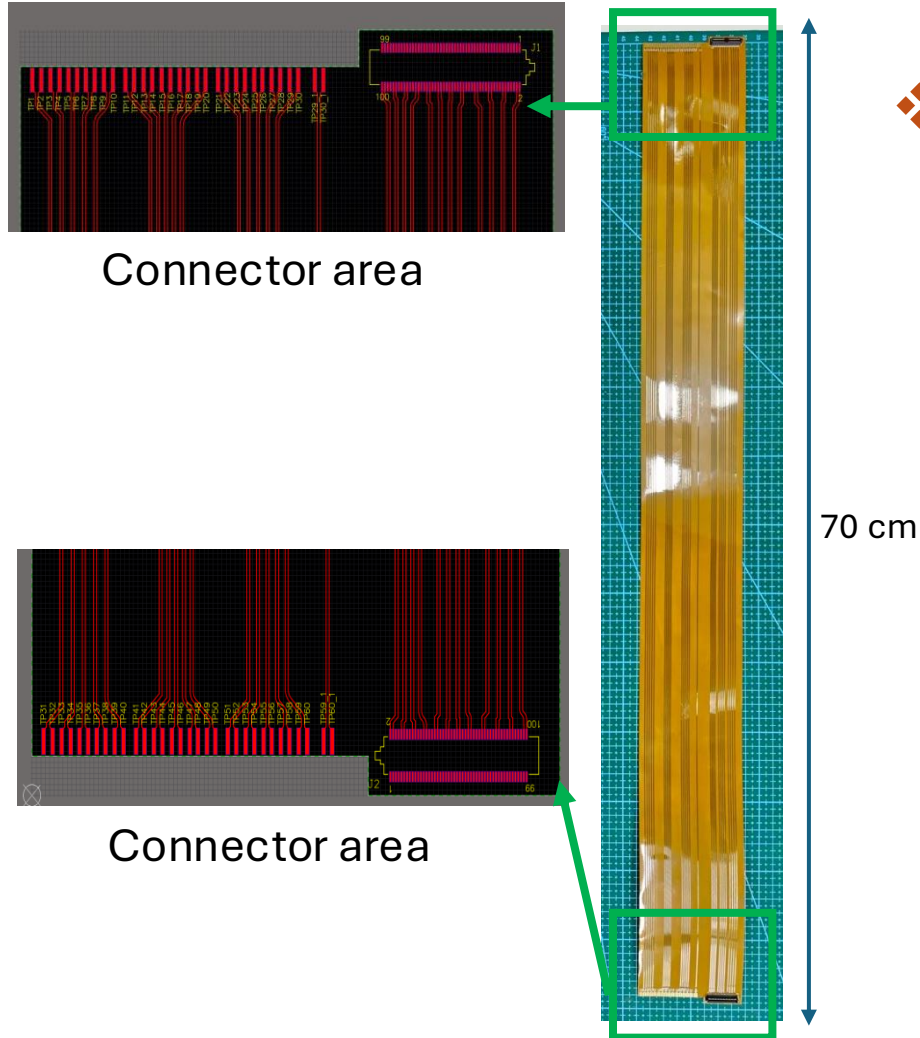
BER < 8.42×10^{-15} , 95% CL at 1.28 Gb/s, 63 hours test

Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
				<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit
5.120 Gbps	3.258E14	0E0	3.07E-15	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit

BER < 9.2×10^{-15} , 95% CL at 5.12 Gb/s, 16 hours test

Trace parameters can fit all the requirements we need for all 3 flexes used in test. 

Electronic R&D – Cross Talk



- ❖ The high granularity and challenges in layout require:
 - Small spacing between differential pairs

- ❖ Prepare prototype to:

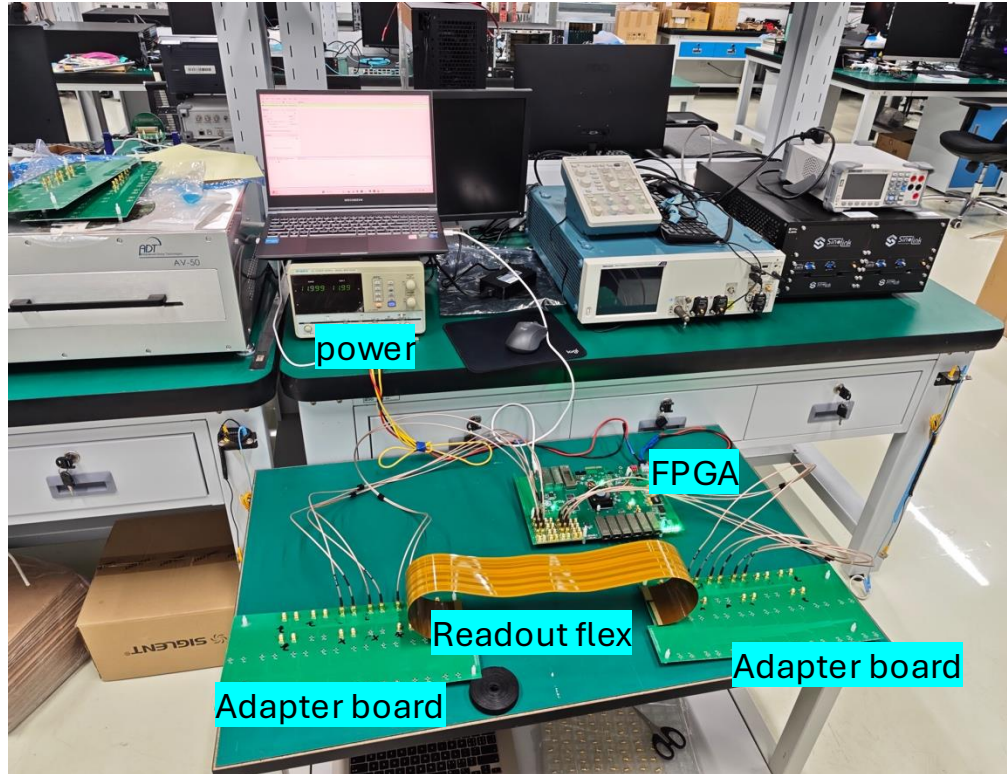
- Test the influence the crosstalk.
- Different spacing options.

1 mm
conservative choice

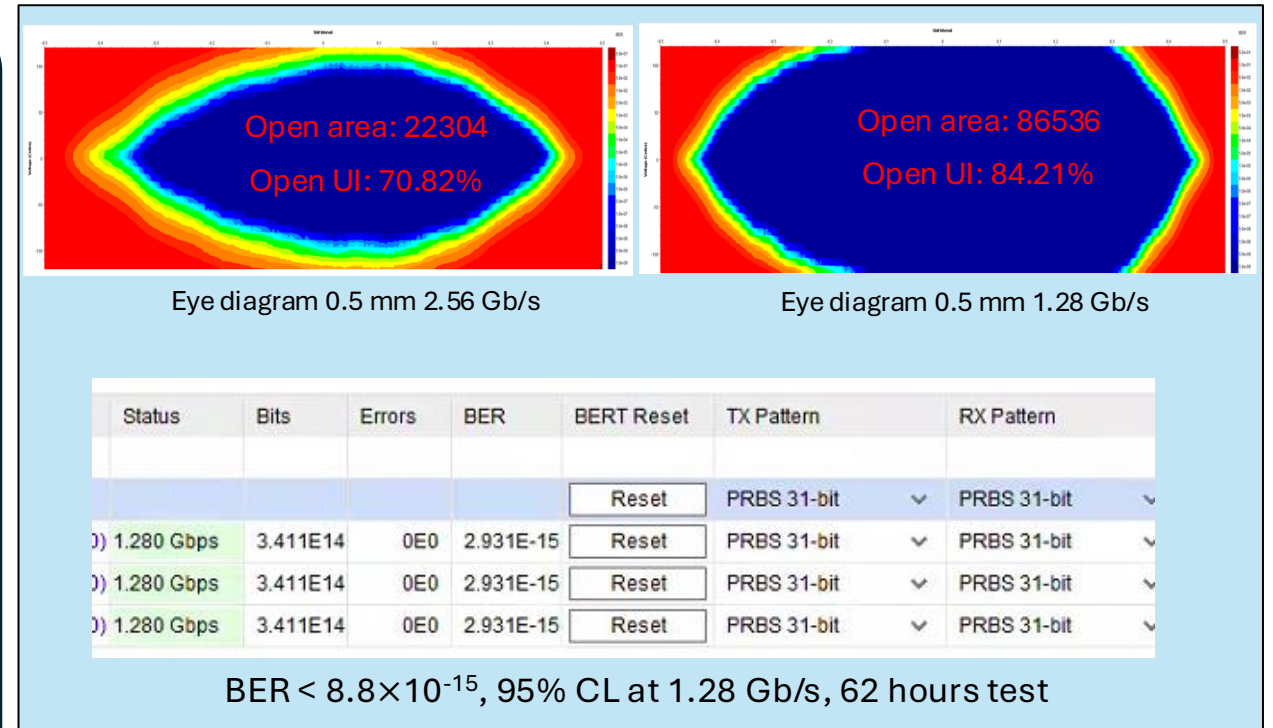
0.762 mm
Industry experience

0.5 mm
Aggressive choice

Crosstalk - Prototype



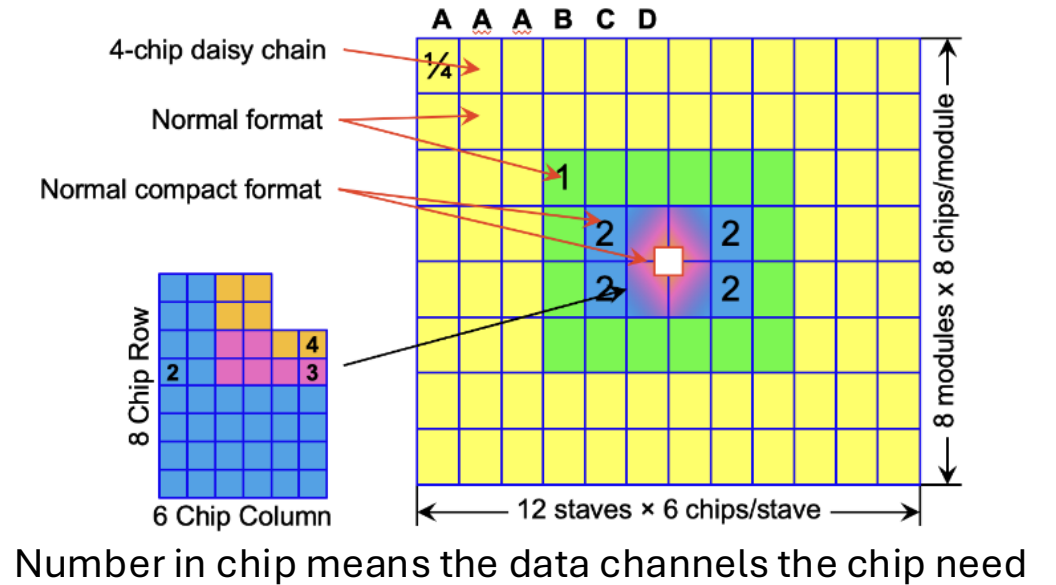
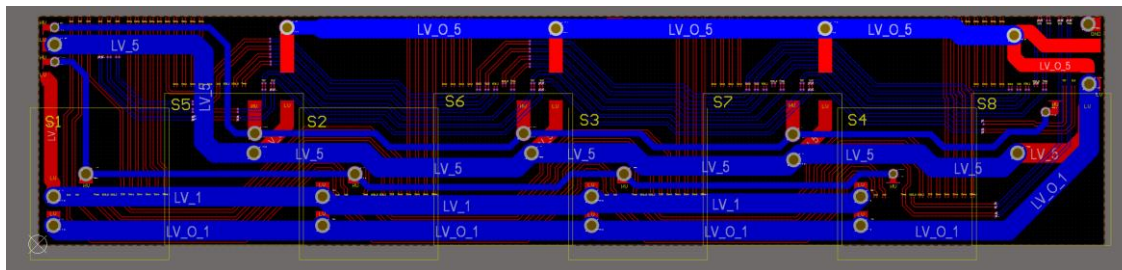
Test the signal integrity



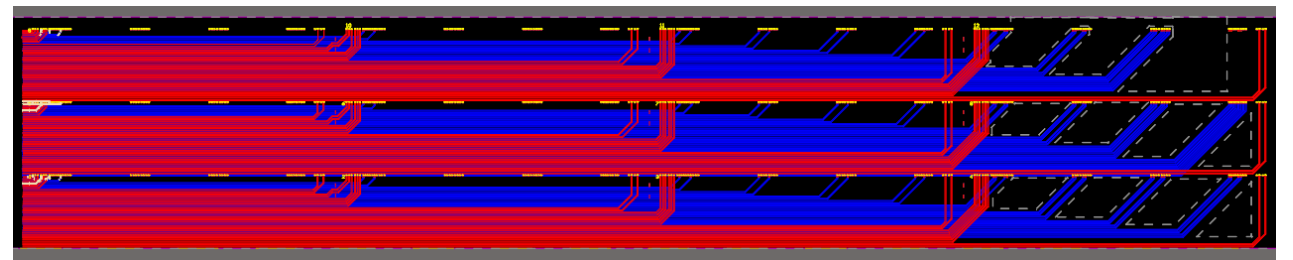
- ❖ Base on the test result, the 0.5 mm choice:
 - Good eye diagram performance
 - BER < 8.8×10^{-15} with 95% CL

Electronic R&D – PCB Layout

- ❖ High granularity and a large number of channels make PCB layout challenging:
 - Efficient use of the available space
 - Routing for the required data rates
- ❖ Preliminary designs completed.
 - Further optimization required.
 - Simulation ongoing.



Hybrid-flex (initial version)

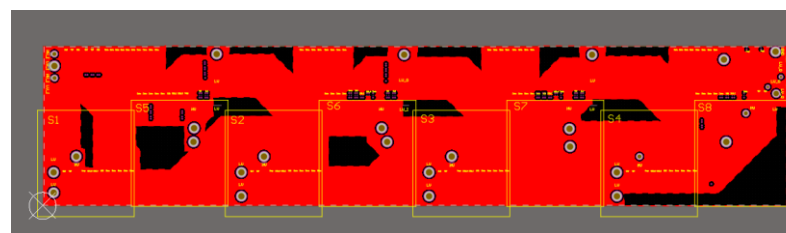


Readout-flex (initial version)

Material Budget Optimization

- ❖ Excellent tracking performance requires a detector design with a low material budget.

EMI:	15	um
PI coverlay:	12.5	um
adhesive:	15	um
base copper(9)um+plated	18	um
Polyimide	100	um
adhesive:	25	um
base copper(9)um	9	um
Polyimide	100	um
base copper(9)um+plated	18	um
adhesive:	15	um
PI coverlay:	12.5	um
EMI:	15	um
Stack up parameters	355	um

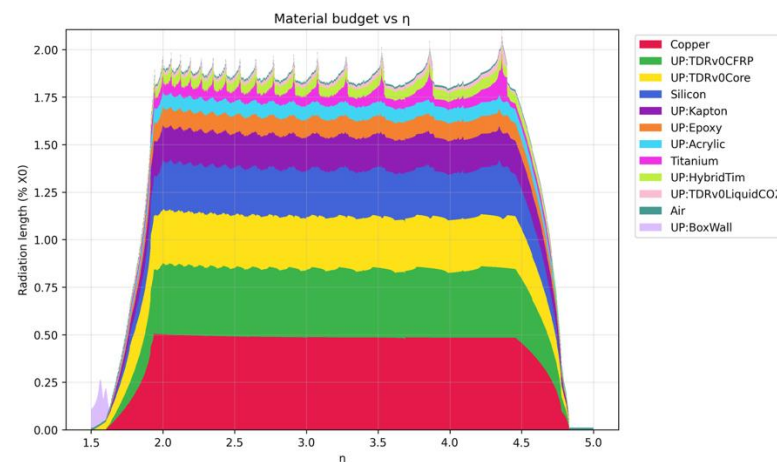


Hybrid-flex ground layer



Readout-flex ground layer

Cutouts in the flex ground layer to reduce the material budget.



Copper thickness: 34.84 μm (calculate by geometric factor)

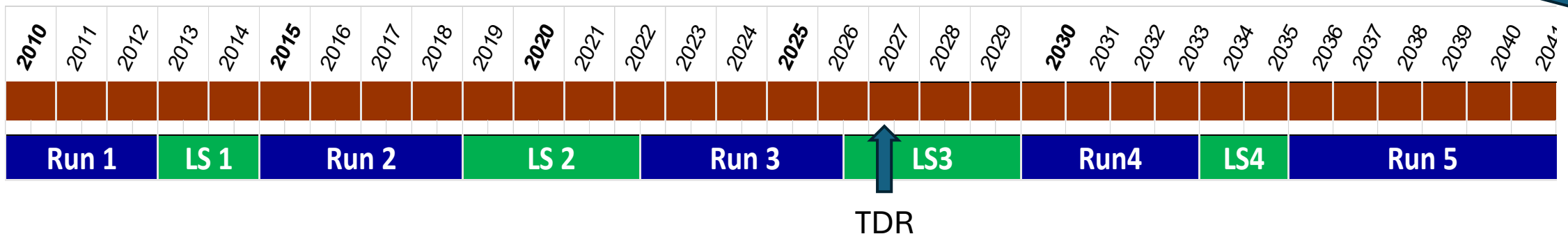
← Estimation of material budget for the **busiest** stave

➤ Will do further optimization.

Conclusion and Prospects

- **For the hybrid-flex and readout-flex in R&D:**
 - **Mechanical:** prototype development and feasibility validation.
 - **Thermal:** flex production and development of a full-scale stave prototype.
 - **Electronic:** preliminary design based on hit density and data rate.
 - Trace parameters □ FPC layout
 - Cross talk
 - **Material budget** Radiation resistance and power check is scheduled
- Thanks for

- ◆ **Studies for the LHCb TDR are continuing.**



Back up

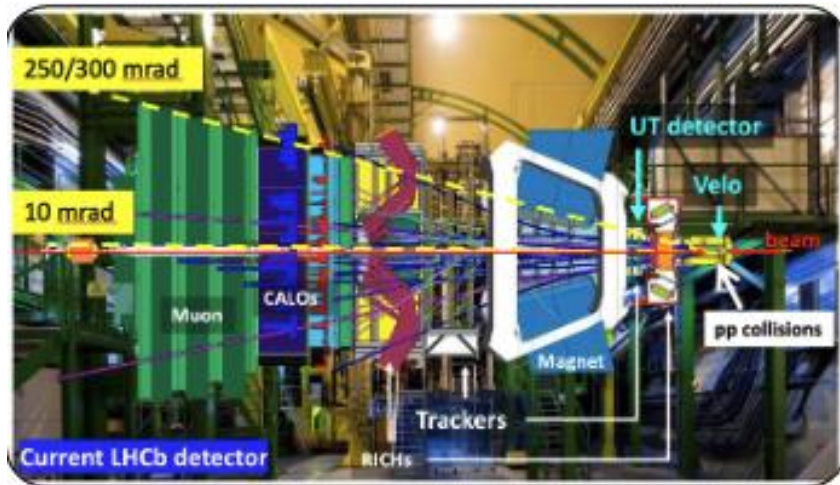
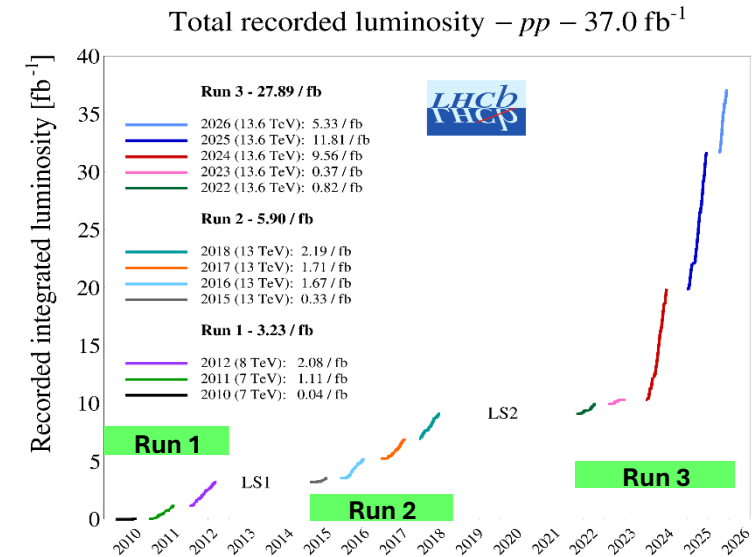
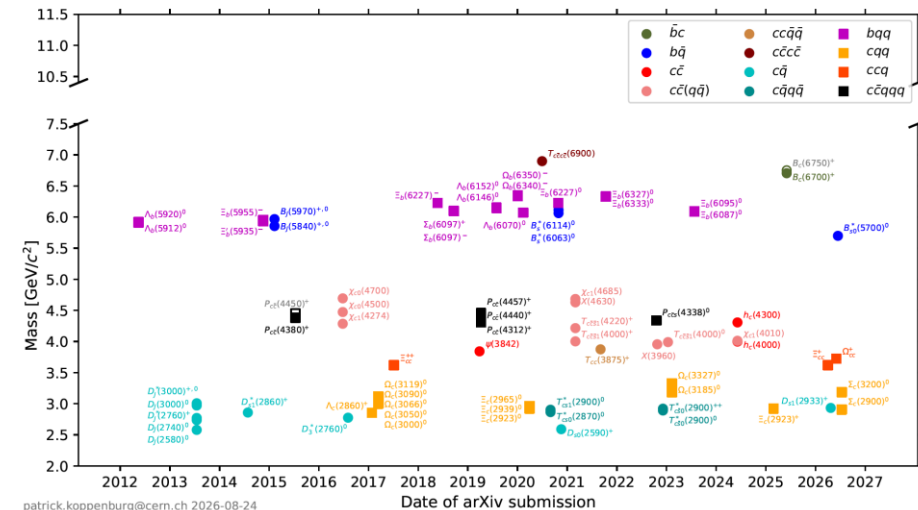
LHCb Overview

LHCb: single-arm forward spectrometer at LHC

- Searches for NP and tests SM at the precision frontier

Upgrade I (2019~2023)

- No hardware trigger
- Lumi x5: $4 \times 10^{32} \text{cm}^{-2} \text{s}^{-1} \Rightarrow 2 \times 10^{33} \text{cm}^{-2} \text{s}^{-1}$
- New tracker, including UP
 - ❑ UP: 4-layer silicon strip detector



Backup-UP Electronic Architecture Overview

