Projects for FCC-ee Vertex Detectors

FCC-week 2026
Helsinki
June 8-12, 2026

Dominik Dannheim (CERN)

Outline

- FCC-ee vertex-detector requirements
- Vertex-detector concepts
- Detector R&D projects
- Conclusions

Disclaimer:

- Not a complete overview, showing only few examples
- Focus on specific R&D for FCC-ee / CEPC vertex-detector

→ not covering the (many!) developments for outer tracking + timing layers

Physics requirements and experimental constraints

- **Physics goals**:
  - Precision Higgs / EW / top measurements
  - Direct/indirect BSM searches
- Requires excellent Flavour tagging (c, b), life-time measurements
  - → Vertex resolution: $\sigma(d0) \sim 5 \oplus 15/(p[\mathrm{GeV}]\sin^{3/2}\theta)$ μm
    - → single-plane resolution ~3 μm
    - → low material budget <0.2% X0 per layer → low power+ air-flow cooling
  - Pile-up / background rejection
    - → low-angle coverage, timing

Experimental constraints:

- 30 mrad crossing angle, focusing quadrupoles inside detector

→ B-field limited to ~2 Tesla

- High rate of physics events (up to 100 kHz, bx spacing down to 30 ns)

→ Integration time <1 μs for occupancy and pile-up (30 ns @ Z-pole)

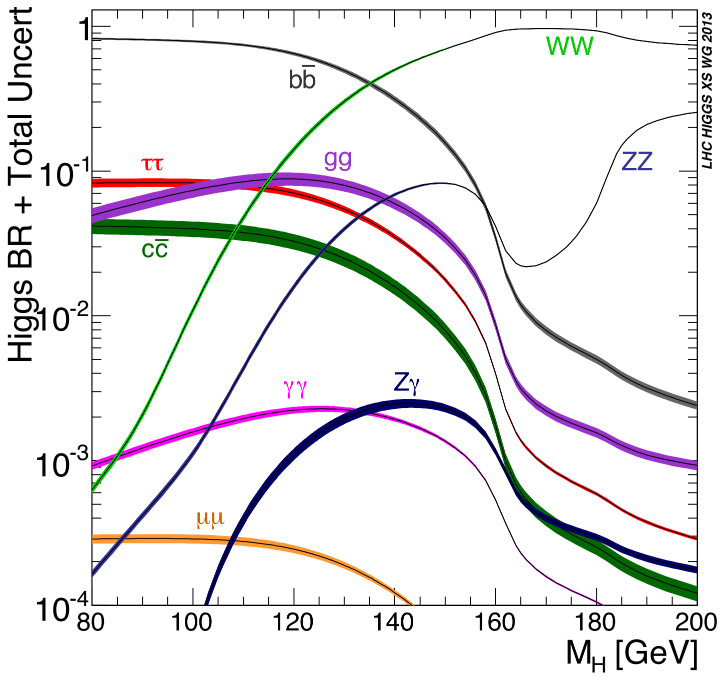
→ Fast detector frontend and DAQ

- Main backgrounds:
  synchr. rad. (requires shielding) + incoherent pairs (up to ~200 MHz/cm^2)
- Continuous collisions (100% duty cycle)

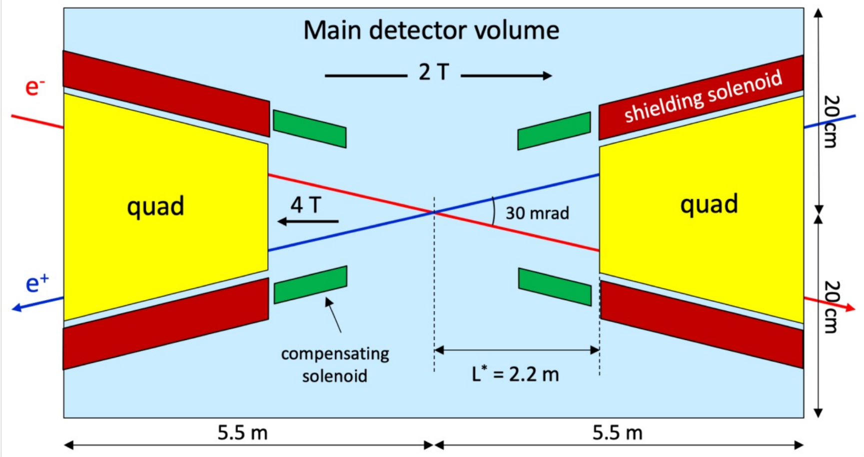
→ Pulsed powering not possible

- Moderate radiation exposure:
  NIEL: < 10^{14} neq/cm^2/y; TID: < 100 kGy / year

Higgs branching ratios



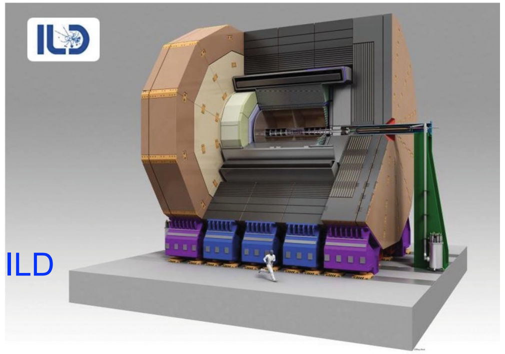
FCC-ee detector region



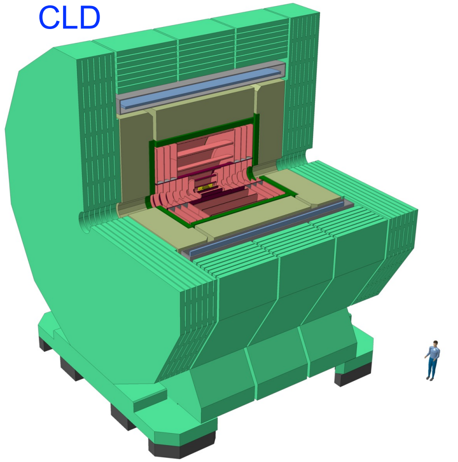
Detector concepts

Collider	**FCC-ee**				**CEPC**	
Detector Concept	FCC-ee ILD	CLD	FCC-ee IDEA	ALLEGRO	CEPC baseline	CEPC IDEA
B-field [T]	2	2	2	2	3	2
Vertex inner radius [mm]	13	13	14	14	11	11
Tracker out. radius [m]	1.8	2.2	2.0	2.0	1.81	2.05
Vertex	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel	Si-pixel
Tracker	TPC/ Si strips	Si-pixel	DC/ Si-strips	DC/Si-strips or Si-pixel	TPC/Si-strips or Si-strips	DC/ Si-strips

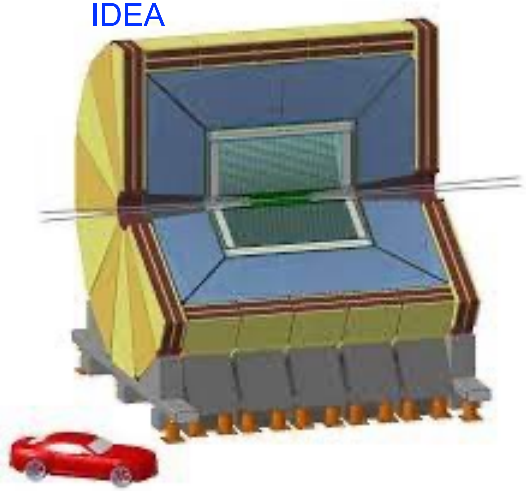
https://europeanstrategyupdate.web.cern.ch/sites/default/files/Submitted_Input_2025.05.26.pdf *arXiv:1811.10545*



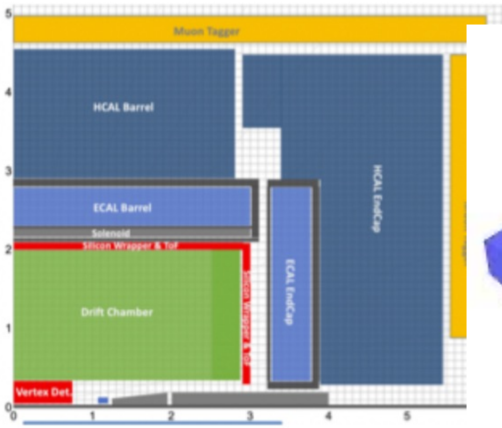
CLD



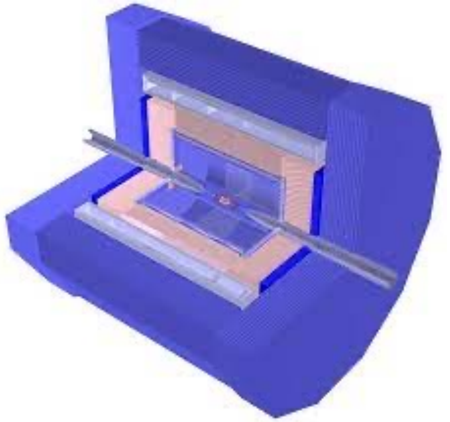
IDEA



ALLEGRO



CEPC baseline



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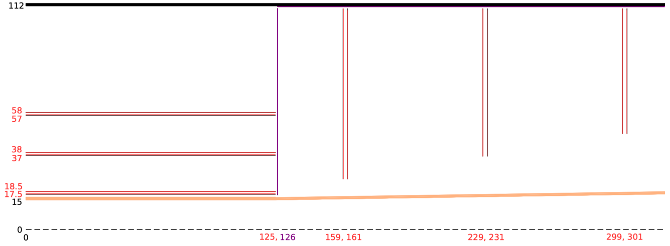
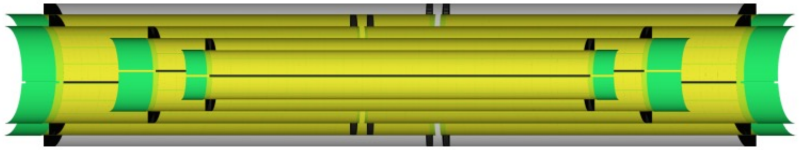
https://europeanstrategyupdate.web.cern.ch/sites/default/files/Submitted_Input_2025.05.26.pdf *arXiv:1811.10545*

All concepts contain MAPS vertex detectors:
- 5-6 layers in doublets or singlets
- Different layouts under consideration:
    - Barrel + endcap
    - Barrel-only (stitched bent silicon, like in ALICE ITS3)

CLD double-layer VXD layout

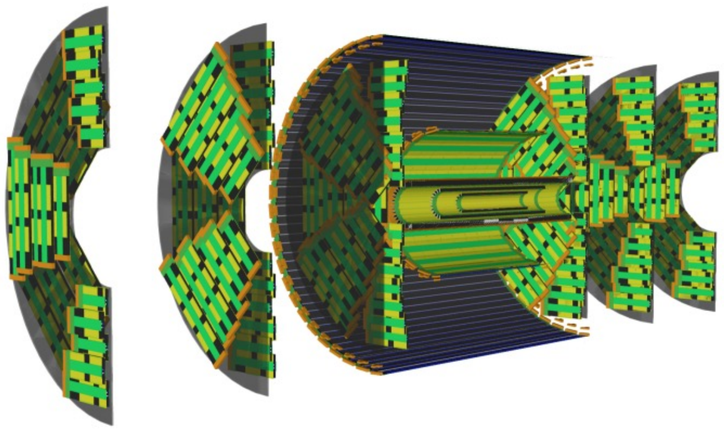


Ultra-light FCC-ee VXD concept



https://pos.sissa.it/476/1062/

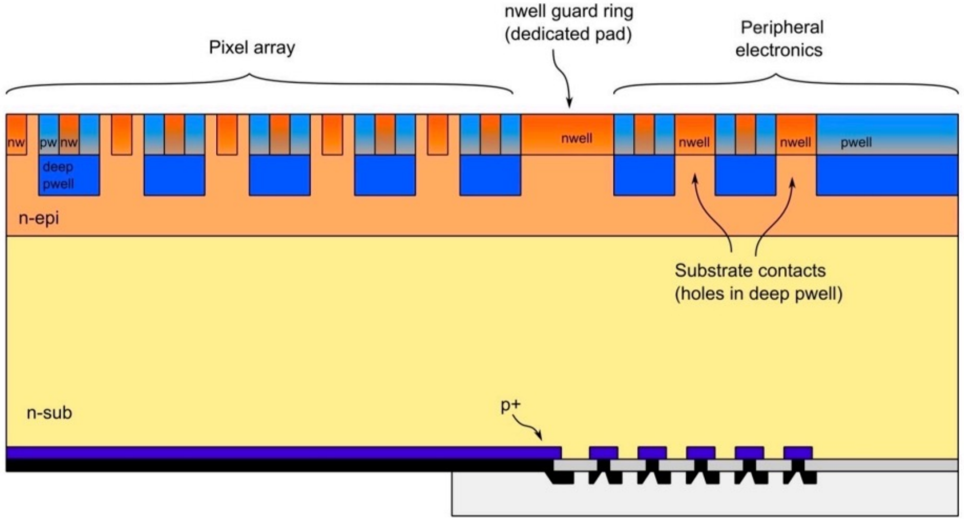
IDEA/ALLEGRO VXD



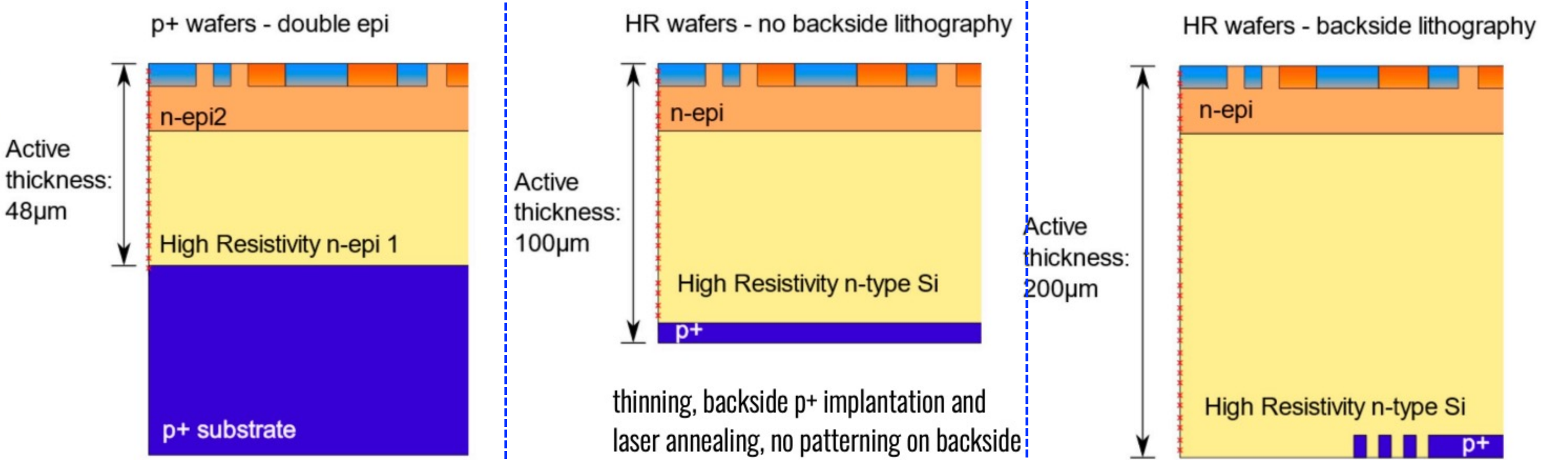
ARCADIA fully-depleted 110 nm MAPS

ARCADIA collaboration between INFN and L-Foundry

- R&D on semiconductor sensor technology, IP-core design and ASICs, advanced DAQs
- Target applications include FCC-ee (IDEA) vertex and tracker
- Using L-Foundry 110 nm MAPS process
  - backside biasing for full depletion
  - Thickness 50-700 um → large signals, charge sharing
  - Various processing options, including high-resistivity substrates and backside implantations



Process used for FCC-ee vertex R&D



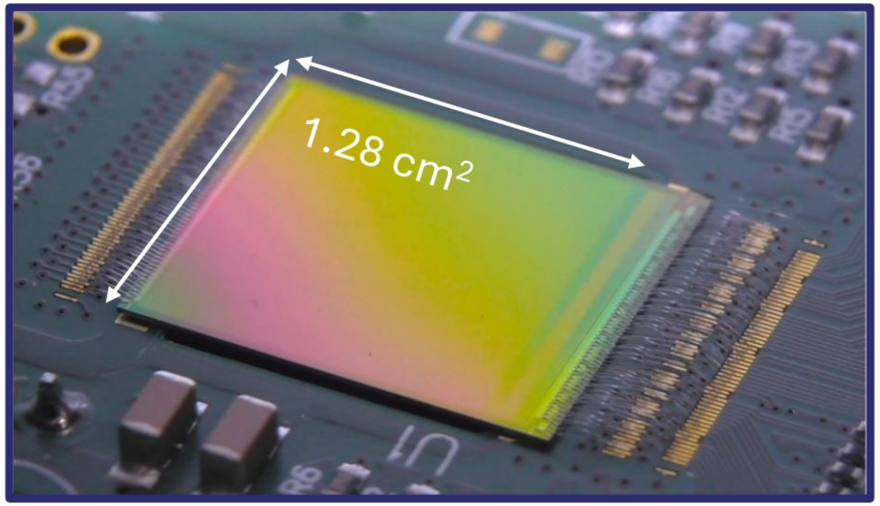
thinning, backside p+ implantation and laser annealing, no patterning on backside

https://agenda.infn.it/event/47923/contributions/276340/

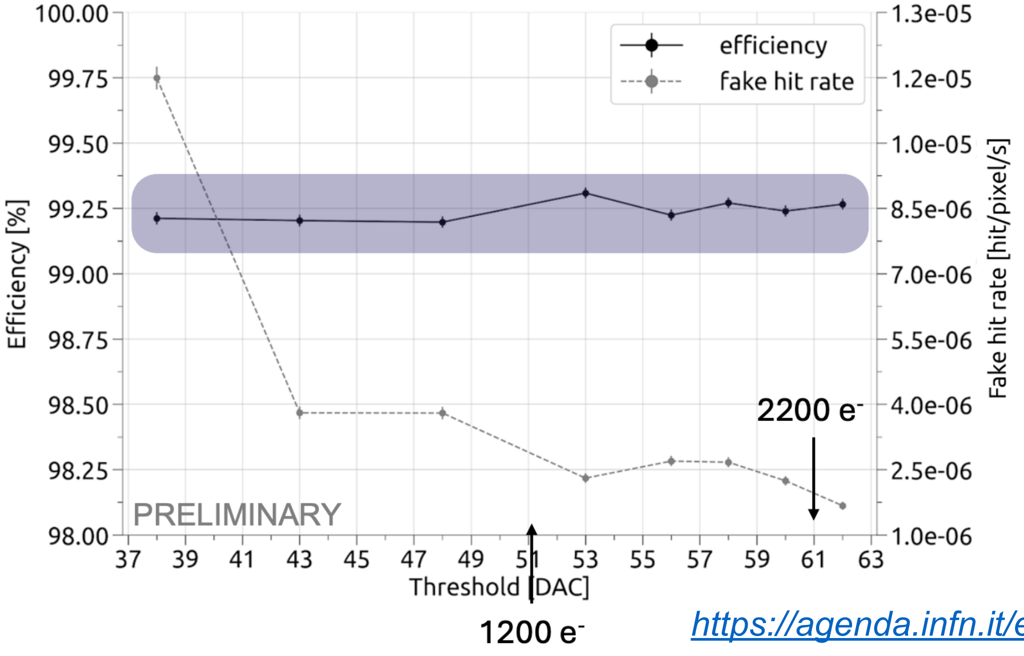
ARCADIA MD3 demonstrator

First full-size prototype ARCADIA MD3

- 512 x 512 pixels, 25 um pitch, 50-200 um active thickness
- data-driven binary r/o, <30 mW/cm^2, 100 MHz/cm^2 rate
- Encouraging lab and test-beam characterization results:
  - Noise ~30 e-
  - Efficiency >99%
  - Thick active region and low threshold range → significant charge sharing
  - Spatial resolution: minimum residual width of 4.6 μm with 1D average cluster width of about 1.6 pixels



MD3 efficiency and fake-hit rates



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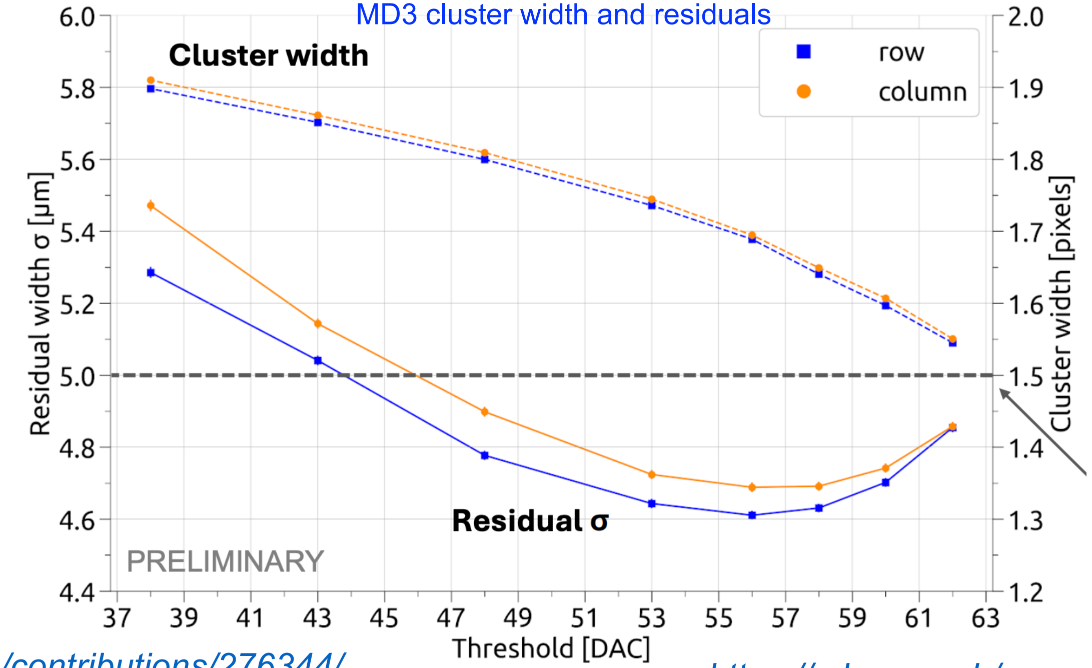
MD3 cluster width and residuals



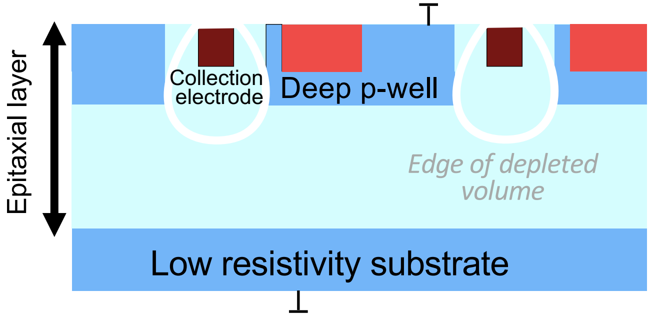
https://cds.cern.ch/record/2954917/

CEPC 180 nm MAPS vertex-detector project

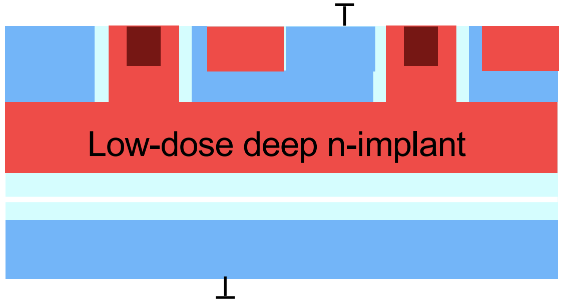
CEPC vertex-detector project

- IHEP Beijing: Chip designs, electronics, DAQ and prototype assembly
- IPHC/CNRS: Collaboration in framework of FCPPL, BELLE II upgrade
- IFAE: Collaboration in Taichu chip design
- ShanDong U.: Stitching chip design, Taichu chip design
- CCNU: Jadpix chip design
- Northwestern Polytechnical U. : Taichu Chip design
- Nanchang U. : Taichu chip design
- Nanjing U. : testbeam study

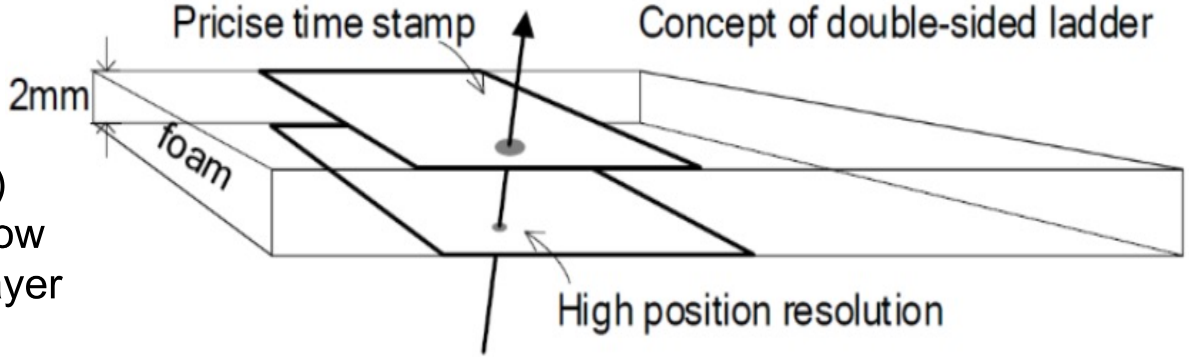
Standard 180 nm process (JadePix, TaichuPix)



Modified 180 nm process (TaichuPix)

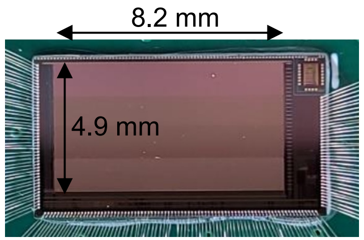


Double-sided ladder

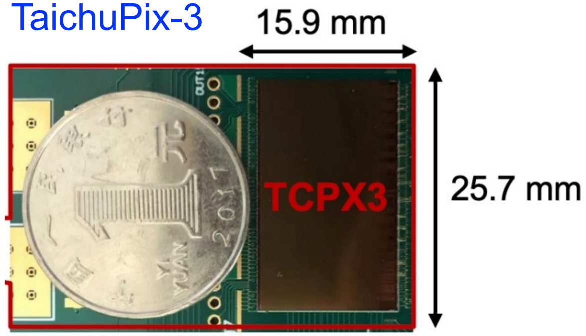


- Main target: CEPC vertex detector (very similar specs as FCC-ee)
- Using TJ 180 nm standard/modified CMOS imaging process for now
  - Small-collection electrode + 20 µm high-resistivity epitaxial layer
  - Plan to move to TPSCo 65 nm for final chips
- Considering separate layers for timing (~1 µs) + position resolution (<=3 µm)
- Baseline for inner vertex layer: bent stitched silicon (like ALICE ITS3)
- Several prototypes, focusing on different aspects
  - JadePix-3 → small prototypes: 23 x 16 µm^2 pitch, rolling shutter r/o, low power, high spatial resolution
  - TaichuPix-3 → full-size prototypes: 25 µm x 25 µm^2 pitch, hit-driven r/o, high data rate (36 MHz/cm^2)

JadePix 3



TaichuPix-3



See also presentation on CEPC detector R&D by Joao on Wednesday

https://indico.cern.ch/event/1439336/contributions/6242103

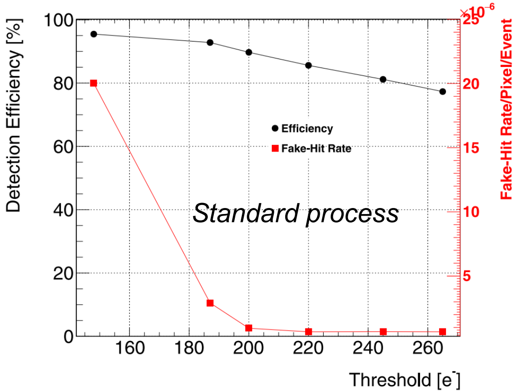
CEPC vertex detector – beam-test results from prototypes

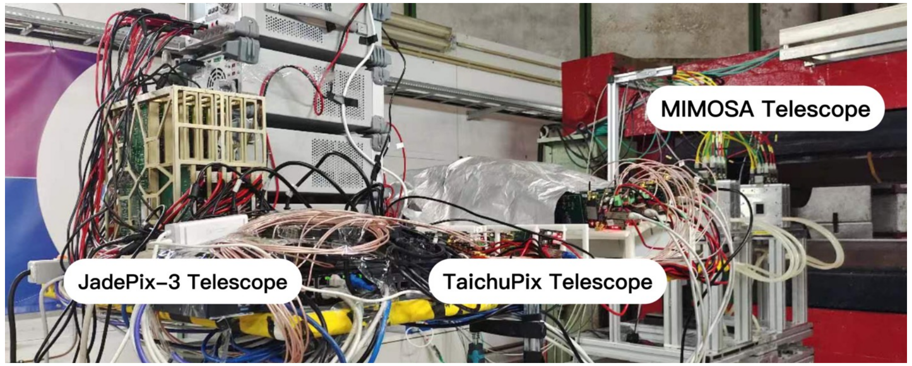
Several test-beam campaigns with Jadepix-3 and TaichuPix-3 prototypes in beam-telescope configuration

→ Testing sensor performance and system aspects of multi-plane detector system

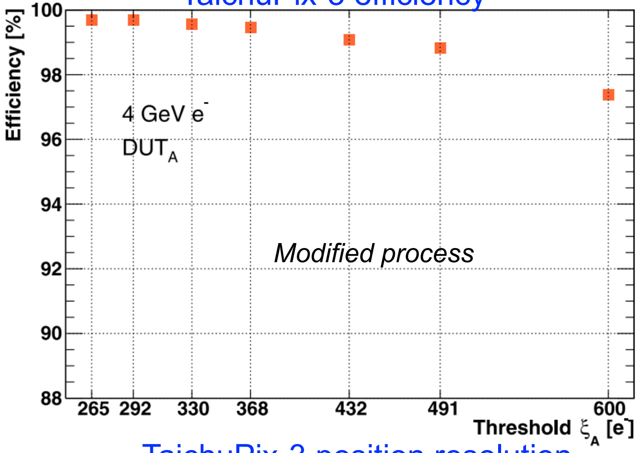
→ Achievable position resolution above target of 3 μm

JadePix-3 efficiency + fake-hit rate

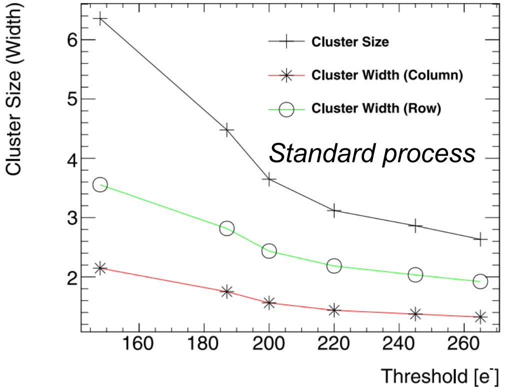




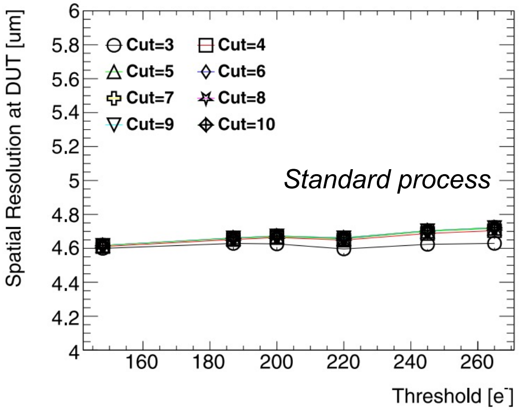
TaichuPix-3 efficiency



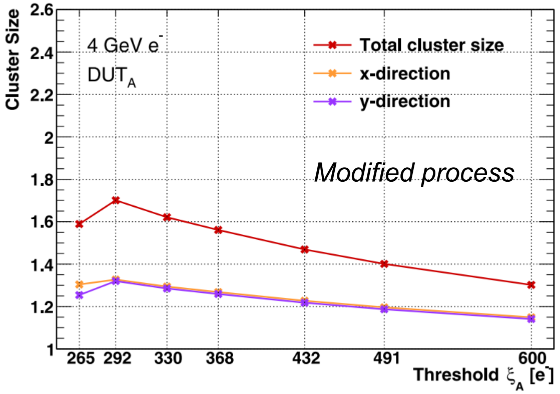
JadePix-3 cluster size



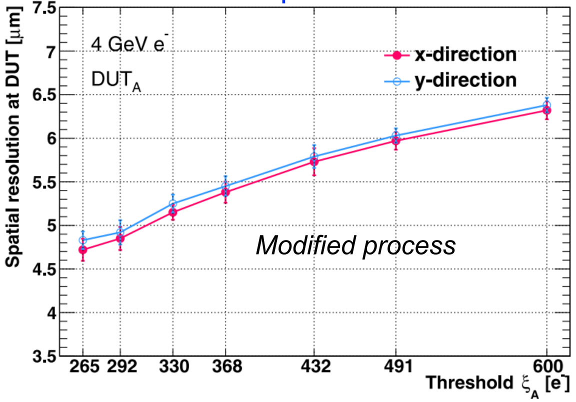
JadePix-3 position resolution



TaichuPix-3 cluster size



TaichuPix-3 position resolution



JadePix-3 (23 x 16 μm^2 pitch)

- Efficiency >90% for negligible fake-hit rate
- Significant charge sharing → multi-pixel clusters
- binary-resolution limit achieved: 6.0 μm x 4.6 μm

https://doi.org/10.1016/j.nima.2024.169551

TaichuPix-3 (25 x 25 μm^2 pitch)

- Efficiency >99.5% for negligible fake-hit rate
- Significant charge sharing → multi-pixel clusters
- Resolution better than binary limit: ~4.5-5 μm
- Better performance with modified process

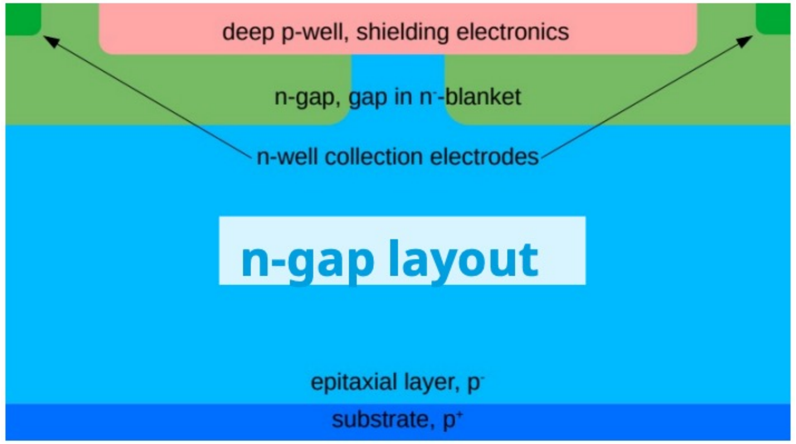
https://doi.org/10.1016/j.nima.2023.168945

65 nm MAPS technology validation

TPSCo 65 nm ISC CMOS imaging process validation for HEP

- 10 µm epitaxial layer, 7 metal layers, 300 mm wafers with stitching
- Collaboration CERN EP R&D, ALICE ITS3, DRD3/7, many institutes + other projects
- Small feature size → small pixels (~10-35 µm), enhanced performance
- Encouraging results from common MLR1 and ER1 productions in 2021-22:
  - Common submission of technology demonstrators from various groups
  - Stitched sensors (MOSS/MOST) for ALICE ITS3
  - Successful large-scale testing + simulation campaigns
  - Process modifications and sensor-design optimizations proven to work as expected
  - → Full efficiency, <100 ps sensor timing for optimized designs, up to 10^{15} n_{eq}/cm^2
  - → Feasibility of stitching for wafer-scale sensors
  - → Feasibility of porting hybrid r/o architecture to monolithic process (H2M)
  - → Thinning to <20 µm w/o performance loss
- Candidate technology for ALICE3 and FCC-ee vertex developments

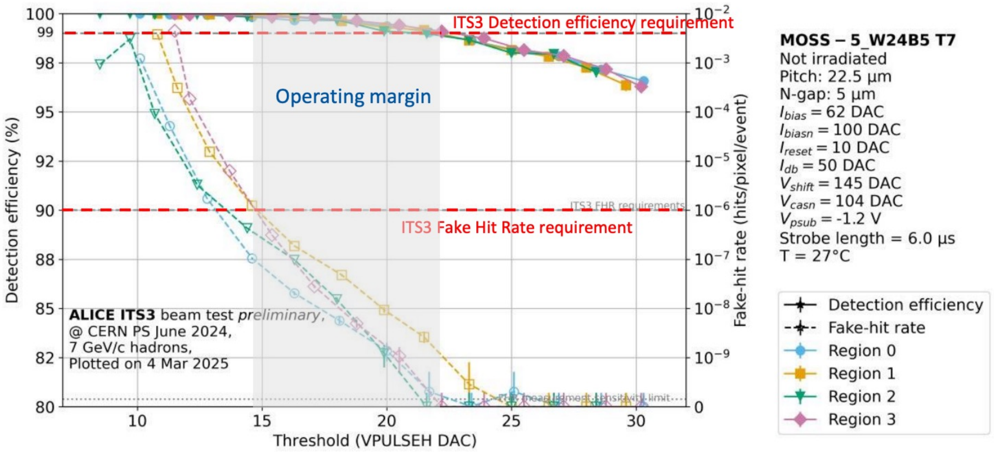
Small-collection-electode sensor layout in TPSCo 65 nm



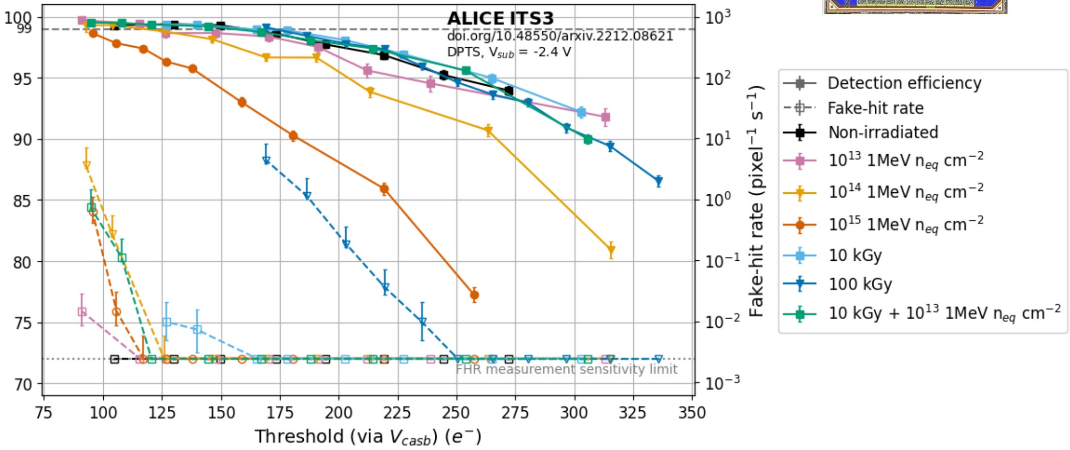
https://indico.cern.ch/event/1581713/contributions/6763822

Comprehensive review of 65 nm results: *F. King et al.*, https://doi.org/10.1016/j.nima.2026.171672

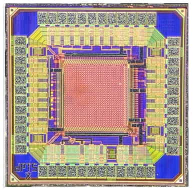
MOSS test-beam results



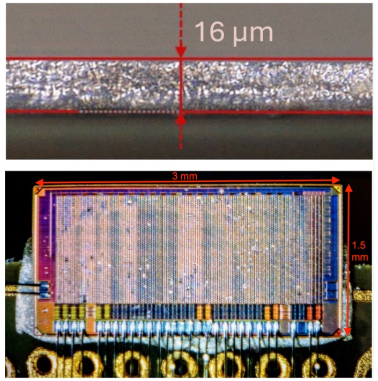
DPTS efficiency + fake-hit rate in test beam



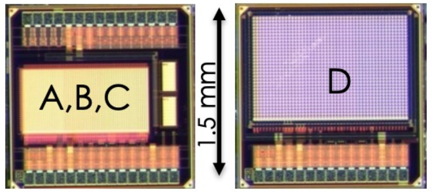
DPTS, 15 µm pitch, CERN



H2M, 35 µm pitch, DESY/CERN



CE-65, 15-25 µm pitch IPHC



OCTOPUS 65 nm

OCTOPUS: Optimized CMOS Technology fOr Precision in Ultra-thin Silicon
(octopus.web.cern.ch)

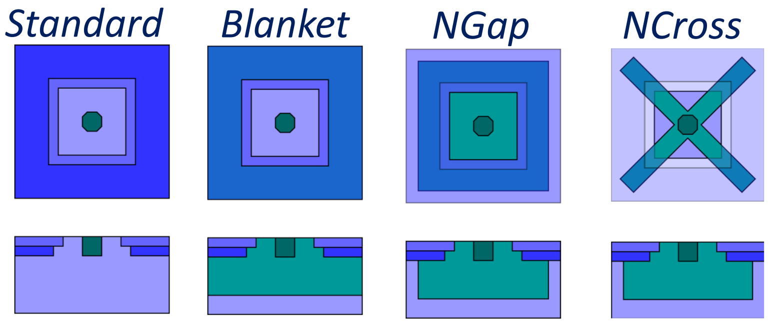
- DRD3 R&D project towards vertex detectors for future lepton colliders
  - Intermediate target: sensors for beam telescopes
- Reticle-size CMOS sensor in TPSCo 65 nm process
- Full R&D chain performed by 13 institutes across Europe
- First test-chip submission planned for Q4/2026 (ER3) in collaboration with MANTA tracker project

Member institutes	
APC Paris	GSI Darmstadt
Universität Bonn	IPHC Strasbourg
CPPM Marseille	MBI Vienna
CERN Geneva	NIKHEF Amsterdam
DESY Hamburg	University of Oxford
ETH Zürich	Universität Zürich
FNSPE CTU Prague	

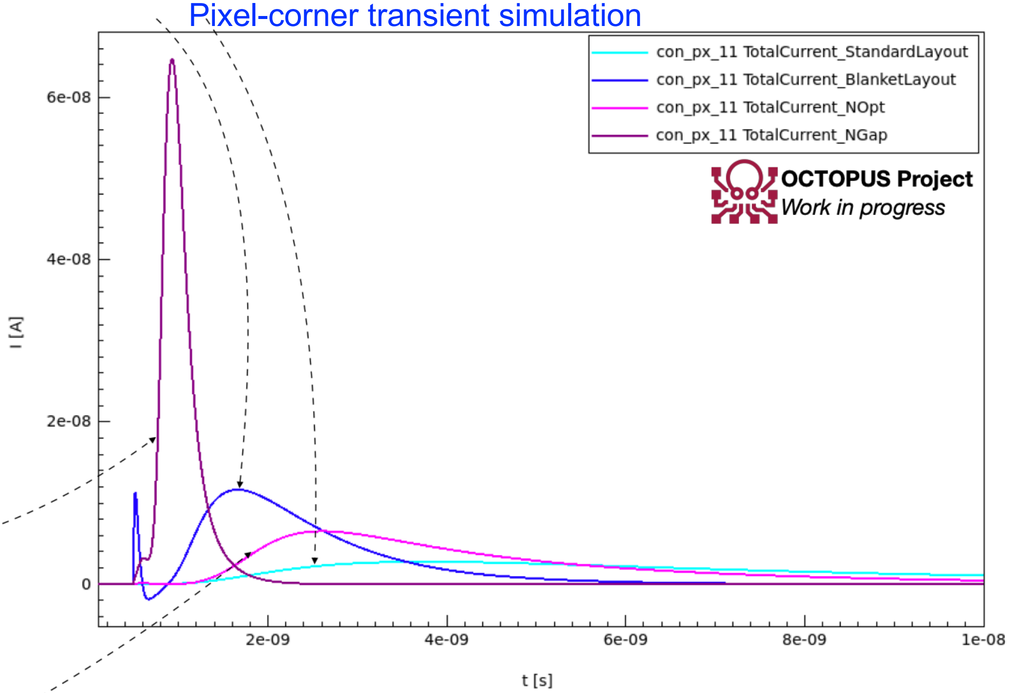
OCTOPUS sensor layout optimization

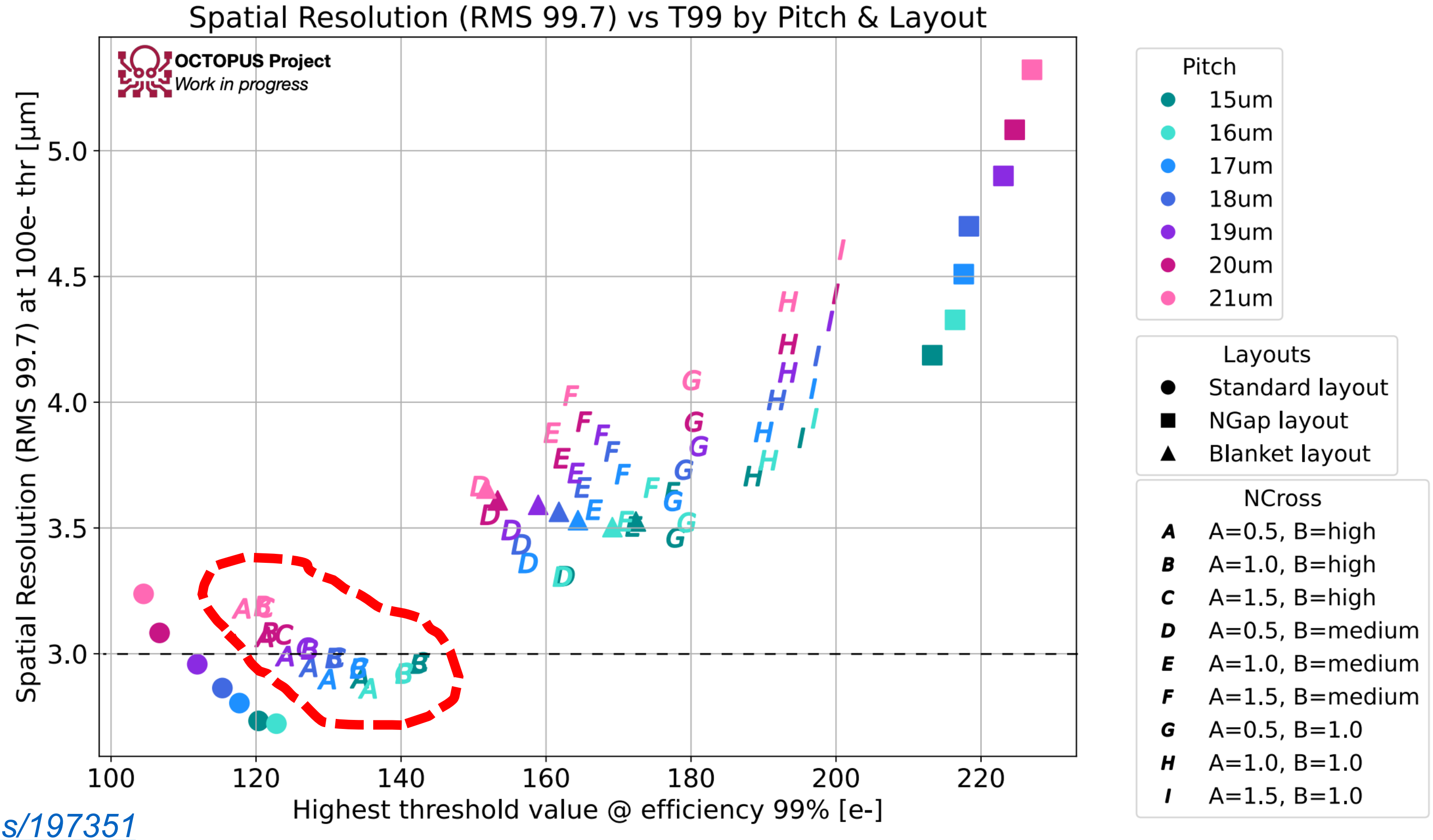
Sensor-design optimization with TCAD + AllpixSquared MC simulations

- Aim: 3 µm resolution with full efficiency and few nanosecond timing
- Use results from existing TPSCo 65 test chips to benchmark simulations
- Large parameter space of process variants, pitch, ToT resolution
- Trade-off between: charge sharing, efficiency, timing
- Targets are in reach with cross-shaped implementation of deep N-layer in the *modified* process (*NCross*) for 18-20 µm pitch



Pixel-corner transient simulation



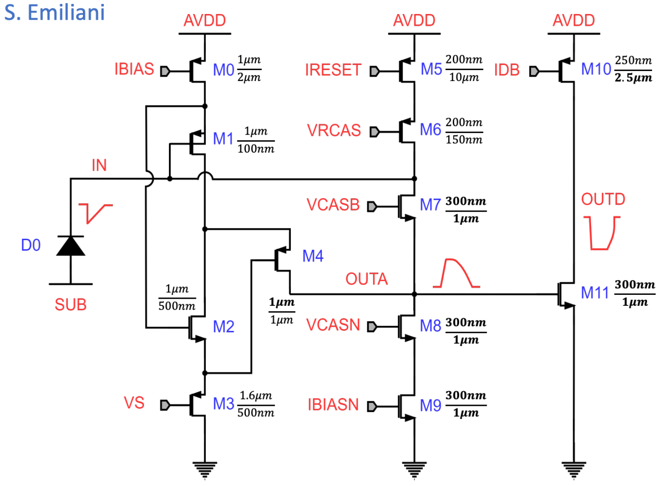


https://indico.desy.de/event/51462/contributions/197351

OCTOPUS ASIC design

FE based on MOSAIX compact amplifier S. Emiliani
- Small footprint
  → Leaves space to place readout
- Time-over-Threshold measurement
  → correct for time walk
  → improve spatial resolution
  by charge interpolation
- Alternative designs also considered

MOSAIX frontend



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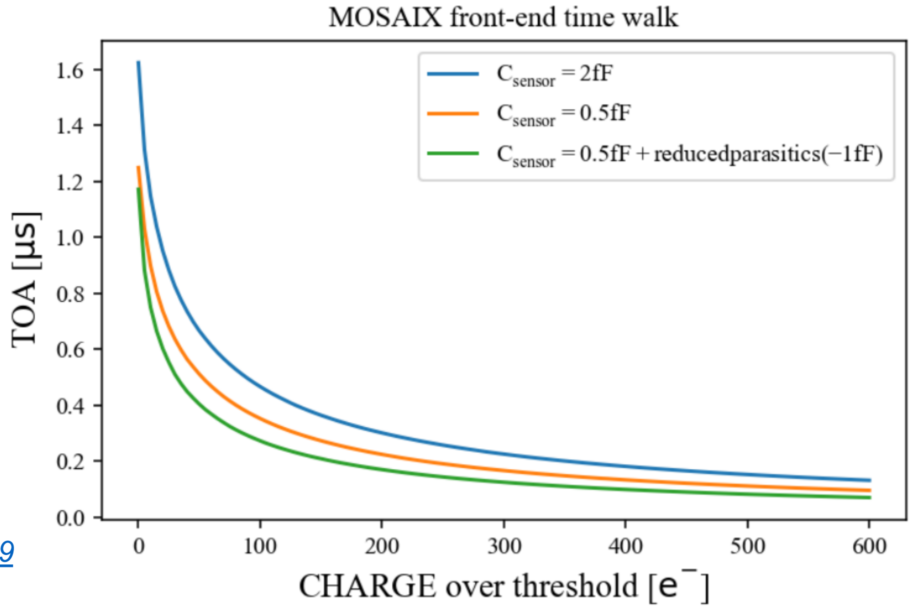
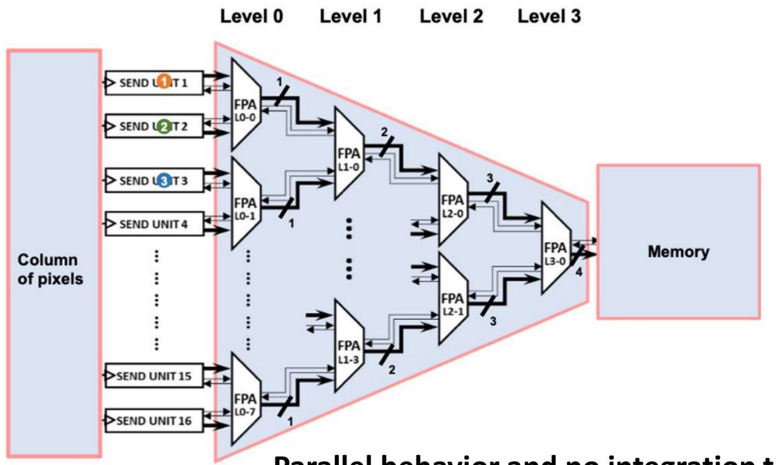


Asynchronous Priority Arbiter (APA) r/o scheme

- Pixel grouping and multi-column readout
- Data-driven hit readout through arbiter tree
- Compact scheme ➔ fits in <= 20µm^2 pitch
- High-rate readout at low power
- No clock in matrix (TDC time stamping in periphery)
- Resolution <5ns feasible
- 65nm proof-of-concept test chip SPARC (IPHC) currently under test

APA r/o architecture considered for OCTOPUS/MANTA

Asynchronous Priority Arbiter Tree



Parallel behavior and no integration time

https://indico.desy.de/event/51462/contributions/197348/

Conclusions + Outlook

- Stringent requirements for FCC-ee vertex detectors:
    - Precision physics needs
    - Environmental conditions

- All detector concepts include MAPS vertex detectors

- Currently only few projects dedicated to vertex-detector R&D

- MAPS R&D projects profit from advancements in semiconductor industry + simulation-based process optimizations

- Fulfilling all FCC-ee vertex requirements simultaneously remains challenging
    - Will require optimized designs in advanced technology nodes
    - Synergies with ALICE3 expected

Thanks to everyone who provided material for this talk!