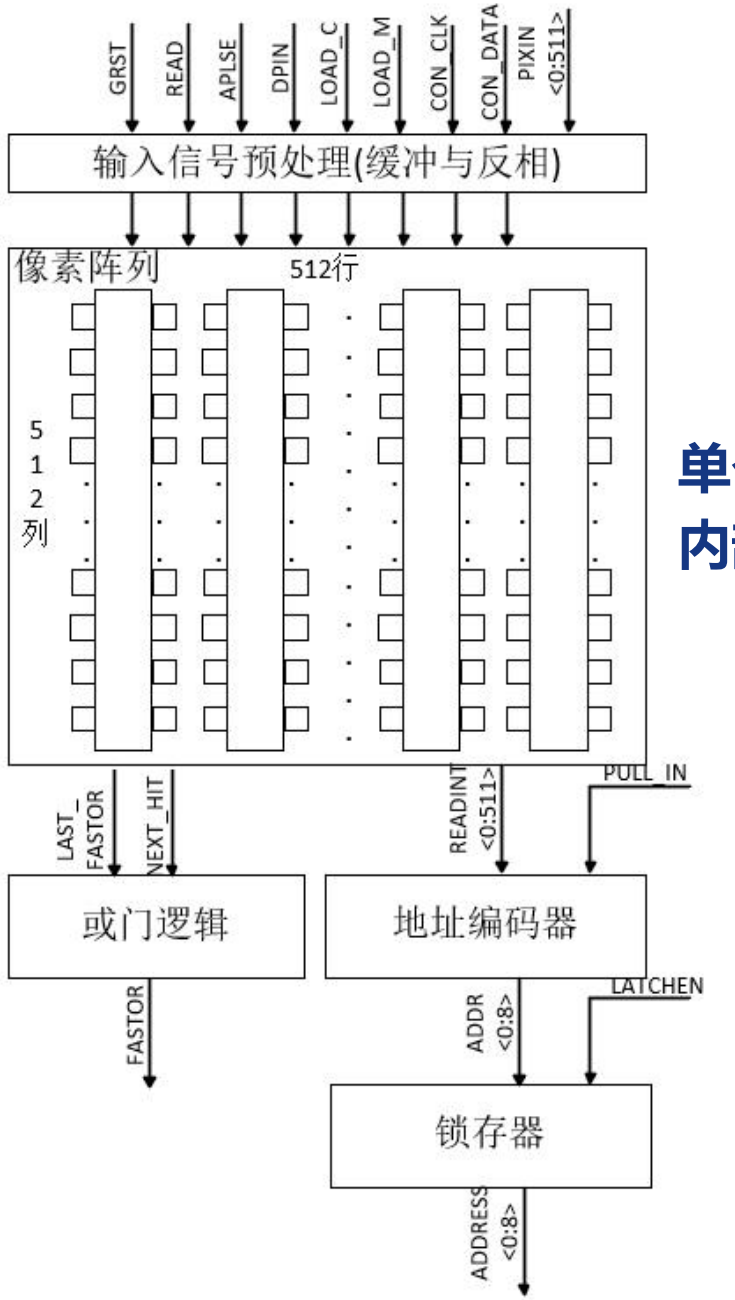
南昌大学
NANCHANG UNIVERSITY

2026.06.25

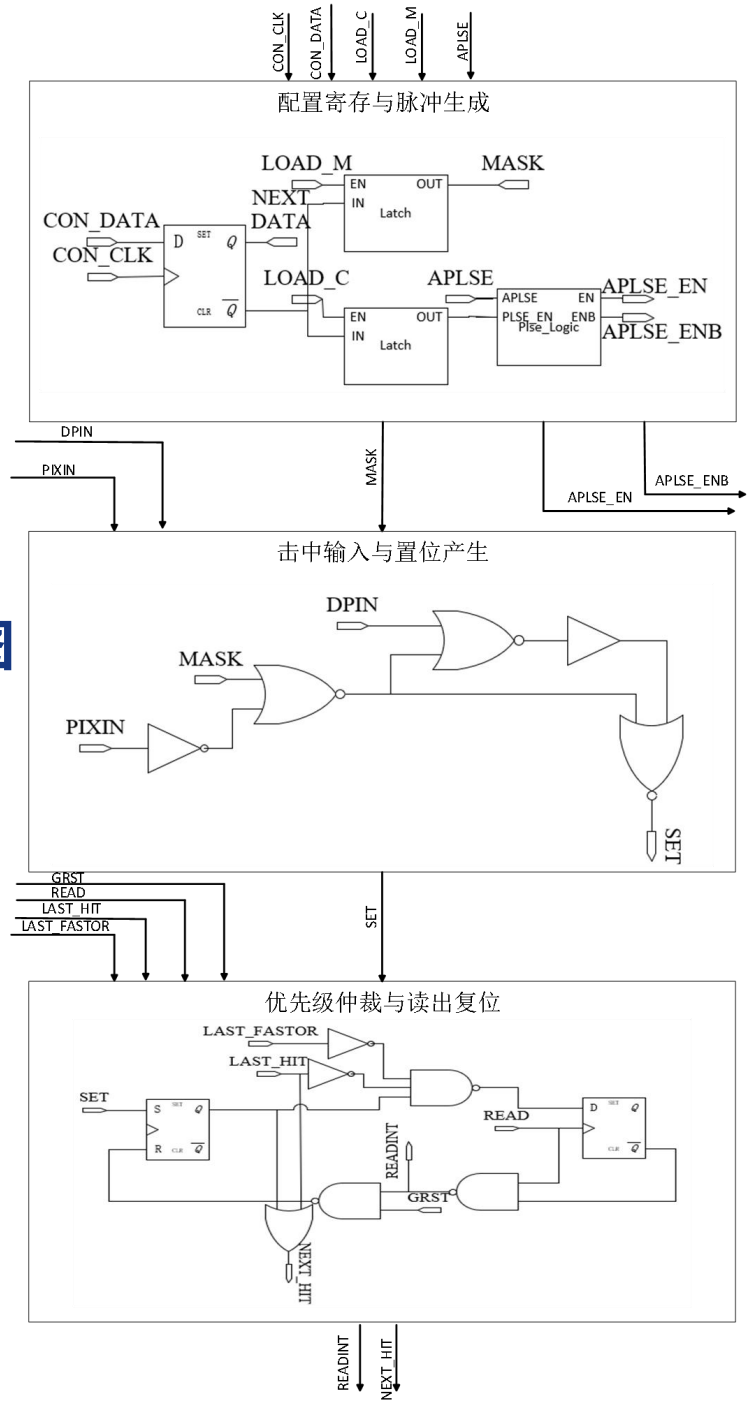
电路框架

南昌大学 NANCHANG UNIVERSITY

整体框架图



单个像素内部框架图



电路结构

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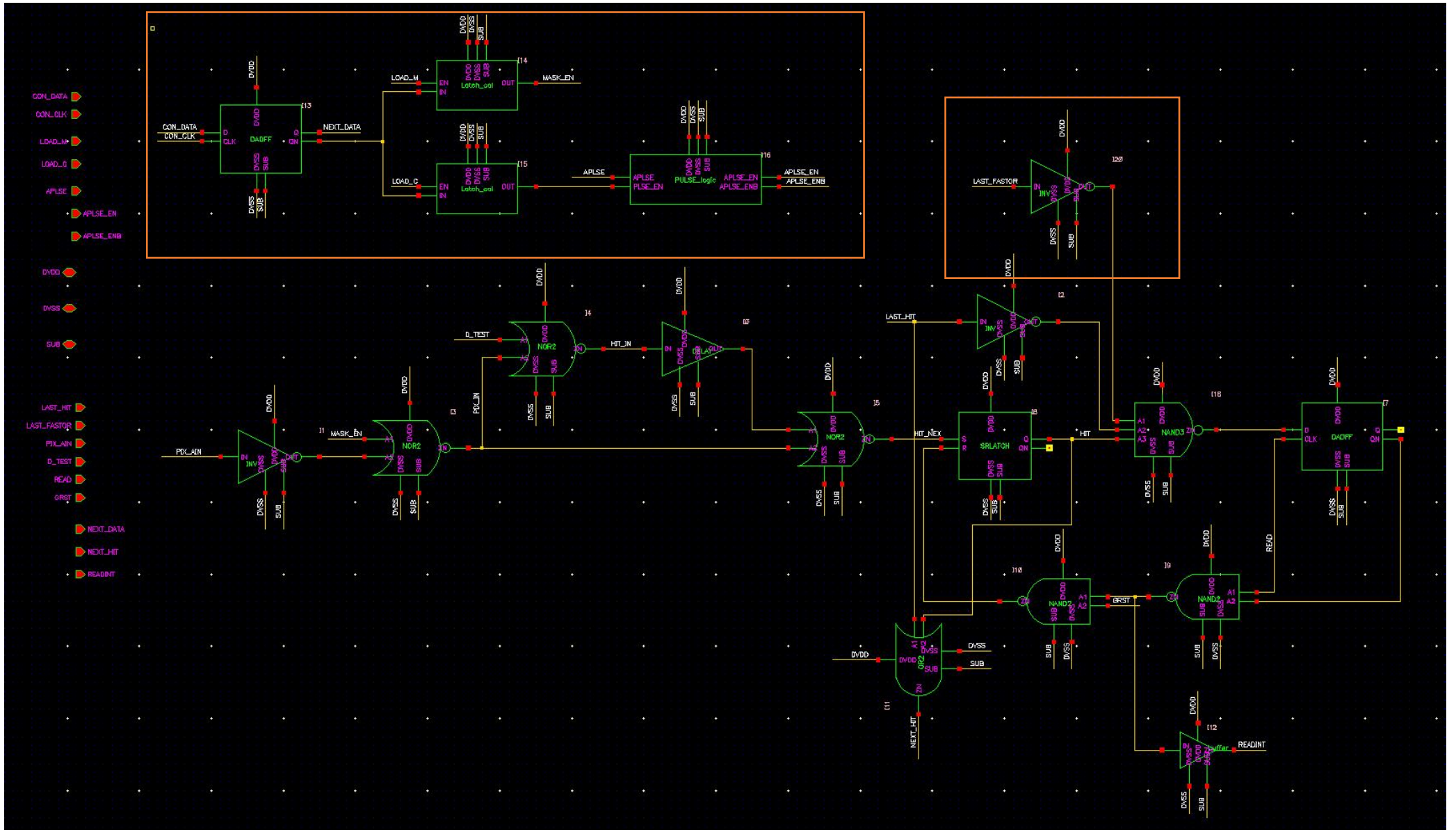
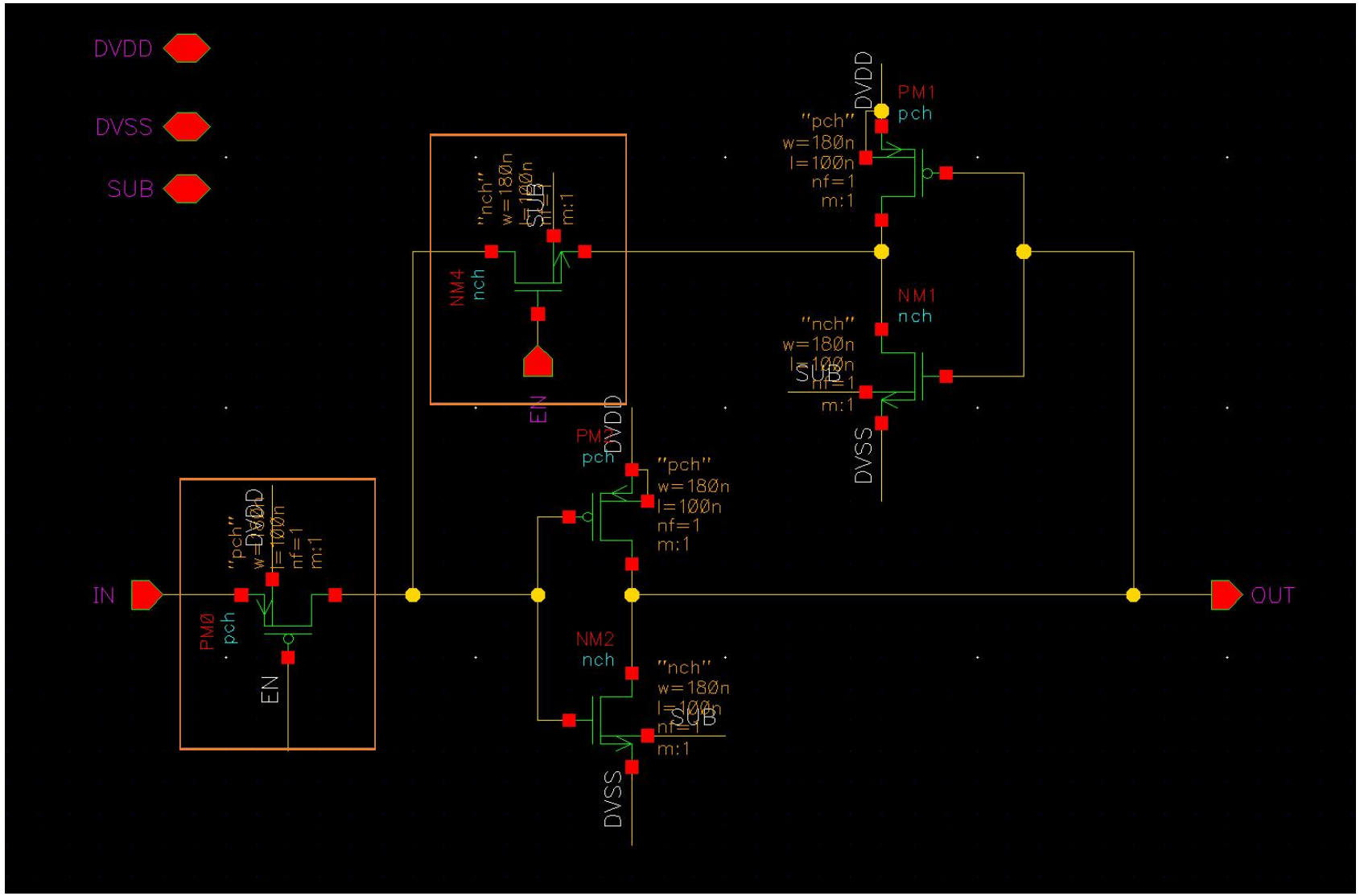
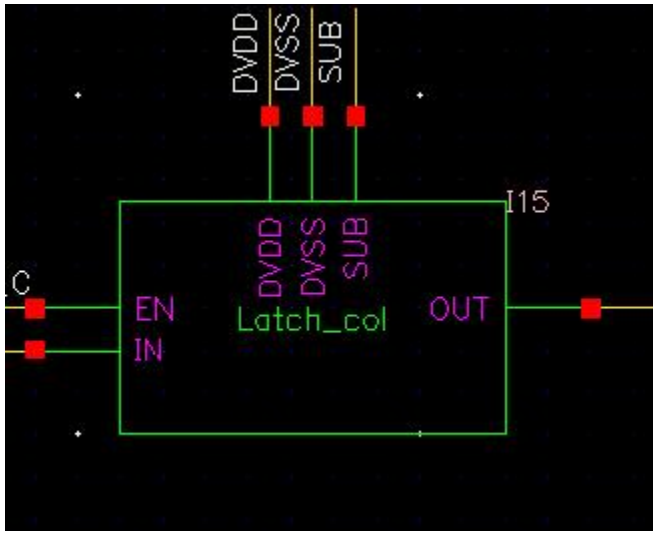
修改电路结构



锁存器结构



是否要将半个传输门改为整个传输门?



4像素单元电路结构

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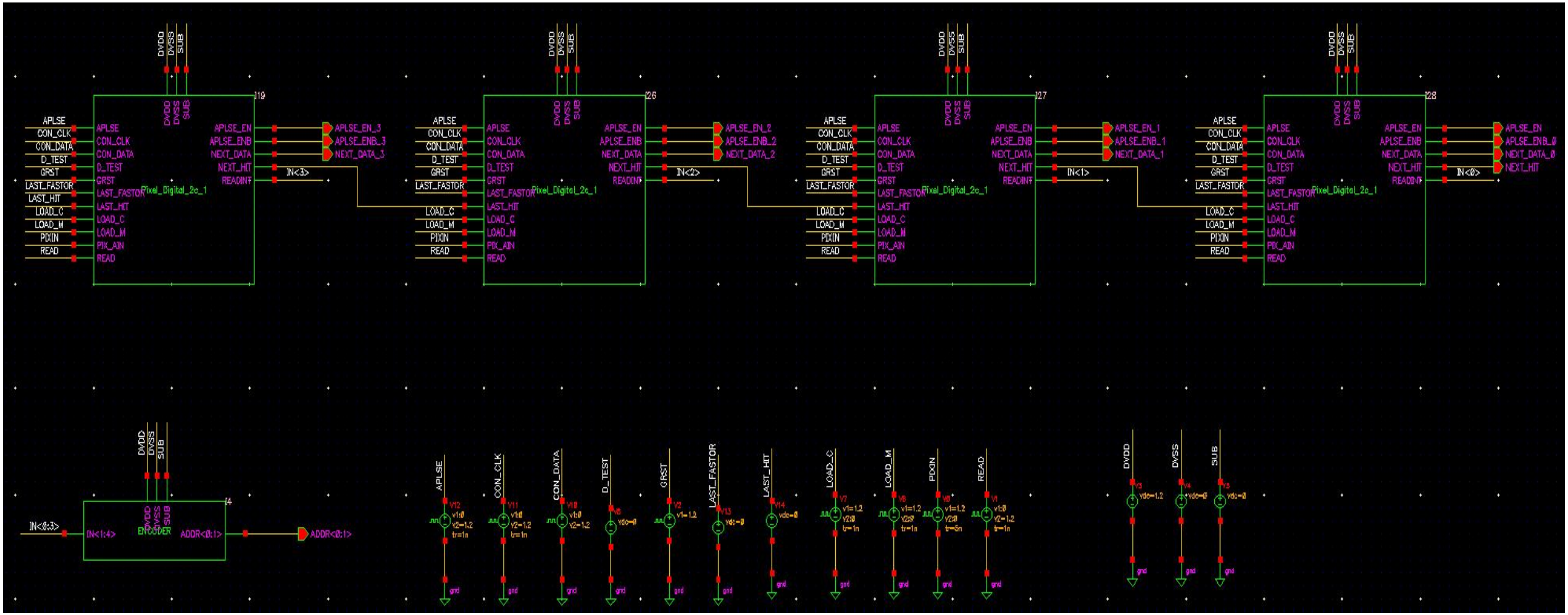
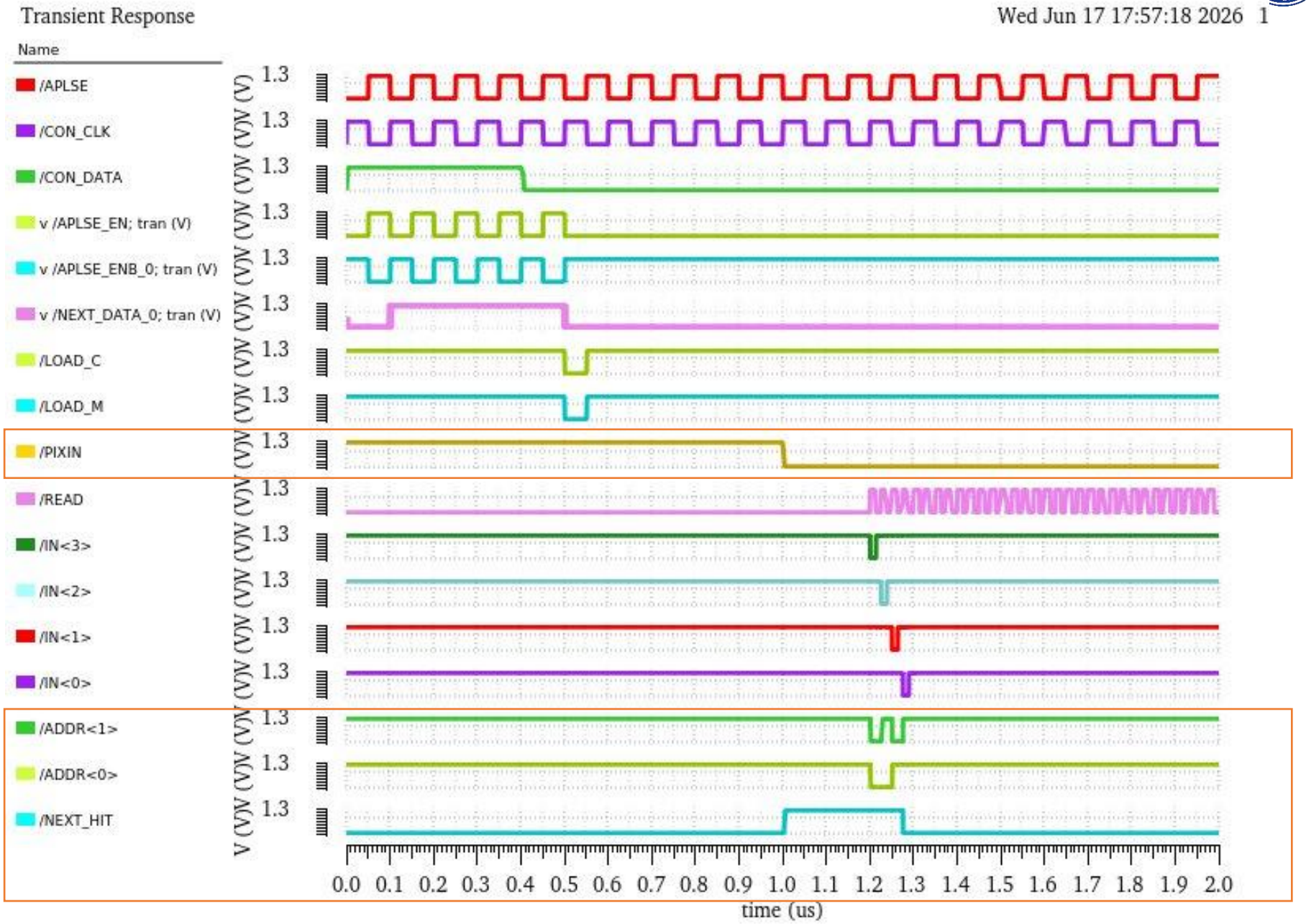


电路仿真结果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Wed Jun 17 17:57:18 2026 1
Name
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/CON_DATA
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v /APLSE_ENB_0; tran (V)
v /NEXT_DATA_0; tran (V)
/LOAD_C
/LOAD_M
/PIXIN
/READ
/IN<3>
/IN<2>
/IN<1>
/IN<0>
/ADDR<1>
/ADDR<0>
/NEXT_HIT
V (V)
1.3
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2.0
time (us)