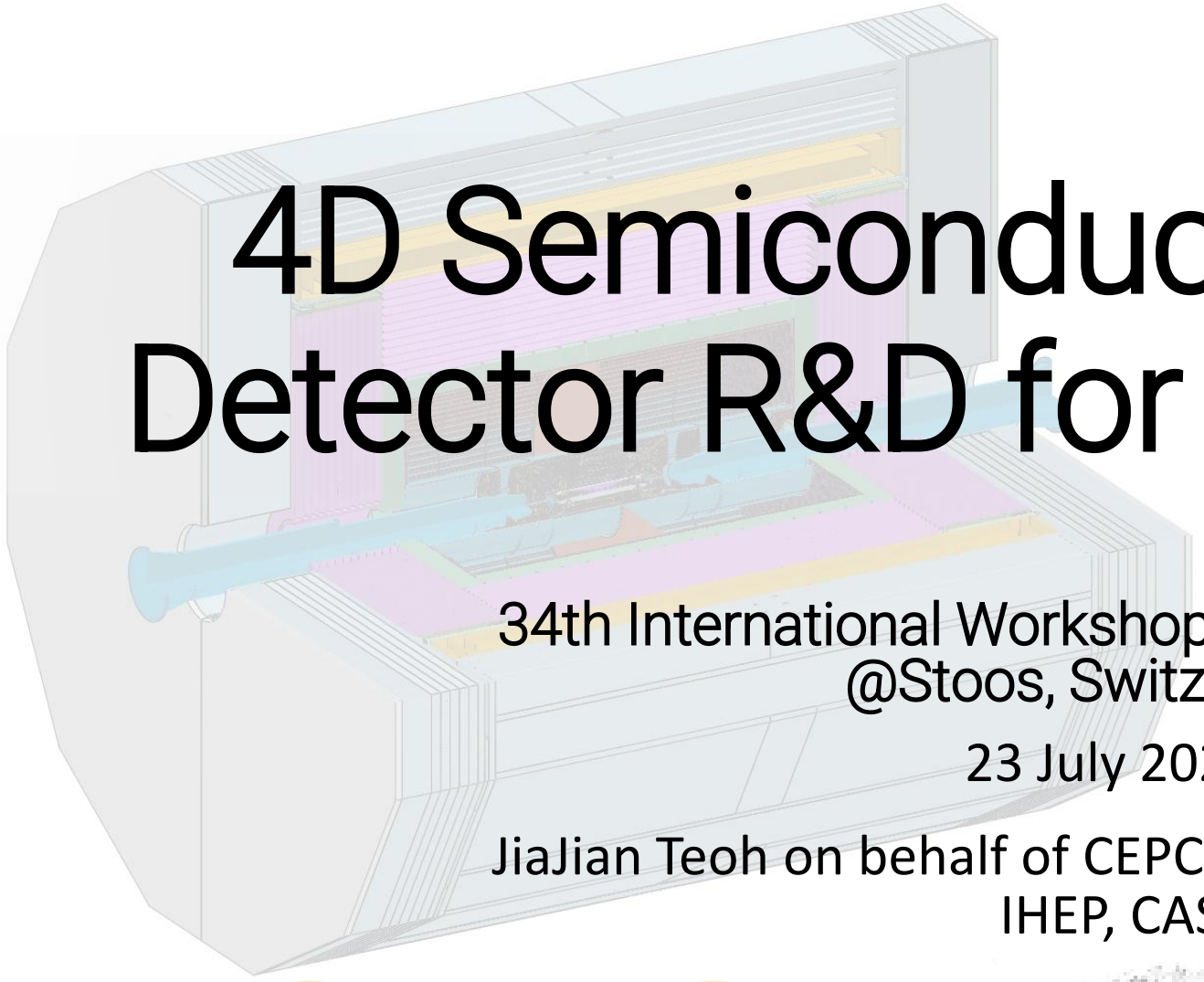


4D Semiconductor Tracking Detector R&D for CEPC/FCC-ee

34th International Workshop on Vertex Detectors
@Stoos, Switzerland.

23 July 2026

JiaJian Teoh on behalf of CEPC Silicon Tracker Group.
IHEP, CAS

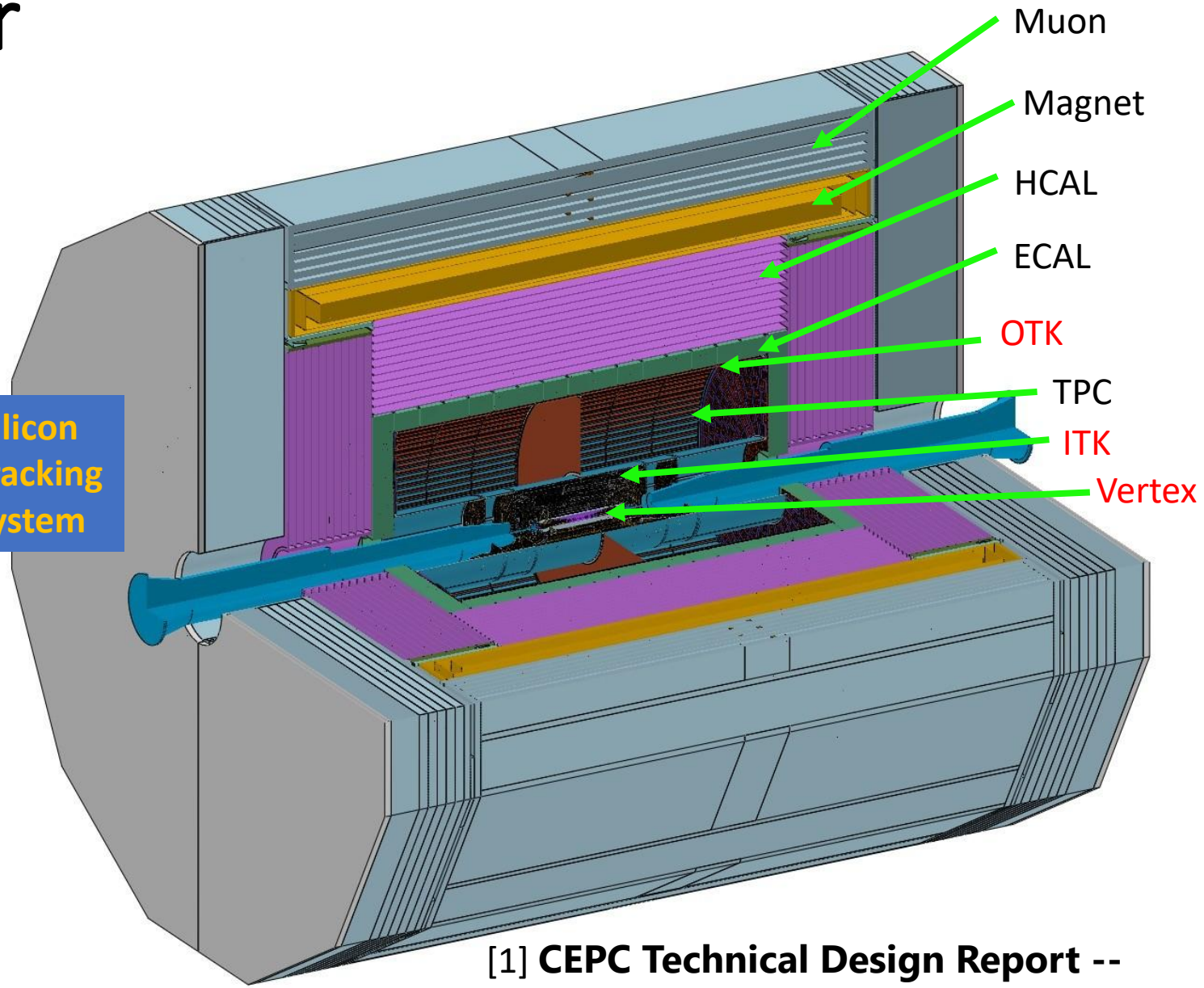
CEPC
CIRCULAR ELECTRON POSITRON COLLIDER

AGORA
ADVANCED GLASS OPTIMIZED RESEARCH APPARATUS

CEPC/AGORA Detector

Sub-system	Technologies
Beam pipe	Beryllium, ϕ 20 mm
LumiCal	Silicon tracker + LYSO crystals
Vertex	**Si Pixels: CMOS MAPS + stitching**
Inner tracker (ITK)	**Si Pixels: CMOS MAPS 55-nm**
Gas detector	TPC with high granularity
Outer tracker (OTK)	**AC-LGAD → TOF**
ECAL	4D transverse crystal bars
HCal	Glass scintillator, SiPM + Fe
Magnet	LTS Solenoid
Muon	Plastic scintillator bars, SiPM
TDAQ	Conventional
Back-end electronics	Common

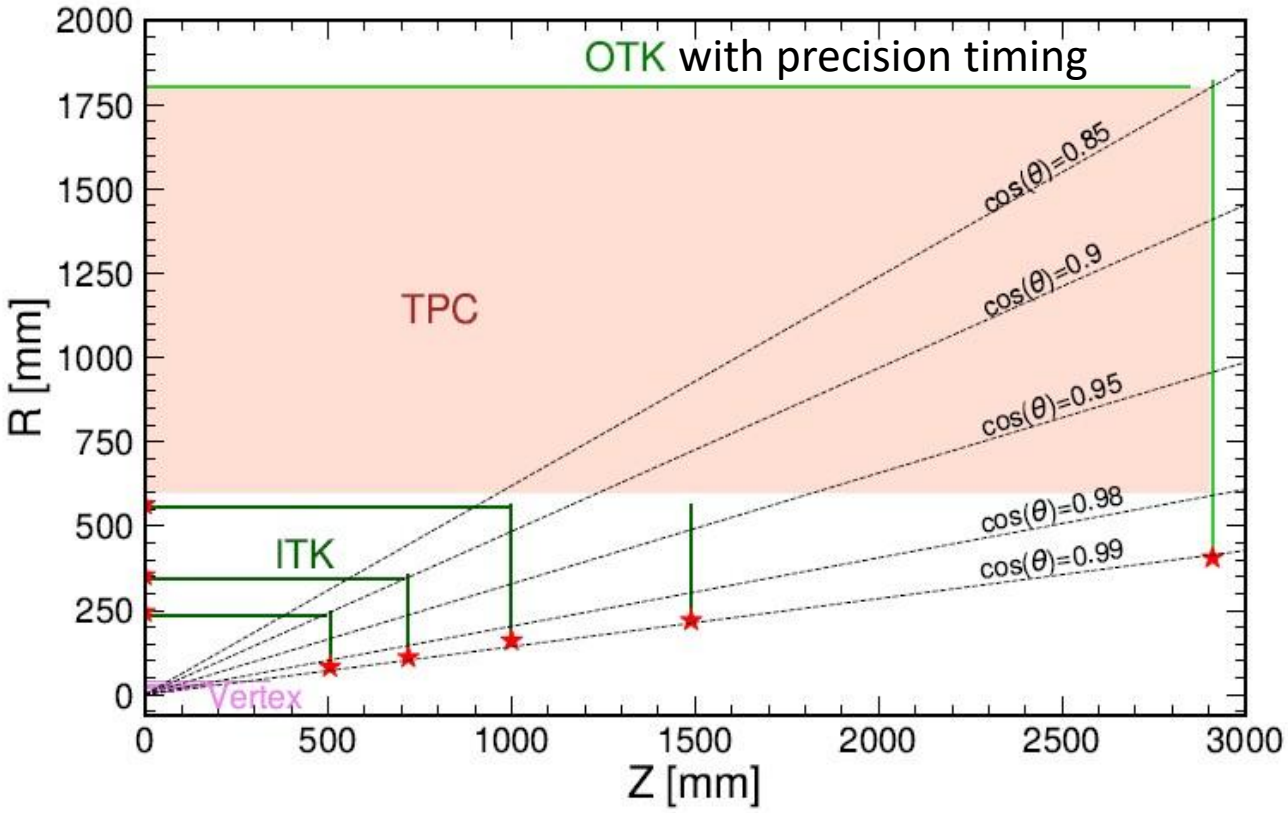
Silicon tracking system



[1] **CEPC Technical Design Report -- Reference Detector**
https://doi.org/10.48550/arXiv.2510.05260

Overall Silicon Tracking System Performance Requirements

- The tracking system must achieve $\delta p/p \sim 0.1\%$ for $p<100$ GeV/c to resolve kinematic details of Higgs boson decays and electroweak processes.
- Silicon microstrip/pixel detectors provide sub-10 μm impact parameter resolution, enabling efficient b/c– jet tagging through secondary vertex reconstruction
- Outer layer timing resolution <50 ps, together with primary ionization counting in TPC (dN/dx) , should enable π/K/p separation at 3σ up to 20 GeV/c



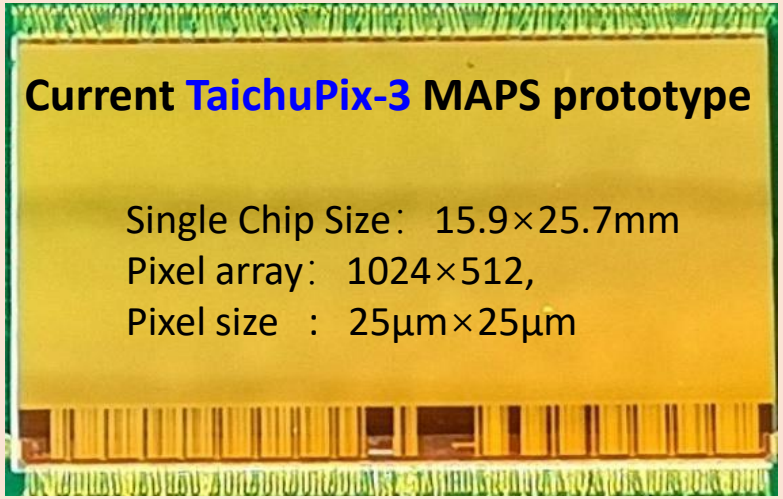
Layout of the Silicon Vertex & Tracker

Sensor & ASIC Requirements

Vertex Detector

Monolithic Active Pixel Sensors (MAPS)

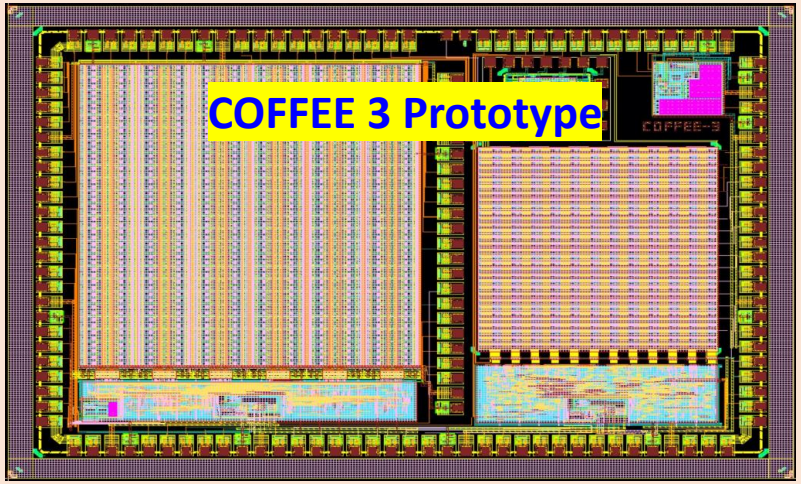
- Base on stitched bent MAPS
- Spatial Reso.: 3-5μm
- Material budget per layer: 0.15% X_0
- Power consumption: < 40 mW/cm^2



Inner Tracker

HV-CMOS MAPS

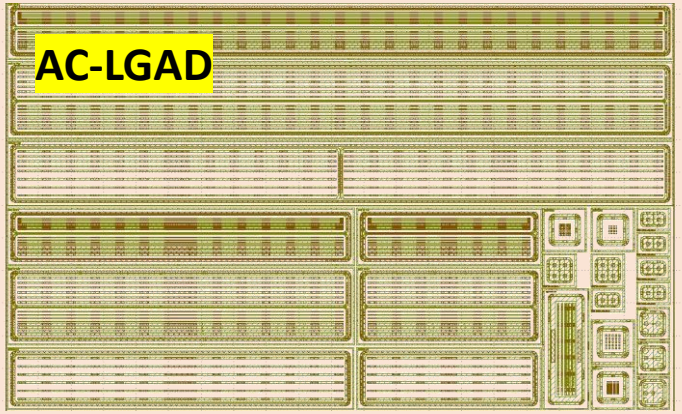
- Chip size: 2 cm×2 cm
- Array size: 512 × 128
- Pixel size: 34 μm × 150 μm
- Process : 55nm
- Time reso.: 3-5ns
- Spatial reso.: 8μm×40μm



Outer Tracker

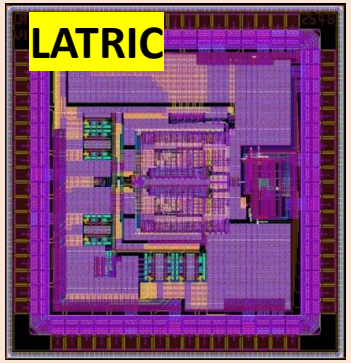
AC-LGAD Microstrip

- Timing resolution: <50ps
- Position resolution: <10μm
- R&D in progress



LATRIC Readout ASIC

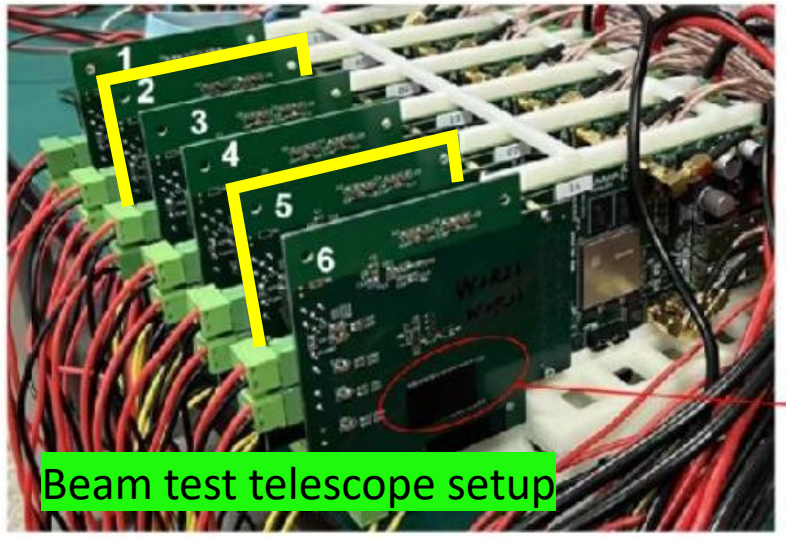
- 55nm CMOS
- 128 channels
- Power dissipation per ASIC 1.5 W
- Maximum jitter 30 ps at 16 fC



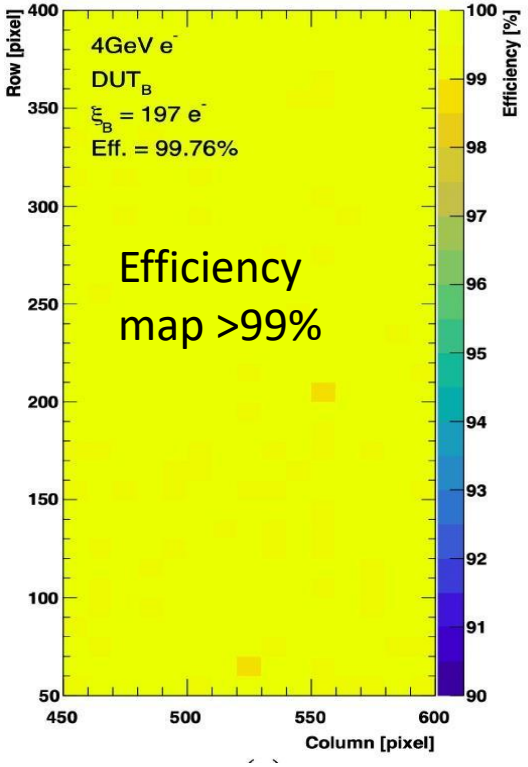
Following slides: Current R&D status and plan

TaichuPix-3 R&D Efforts

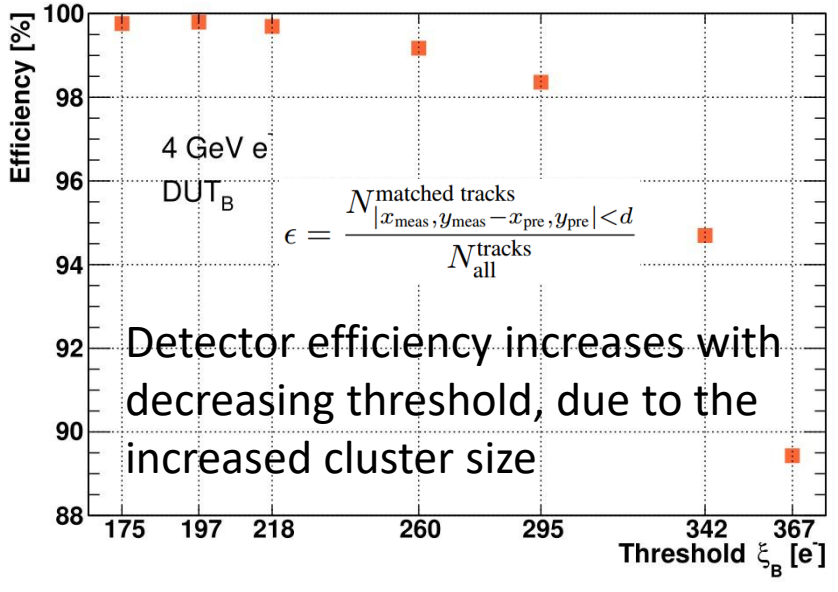
- Completed the 1st engineering run in a 180 nm CMOS process
  - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023
- TaichuPix-3 beam test @ DESY



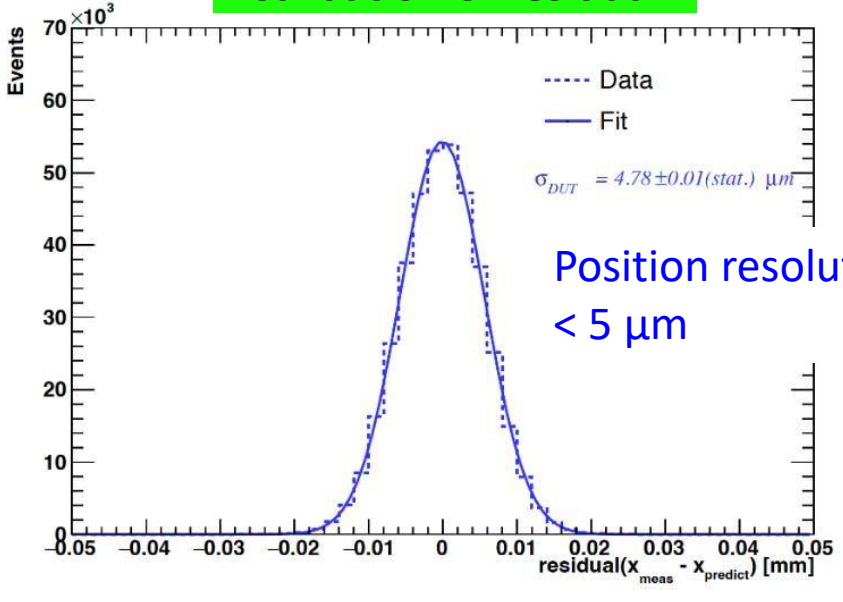
6-layer of TaichuPix-3 telescope. Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board



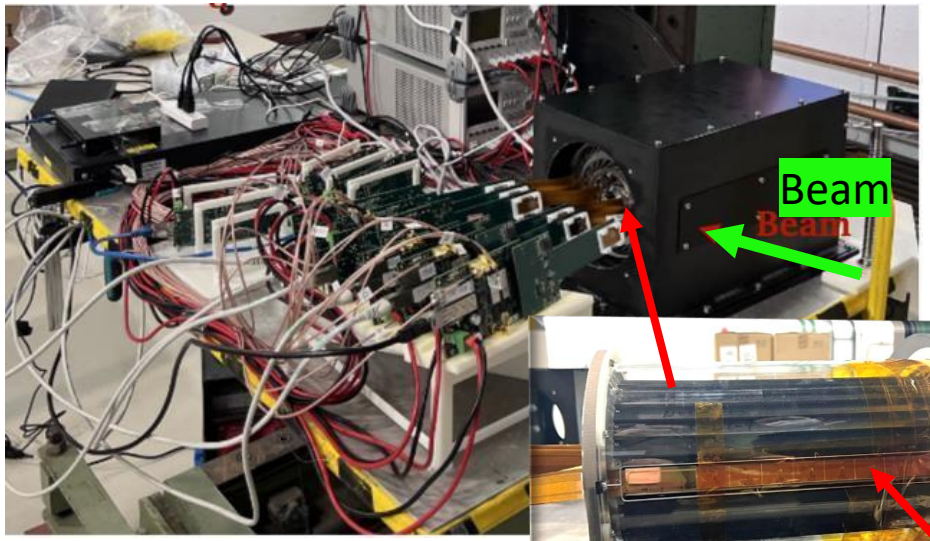
Detection efficiency vs. pixel threshold



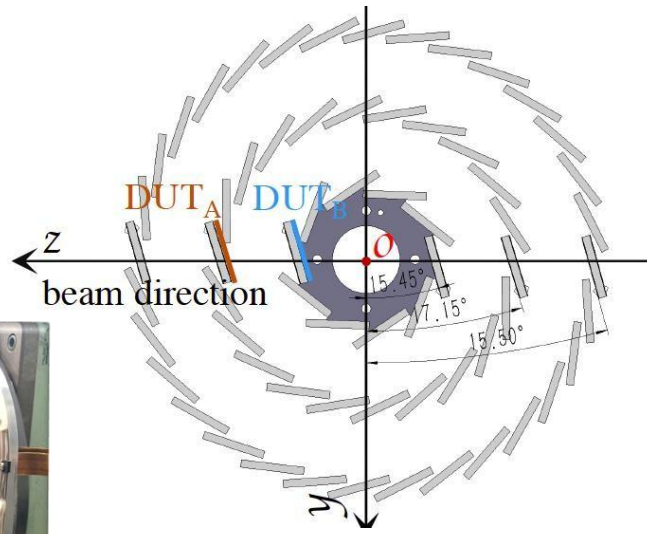
Distribution of residual X



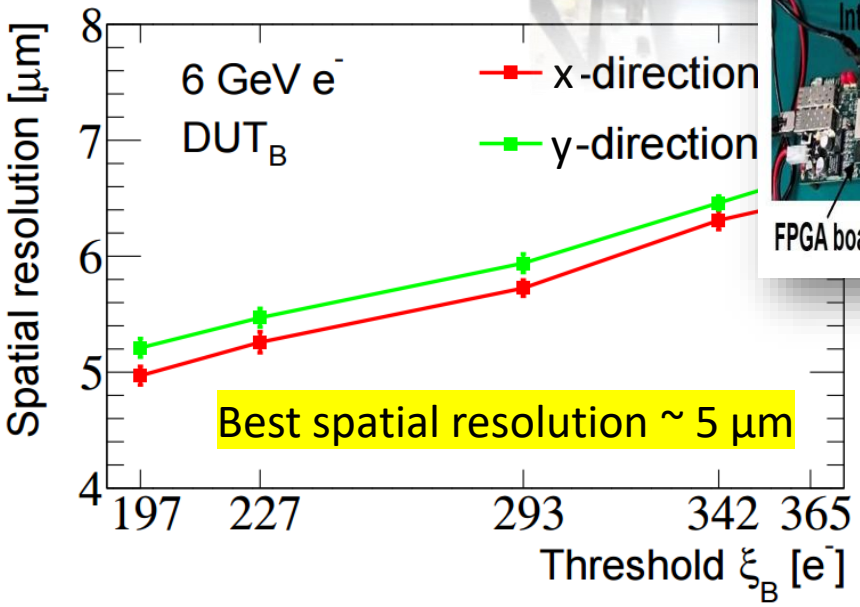
TaichuPix3 Vertex Detector Prototype Beam Test @ DESY II



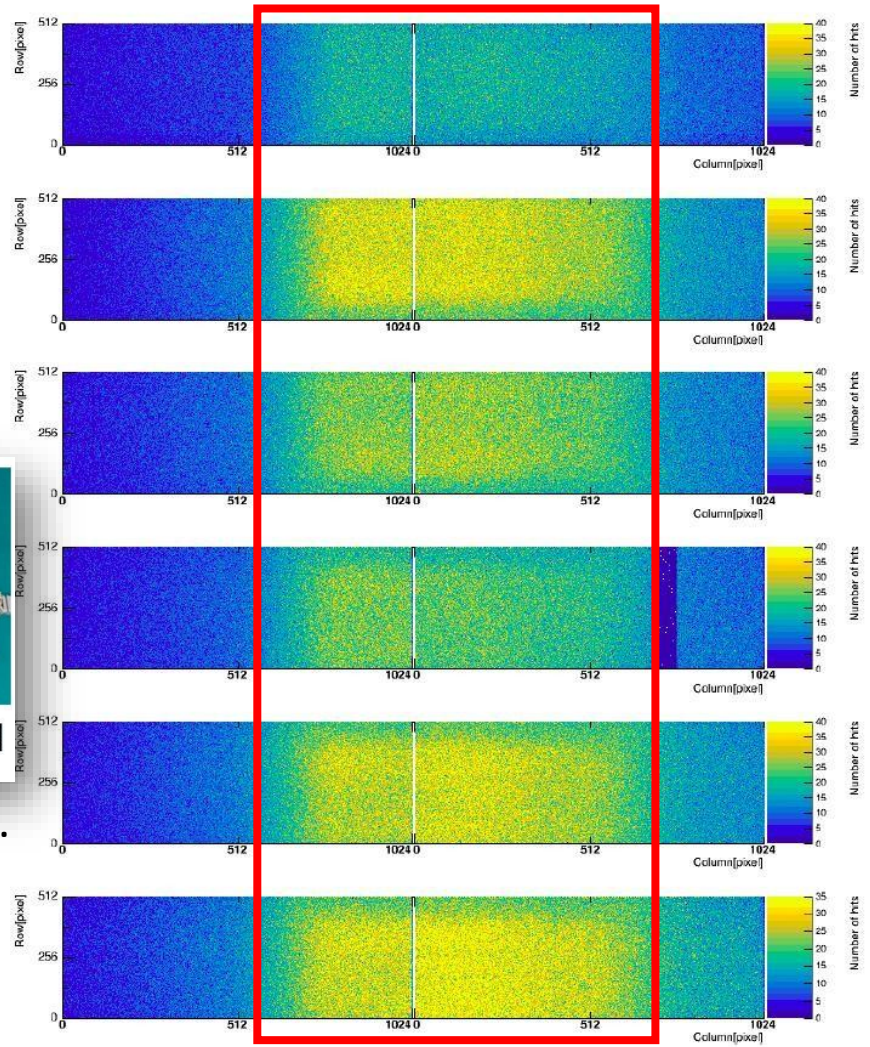
6 double-sided ladders



Ladder prototype with readout system.



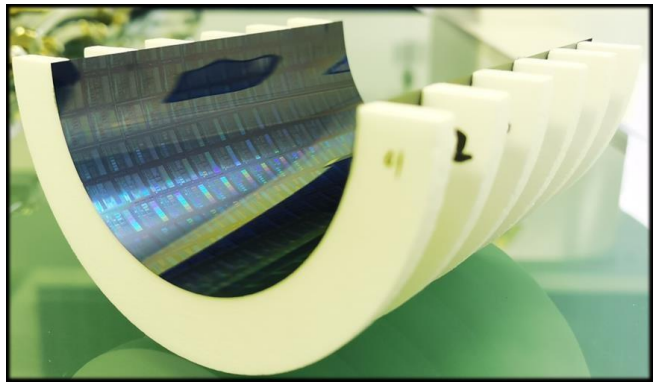
Beam spot (2cm x 2cm) clearly visible on the hit maps of multiple layers of vertex detector



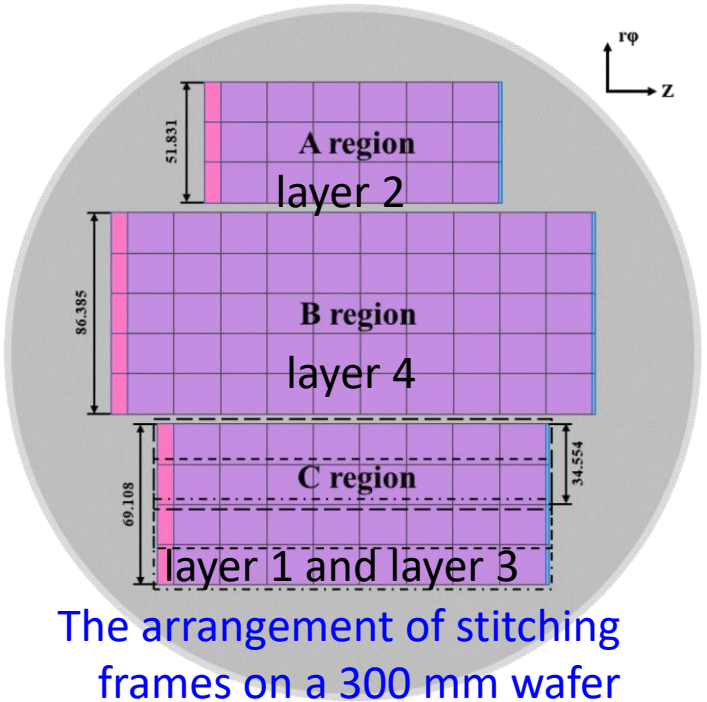
Beam spot

Vertex Detector Baseline Layout

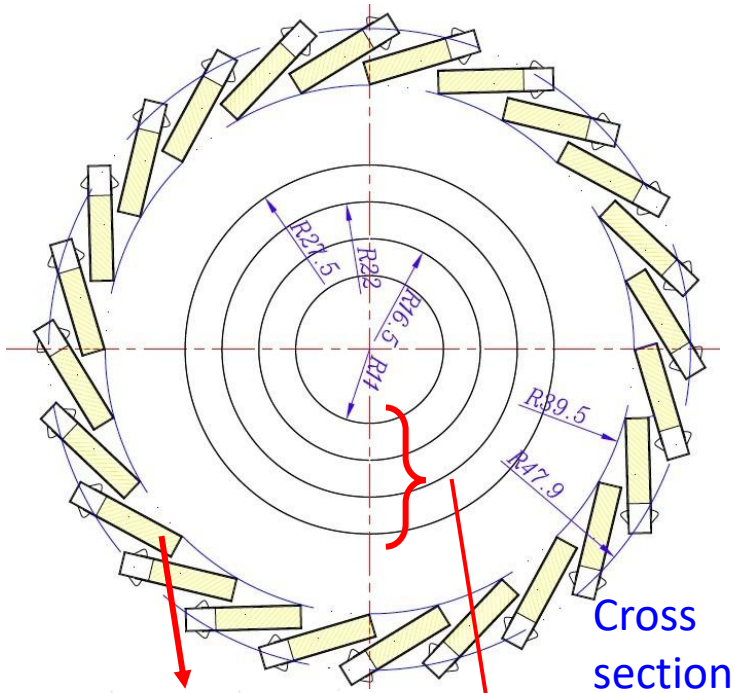
- 3 double-layer ladders layout is the alternative option
- Baseline: 4 single layer of bent stitched MAPS + 1 double layer ladders
  - Advantage: 3~5 times smaller material budget compared to alternative options
  - Inner layer: one/two bent MAPS structures spliced together
  - Outer layer: double layer ladder (target ~0.15% X_0 per layer)

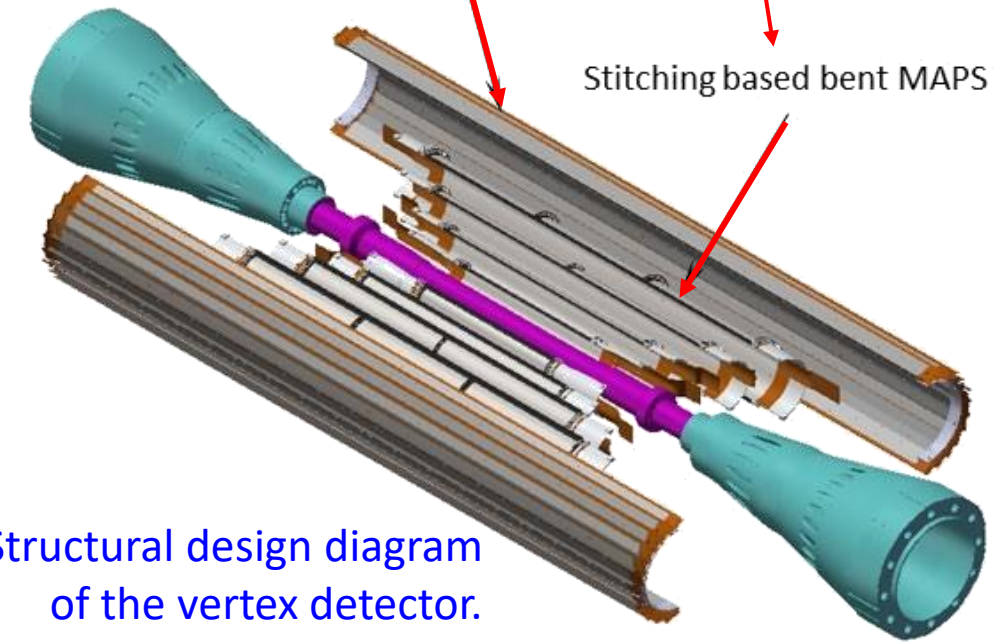


Dummy wafer has been bent to a radius of 12 mm (requirements is 11mm)



The arrangement of stitching frames on a 300 mm wafer





Structural design diagram of the vertex detector.

Choice of Technology for Stitched MAPS R&D

- Collaborate with new foundry: SK Hynix System Fab in Wuxi China
- HC90L offers 90 nm CIS, different epi/resistivity options, stitching feasibility, and relatively low NRE cost.
- Cost effective option with stitching combability, candidate technology for vertex detector in future collider
- The first engineering run should validate the process before attempting stitched sensors.
- Propose 3-4 years research program should end with a clear technology-readiness decision.

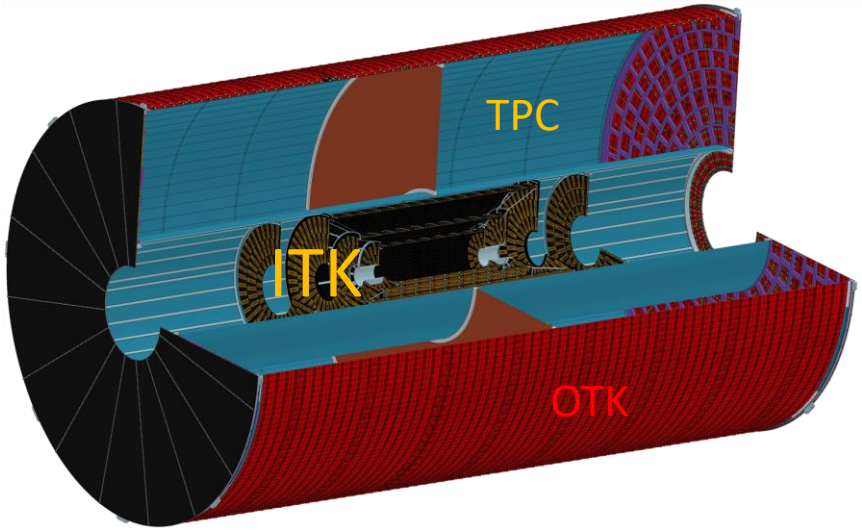
Requirements vs. CIS technologies from domestic candidate

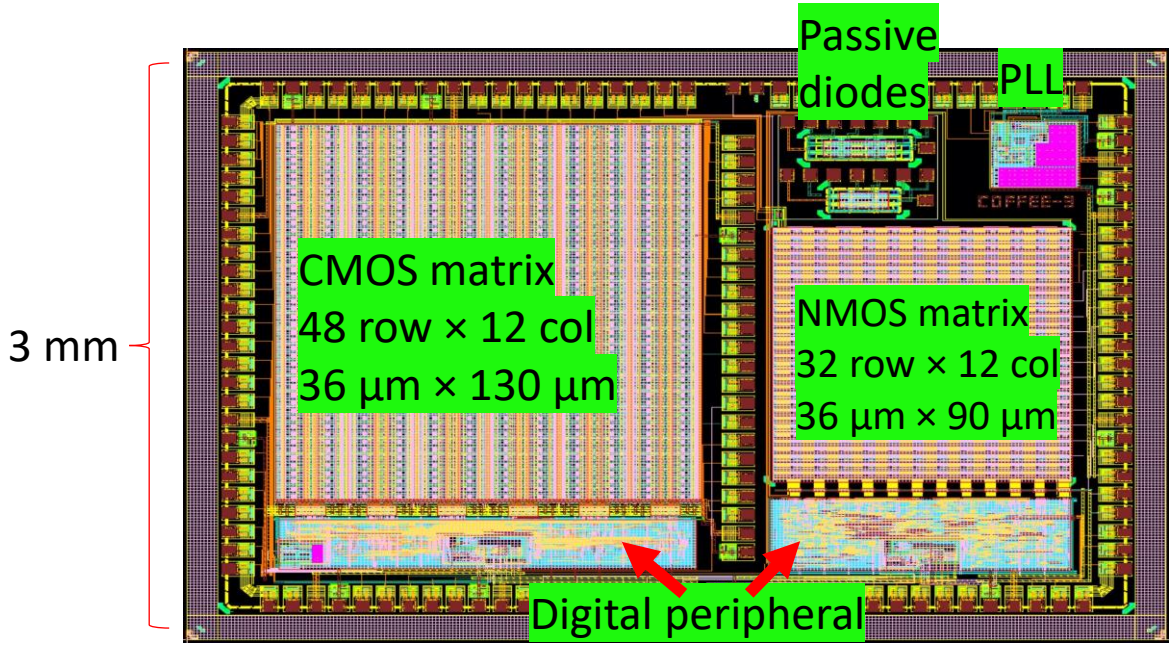
	Requirements	TPSCo 65 nm	HLMC 55 nm	HC90L
Feature size	55 – 90 nm	65 nm	55 nm	90 nm
Epitaxial layer thickness	10 - 25 μm	10 μm	3-5 μm	4 – 8.5 μm (default) Can be changed to 20μm
Resistivity of epi-layer	> 1 kΩ•cm	~130 Ω•cm	Low resistivity ~10 Ω•cm	30-50 Ω•cm (default) Can upgraded to 5kΩcm
Availability of deep N-well	Yes	Yes	Yes	Yes
Availability of deep P-well	Yes	Yes	Yes	Optional
Numbers of metal layers	> 6	Max. 7	Max. 5	Max. 5
Availability of stitching	Yes	Yes	Yes	Yes
Cost (NRE)		~7.0 M RMB	~6.0 M RMB	2~3 M RMB

Seeking for collaboration for R & D using HC90L CIS technology → Zhijun Liang's report in the 5th DRD3 Week @ Bucharest

COFFEE 3 HVCMOS Pixel Chip For The Inner Tracker

- The latest COFFEE 3 sensor, summited for tape-out in Jan 2025 and received in May 2025.
- Tape-out in 55nm HVCMOS process includes a matrix of design variants
  - Passive diodes for sensor study (IV, CV)
  - IP validations: PLL, DLL, LVDS driver/receivers etc.
  - 'CMOS matrix': digital TDC in pixel
    - for high hit density processing capability (>100 Mhz/cm^2)
    - for lower power dissipation
  - 'NMOS matrix': limited design flexibility yet no crosstalk using 3-well process

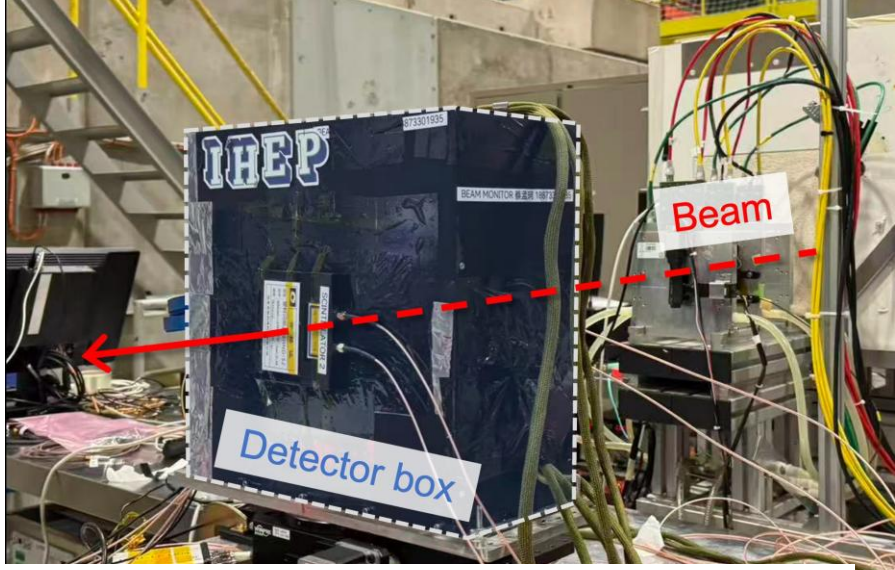


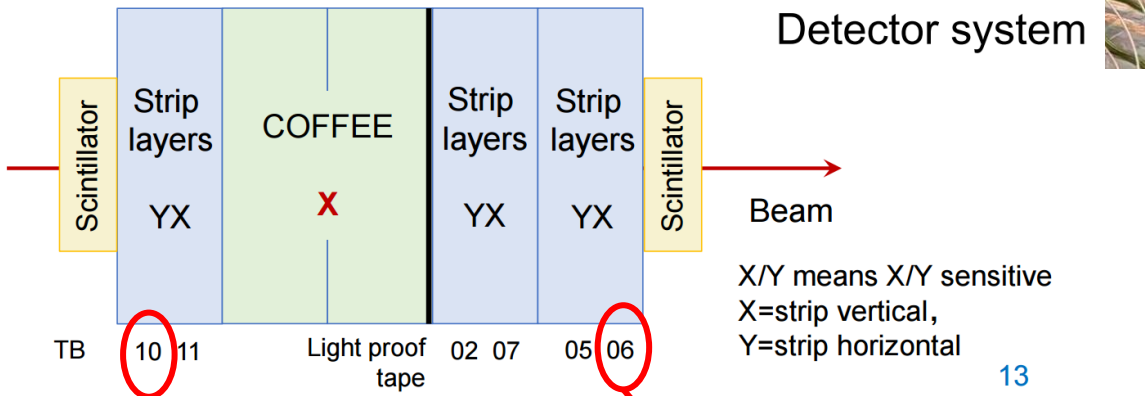


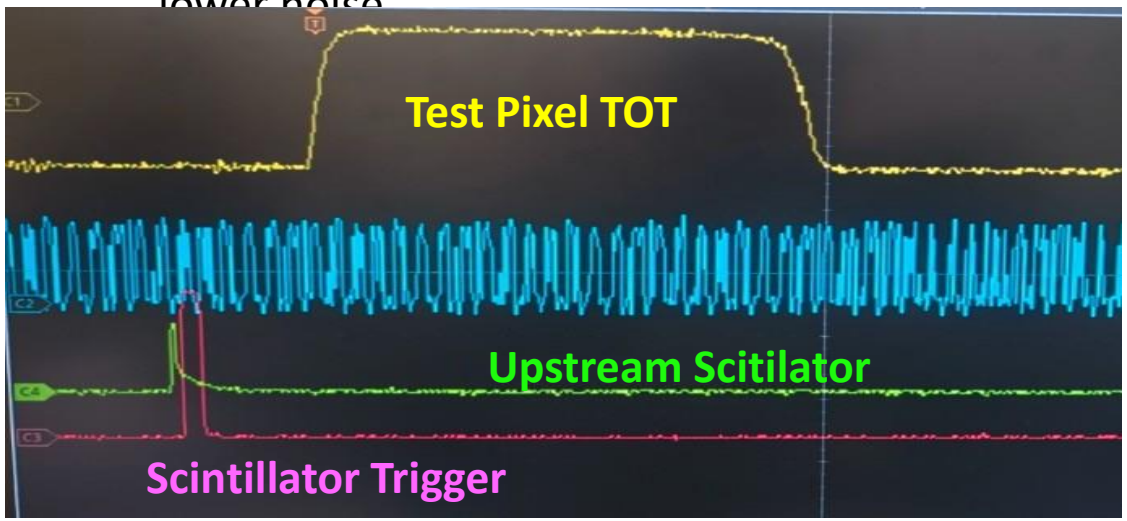
JINST 21 (2026) C04075

COFFEE 3 Beam Test

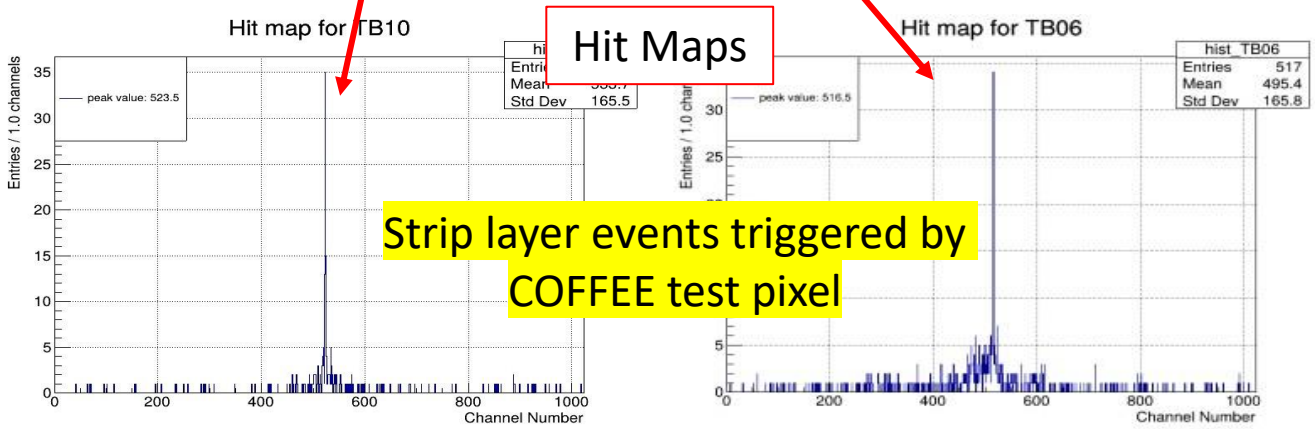
- Beam test campaigns @ CERN SPS 120GeV hadron beam
  - May 2026 with DRD3
- Device under test:
  - COFFEE3: two chips tested
  - Focused on left (CMOS) array, double column 1
- COFFEE was alive in beam! The full readout chain of a full column works
- More analysis needed for an estimation of resolution
- Plan for future beam tests
  - More timing study / DAC tuning for a more uniform response
    lower noise







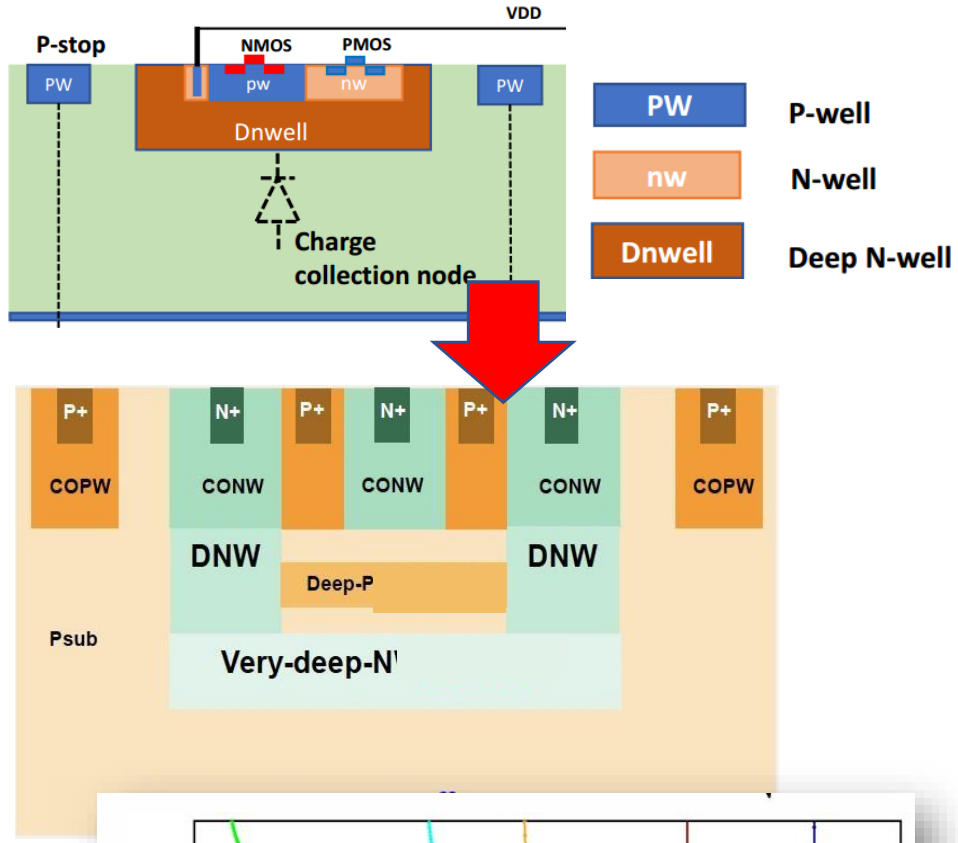
Hit Maps

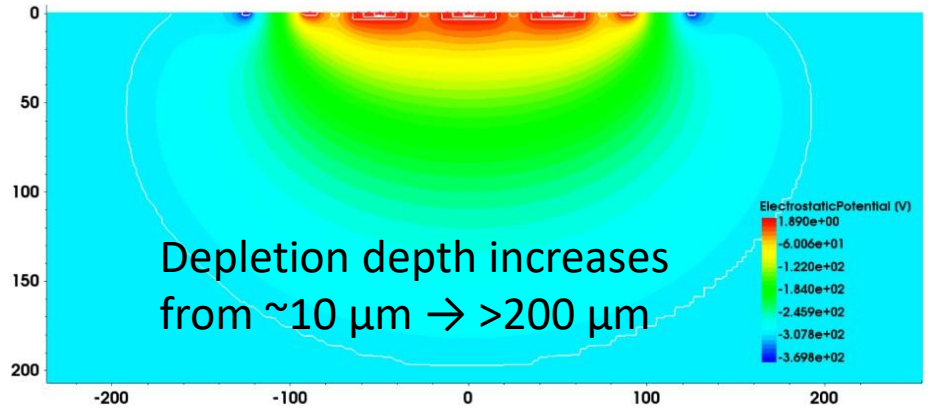


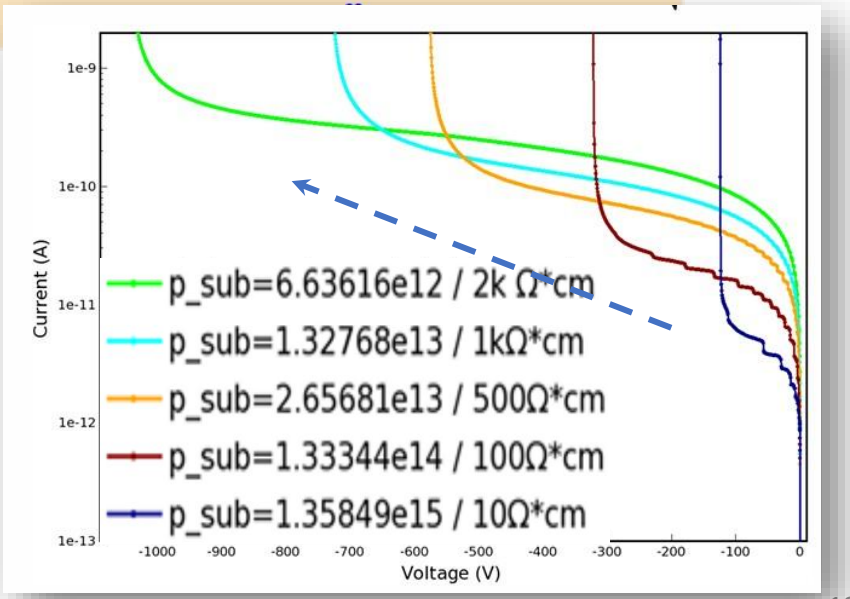
Strip layer events triggered by COFFEE test pixel

Process Modifications

- Limitation of the current foundry:
  - No access of high-resistivity wafers, leads to
    - Small depletion, large capacitance, low S/N ratio
  - Triple-well process → cross-talk between sensor (deep-n) and PMOS circuit, lead to voltage changes in the deep N-well
- New foundry to carry on future R&D:
  - Add Deep-PW & Very-deep-NW;
  - Change doping rules
  - Replace wafer: from 10 Ω·cm --> 1k/2k/4k Ω·cm;

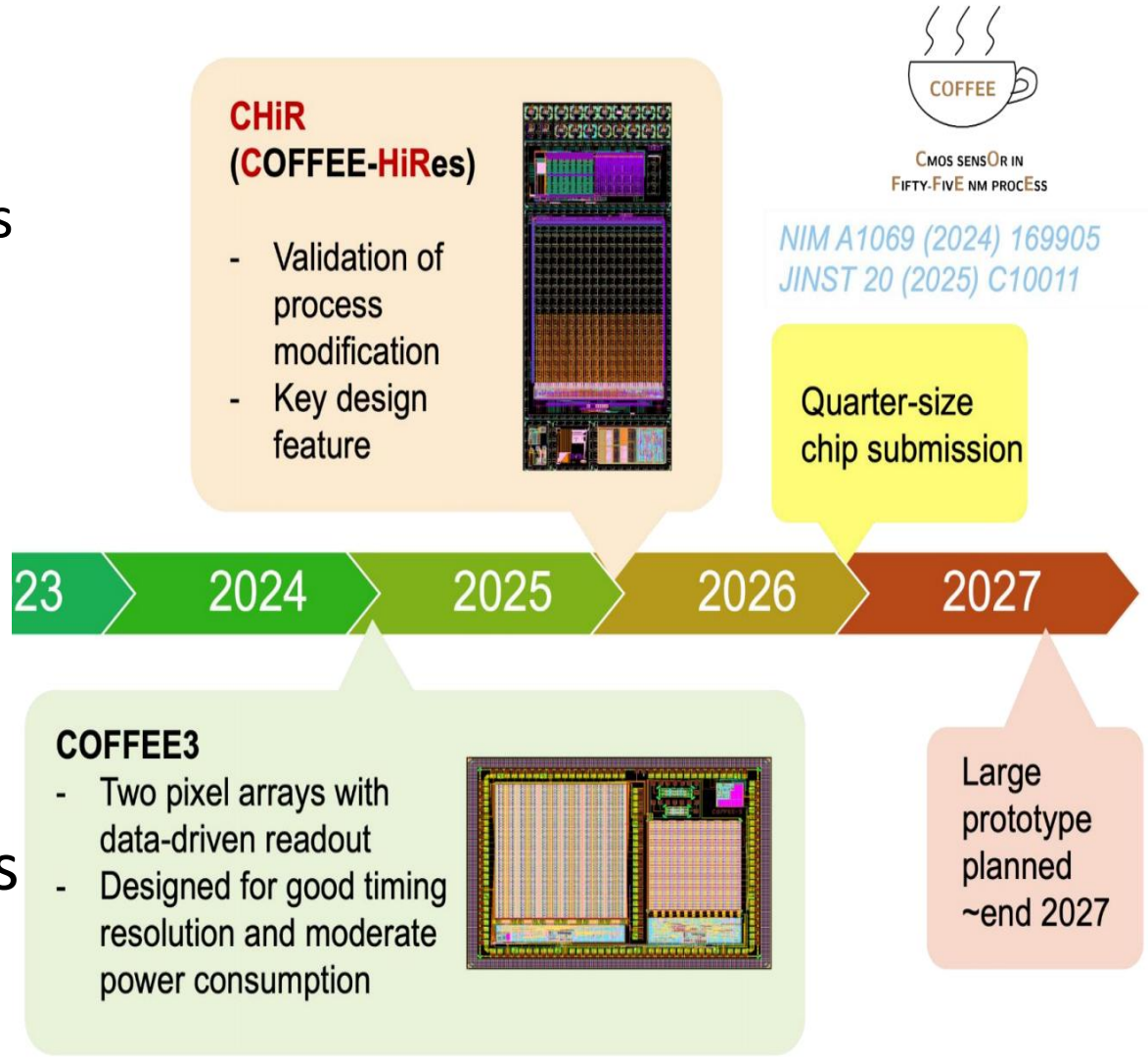




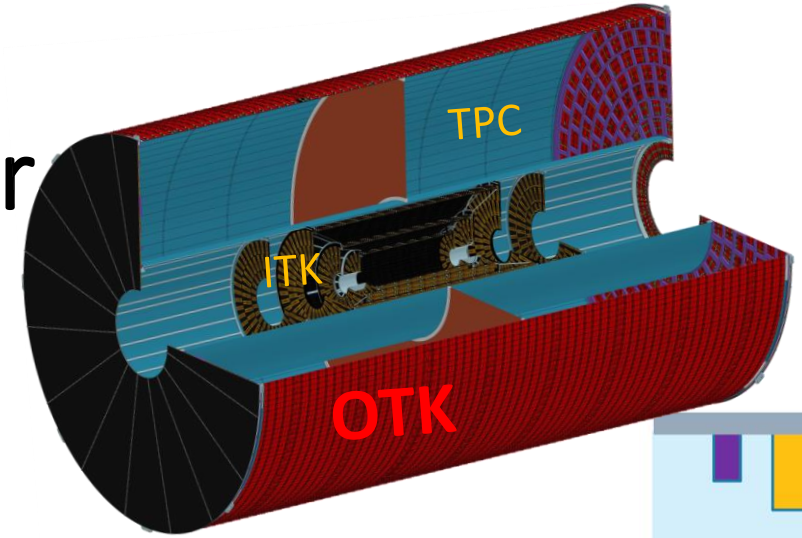


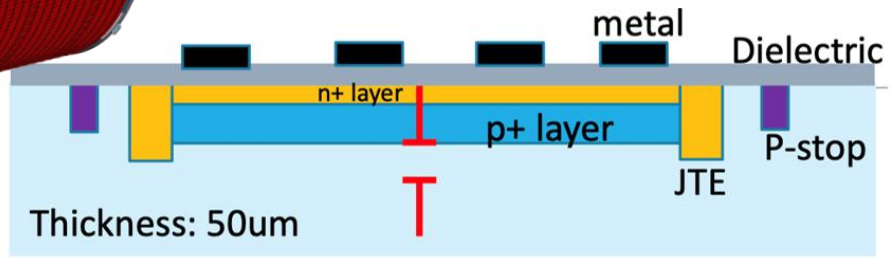
CHiR (COFFEE-HiRes)

- CHiR's design goals:
  - Priority is to validate the process with high-res wafers (1k/2k/4k Ohm*cm)
  - Study radiation effects of simple components with or w/o radiation hardening
  - To validate basic IP not affected by process modification ("Five-well process")
- Submitted in Jan 2026
  - First batch with 2kOhm cm wafer expected back in July
  - Iteration within fab in ~2 months for the rest
- Future MPW planned in early 2027 if tests positive

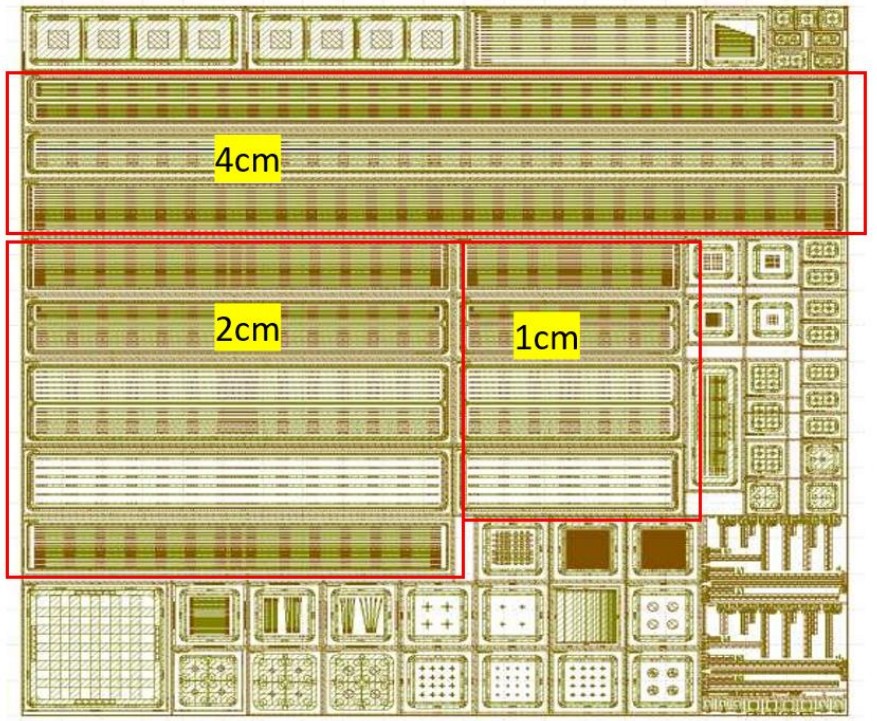


AC-LGAD and LATRIC For The Outer Tracker



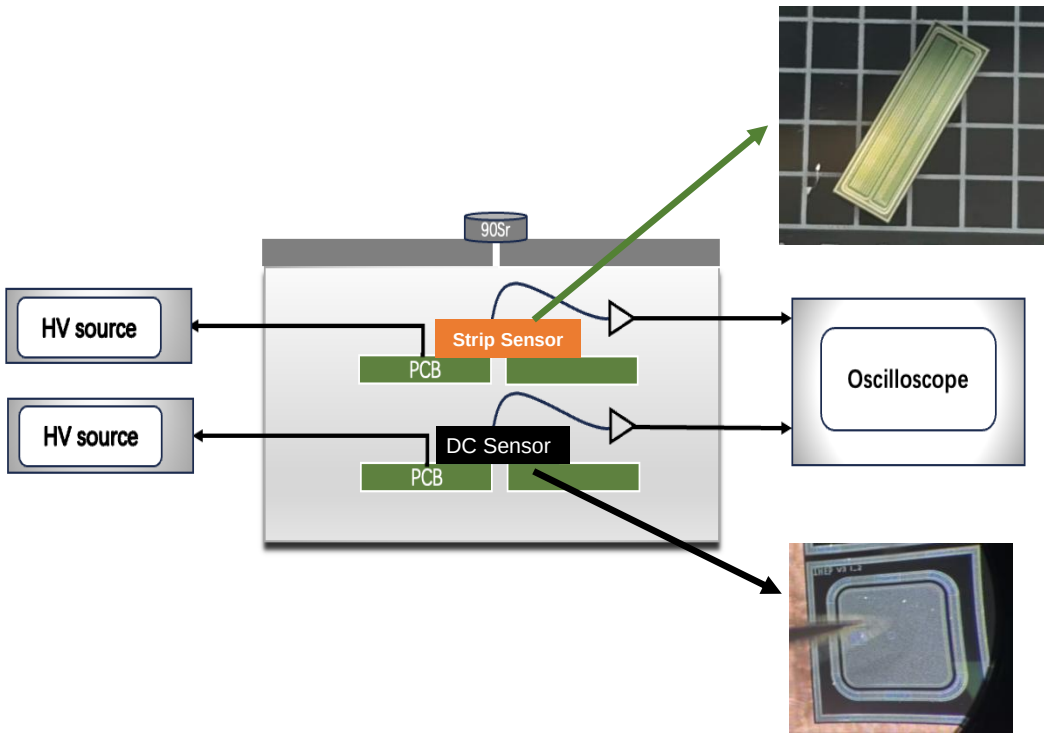


- AC-LGAD with long strip been submitted for fabrication in April 2025,
  - Strip lengths: 1 cm, 2 cm, and 4 cm
  - Strip pitch sizes: 100 µm, 200 µm, and 500 µm
  - Electrode widths: 25 µm, 50 µm, and 100 µm
  - Isolated structure design and EPI thickness (50 µm, 80 µm) to reduce sensor capacitance
  - Optimize N+ doping concentration to improve position resolution (two wafers delivered in May 2026)

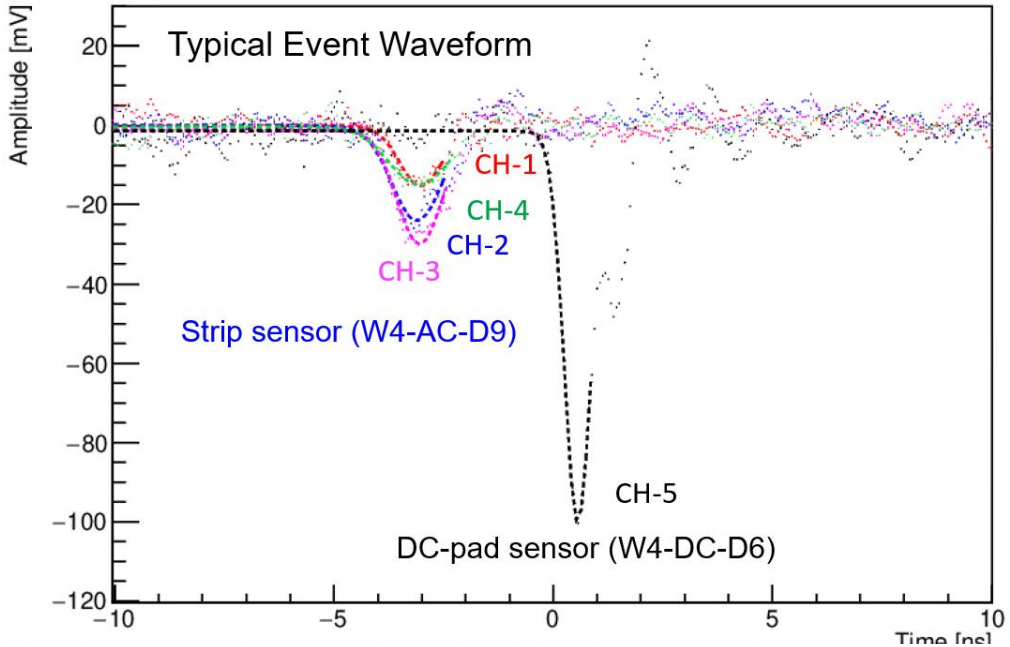


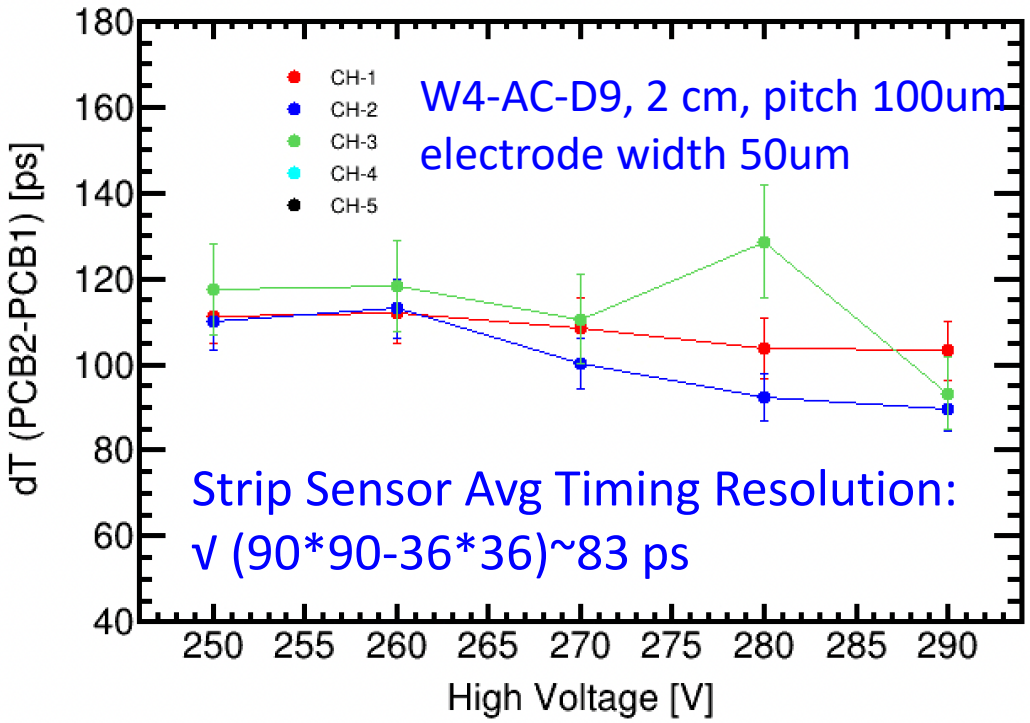
Sensor Characterization with a ^{90}Sr Beta Source

DUT Strip sensor (W4-AC-D9, 2 cm)

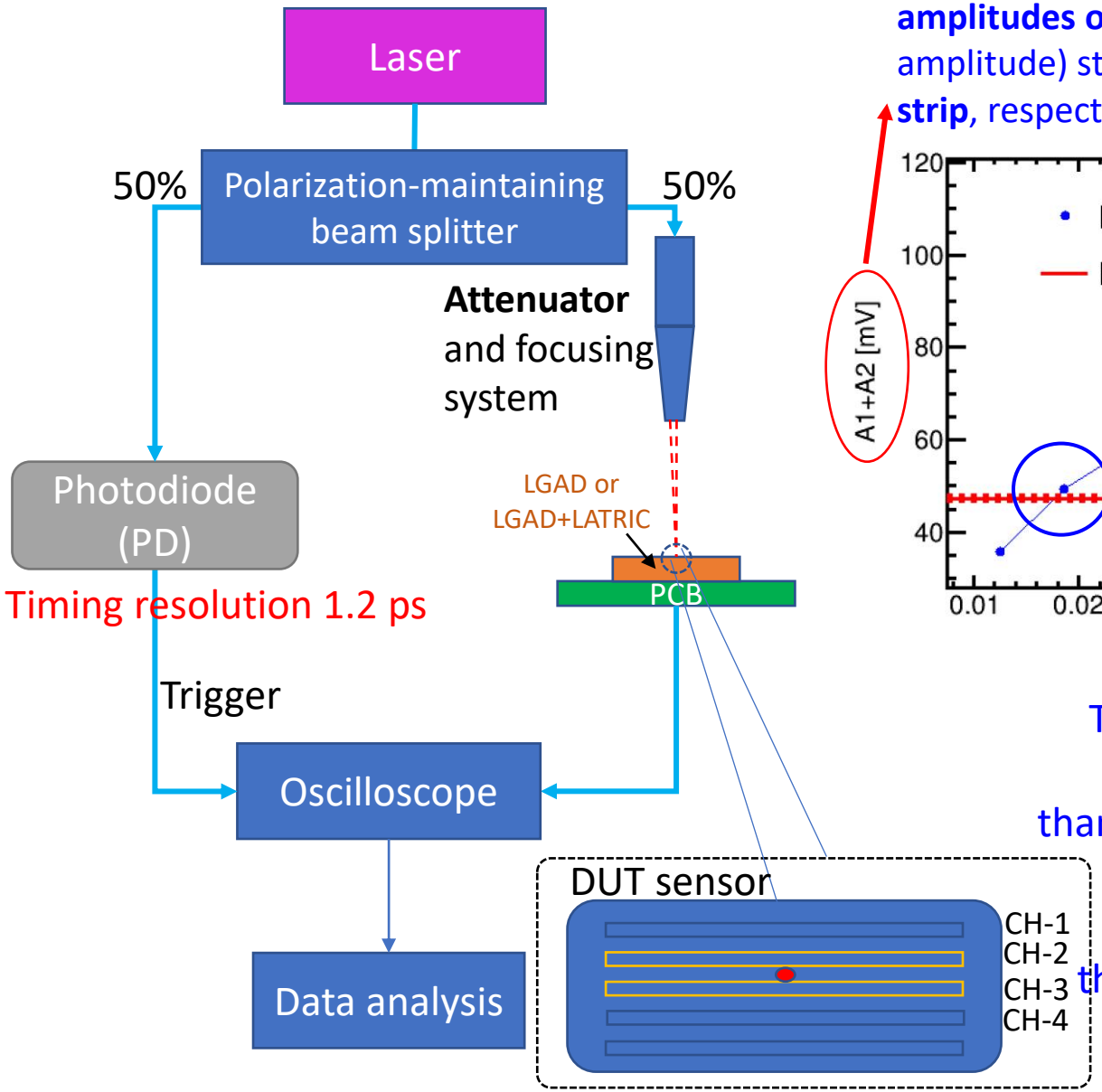


DC-pad sensor (W4-DC-D6)
Time resolution 36 ps

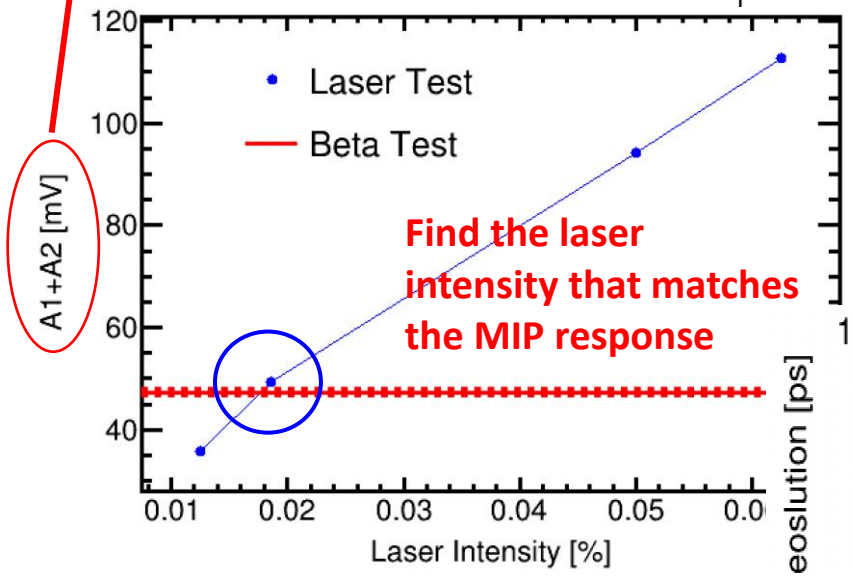


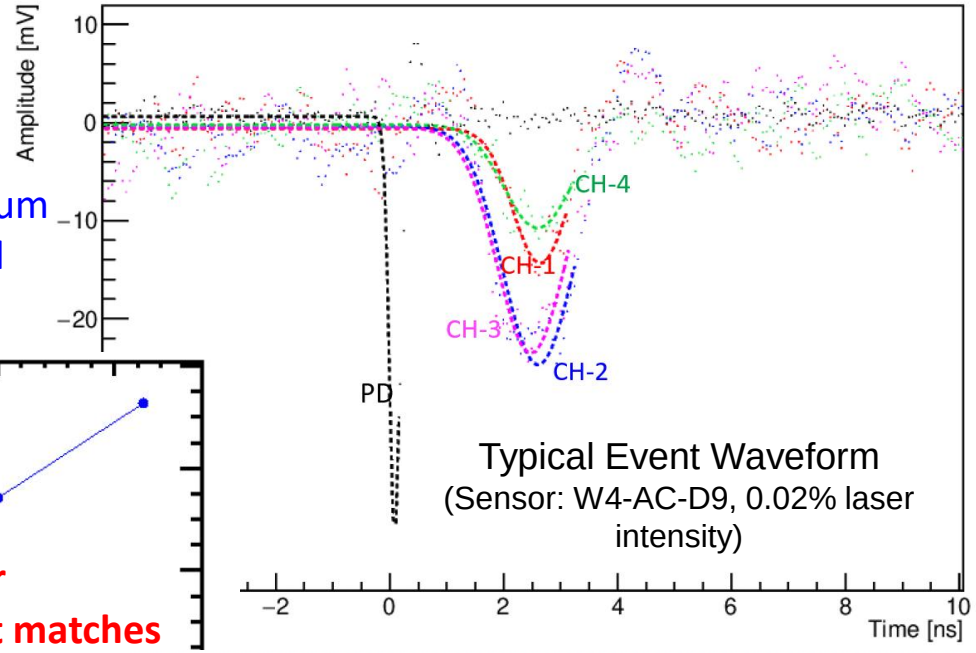


Sensor Characterization

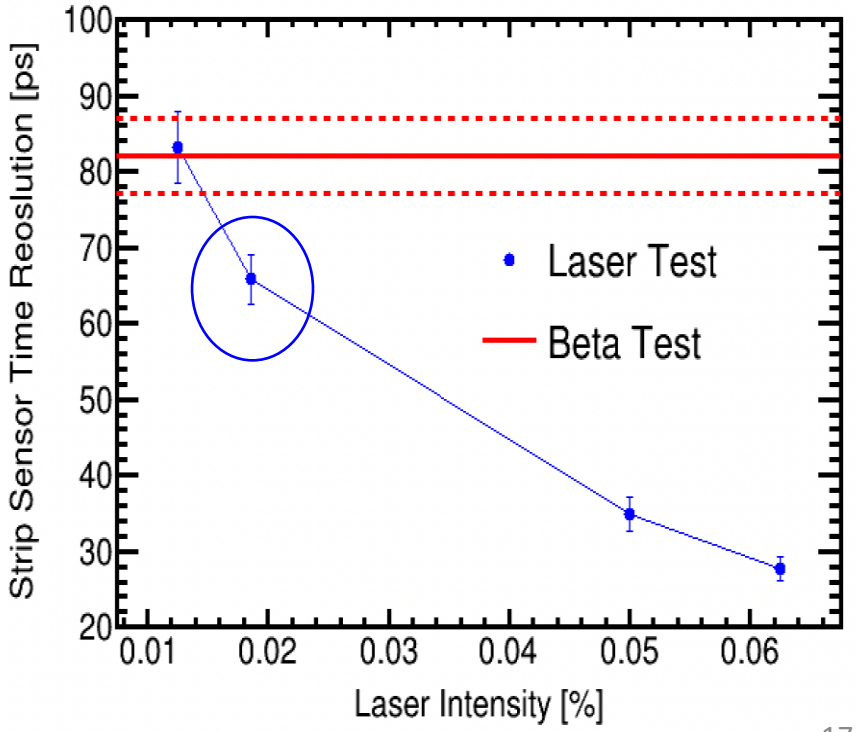


A1 and A2 are **the waveform amplitudes of the seed** (maximum amplitude) strip **and the second strip**, respectively.





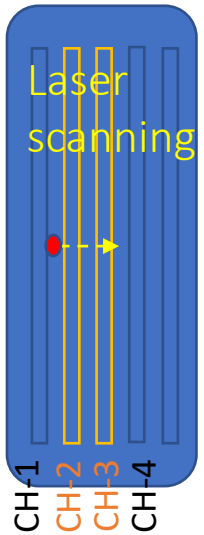
The **time resolution ~65 ps**, which is 20% better than the beta test (~80 ps), as Landau fluctuations in dE/dx are absent in the laser measurements.

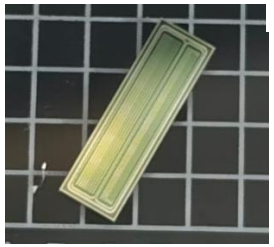


Strip Sensor Spatial Resolution with MIP-Equivalent Laser (0.02% Intensity)

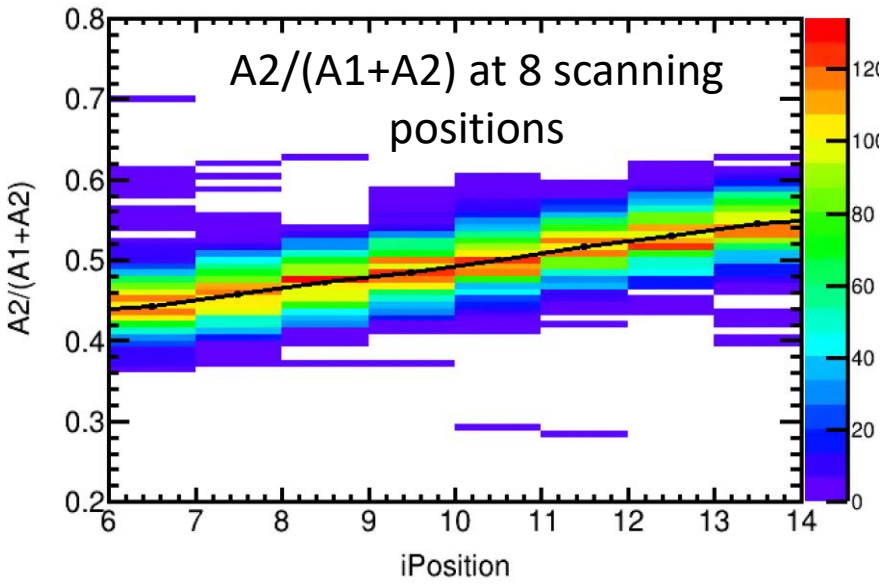
A_1 and A_2 are the waveform amplitudes of the seed (maximum amplitude) strip and the second strip, respectively.

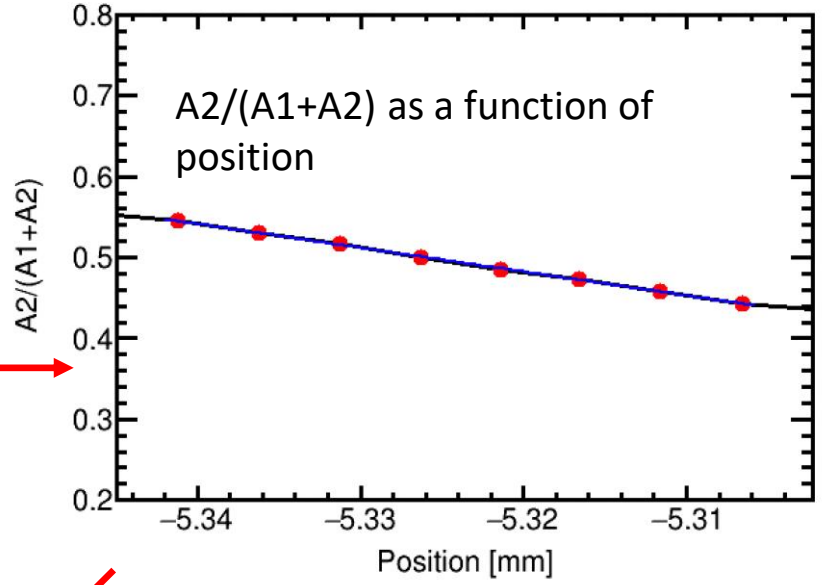
5µm per scanning step
1000 waveforms per step

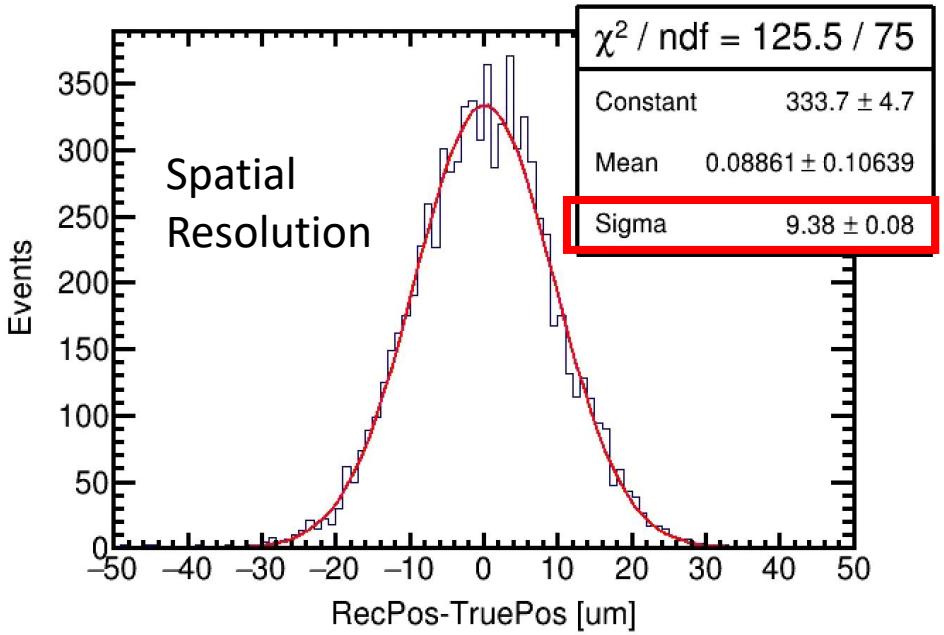




Strip sensor (W4-AC-D9, 2 cm): Open window of 50 µm between 2 strips.



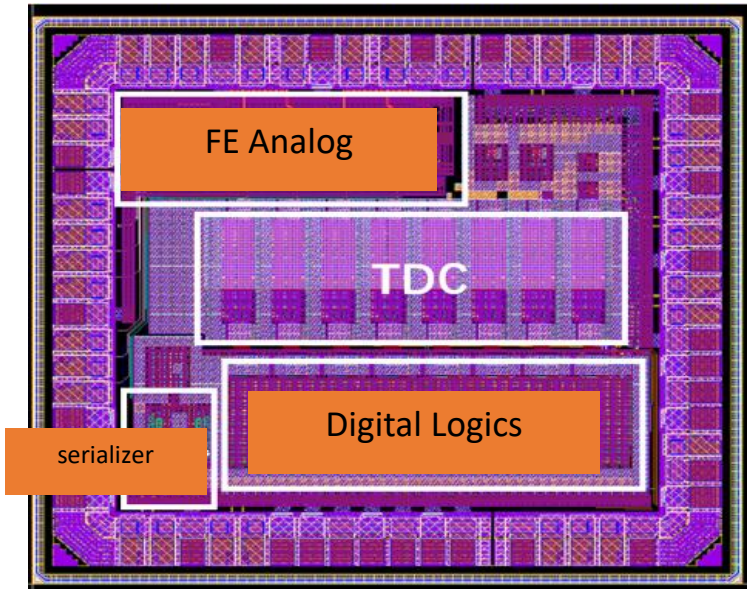




The latest tape-out optimized n^+ strip sensor (W4-AC-D9: 2 cm, pitch 100 µm, 50 µm electrode width, and n^+ dose = 0.1 p) achieved a spatial resolution of 9.4 µm.

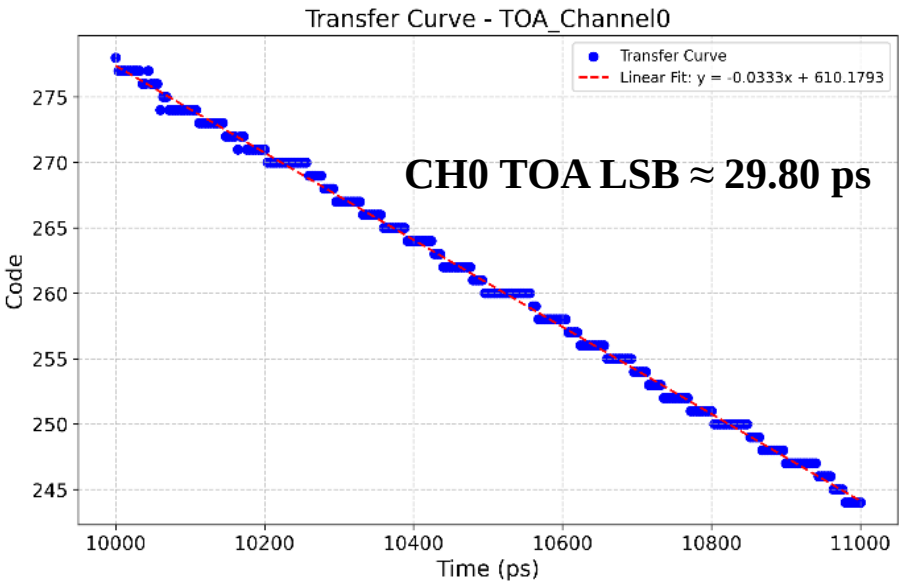
AC-LGAD Readout ASIC, LATRIC-1

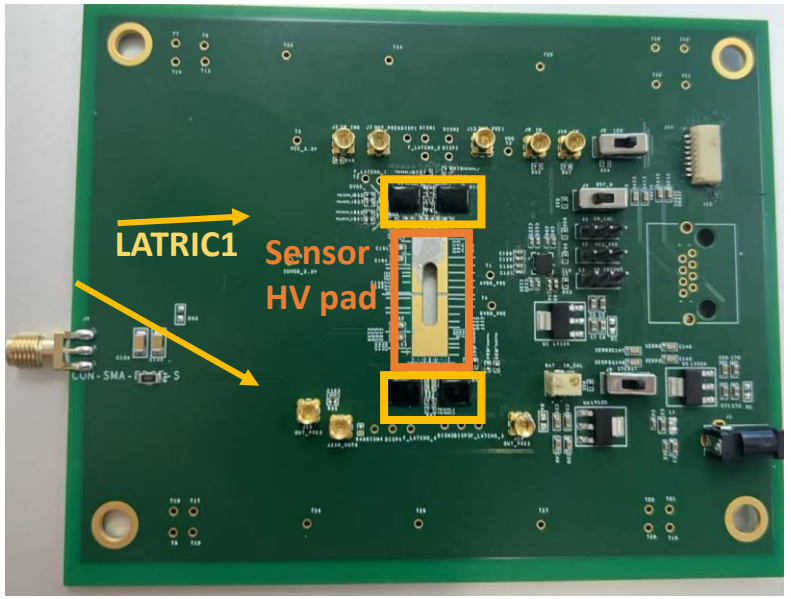
- The second version readout ASIC, LATRIC-1
  - Submitted for tape-out in October 2025
  - The channel pitch is **100 µm.**
  - **8 channels:** Four channels integrate the analog front-end and TDC. The other four channels consist of TDCs connected to differential pulse receivers.
- Performance optimizations include:
  - An enhanced analog front-end with **increased preamplifier gain** to improve the signal-to-noise ratio.
  - **Refined encoder logic**, addition of an **event builder and timestamp functionality**, etc.



LATRIC1 layout

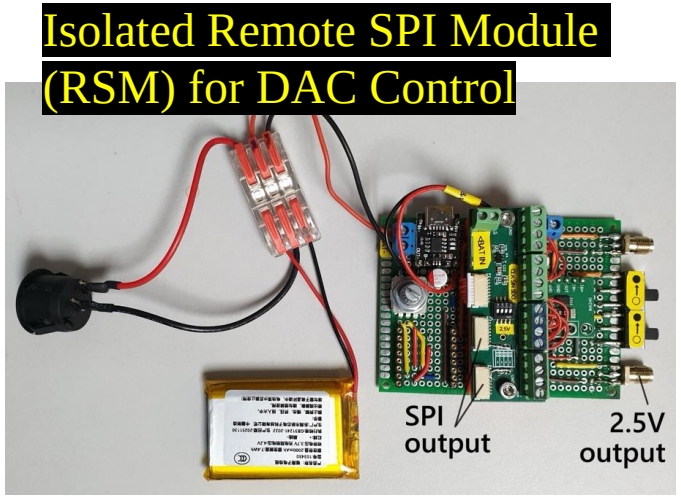
Tests find that **the LSB is ~30 ps**, meeting the 30 ps design goal.



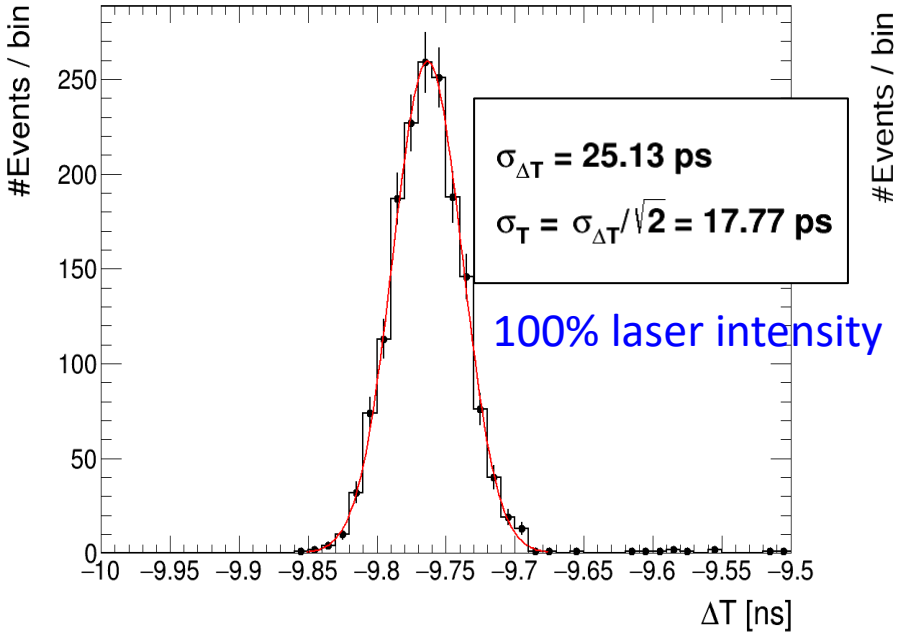


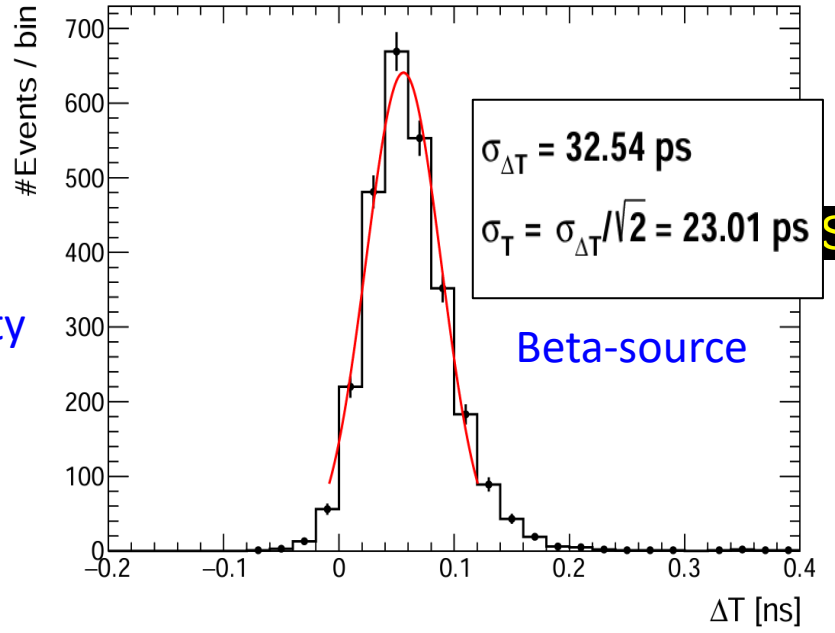
The latest designed LATRIC1-Sensor Integration Test Board

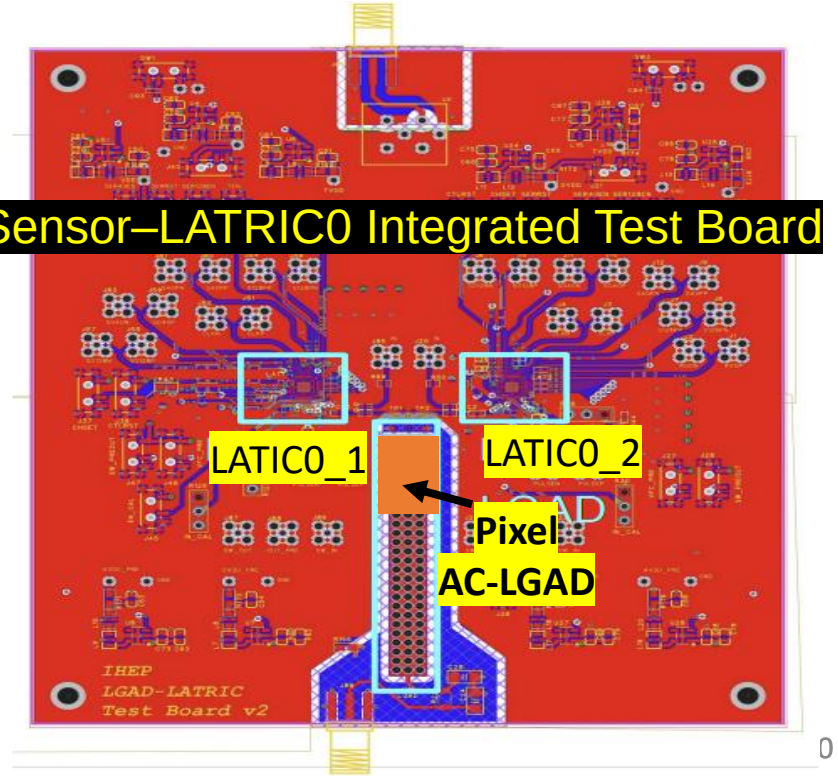
LATRIC0 (Single Channel) and Sensor Combined Test



Time difference measured with two LATRIC0 chips



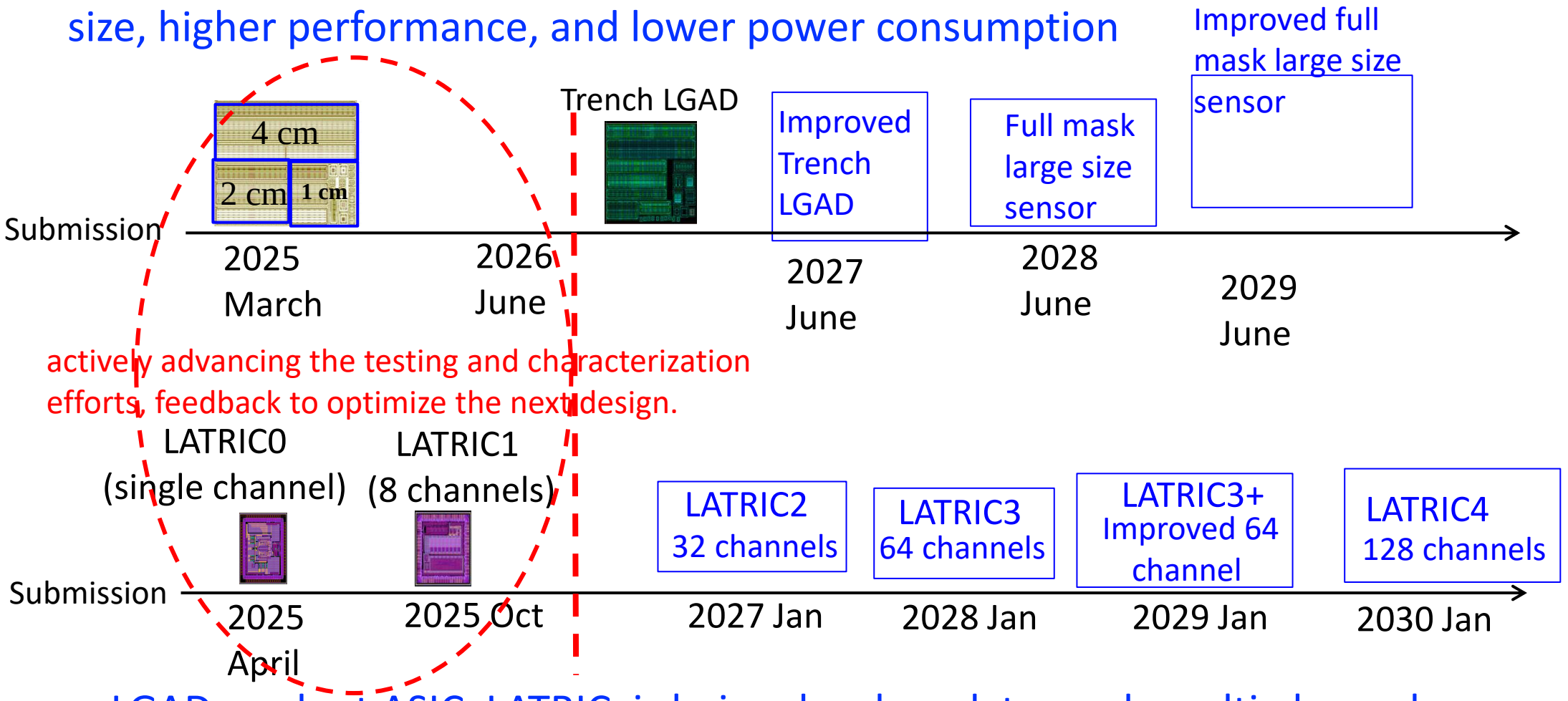




Beta- equivalent laser intensity studies are ongoing.

AC-LGAD and LATRIC R&D Timeline

- LGAD sensors are evolving toward improved process, larger size, higher performance, and lower power consumption



- LGAD readout ASIC, LATRIC, is being developed towards multi-channels

Summary

- The R&D of the CEPC/AGORA Silicon Trackers is progressing rapidly.
- Sub-detector development spans a spectrum of maturity: from initial prototype R&D, through design refinement.
  - Vertex: TaichuPix Stitched MAPS
    - Ladder based prototype has been built and tested, next step is develop sensor with stitching technology
  - Inner Tracker: COFFEE HVCMOS
    - COFFEE3 lab & beam tests proves most of the design functionalities
    - CHiR1 submitted with improved process & high-res wafers, paving the way for future development with better performance
  - Outer Tracker: AC-LGAD + LATRIC Readout ASIC
    - Preliminary timing and position resolution studies with laser and beta source
    - More testing and characterization needed, feedback to optimize the next sensor & ASIC design.

Additional Slides

CEPC Vertex Detector Requirement

Parameter	Design
Spatial Resolution	~ 5 μm
Detector material budget	$\sim 0.8\%\ X_0$
First layer radius	11.1 mm
Power Consumption	< 40 mW/cm^2 (air cooling requirement)
Time stamp precision	100 ns
Fluence	$\sim 2 \times 10^{14}$ Neq/cm^2 (for first 10 years)
Operation Temperature	~ 5 °C to 30 °C
Readout Electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

TaichuPix3's Pixel architecture – Analog

- Digital-in-Pixel scheme: in pixel discrimination & register
- Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)
  - As most of ATLAS-MAPS sensors' scheme
- Biasing current has to be increased, for a peaking time of ~25ns for 40MHz BX @ Z pole
- Consequence:
  - Power dissipation increased
  - Faster CIS process has to be used
    - With faster charge collection time, otherwise only fast electronics is of no meaning

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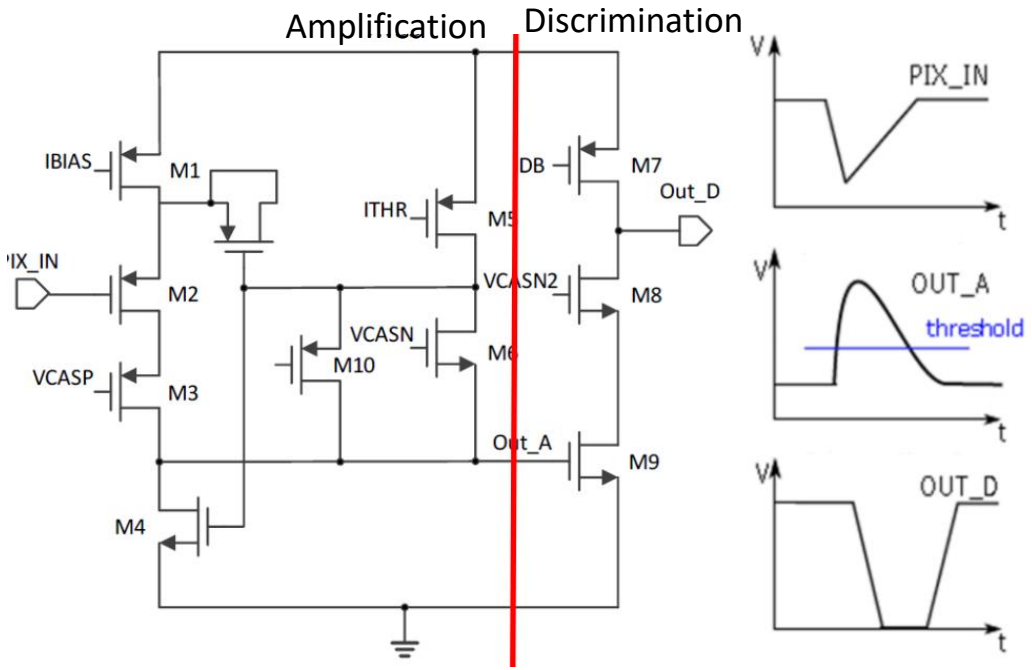
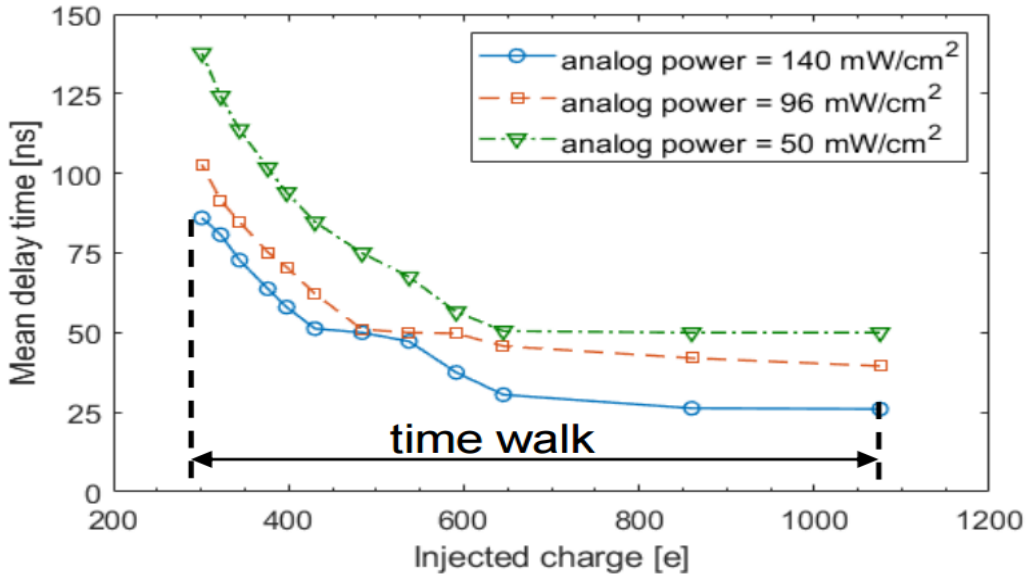
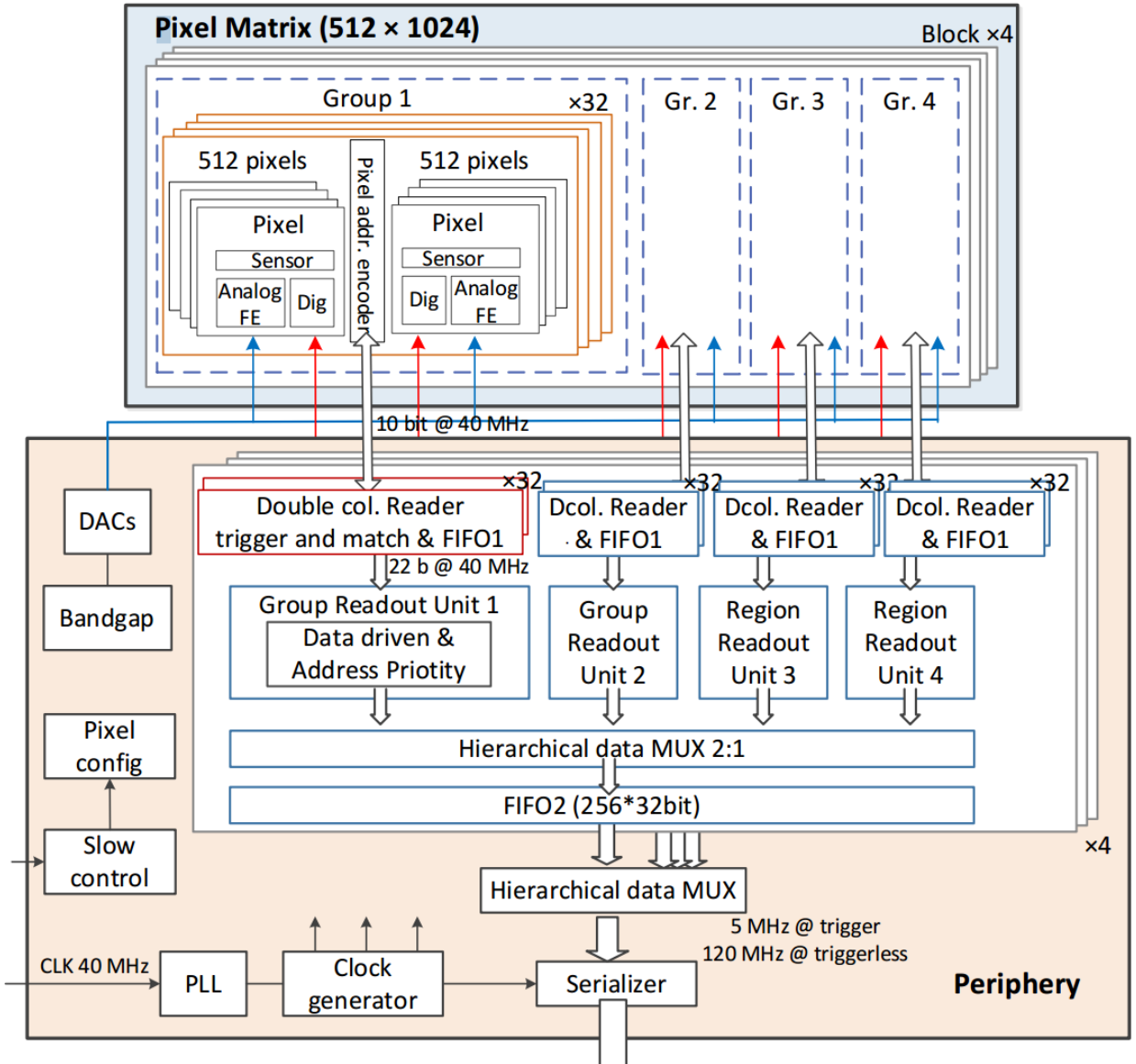




Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

TaichuPix sensor architecture

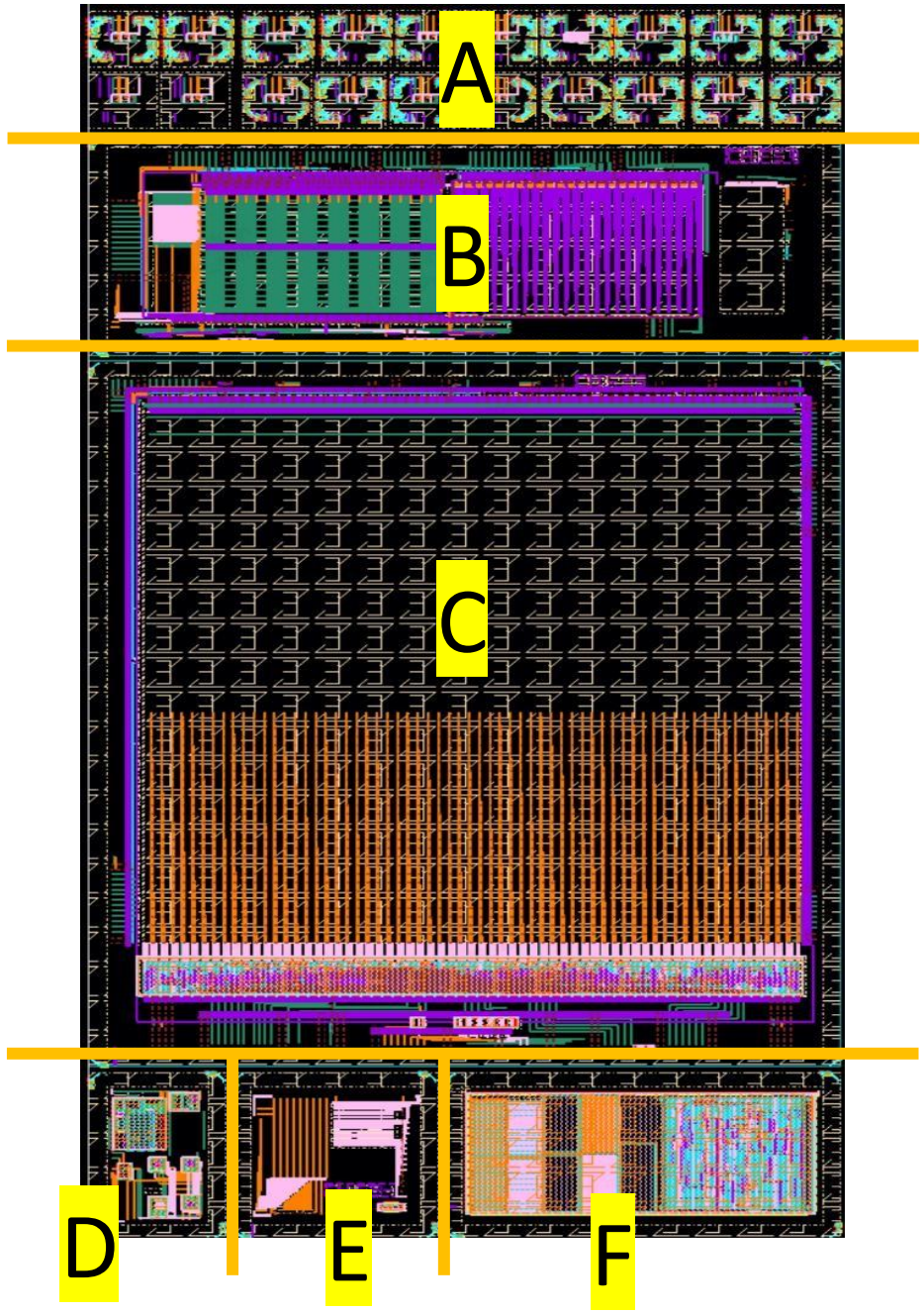


- Pixel 25 µm × 25 µm
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- Column-drain readout for pixel matrix
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- 2-level FIFO scheme
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- Trigger-less & Trigger mode compatible
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- Features standalone operation
  - on-chip bias generation, LDO, slow control, etc.

Slide material from Wei WEI

CHiR1 chip

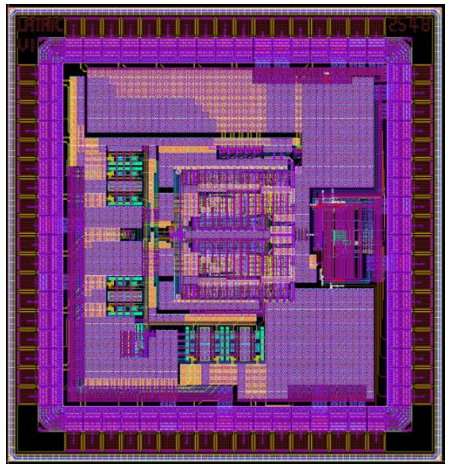
- Can be diced into a number of chips serving various goals
- Passive sensor validation:
  - (A) 20 arrays of 3x4 passive pixels with diff guard ring designs, each can be diced into individual 1x1 mm2 chip
  - Pixel size: 38 um x 175 um
- Pixel array design
  - (B) 9 variations of in-pixel frontend designs
  - (C) main pixel array of 256 x 64 pixels; similar as COFFEE3 with readout data format compatible with 32-bit UP spec
- IP validations
  - (D) necessary analog Ips: PLL, DLL, LVDS transceivers …
  - (E) alternative small pixel arrays
  - (F) digital modules and transistors for TID and SEE studies

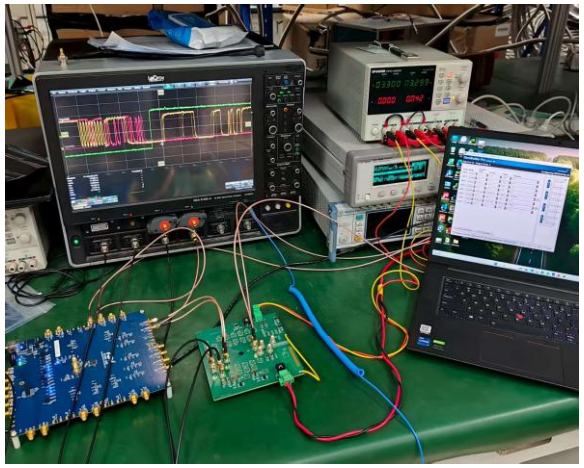


AC-LGAD Readout ASIC, LATRIC

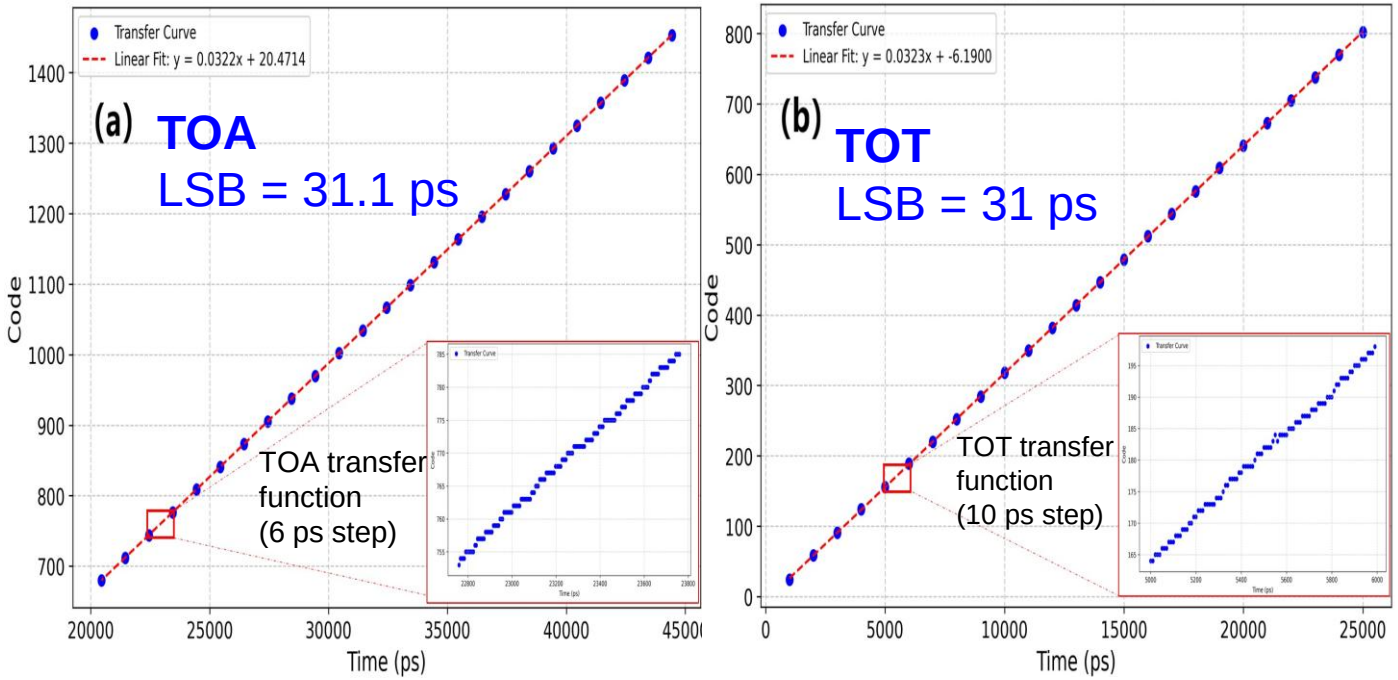
The first LATRIC prototype, LATRIC-V0:

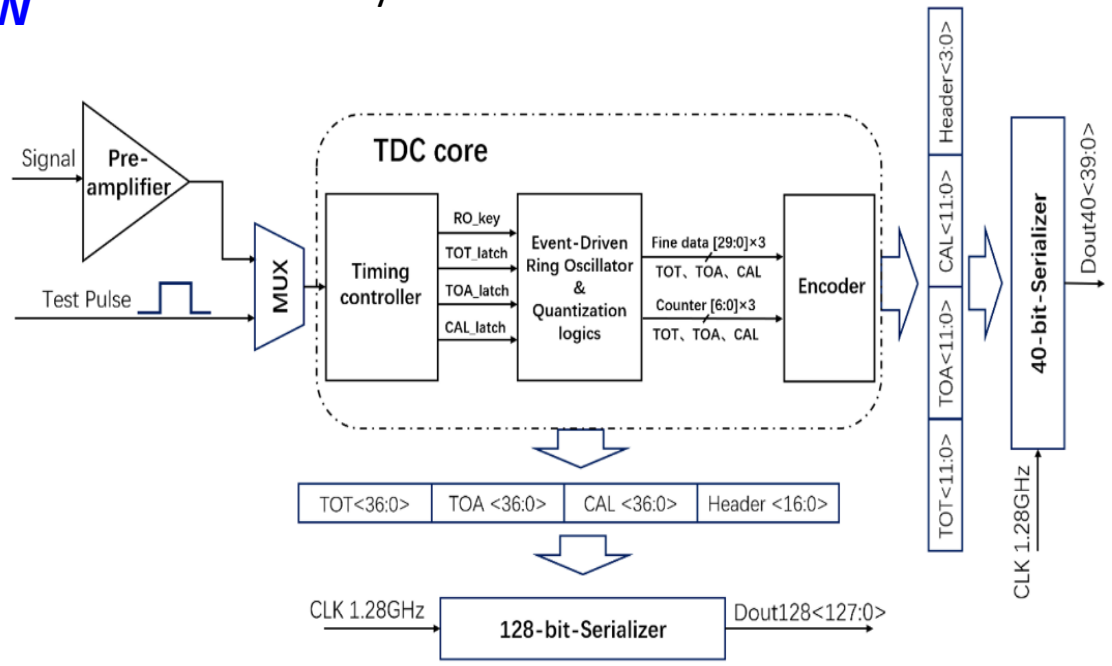
- Fabricated using a 55nm CMOS process
- Has a pre-amplifer, a discriminator, a TDC, and a serializer for data output.
- Tests find that **the LSB is ~30 ps**, meeting the 30 ps design goal.
- Power consumption remains **below 6.24 mW per channel** at 1 MHz event rate, with the **TDC core consuming 0.36 mW**





LATRIC-V0 layout





DOI 10.1088/1748-0221/21/04/C04028

29

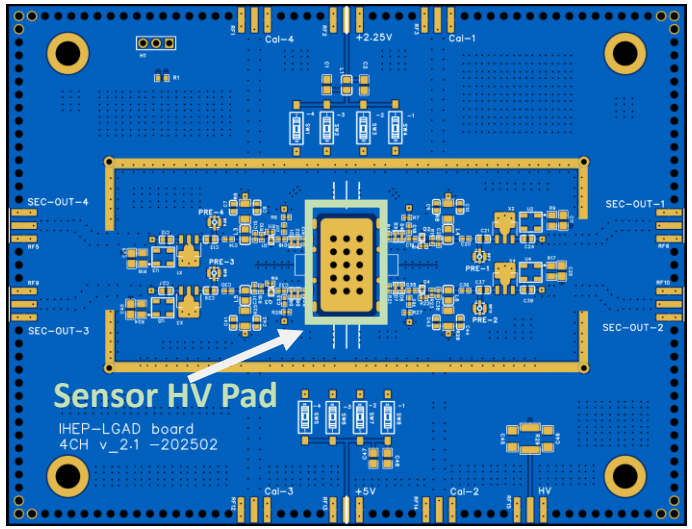
Voltage	1.2 V
Channel	128
Channel pitch	< 100 µm
Senor capacitance	8 pF
Power dissipation per area	300 mW/cm^2
Power dissipation per ASIC	1.5 W (Occupancy $< 1\%$)
e-link driver bandwidth	43.33 Mbps or 86.67 Mbps
Temperature range	-40 °C to 40 °C

Table 5.11: Geometrical, environmental, electrical, and power requirements for the LATRIC ASIC

Maximum leakage current	5 µA
Single channel noise (ENC)	$<$ 10000 e = 1.6 fC
Cross-talk	$< 10\%$
Threshold dispersion after tuning	$< 10\%$
Maximum jitter	30 ps at 16 fC
TDC contribution	$<$ 30 ps
Time walk contribution	$<$ 10 ps
Minimum threshold	4 fC
Dynamic range	16 fC–50 fC
TDC conversion time	$<$ 23 ns

Table 5.12: Performance requirements for the OTK ASIC. The values given for the noise, minimum threshold, and jitter have been specified considering a detector capacitance Cd = 8 pF.

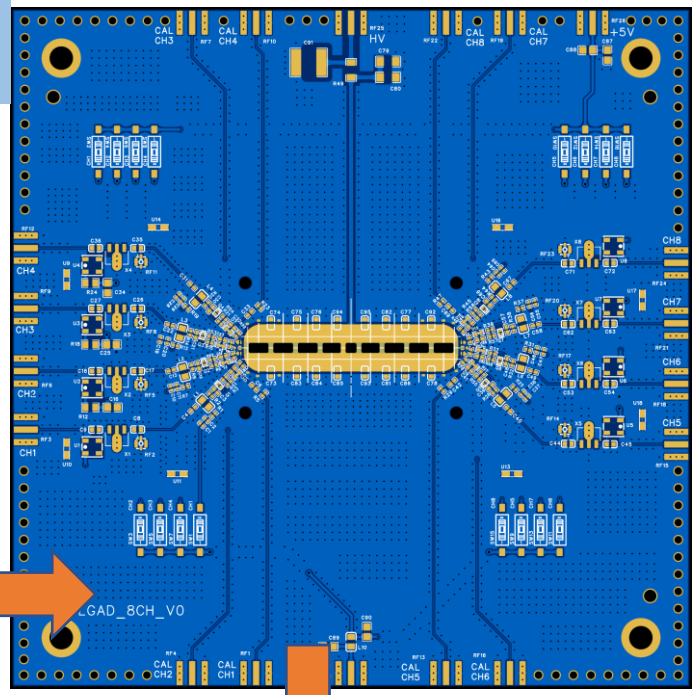
AC-LGAD Pre-Amplifier Board Optimization



10cm x 13cm

V1: 4-Channel LGAD Pre-Amplifier Board:

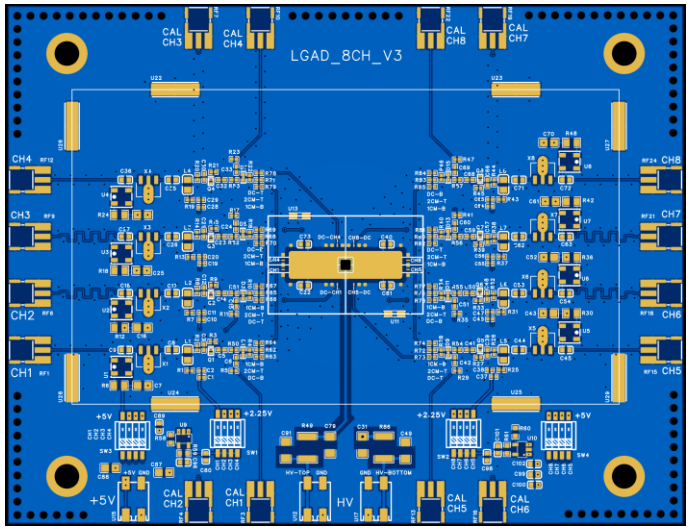
- Provides high-voltage bias for LGAD sensors.
- Four signal readout channels
- ~100× amplification per channel



13cm x 13cm

V2: 8-Channel LGAD Pre-Amplifier Board:

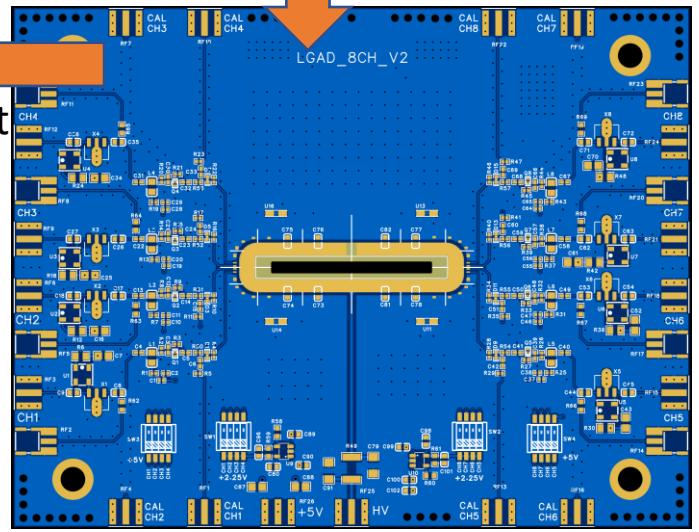
- **Increased number of channels**
- **Extended high-voltage pads** for better compatibility with strip sensors
- Optimized HV pad geometry with cut-outs to improve particle detection efficiency



10cm x 13cm

V4: 8-Channel Double-Sided LGAD Pre-Amplifier Board:

- Double-sided to support different LGAD types (pixel and strip)
- Optimized routing with equal-length traces for all 8 channels
- Reduced board thickness to ~5 mm

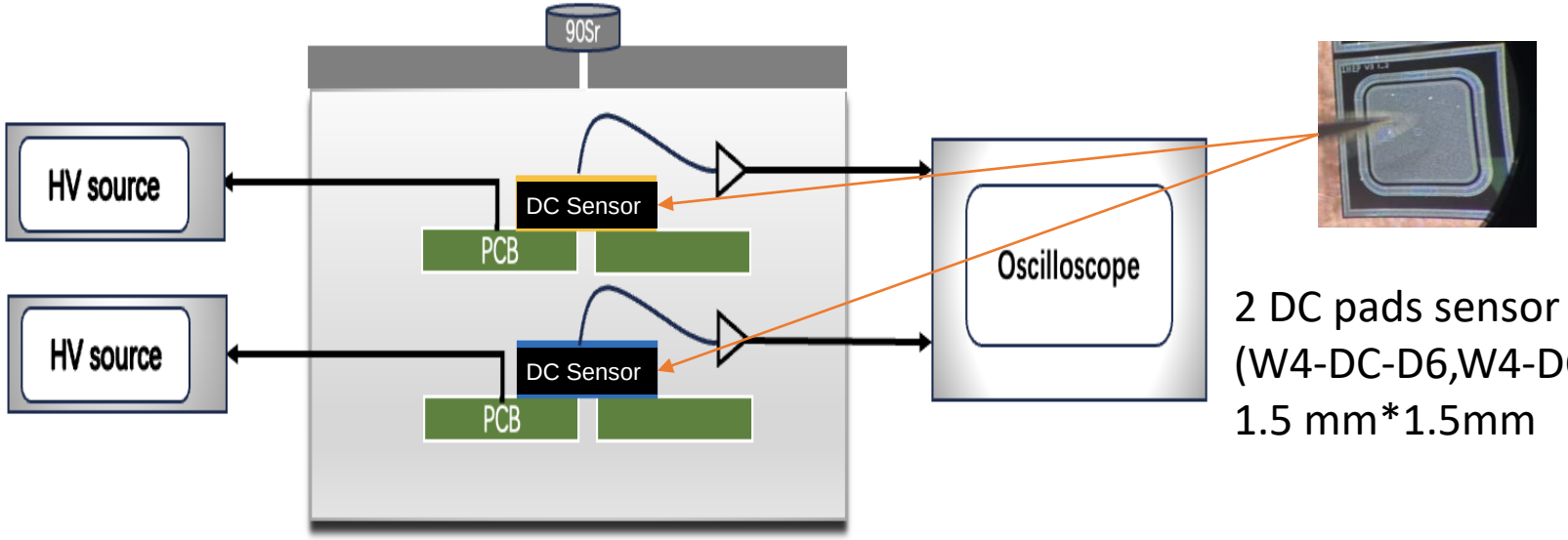


10cm x 13cm

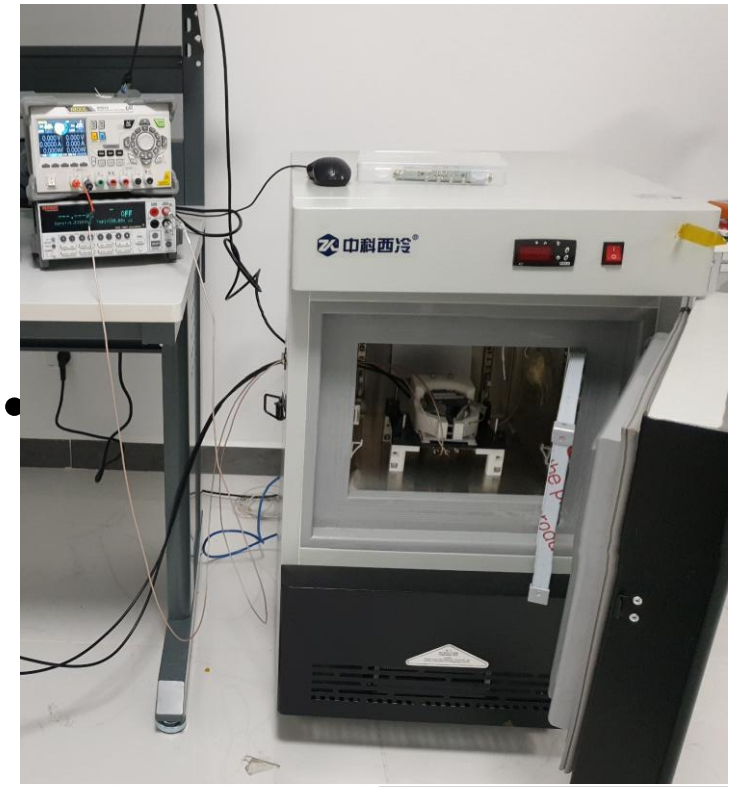
V3: 8-Channel LGAD Pre-Amplifier Board

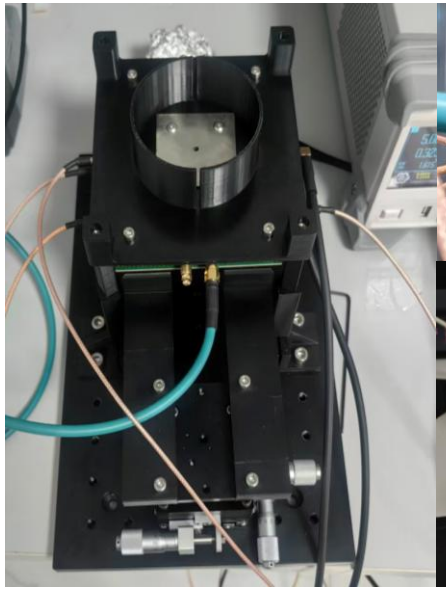
- Reduced board size for better integration
- Simplified power connectors for easier cabling
- **Optimized HV pad cut-out geometry** to further enhance particle detection efficiency

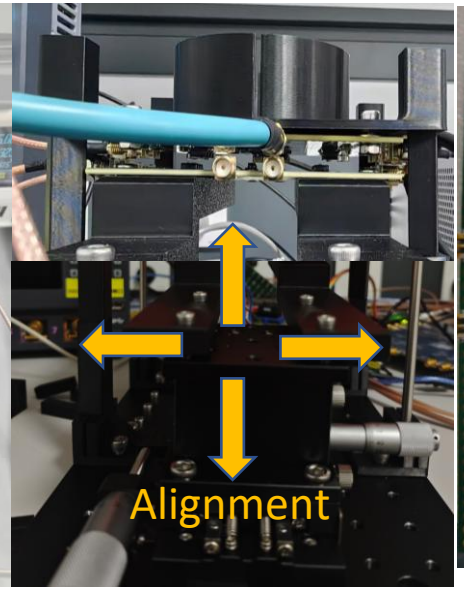
Sr-90 β-Source Test Setup

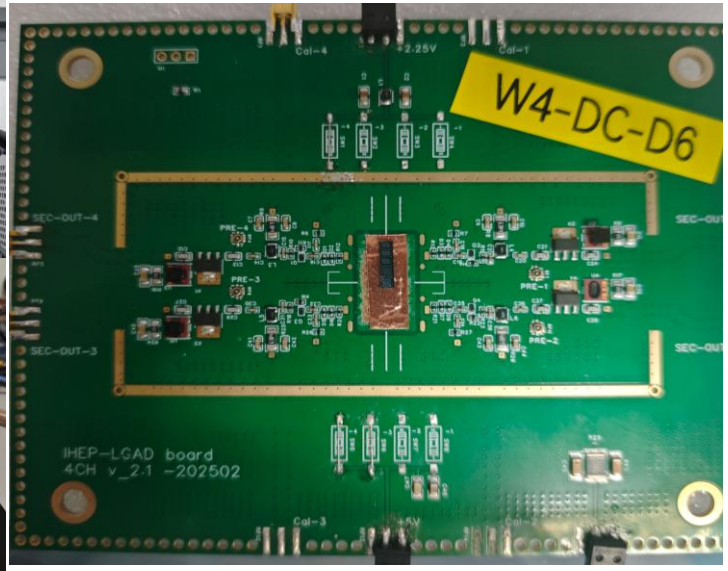


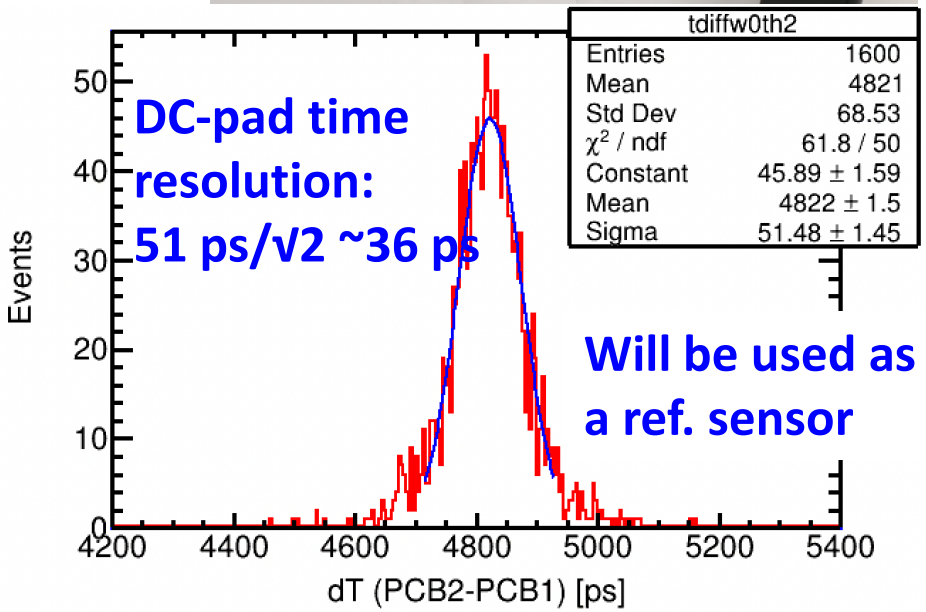
2 DC pads sensor
(W4-DC-D6,W4-DC-12):
1.5 mm*1.5mm





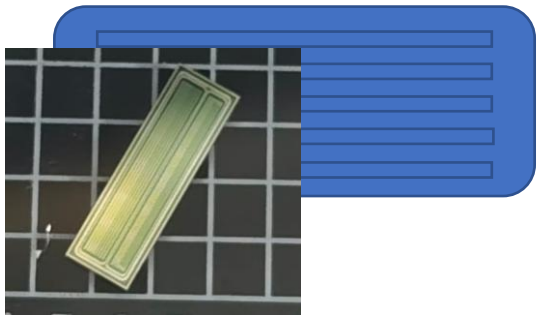




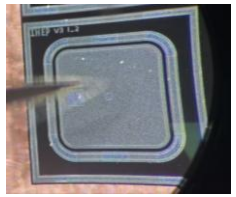


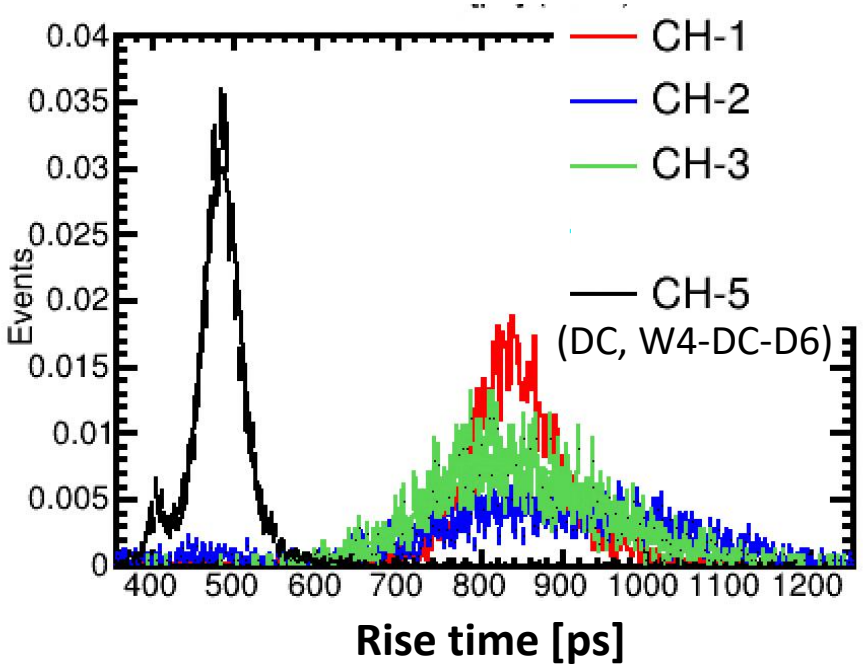
Strip Sensor Timing Resolution (β-Source Test)

DUT sensor (AC-LGAD)

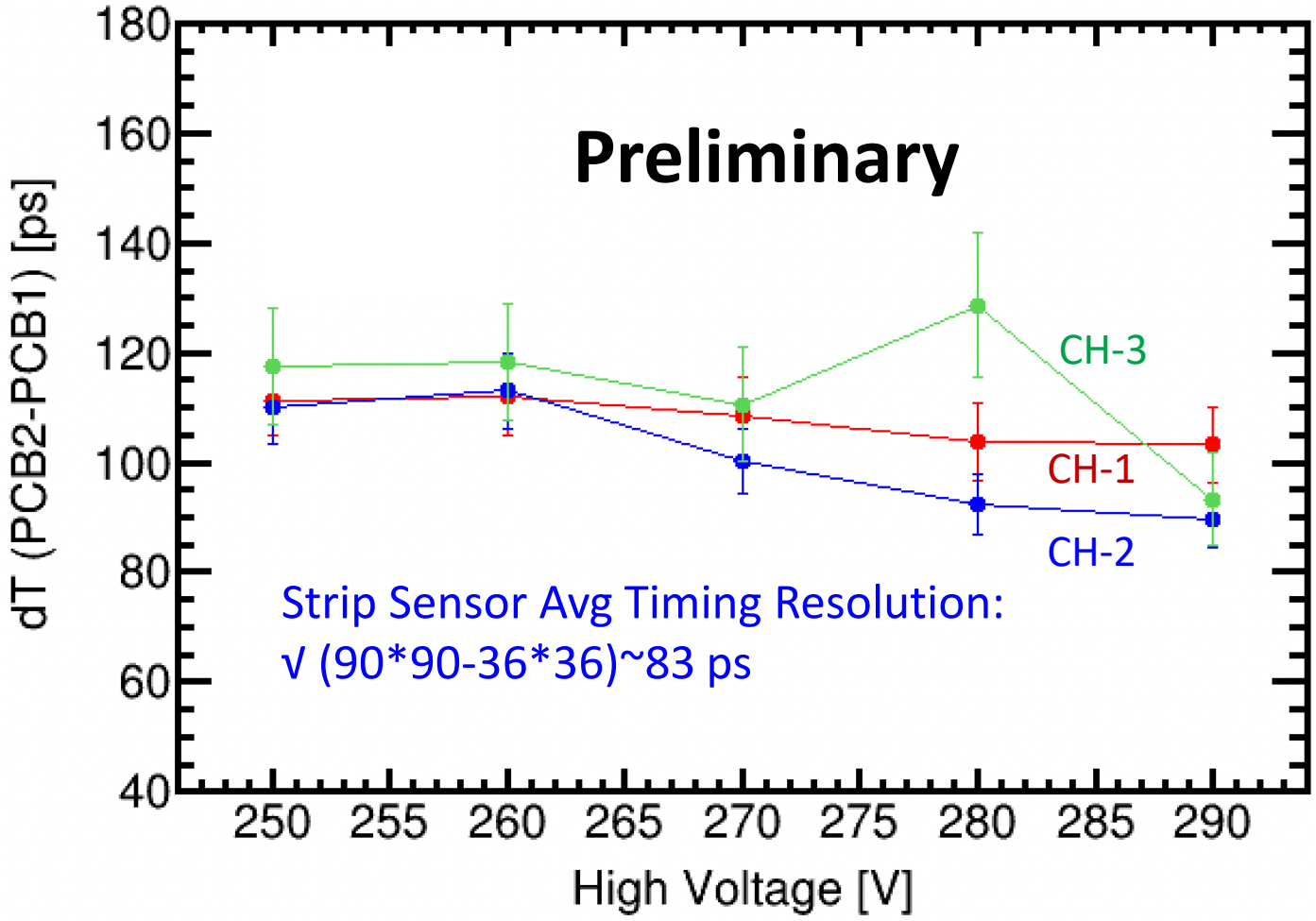


Ref sensor (DC)





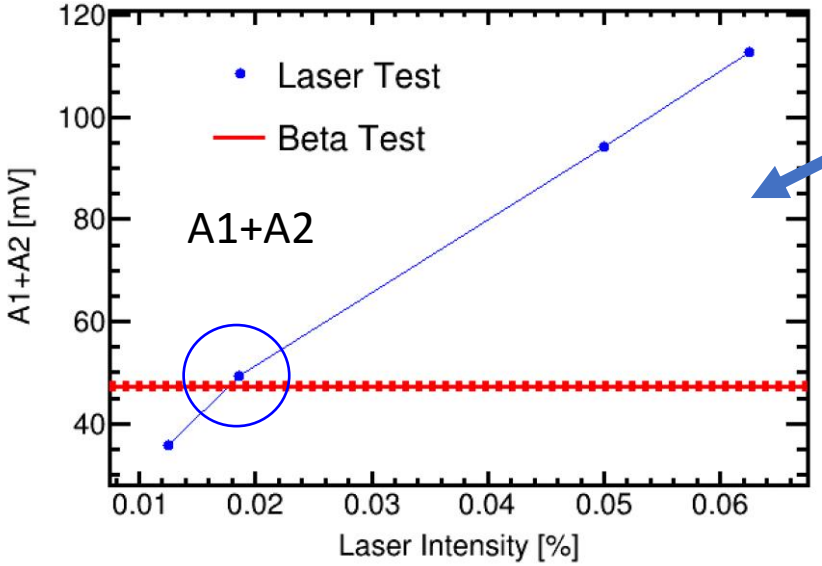
W4-AC-D9, 2 cm, pitch 100um electrode width 50um



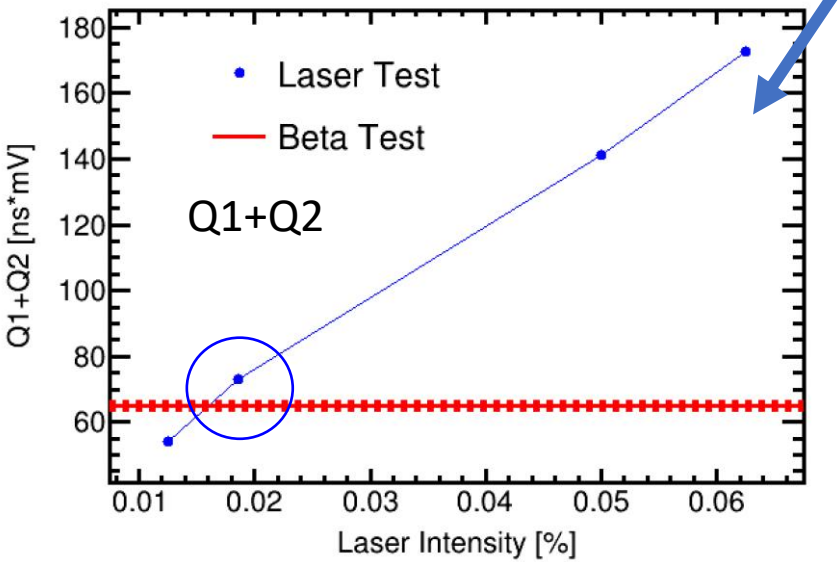
The signal rise time of strip sensors is substantially longer than that of pad sensors.

The strip sensor (2cm, pitch 100um electrode width 50um) achieved a timing resolution of ~83 ps.

Beta-Equivalent Laser Intensity Tuning



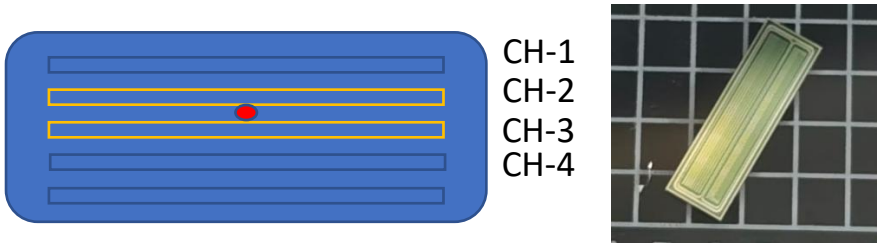
A1 and A2 are **the waveform amplitudes of the seed** (maximum amplitude) strip **and the second strip**, respectively.

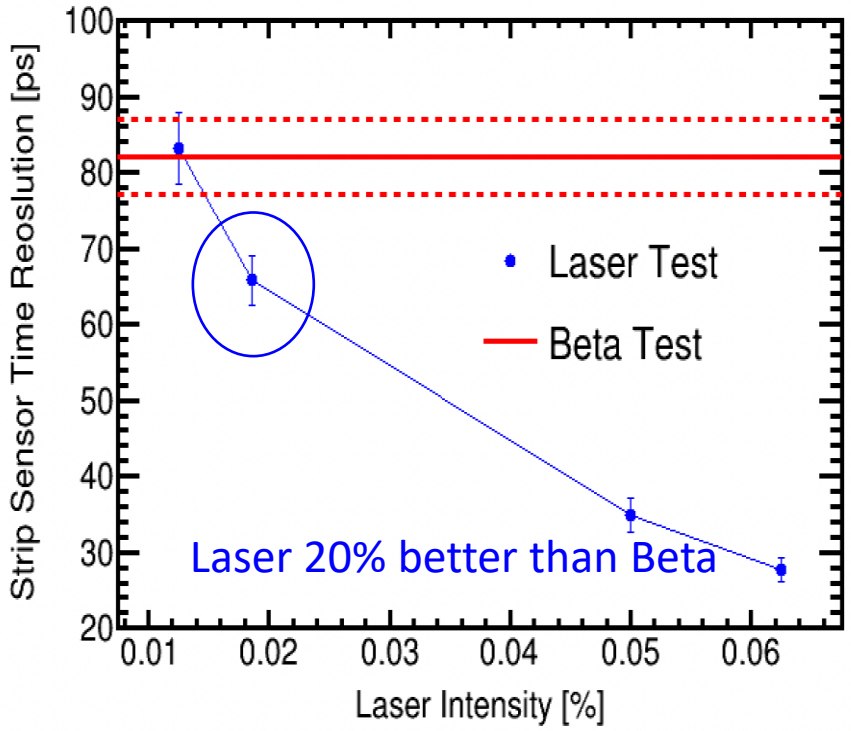


Q1 and Q2 are the **integral charge** (negative polarity) of the corresponding waveforms.

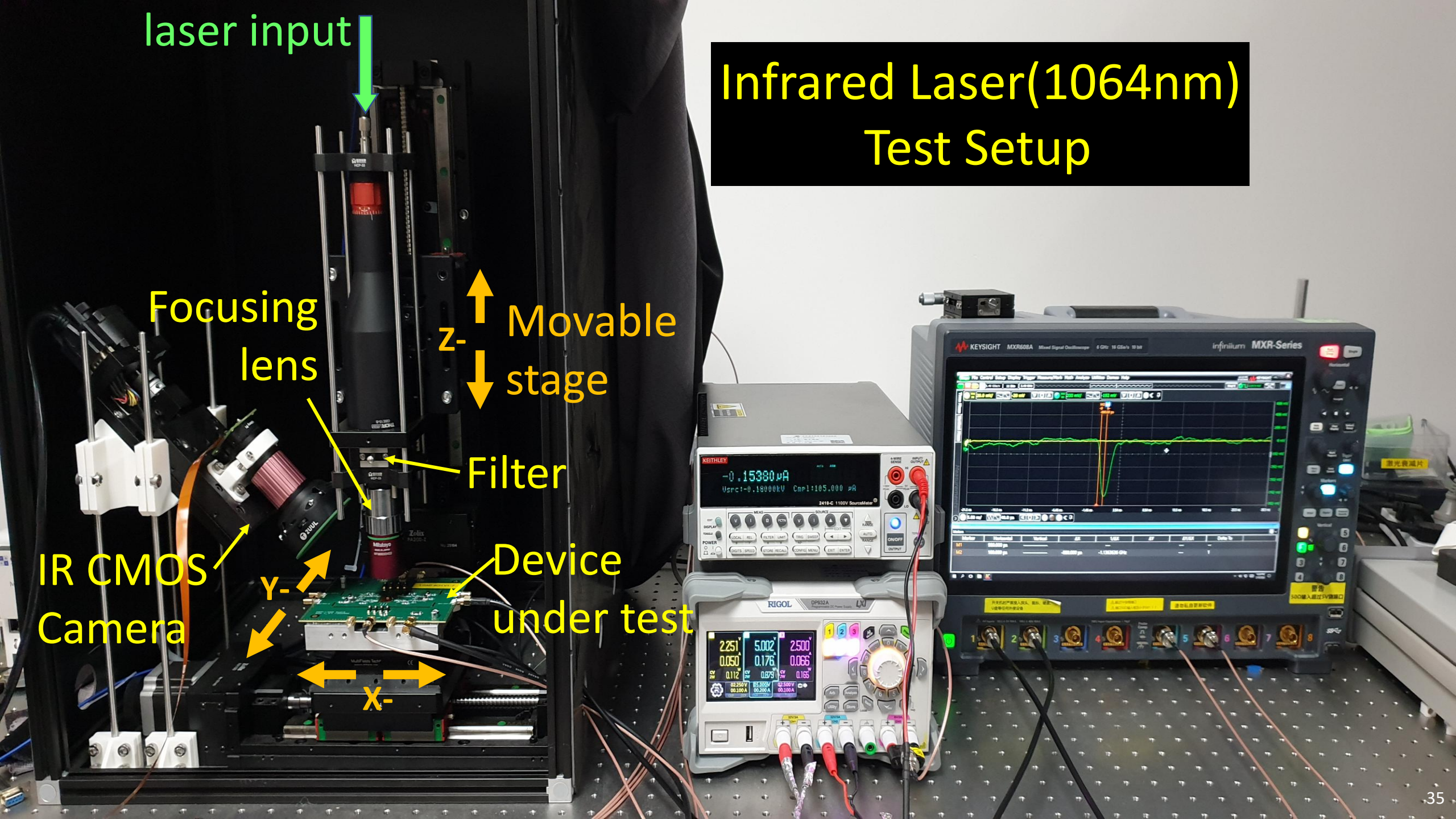
The laser intensity of 0.02% matches the MIP response in both amplitude and integrated charge.

Strip sensor (W4-AC-D9, 2 cm)

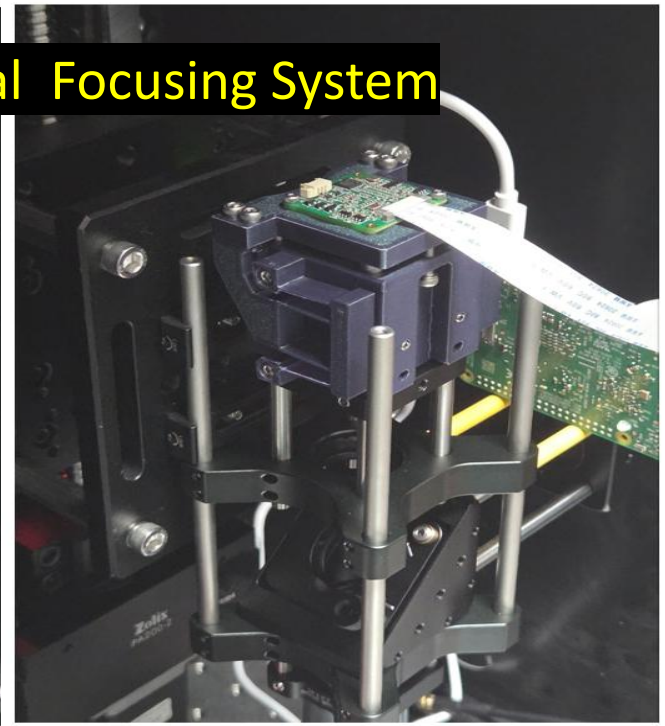




The **time resolution of the strip sensor** (W4-AC-D9, 2 cm) obtained from the laser test is **~65 ps**, which is 20% better the beta test (~80 ps), as Landau fluctuations in dE/dx are absent in the laser measurements.

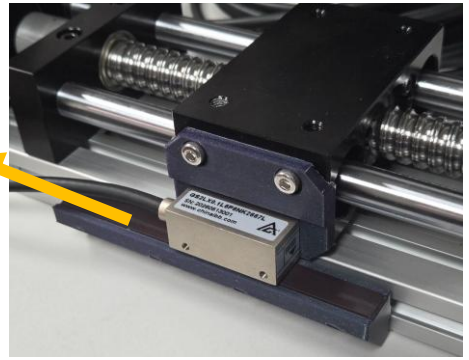

laser input
Focusing lens
z-
Movable stage
Filter
IR CMOS Camera
Y-
Device under test
X-
Infrared Laser(1064nm) Test Setup

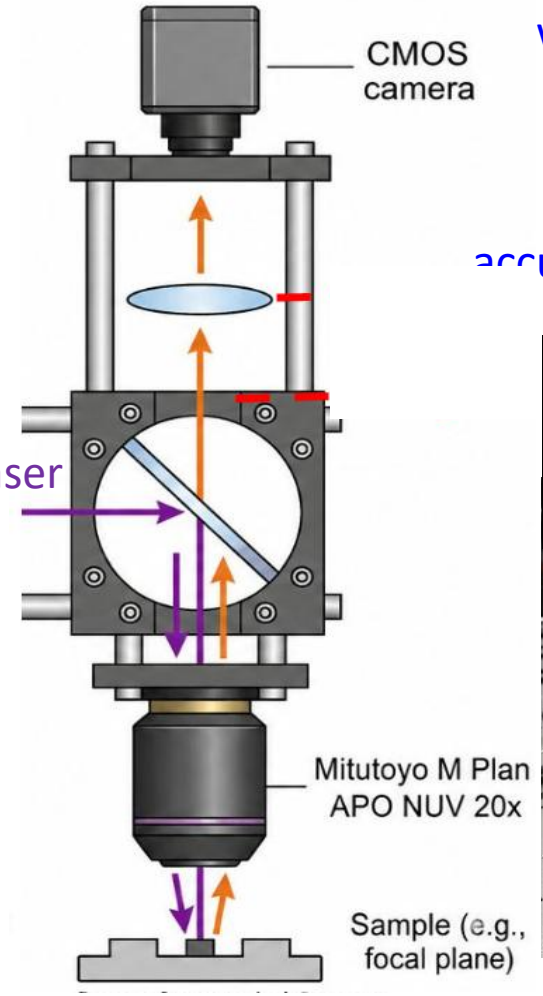
In addition to the infrared test system, a customized **UV laser test platform for SiC sensor** has been developed. Both Si and SiC sensor development activities share a unified R&D framework with common test infrastructure, front-end electronics, and system integration resources.



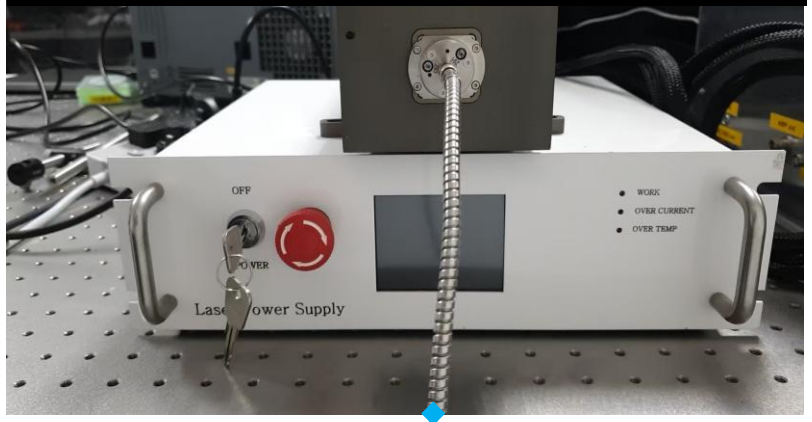
Camera Optical Focusing System

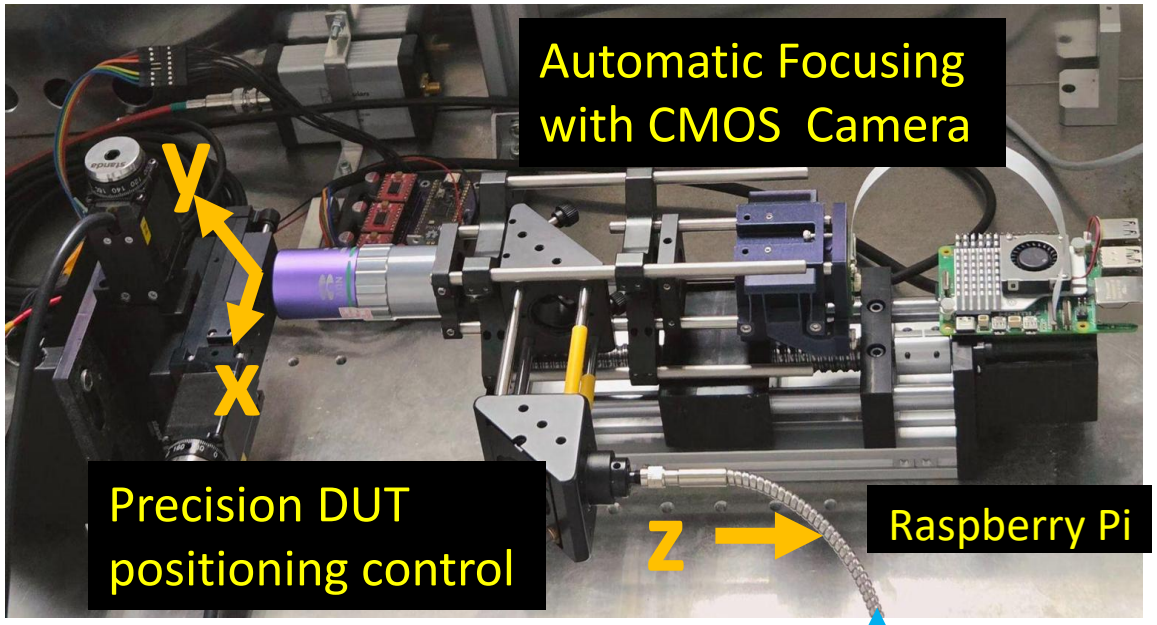
Stepper motor with magnetic encoder feedback: positioning accuracy <0.1 µm





- 355 nm UV laser
- Repetition rate: 1–10 Hz
- Pulse width: ~10 ns





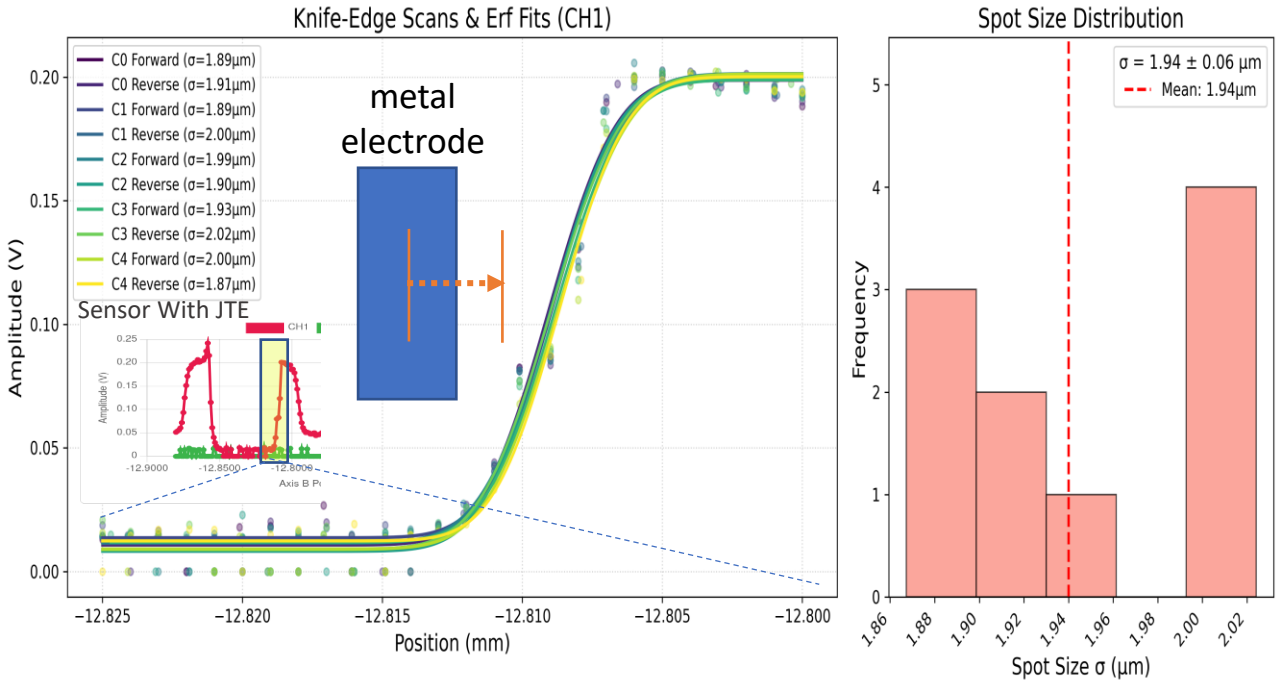
Automatic Focusing with CMOS Camera

Precision DUT positioning control

Raspberry Pi

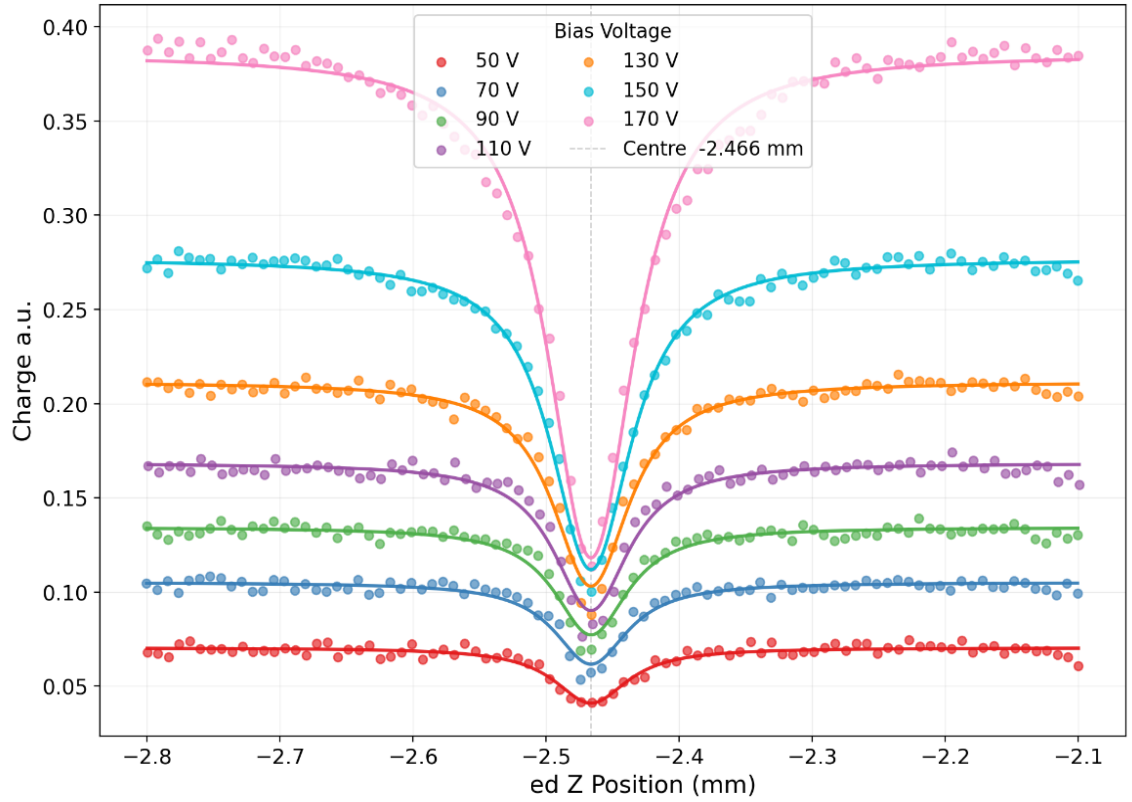
Minimizing Beam Spot Size

- Two independent methods for cross check:
  1. Gain suppression effect→ scan Z position
  2. Knife-edge method → scan across electrode edge for each Z-position



10.1016/j.nima.2025.170844

Gain suppression effect



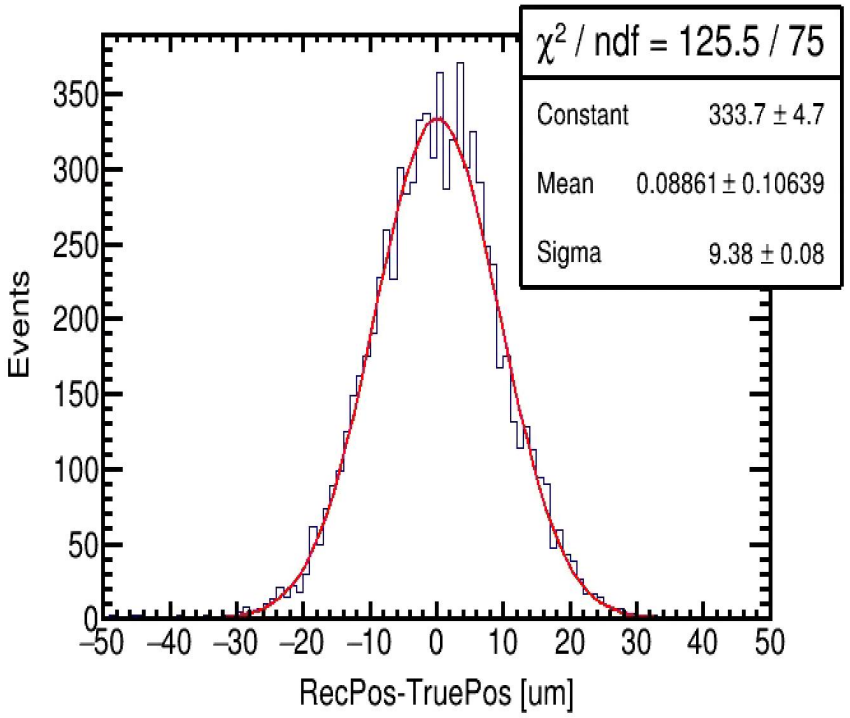
$$S(z) = S_{max}\exp\left(-\frac{A}{w_o^2\left[1+\left(\frac{z-z_o}{z_R}\right)^2\right]}\right)$$

- w_0: The beam waist (minimum radius).
- z_0: The focal point position.
- z_R: The Rayleigh length.

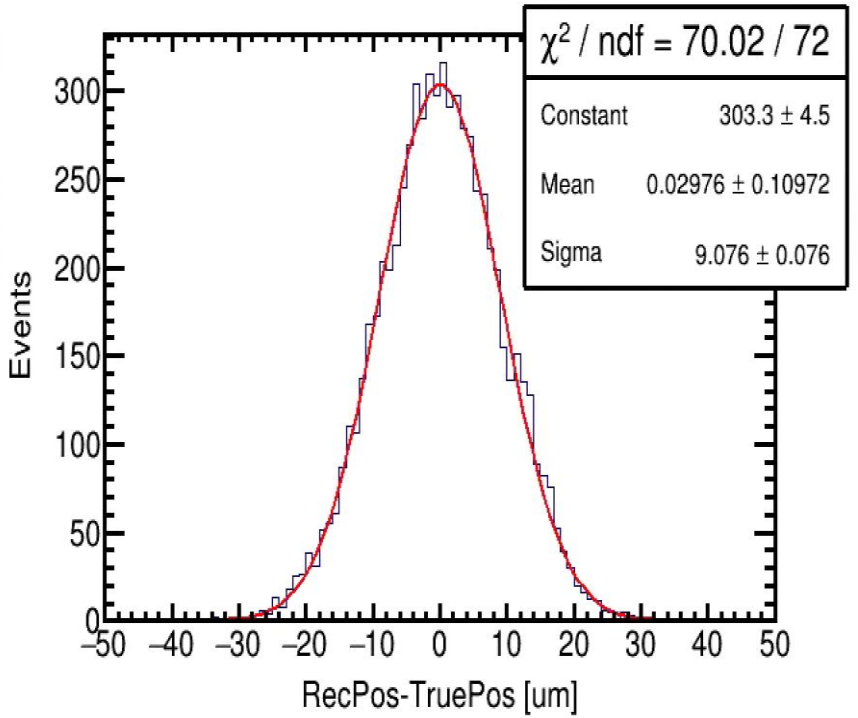
Validated beam waist: < 3um

Sensor Spatial Resolution Using Different Amplitude Estimators

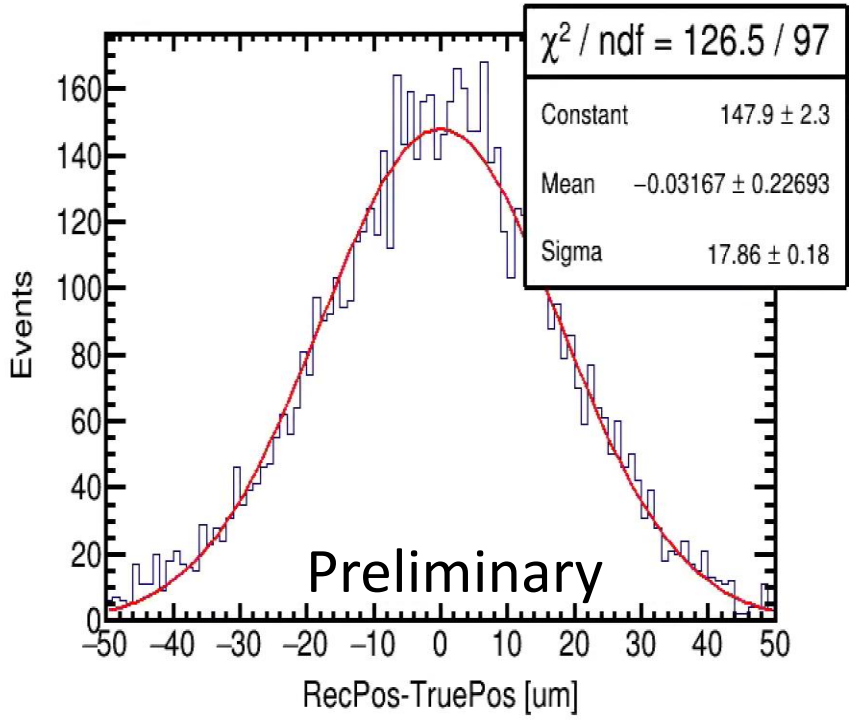
1) Max amplitude



2) Integral charge



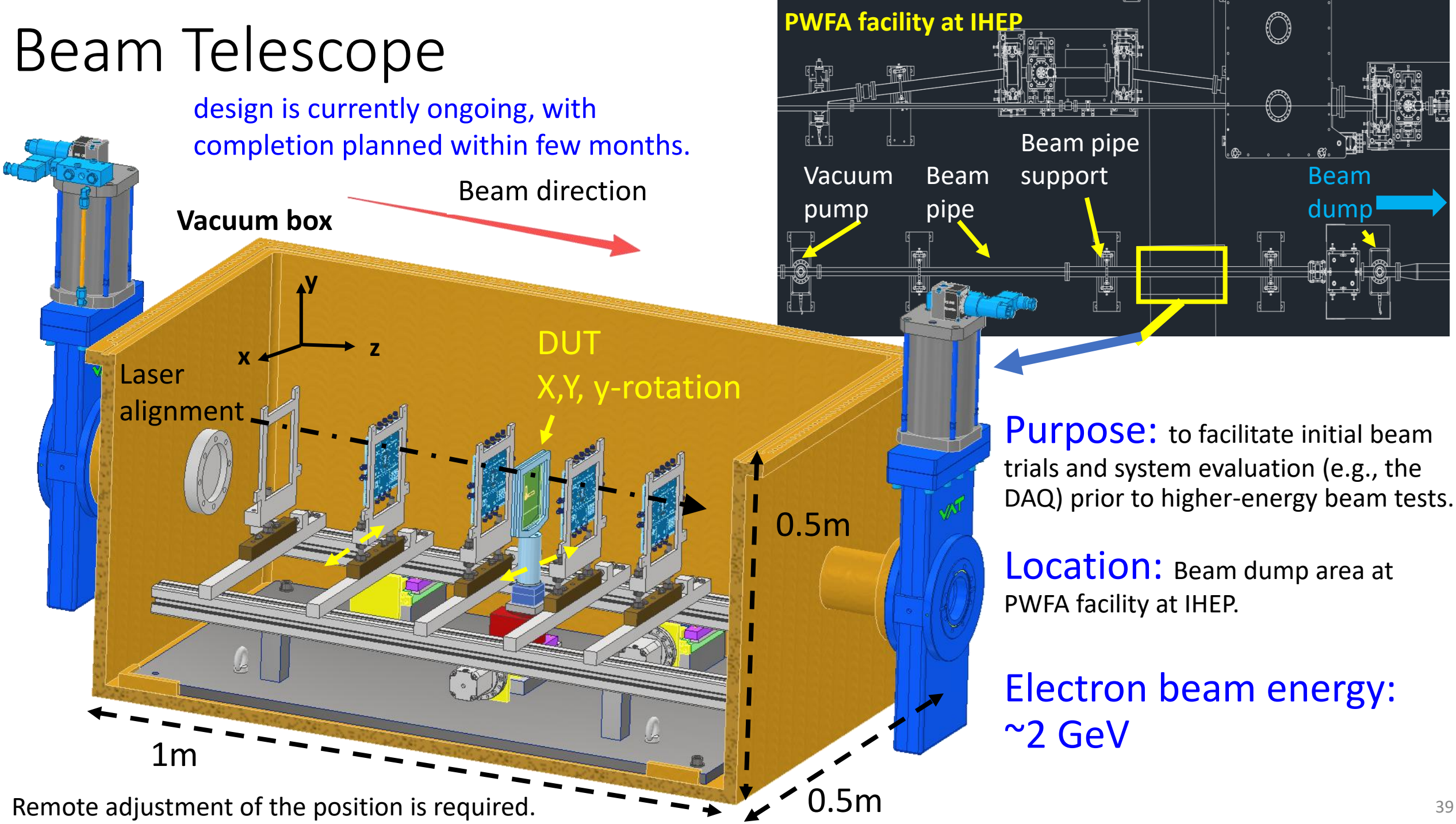
3) TOT



Achieving a spatial resolution below 10 µm using Time Over Threshold (TOT) information of LATRIC with a 100 µm strip pitch appears to be challenging and may offer limited flexibility.

Beam Telescope

design is currently ongoing, with completion planned within few months.



Purpose: to facilitate initial beam trials and system evaluation (e.g., the DAQ) prior to higher-energy beam tests.

Location: Beam dump area at PWFA facility at IHEP.

Electron beam energy: ~2 GeV

Remote adjustment of the position is required.