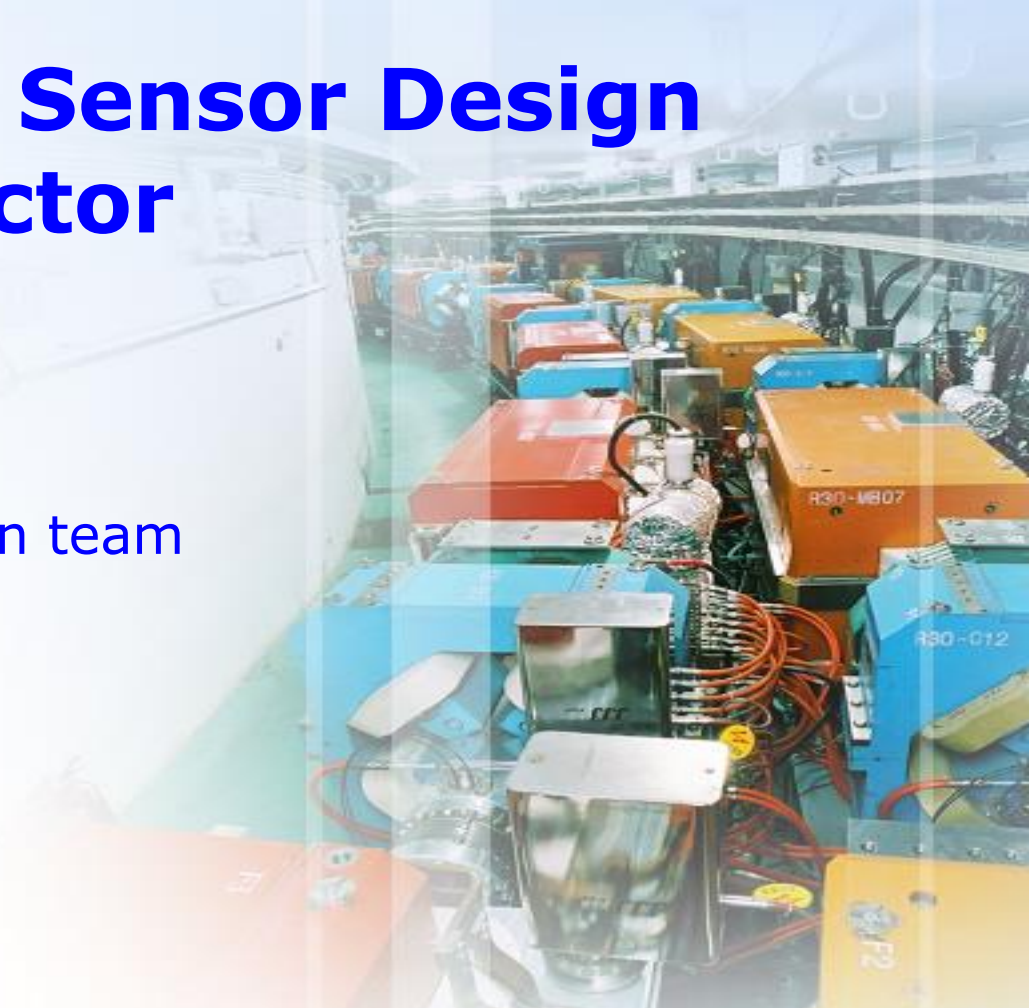
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Status Report on the Pixel Sensor Design for Vertex detector



Yunpeng Lu

On behalf of Vertex design team

2026/07/26

Vertex Specification

- CEPC Reference Detector(AGORA)
  - Spatial resolution < 5 um
  - Time stamp precision < 100 ns
  - Power Consumption < 40 mW/cm^2
  - Higgs & low-luminosity Z operation
  - Hit rate expected ~ 12 MHz/cm^2 (average)@ r_{min}=11 mm

Table 4.2: Vertex Detector Design Parameters

Parameter	Design
Spatial Resolution	~ 5 μm
Detector material budget	~ 0.8% X_0
First layer radius	11.1 mm
Power Consumption	< 40 mW/cm^2 (air cooling requirement)
Time stamp precision	100 ns
Fluence	~ 2×10^{14} Neq/cm^2
Operation temperature	~ 5 °C to 30 °C
Readout electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

Synergy with FCC-ee

- FCC-ee Vertex detector
  - **High-luminosity Z operation**
  - Average hit rate > 125 MHz/cm^2 @ r_{min}=11.7 mm
  - Average hit rate > 70 MHz/cm^2 @ r_{min}=13.7 mm
  - Single point resolution
  - Integration time
- CEPC-stitching design maximum readout speed up to 43.3 MHz per RSU
  - constrained by the RSU power 38 mW/cm^2

Projects for FCC-ee vertex detector, Dominik Dannheim
Detector background in vertex detector, Armin Ilg
@ **FCC week 2026, Helsinki**
Detector requirements for FCC-ee, E. Perez
@ **4th FCC Physics and Experiments Workshop, 2020**

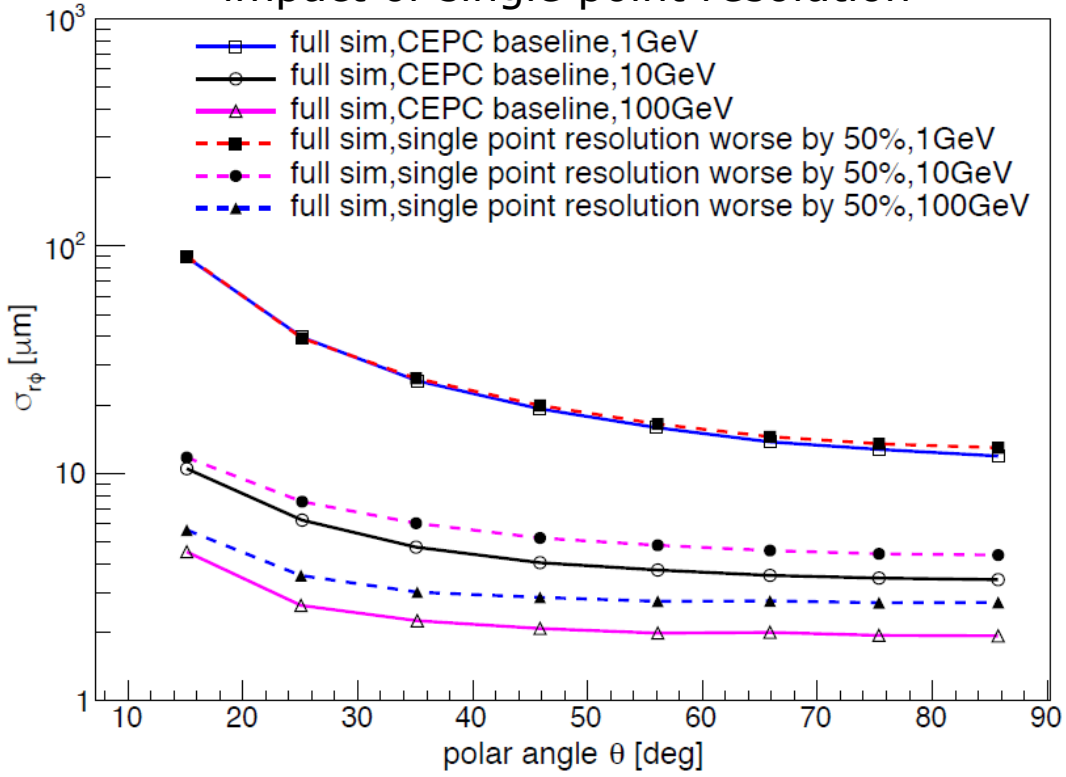
Table 4.9: Estimates of power consumption of one RSU. All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	Pixel Analog	Pixel Digital	Biasing Block	Matrix Readout	Data Interface	RSU Total
Power [mW]	36	30	8	40	17	131

Adaption to the FCC-ee requirement

- Keep CEPC-stitching design not changed
  - Increase r_{min} and lower hit rate for FCC-ee
  - Rectangular pixel → improve single point resolution at rφ direction < 3 um

impact of single point resolution



Assume
single point resolution = 3um

$$\sigma_{r\phi} = a \oplus \frac{b}{p(\,\mathrm{GeV})\sin^{3/2}\theta}$$

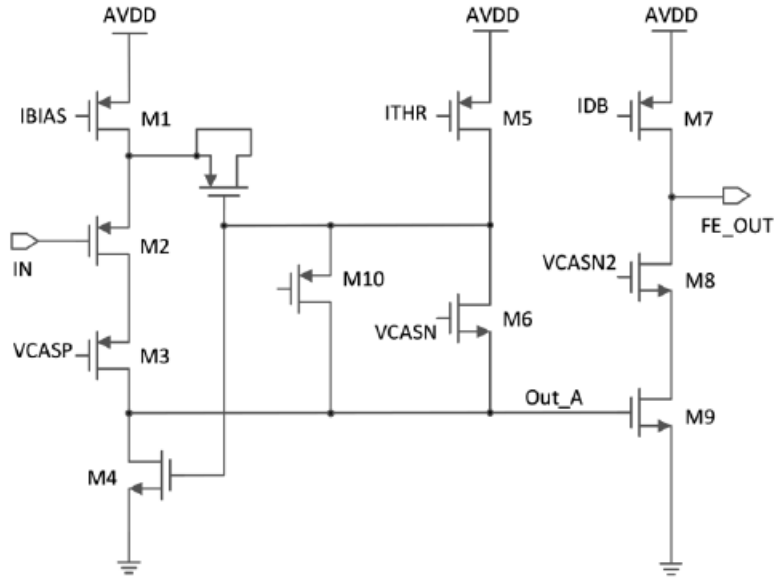
Bread down the specification

- Pixel pitch: 16 x 30 um
  - Analog front-end 16 x 16 um, pixel logic and readout 14 x 16 um
- Time precision: 100 ns (σ_t)
  - Dominated by time walk (analog frontend) + clock sampling (timestamp)
- Average power: Targeting < **40 mW/cm²** (Total power 64 mW) but design just started and not converged yet
  - Trying to reduce power budget for Analog Front-end and Matrix readout

Components	Pixel Analog	Pixel Digital	Biasing Block	Matrix Readout	Data Interface	Total
Power estimated from TDR [mW]	16.7	13.9	3.8	18.7	7.9	61
Current power budget [mW]	52	10	4	40	12	118

Tradeoff between Analog power and time walk

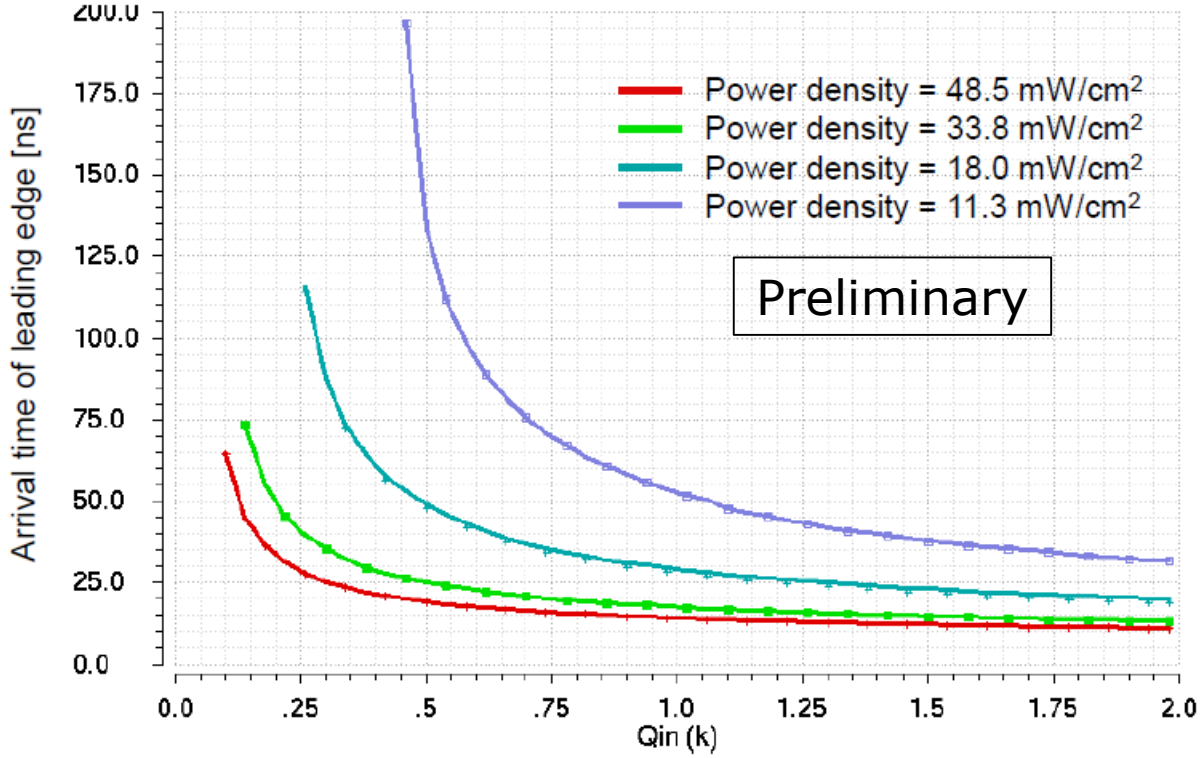
FE schematic



Power density [mW/cm^2]	Time-walk [ns]	Threshold [e$^-$]
64.3	37	~100
initial design point → 48.5	53	~100
33.8	60	~100
18.0	95	~240
Targeting → 11.3	165	~470

Simulation of Leading edge vs. charge

Ying Zhang



Time-walk: Time difference between the arrival time for Q2000 e$^-$ and Qth

Comparison of CIS technologies

- HC90L technology is cost-effective option with stitching combability
  - Power consumption of HC90L chip is expected to be similar to 55nm technology

Ying Zhang, Zhijun Liang

	Requirements	TPSCo 65 nm	HLMC 55 nm	Hynix HC90L
Feature size	55 – 90 nm	65 nm	55 nm	90 nm
Epitaxial layer thickness	10 - 25 μm	10 μm	3-5 μm	4 – 8.5 μm (default) Aiming to change to 20μm
Resistivity of epi-layer	> 1 kΩ•cm	High resistivity	Low resistivity ~10 Ω•cm	30-50 Ω•cm (default) Aiming to upgraded to 5kΩcm
Availability of deep N-well	Yes	Yes	Yes	Yes
Availability of deep P-well	Yes	Yes	Yes	Optional
Numbers of metal layers	> 6	Max. 7	Max. 5	Max. 5
Availability of stitching	Yes	Yes	Yes	Yes
Cost (NRE)		N/A	~6M RMB	2~3 M RMB

Pixel sensor process

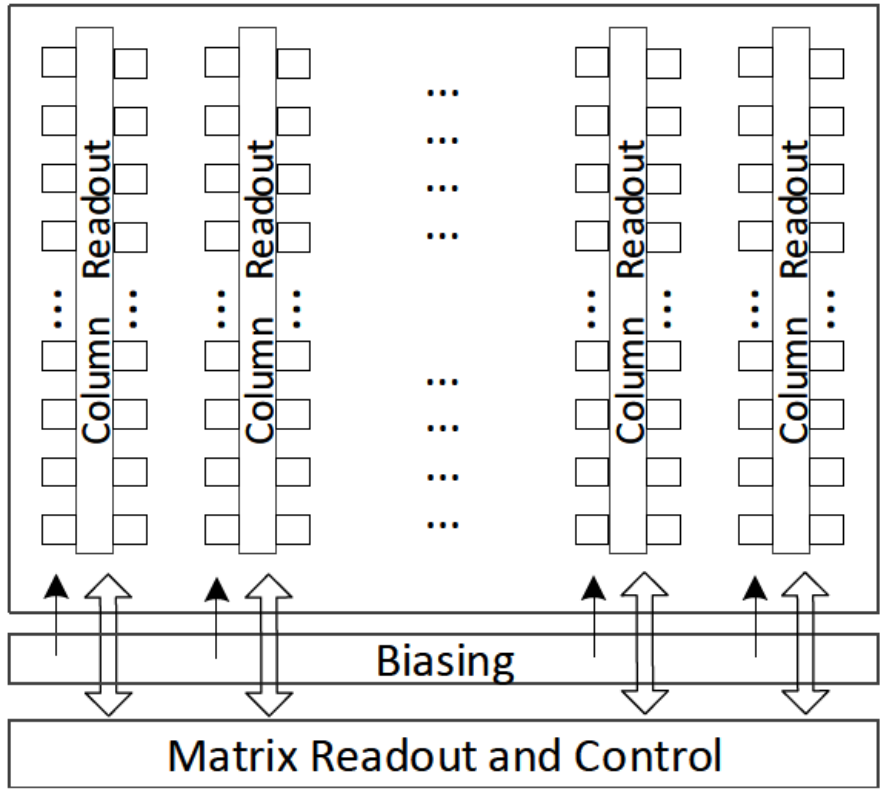
Ying Zhang, Zhijun Liang

- 90 nm HC90L process, domestic foundry
  - **Mature production line**
  - **Quadruple-well**
  - **Support High-resistivity epitaxial layer**
  - Custom implant not allowed yet, needed for high radiation hardness
- Contacting the foundry via an agent
  - PDK provided, 5 metal layers
  - Qualified HR wafers are under investigation
  - Engineering run only
  - Quotation will be provided based on the device choice

Design scheme of first submission

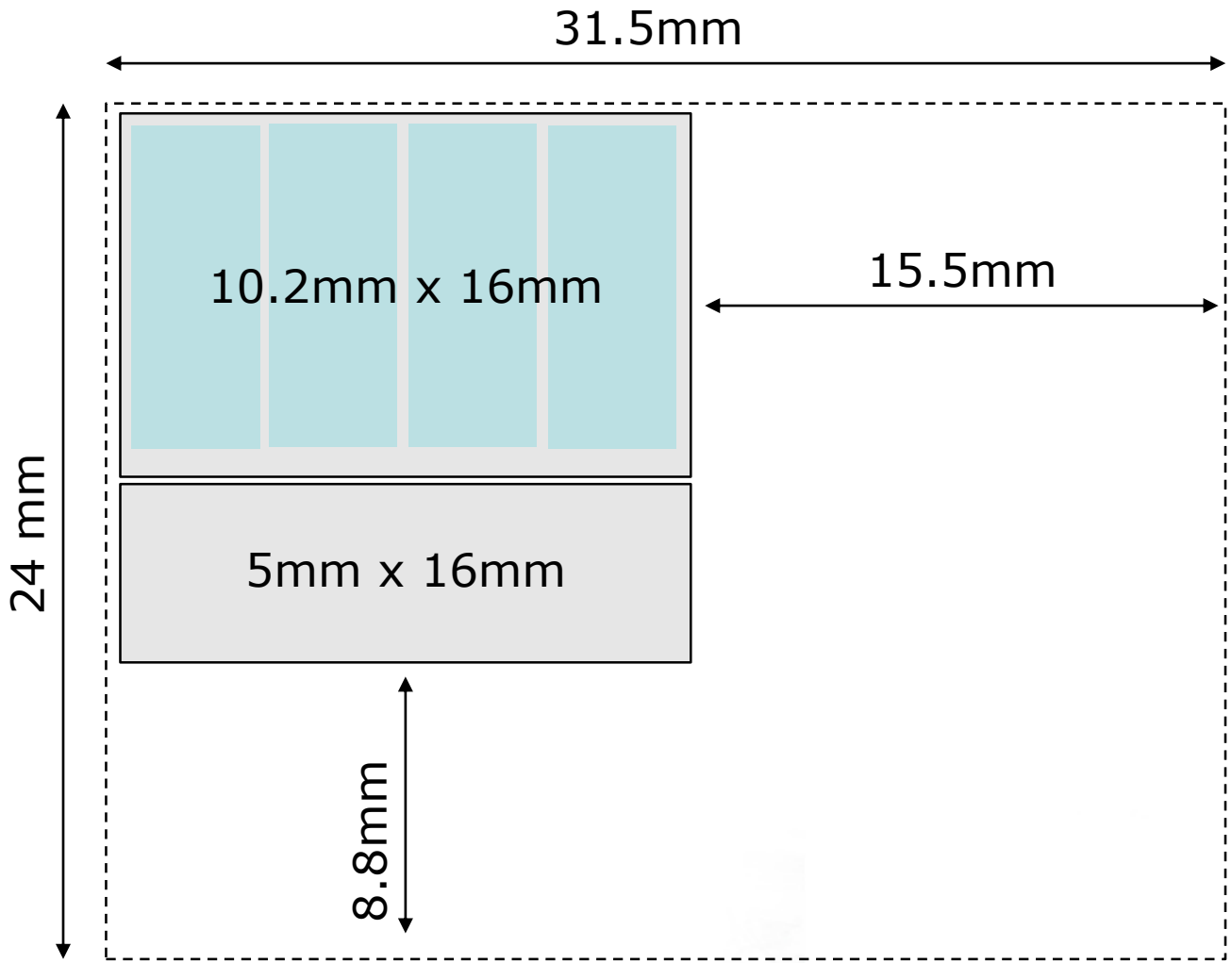
- Only Sensor Block for this submission
  - Compatible with the **Stitched sensor prototype design** (Reference Detector TDR)
- Readout out speed **per Sensor Block**
  - 160 M bit/s or 5 M Pixel hit/s
  - Background estimation = 3.8 MHz pixel hit/s (average)

Architecture of the Sensor Block



Preliminary floor plan

- Maximum Mask Area：24mm x 31.5mm
- Estimated design Area: 10.2mm x 16mm
  - Pixel pitch 16um x 30um
  - Matrix height 16um x 512行 = 8.192 mm
  - Matrix width 30um x 512列 = 15.36 mm
  - **4 sensor blocks**
  - Peripheral + Pad height 2mm
- Independent test circuit module
  - 5mm x 16mm
  - Mini-sensor for process verification
  - High speed data transmission
  - Others



Pixel Sensor Task Assignment

- Team members from the past TaichuPix and JadePix team

Task	Responsible person	Affiliation
Integration and verification	Yunepng Lu & Han Yu	IHEP
Process and analog front-end	Ying Zhang	IHEP
Matrix readout logic	Tianya Wu & Tong Li	NCU
Peripheral data readout	Xiaoming Wei & Student	NWPU
LVDS	Ping Yang & Student	CCNU
DAC	Ping Yang & Baoshu Hao	CCNU
Negative biased PAD	Ping Yang & Student	CCNU
Analog buffer	Hao Xiong	IHEP
PLL & Serializer & CML	Ping Yang & Quanwei Hu	CCNU
ASIC consultant	Wei Wei	IHEP
TCAD	Bo Liu, Ziying Liu, Ying Zhang, Zhijun Liang	NKU & IHEP

Key points of design

Items	Content	status
Analog front-end	TN，FPN，Time walk，power	on going
Logic analysis on FastOR signal	FastOR assertion and Freeze function	见郁晗报告
	FastOR desertion and readout debug	见邓思琪的分析
Understanding and definition of time stamp precision	Identify key contributor	见郁晗报告
peripheral readout	Timing, power and area optimization	in plan
Static power analysis on full chip	IR drop, leakage	in plan
Testability	Single module verification	in plan
	Avoid single-point failure in the signal chain	in plan

Not a full list of task

Schedule

- Tape-out in March 2027 (Preliminary plan, 9 months)
  - Scheme Design – 8 weeks, mid-July
  - Scheme Review – 1 week, late July
  - Module Design – 4 weeks, late August
  - Schematic Review – 1 week, mid-September
  - Layout Design – 8 weeks, mid-November
  - System Integration – 8 weeks, mid-January
  - Design Verification – 4 weeks, mid-February
  - Design Review – 1 week, late February
  - Submission – 1 week, early March
  - Tape-out in March 2027

Relevant task in MOST3

- TASK：Silicon pixel detector and Wireless data transmission technology
  - **Vertex detector prototype:** position resolution 3 um, time stamp precesion100 ns, power consumption 100 mW/cm^2
  - HVCMOS tracker prototype: position resolution 10 um, time stamp precesion10 ns, power consumption 200 mW/cm^2
  - Wireless data transmission: total data rate > 30 Gbps

Proposal of the design name

- Pixelated Resolution-Enhanced CMOS Imaging Sensor （PRECIS）
- Interpretation：
  - PRECIS: Derived from the English words "Precision" and "Precise", reflecting the ultimate pursuit of high precision in particle physics experiments.
  - Pixelated: Emphasizes the pixelated imaging capability.
  - Resolution-Enhanced: Highlights the advantage of high spatial resolution.
  - Advantages: Concise and clear; the name itself directly vouches for the detector's quality.

Thank you for your time!