

MicroTCA Tutorial

The backplane, PCI Express, Point-to-Point links

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Huairou, Beijing, China, 14.09.2026

Who am I?

- > FPGA Developer for MSK Group of DESY.
- > MicroTCA trainer at DESY.
- > PhD in Engineering and Applied Science for Energy and Industry.
- > Responsible for firmware the Laser Interferometer Space Antenna (LISA) mission.



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MicroTCA Training at DESY



Outline

Introduction

Components

- MicroTCA Carrier Hub (MCH)

- Advanced Mezzanine Card (AMC)

- AMC Backplane

Peripheral Component Interconnect Express (PCIe)

Point to Point links

Conclusions

What is MicroTCA?

- > Open-standard embedded computing specification by PICMG [1].
- > **Key focus:** Reliability, Availability, Serviceability.

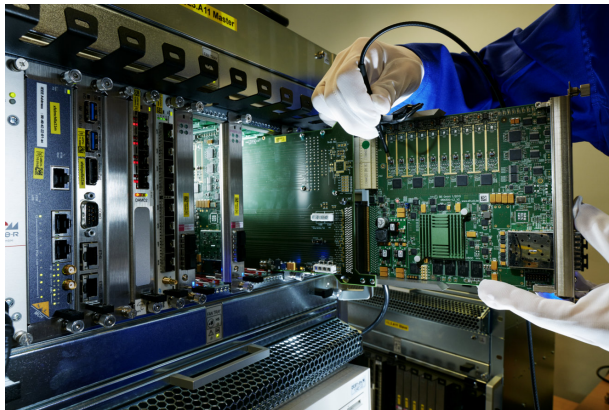


Figure: MicroTCA crate, from [2].

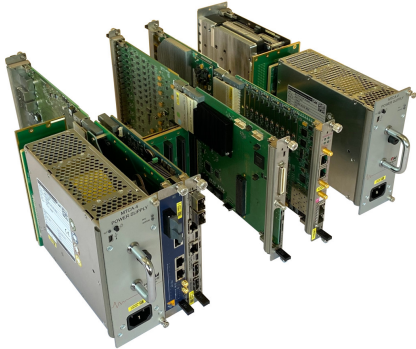
MicroTCA Crate

- > The MicroTCA crate is an enclosure that provides support to all the MicroTCA components.

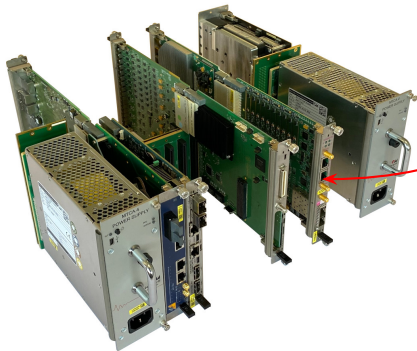


Figure: Example of MicroTCA chassis, adapted from [3].

What's inside the MicroTCA Crate?

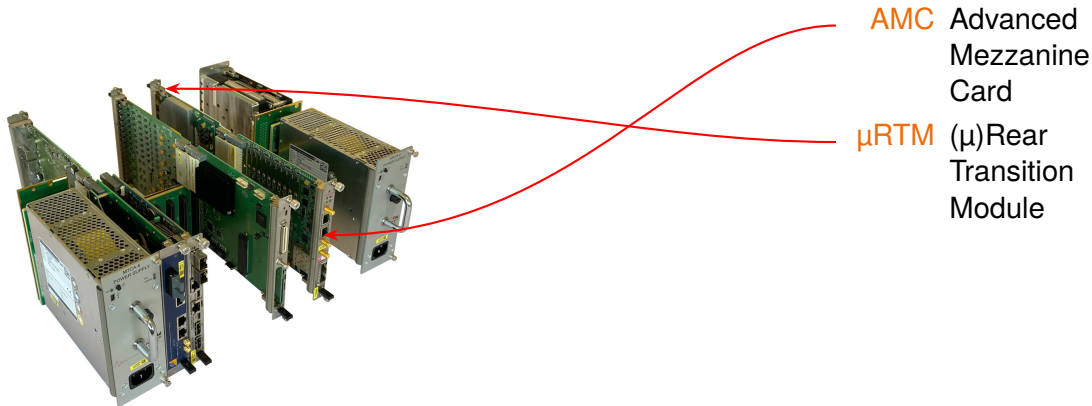


What's inside the MicroTCA Crate?

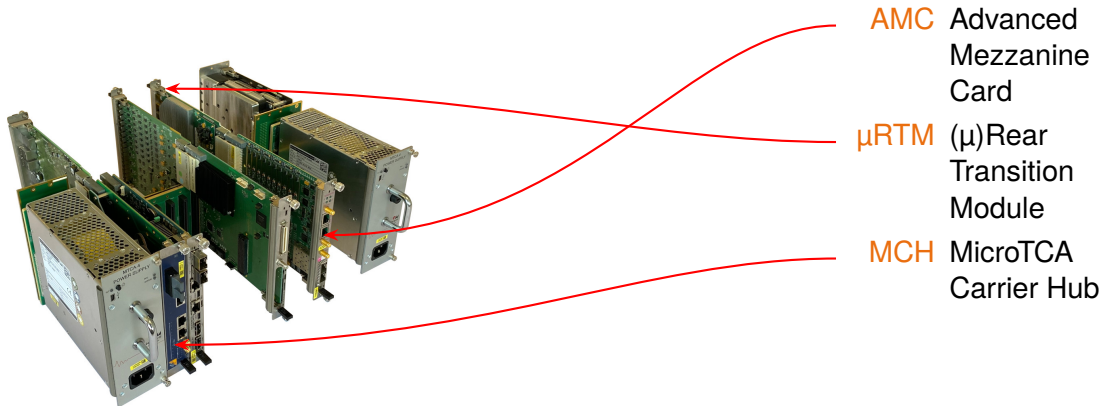


AMC Advanced
Mezzanine
Card

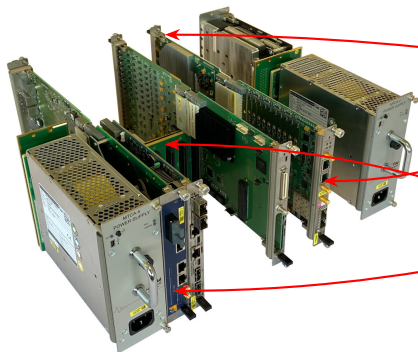
What's inside the MicroTCA Crate?



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What's inside the MicroTCA Crate?



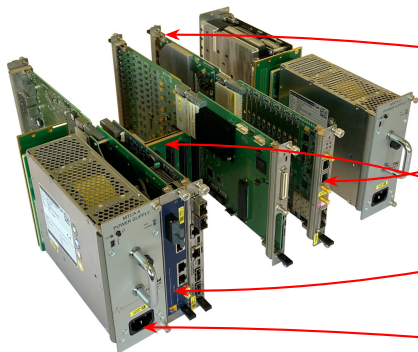
AMC Advanced Mezzanine Card

μRTM (μ)Rear Transition Module

MCH MicroTCA Carrier Hub

BP AMC Backplane

What's inside the MicroTCA Crate?



AMC Advanced Mezzanine Card

μRTM (μ)Rear Transition Module

MCH MicroTCA Carrier Hub

BP AMC Backplane

PM Power supply module

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MicroTCA Carrier Hub (MCH)

- > MicroTCA Carrier Hub (*MCH*) is the central management and switching unit of a MicroTCA chassis;
- > It can support up to 12 AMCs (can be redundant).
- > It provides:
 - **Distributes clocks** and synchronization signals across the chassis.
 - Acts as a **switch** for connections (Ethernet, PCIe, etc.), enabling AMCs to communicate.

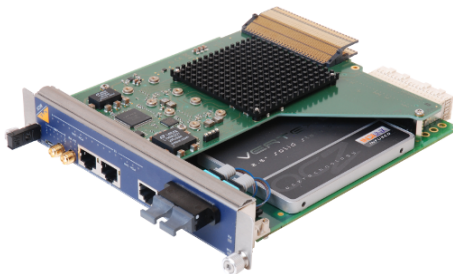
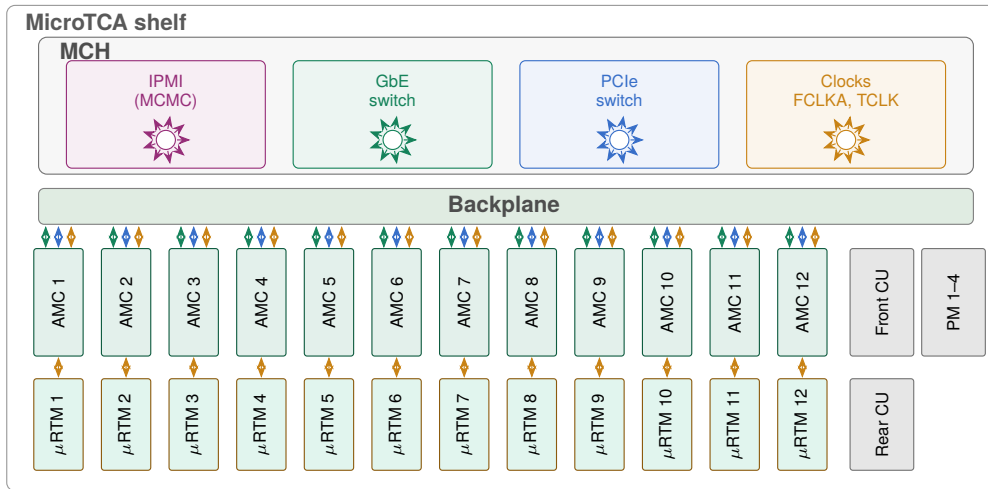


Figure: NAT MicroTCA Carrier Hub, from [4].

The MCH in the system



Advanced Mezzanine Card (AMC)

- > The *AMC* is a board that provides computing (CPU, FPGA), I/O (Ethernet, Optical links), or storage (SSD).
- > They connect directly to the crate's *backplane*.

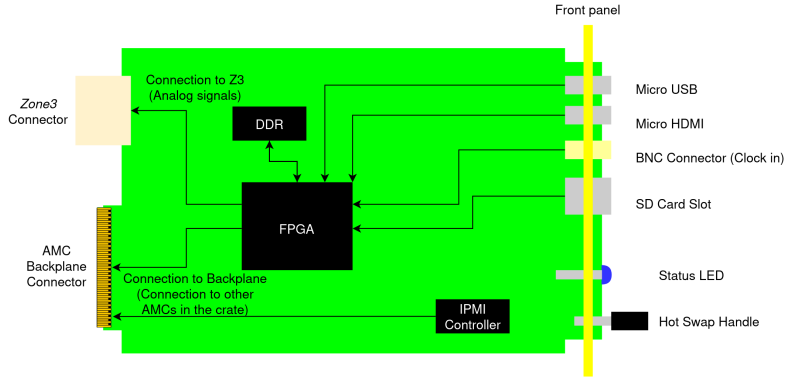


Figure: Simplified block diagram of an FPGA AMC.

AMC Connector and Backplane

- 170 pins grouped into ports.
- Protocols that can be seen on AMC Backplane.
 - Gigabit Ethernet
 - SATA
 - PCIe, SRIO, 10/40 Gbit Ethernet
 - Point-to-point links (Multi-Gigabit Transceiver)
 - Clocks
 - JTAG

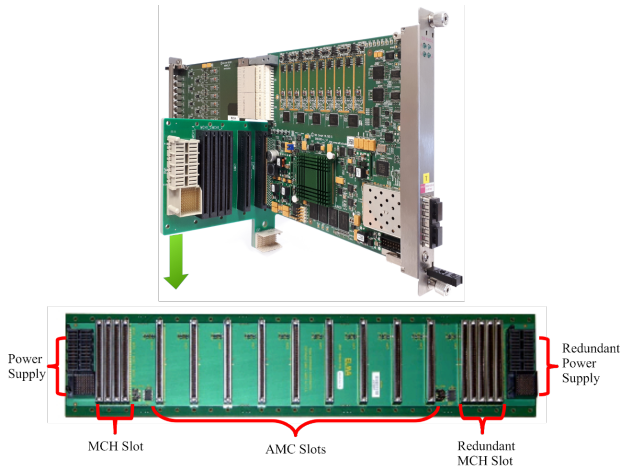


Figure: AMC connected to the AMC backplane.

AMCs in DESY's portfolio

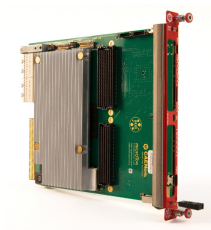


Figure: DAMC-FMC2ZUP [5].

- > Xilinx Zynq UltraScale+ MPSoC;
- > 2 FMC slots (one FMC+ and one standard FMC slot);
- > PCIe x4 Gen. 3 support (x8 option in appropriate chassis).

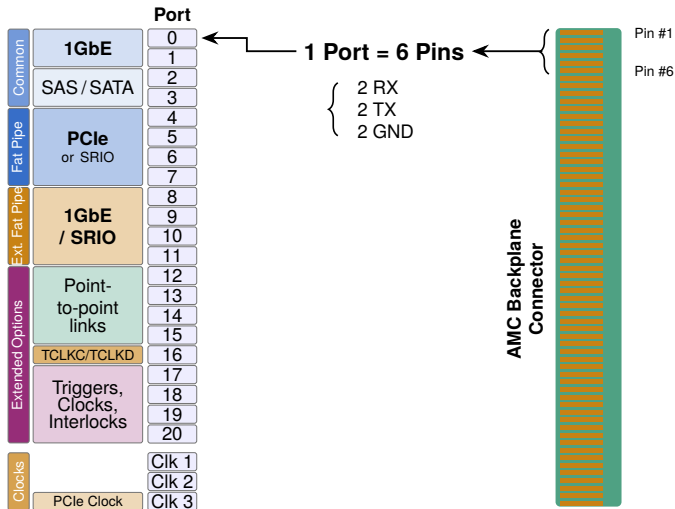


Figure: DAMC-FMC1Z7IO [6].

- > Xilinx Zynq-7000 SoC;
- > 1 FMC slot;
- > 48 bidirectional I/Os;
- > Micro HDMI display controller;
- > SMA connector for external clock input.

AMC Connector and its ports

- > **Common Ports** : 1GbE, SATA (storage communication).
- > **Fat Pipe** : **PCIe** or Serial RapidIO (SRIO).
- > **Extended Fat Pipe** : 1 Gigabit Ethernet (GbE), Serial RapidIO (SRIO).
- > **Extended Options** : Point-to-Point Links, Triggers, Clocks and Interlocks.
- > **Clocks** : PCIe Clock.



Example backplane

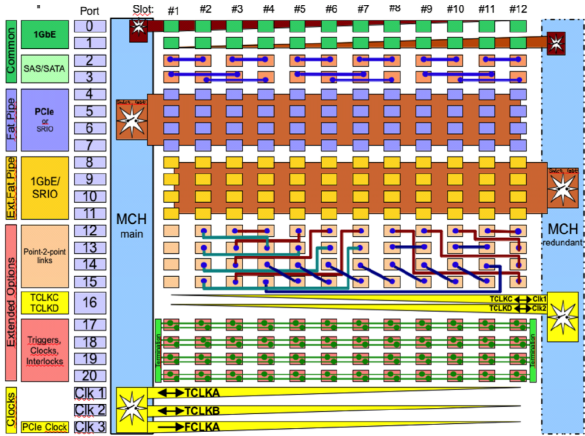
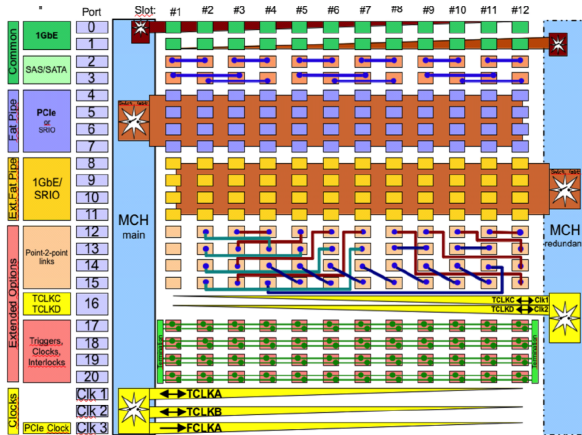


Figure: Example of a backplane topology, from [7].

Example backplane



Check before you design

- Slot-to-slot wiring is **fixed**.
- AMC 3 ↔ AMC 5? Only if the routing table says so.

Figure: Example of a backplane topology, from [7].

PCIe communication in the MicroTCA crate

- > Every AMC gets its own point-to-point link to the switch.
- > PCIe reference clock shared.

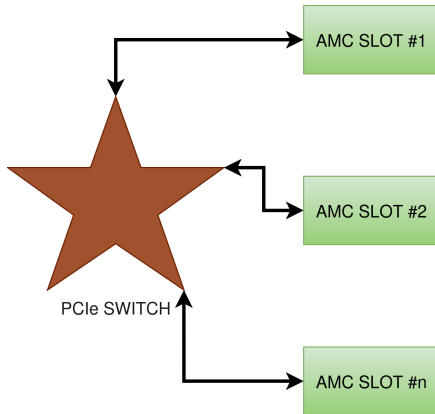
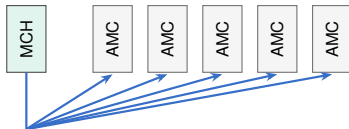


Figure: PCIe Switch connected to multiple slots.

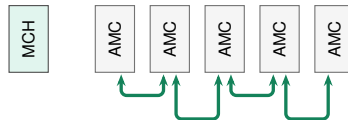
One backplane, four independent fabrics

1. High-speed serial interfaces ports 0–11



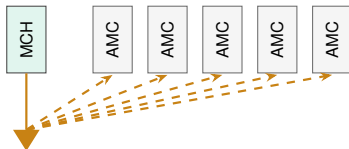
Star: every slot gets its own link to the switch
GbE (0–1), PCIe (4–7), 1GbE (8–11)

2. Point-to-point ports 12–15



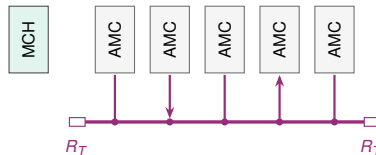
Slot to slot, the **MCH is not in the path**
pattern is **fixed** when the backplane is manufactured

3. Clocks FCLKA, TCLKA–D



Radial fan-out: 100 MHz PCIe reference clock, one dedicated pair per slot

4. Triggers + interlocks ports 17–20



M-LVDS bus: any AMC can drive, all the others listen
Terminated at both ends, no switch.

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What is PCIe?

0–1 1GbE

4–7 PCIe

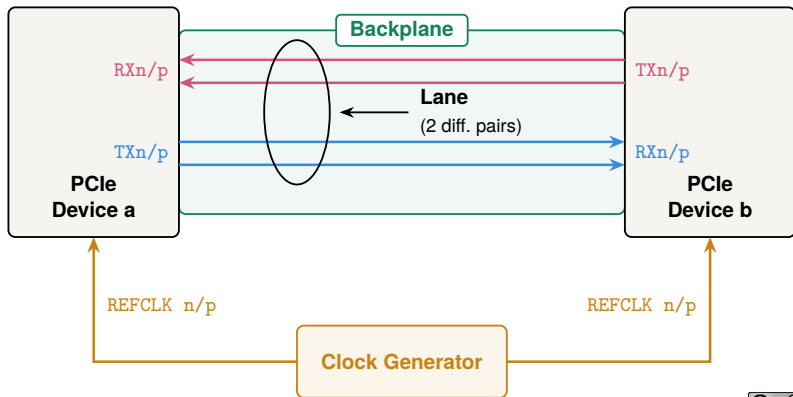
8–11 1GbE/SRIO

12–15 point-to-point

17–20 trig/clk/interlock

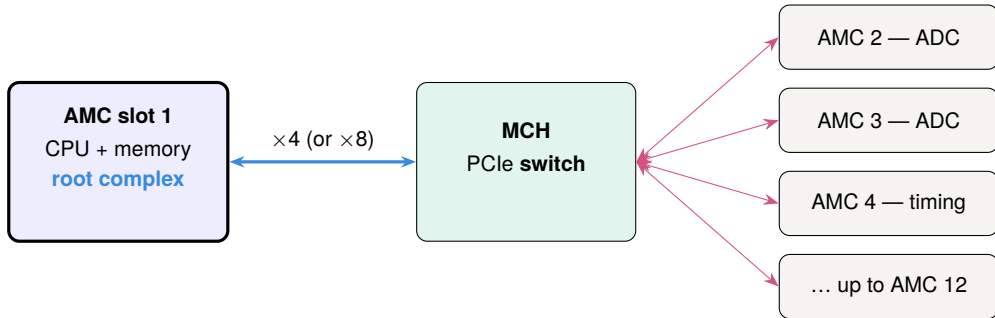
Clk clocks

- > Packet-based protocol.
- > PCIe employs a **switch** directing multiple point-to-point serial links.
- > Each link is a set of full-duplex differential pairs called **lanes**.
- > **Link width** ($\times 1 \dots \times 16$) = how many lanes are wired. In MicroTCA: $\times 4$ (or $\times 8$) on ports 4–7 (or 4–11).



PCIe topology in a MicroTCA crate

One root complex, one switch, many endpoints



×4 (or ×8) to each slot

- > The **root complex** lives on a **processor AMC** (generator/destination of the packets).
- > The **MCH is a switch**, it forwards packets to the endpoints.
- > The MCH also fans out FCLKA, the 100 MHz reference clock, to every slot: common-clock architecture across the backplane.

PCIe generations and MicroTCA support

Gen	Raw rate	Per lane	×4 fat pipe
1	2.5 GT/s	250 MB/s	1.0 GB/s
2	5.0 GT/s	500 MB/s	2.0 GB/s
3	8.0 GT/s	985 MB/s	3.9 GB/s
4	16 GT/s	1.97 GB/s	7.9 GB/s
5	32 GT/s	3.94 GB/s	15.8 GB/s

Gen3 and 5

Per direction, full duplex. Line rate before Transaction Layer Packet overhead: expect 85–90 % in practice.

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What are Point to Point links

- > Offer direct communication from AMC to AMC.
- > Each link is a set of full-duplex differential pairs.

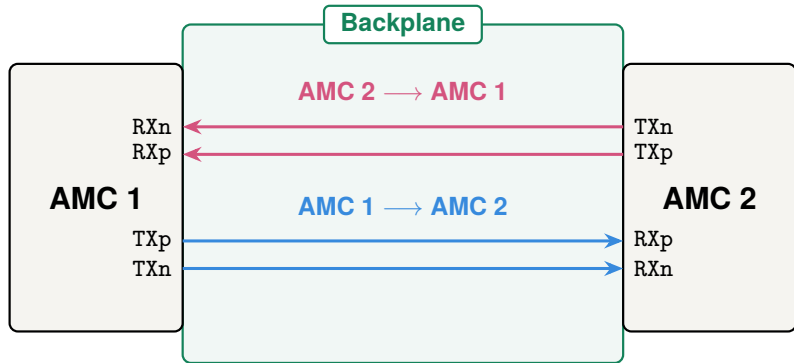


Figure: Point to point link communication between 2 AMCs.

Overview of protocols

Use of point-to-point links is **application specific**. Several protocols can be used:

Aurora

- Xilinx protocol [8].
- Low latency.

Gigabit Ethernet

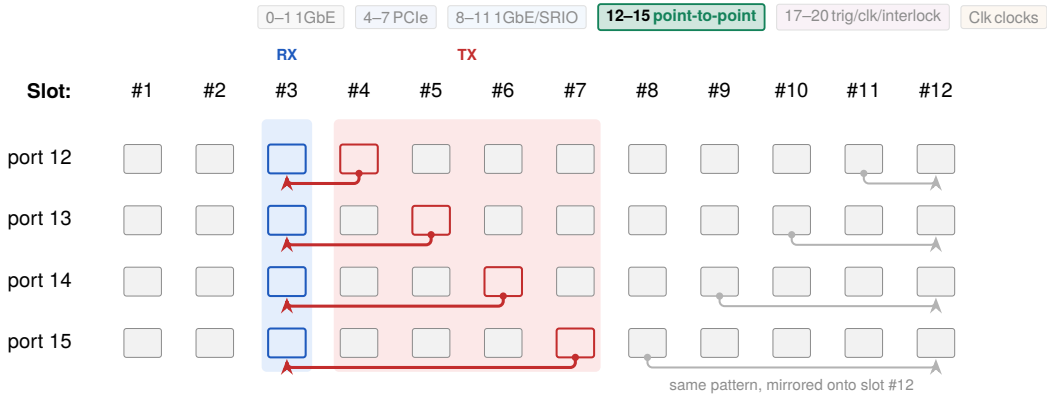
- Easy to interface to PCs.

10 Gigabit Ethernet

- Signal integrity might be an issue on some backplanes.

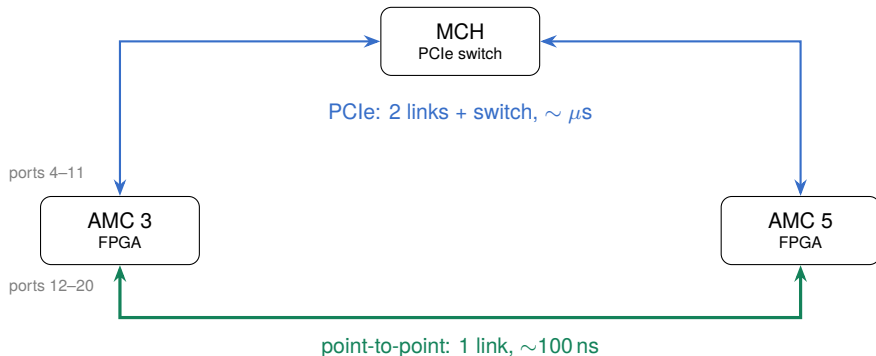
Custom protocols

Point-to-point links: one receiver, four senders



Slot #3 uses **all four** of its point-to-point ports, one per sender. Each link is a direct pair of traces: no switch, no CPU. (Links are full duplex; the arrows show the data flow of **this** application.)

Why not just use the PCIe fabric?



The fabric is flexible and standard; the direct link is fast and deterministic. Backplane wiring for the lower path is **fixed at manufacture**.

Why not just use the PCIe fabric?

	PCIe via the MCH	Direct point-to-point
Path	AMC → switch → AMC	AMC → AMC
Latency	~ μ s round trip	~100 ns one way
Topology	any slot, via switch routing	fixed by backplane wiring
CPU	needed	not involved
Protocol	standard, OS support	you write both ends

Point-to-point wins on latency and determinism; PCIe wins on flexibility and tooling.

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- > The **crate** hosts up to 12 AMCs, all tied together by the **backplane**.
- > The **MCH** is the central hub: it distributes clocks and switches the fabric traffic between AMCs.
- > The **AMCs** carry the payload, FPGA, CPU, I/O or storage, and plug straight into the backplane.

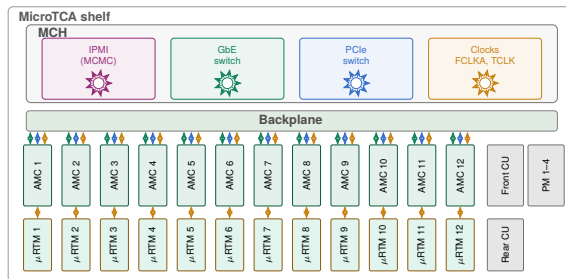


Figure: The MCH supervises every device and provides the PCIe and GbE switches.

Conclusions

- > The backplane interconnects the AMCs.
- > **PCIe via the MCH**: one switch, many endpoints.
- > **Point-to-point links**: fixed backplane wiring, no CPU.
- > Rule of thumb: PCIe for control and configuration, point-to-point for low-latency deterministic data.

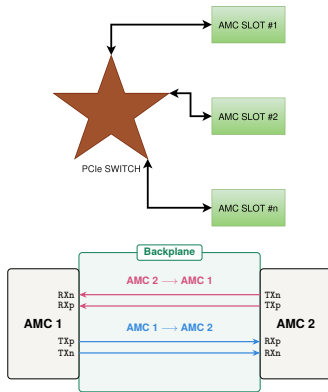


Figure: Top: PCIe star through the MCH. Bottom: direct point-to-point links.

Thank you!

Contact

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<https://cagil-gumus.github.io/>

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[6] Deutsches Elektronen-Synchrotron (DESY).

DAMC-FMC1Z7IO — AMC FPGA board with Zynq-7000 and one FMC slot.

https://innovation.desy.de/technologies/microtca/boards/damc_fmc1z7io/index_eng.html.

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Outline

Backup

Triggers and interlocks

Clocks and timing

MCH Examples from the Industry - N.A.T

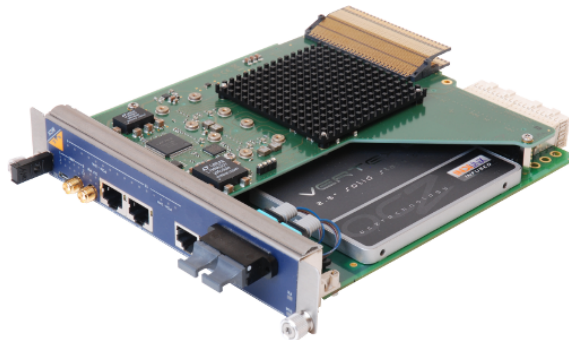
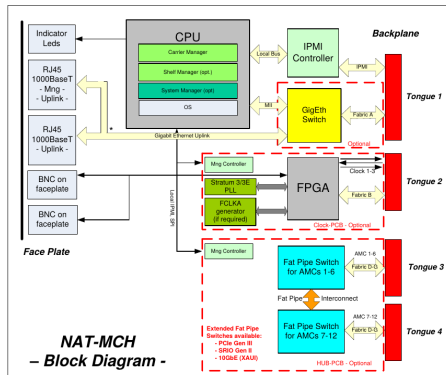


Figure: Block diagram of the PHYS080 MCH by N.A.T, from [4].

Figure: PHYS080 MCH by N.A.T, from [4].

What is PCIe?

0–1 1GbE

4–7 **PCIe**

8–11 1GbE/SRIO

12–15 point-to-point

17–20 trig/clk/interlock

Clk clocks

- > Packet-based protocol.
- > A **rooted** tree: one root complex, switches fan out to endpoints.
- > Memory-mapped: each device gets a window in the CPU's address map, assigned during enumeration.

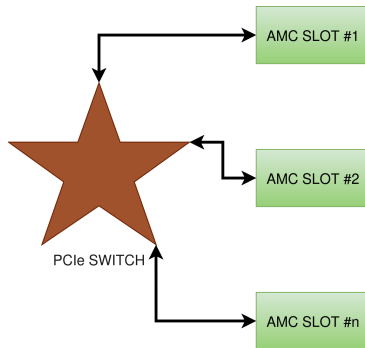


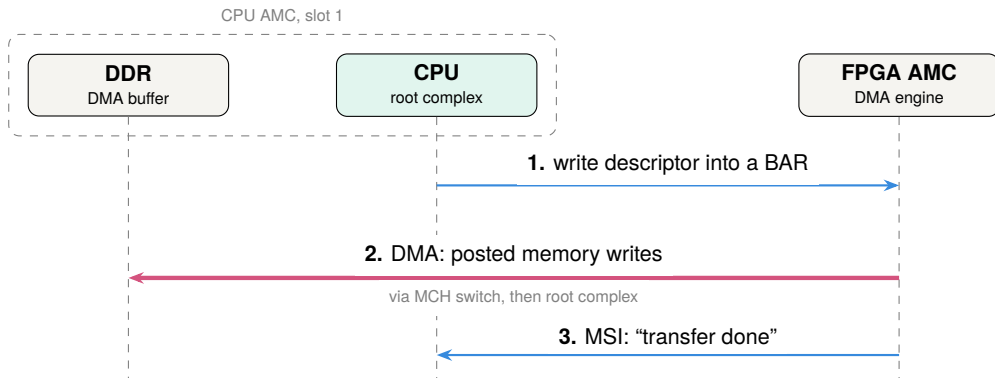
Figure: PCIe Switch connected to multiple slots.

The device tree as software sees it

```
bus 00 root complex
|
+- 00:1c.0 root port      -> bus 01
|
+- 01:00.0 switch up -> bus 02
|
+- 02:01.0 down  -> bus 03
|   +- 03:00.0  AMC 2
+- 02:02.0 down  -> bus 04
|   +- 04:00.0  AMC 3
+- 02:03.0 down  -> bus 05
|   +- 05:00.0  AMC 4
```

- > Each device has an ID:
bus:device.function.
- > Enumeration is done by **software on the CPU**, via the root complex. The switch only forwards the config packets.

How data actually moves, typical use case



- > “Host RAM” is the **DDR on the processor AMC**, behind the root complex.
- > The buffer then sits in DDR: the CPU reads it with no PCIe traffic at all.

Outline

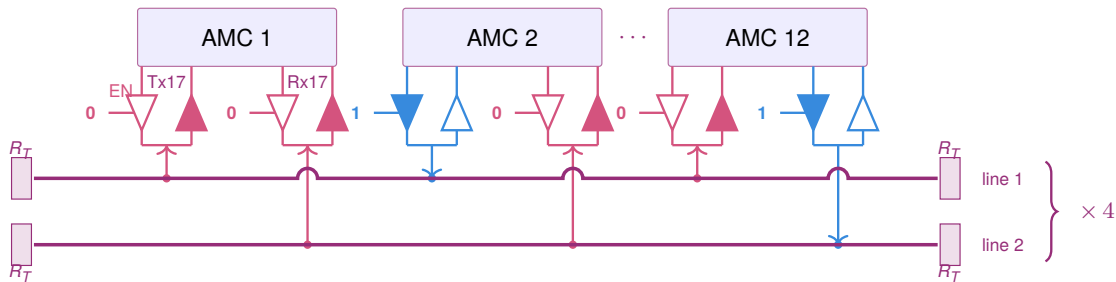
Backup

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Multipoint-LVDS bus in the MicroTCA backplane

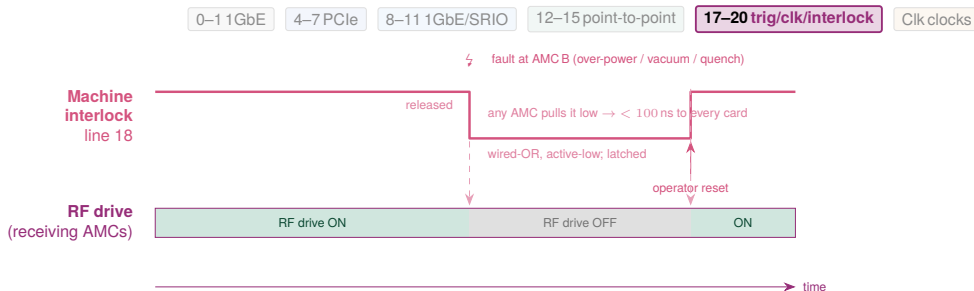
0-1 1GbE 4-7 PCIe 8-11 1GbE/SRIO 12-15 point-to-point **17-20 trig/clk/interlock** Clk clocks



▼ **transmitting:** EN = 1, driver drives the pair ▲ **receiving:** EN = 0, driver high-Z, receiver always connected

- Ports 17–20: Tx and Rx pair of each port bussed **separately**, terminated at both ends.
- One card per line with **EN=1**, every other driver **EN=0**.
- State is per **line**, not per card: AMC 12 listens on line 1 while it drives line 2.

Use case: machine-protection interlock



- > **Machine interlock (line 18):** active-low line. Every AMC watches it and any AMC may drive it low.
- > On a fault (over-power, vacuum, quench, ...) the faulting AMC pulls the line low; every **receiving** AMC sees the asserted level within < 100 ns and switches its RF drive off.

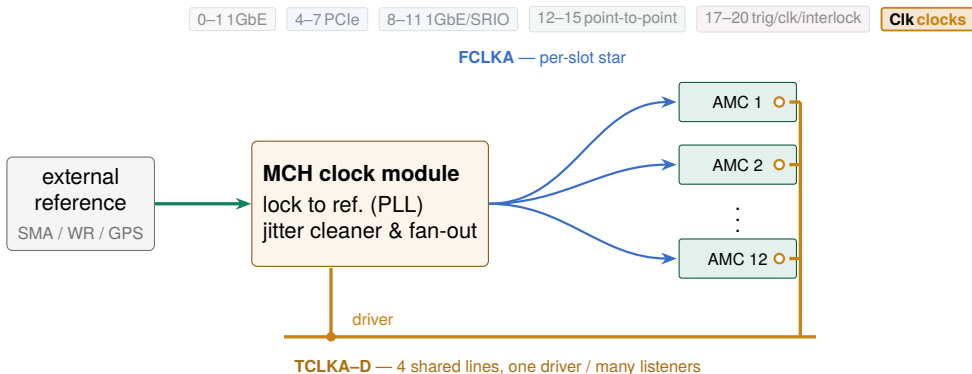
Outline

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Triggers and interlocks

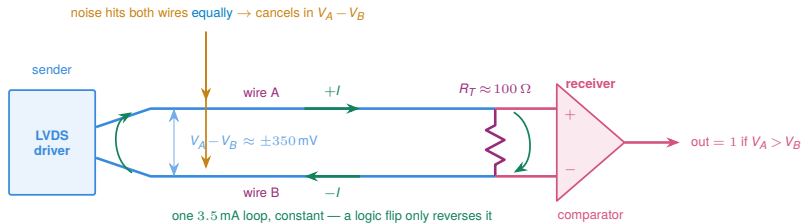
Clocks and timing

Clock distribution in the MicroTCA backplane



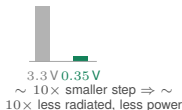
- > **FCLKA**: per-slot star, the 100 MHz PCIe reference $\Rightarrow$ PCIe runs in **common-clock** mode.
- > **TCLKA-D**: four shared backplane lines, one driver / many listeners (like the trigger bus).

What is LVDS?

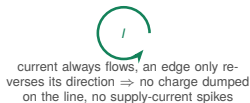


Why LVDS is low-EMI and low-power

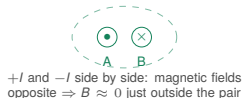
1. Small swing



2. Current steered, not switched



3. Tight pair cancels the field



> **LVDS = Low-Voltage Differential Signalling:** the bit is the **difference** $V_A - V_B$ between two wires, not a level against ground; the receiver is just a comparator, so common-mode noise cancels.

> **M-LVDS** (ports 17–20) is the multipoint variant: many drivers and receivers on one terminated bus.

Working with the backplane clocks

- > The MCH clock module **locks to and cleans** the incoming reference (jitter-cleaner PLL) before fanning it out; cascaded fan-out buffers still add jitter, so keep a budget.
- > Direction and source of each **TCLK** line are set through **MCH management** (like configuring the fabric) — and, as on the M-LVDS bus, only **one** driver per line.
- > Typical use: feed the accelerator RF reference (or a revolution clock) in on TCLKA; every AMC PLL-locks its ADC/DAC clock to it $\Rightarrow$ a deterministic phase between all converters in the crate.
- > **MTCA.4** adds precision clock and trigger distribution through Zone 3 / the μ RTM, and **White Rabbit** for sub-ns synchronisation between crates.

Rule of thumb: FCLKA for the fabric, TCLK for the application; if phase between boards matters, it comes from a backplane clock, not from software.

Glossary

AMC Advanced Mezzanine Card

MCH MicroTCA Carrier Hub

MicroTCA Micro Telecommunications
/ μ TCA Computing Architecture (PICMG
standard)

PICMG PCI Industrial Computer
Manufacturers Group
 μ RTM / (Micro) Rear Transition Module
RTM

Zone AMC edge: power+mgmt / fabric /
1/2/3 (MTCA.4) RTM connector

PM Power Module

CU Cooling Unit

FMC FPGA Mezzanine Card