

Low-Level RF Systems Implementation and Integration Based on MicroTCA.4

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LLRF Introduction

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**MTCA.4 LLRF
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3

**Build a real MTCA.4
system**

4

**FPGA Framework
& Software Implementation**

01

LLRF Introduction

LLRF System

■ Low Level Radio Frequency

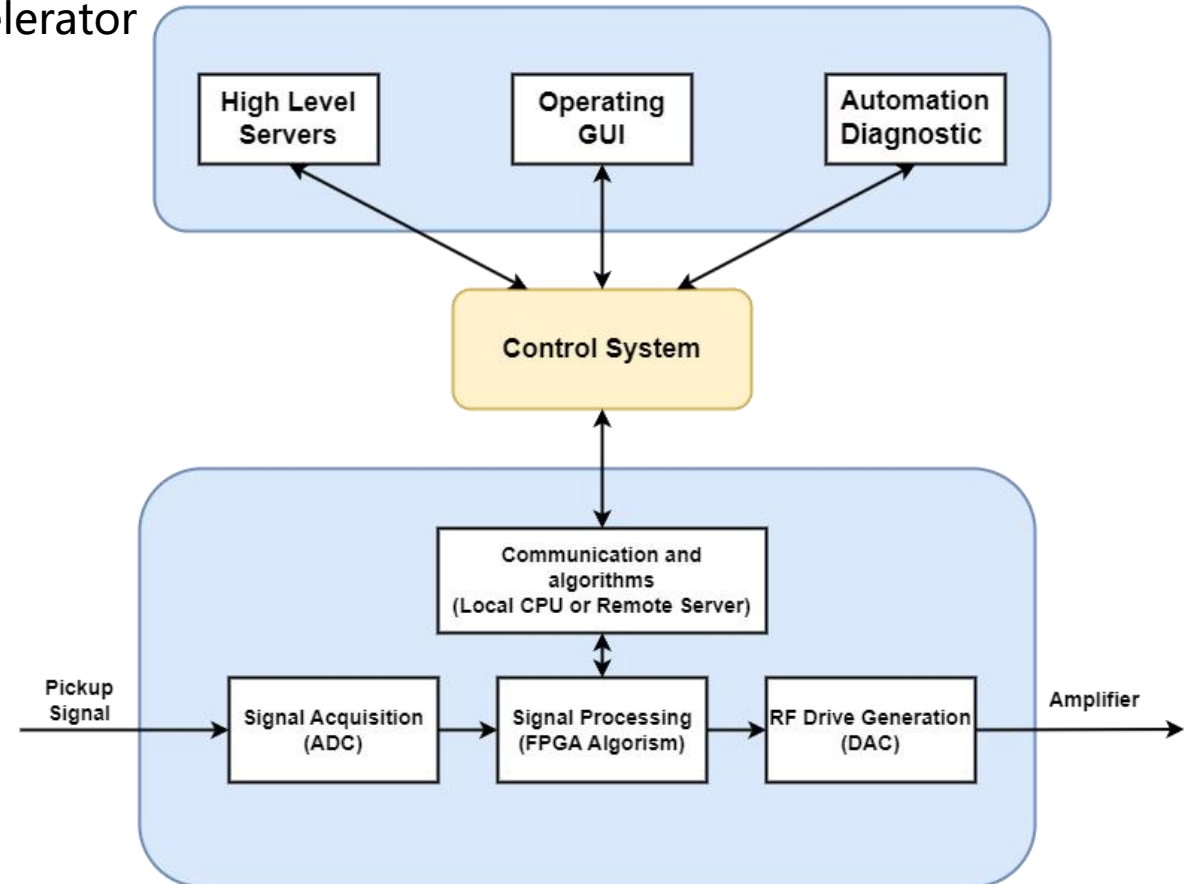
- Regulates the amplitude and the phase of the accelerating voltage inside a RF cavity is essential to ensure the stable operation of charged particle accelerator

■ Basic requirements:

- Cavity Field Control (RF loops)
- Cavity Resonance Control (frequency loops)
- High speed data acquisition
- Built-in system diagnosis
- Automation commission
- Exception handling procedures

■ System Architecture:

- Pizza box: custom-developed and purpose-built hardware
 - Crate-based: High modularity and scalability
- Conform to some standards or protocols



Motivation for MicroTCA.4

■ Limitations of VME/CPCI/PXI:

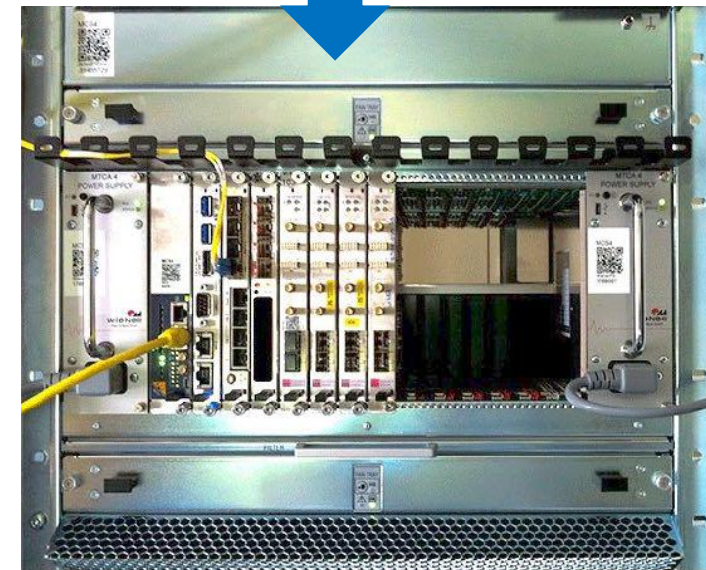
- Low bus bandwidth
- Lack of support for serial fabrics
- Insufficient intelligent platform management

■ Requirements in the High-Energy Physics

- High data rate
- Scalable modular architecture
- Shelf management and monitoring
- Redundancy
- Hot swap capability

■ Evolved from ATCA/MTCA

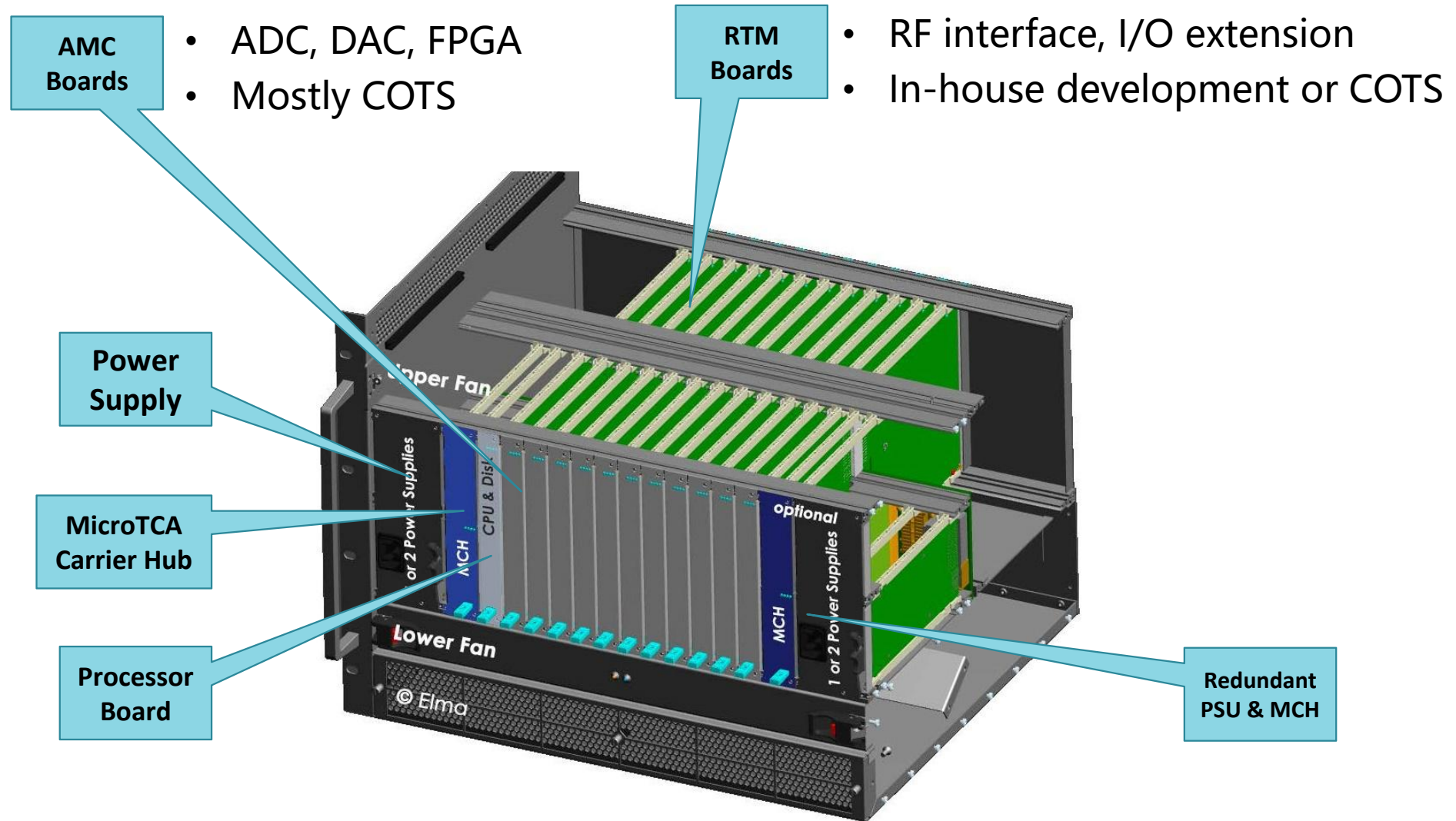
- Modern, high-speed data transfer
- Redundant fans/power supply
- Intelligent platform management
- Excellent signal quality
- Internal clock & trigger distribution



02

**MTCA.4 LLRF
System Hardware**

MTCA.4 LLRF: Overview



Chassis selection



1U Chassis

- Integrated eMCH
- 2-slot Double Mid-Size AMC w/ RTM
- 2-slot Single Mid-Size AMC
- Integrated DCU



3U Chassis

- 4-slot Double Mid-Size AMC w/ RTM
- 1-slot Double Mid-size AMC
- 1-slot Double Full-size MCH
- 2 Double Full-size PM



2U Chassis

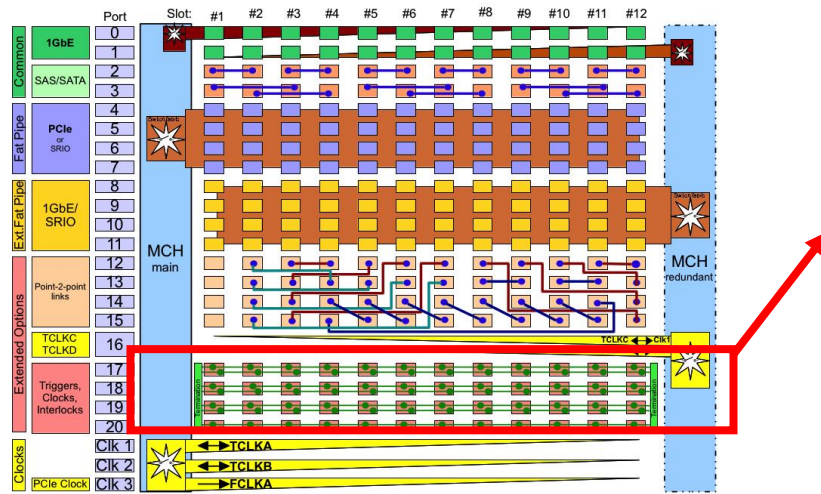
- 5-slot Double Mid-Size AMC w/ RTM
- 1-slot Double Full-size AMC
- 1-slot Double Full-size MCH w/ RTM
- 1 Double Full-size PM



9U Chassis

- 12-slot Double Mid-Size AMC slots w/ RTM
- 2-slot Double Full-size MCH w/ RTM
- 4 Double Full-size PM

Backplane Connections



MLVDS

- Shared across all slots
- 200Mbps max
- Triggers, interlocks, clocks, ...
- Usually one transmitter and multiple receivers
- Example: interlock and trigger interconnect between digitizer, EVR or interlock board



mTCA-EVR-300U

Timing
Trigger



SIS8300L2

MPS
Interlock



DAMC2

Backplane Connections

■ Digital I/O AMC in the IHEP LLRF System

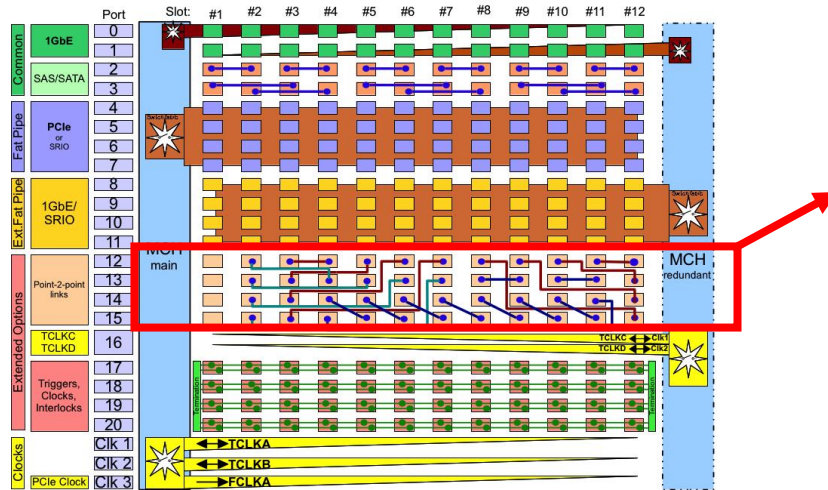
A multi-channel digital signal input/output AMC module compliant with the MTCA.4 standard, primarily designed for Low-Level RF (LLRF) systems to manage timing distribution and interlock signal fan-out.



Key Features:

- **Form Factor:** Dual-width MTCA.4 AMC module
- **Electrical I/O:** 8-channel digital signal input/output with configurable direction
- **Optical I/O:** 2-channel optical signal input and 2-channel optical signal output
- **Backplane Interface:** M-LVDS fan-out via backplane
- **Management:** Integrated MMC management module, Voltage, current, and temperature monitoring
- **Flexibility:** Configurable input/output impedance

Backplane Connections



Point-to-point links

- Direct communication between boards, used for data aggregation
- Protocol selection depends on application: Aurora, 8b/10b, (10)Gigabit Ethernet
- Example: Data exchange between master LLRF controller and multiple slave superconducting cavity resonance controllers



Processing Board

Data
Processing



Digitizer

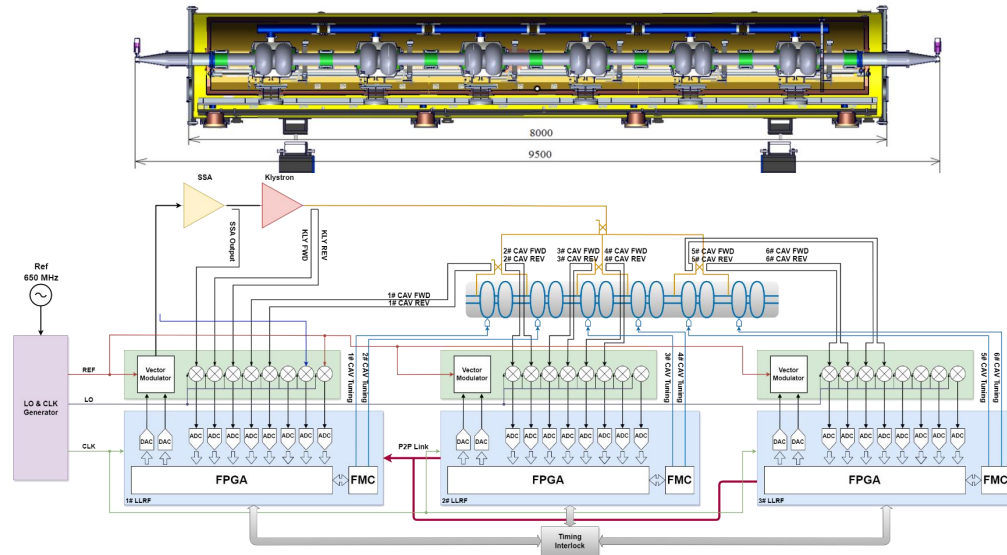
Cavity
Tuning



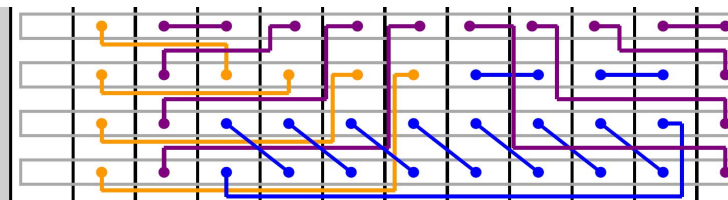
FMC Carrier

Backplane Connections

■ LLRF system for CEPC EDR Full-scale 650 MHz cryomodule

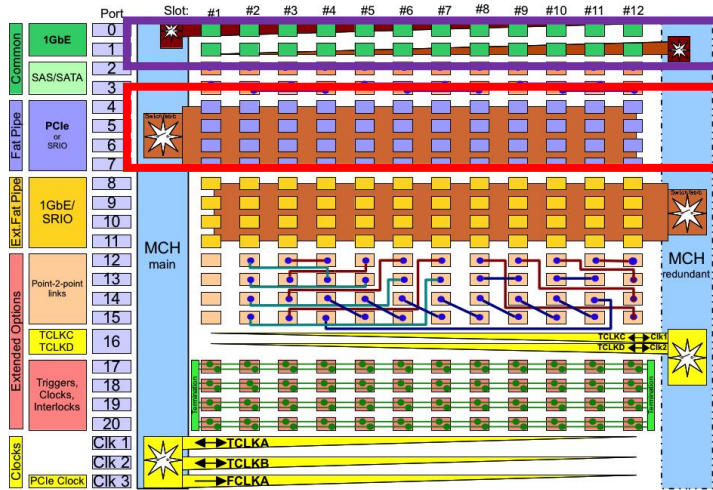


AMC Port 12
AMC Port 13
AMC Port 14
AMC Port 15



- Simplify the system architecture while ensuring high performance, flexibility and reliability
- Different topologies: Daisy Chain, Concentrator

Backplane Connections

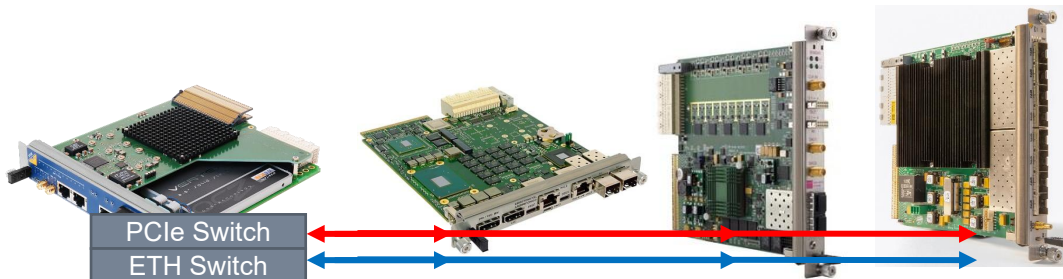


Gigabit Ethernet

- 1000BASE-KX
- TX and RX diff pair at 1.25 Gbps
- Examples: Ethernet interface of Zynq-based boards, UDP transceiver on FPGA

PCI Express

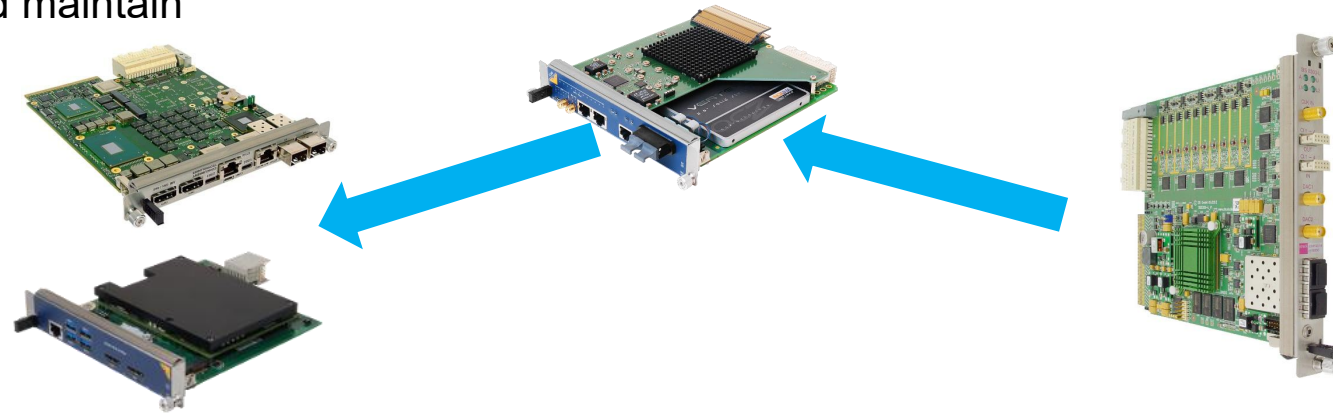
- Gen 3 (8 GT/s), x4 (x8 in special crates) choice for many apps
- Support for PCI Express Gen 4 and 5 in the latest specification and crate
- Other protocols available (SRIO, 10/40Gb Ethernet)



Computing Module

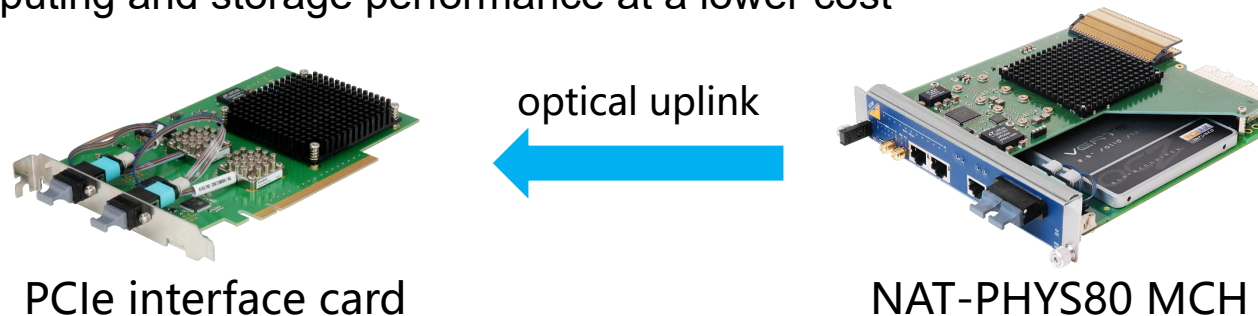
■ CPU module inside of crate (RTM CPU & AMC CPU)

- Processor performance limited by 80 W per slot power limit
- Easy to operate and maintain



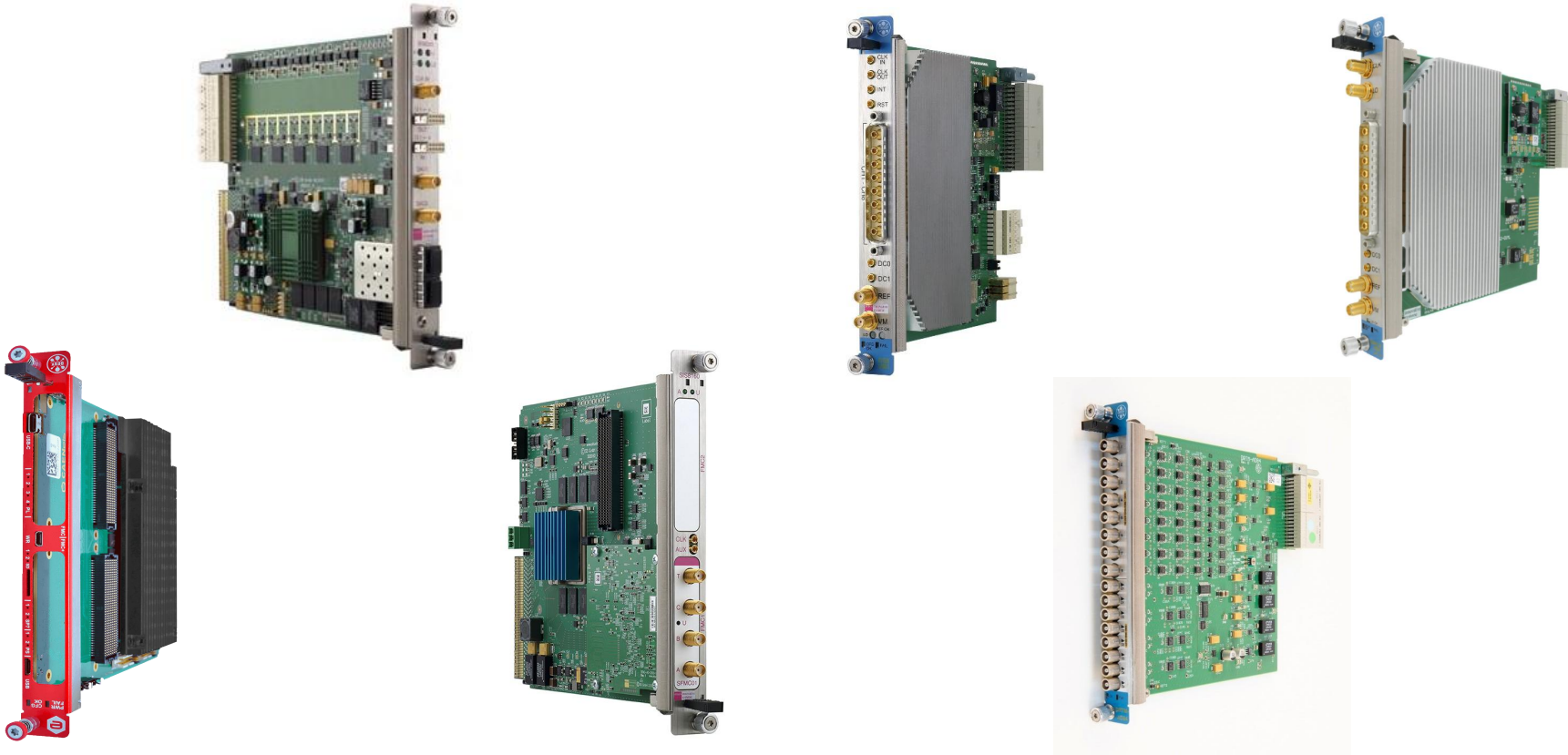
■ PCIe interface card for operation in PCs / servers

- Optical PCIe Gen3 x8/x16 uplink
- Obtaining higher computing and storage performance at a lower cost



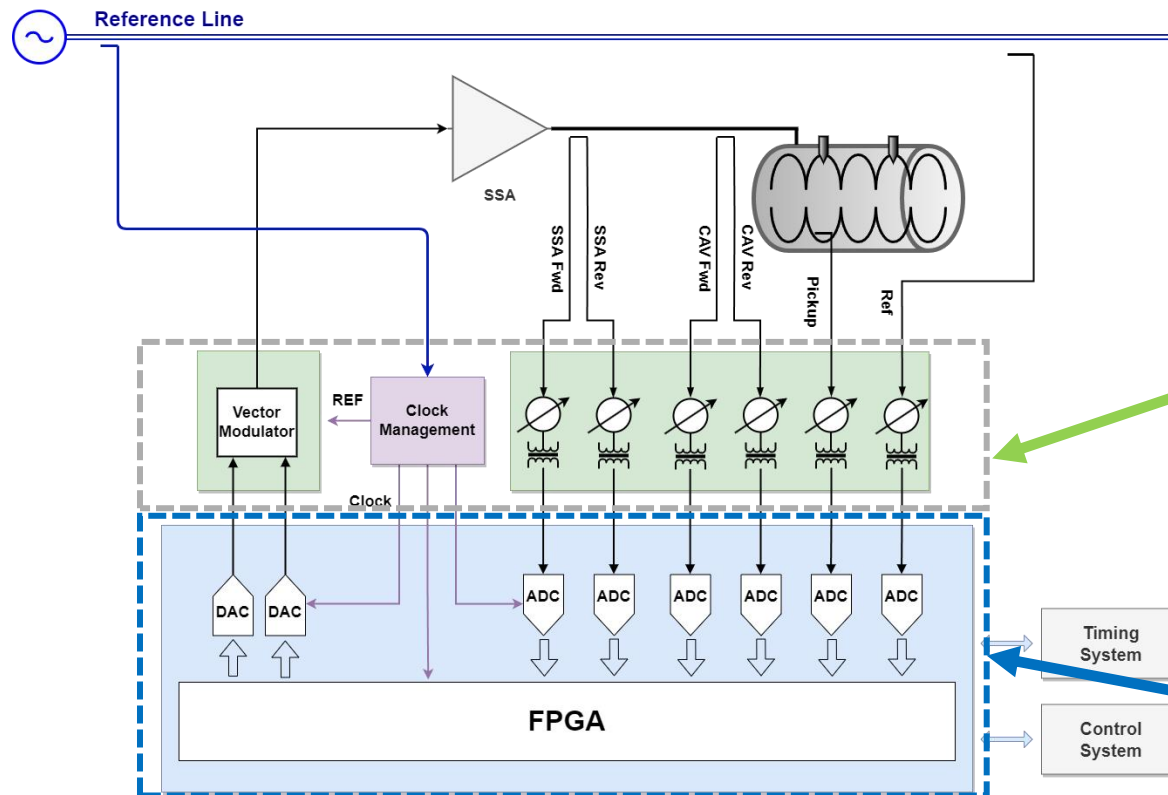
AMC & RTM Selection

- Many AMCs and RTMs available on the market, LLRF system needs to make appropriate choices based on the system architecture and operating frequency band



Direct Sampling Schemes with RTM

- Latest generation of RF sampling ADCs digitize signals at frequency up to several GHz, which makes it possible to sample RF signal directly
- Direct-sampling architecture provides flexibility and simplification for LLRF



Direct Sampling RTM

DC to 400 MHz DS front-end from struck

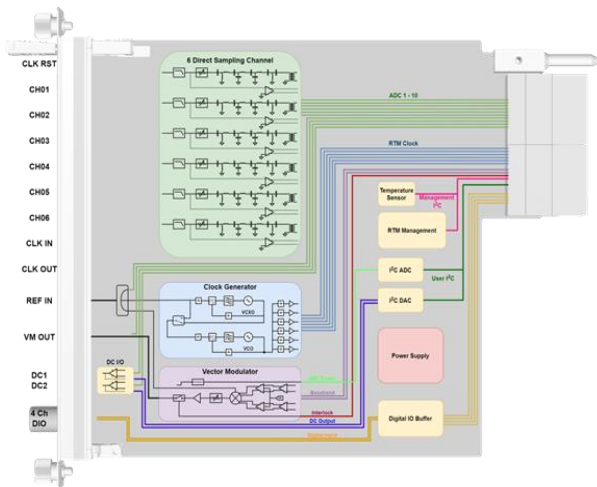


AMC Digitizer

10 channel 125MHz/16Bit digitizer

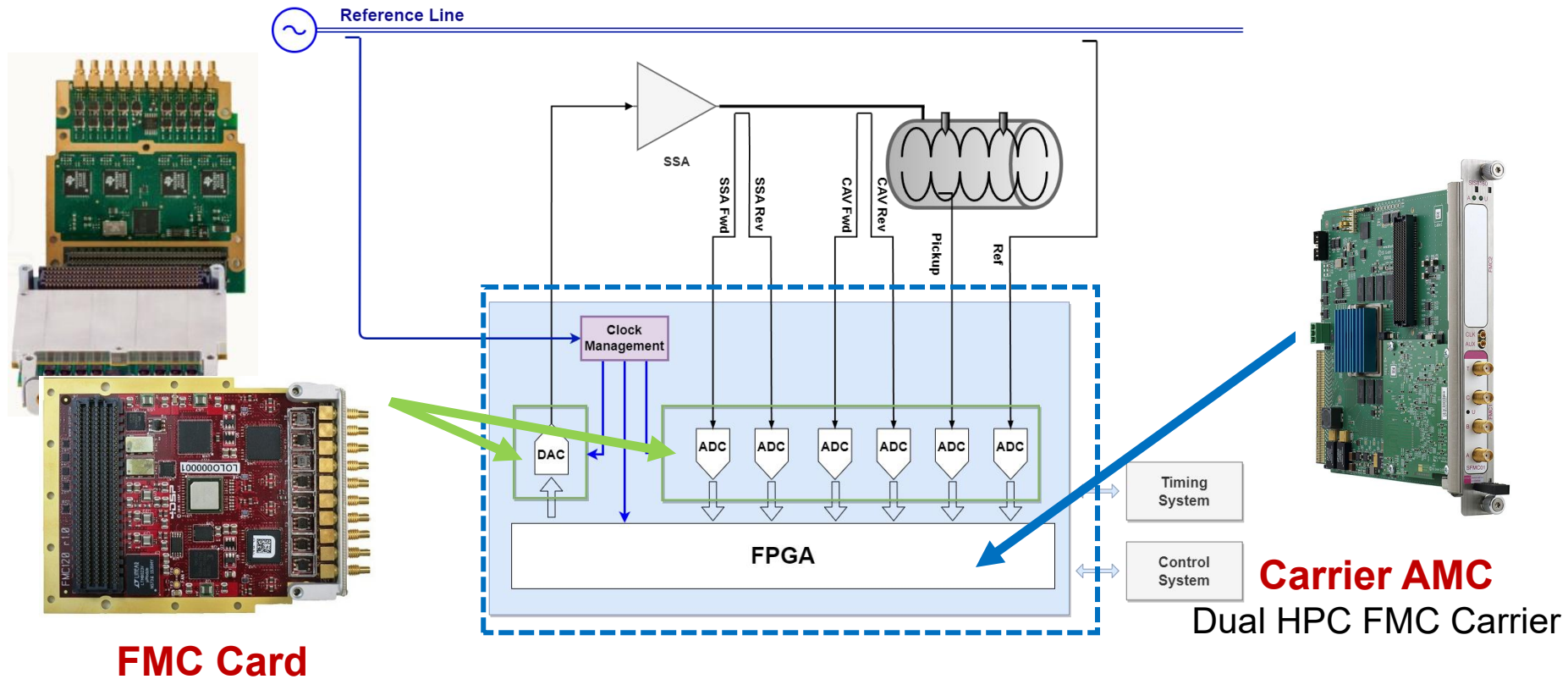
Direct Sampling Schemes with RTM

- Direct-Sampling LLRF System with In-House Developed RTM at IHEP
- Applied in the BEPCII sub-harmonic buncher LLRF system (142.8 / 571.2 MHz) and the HEPS sub-harmonic buncher LLRF system (166.6 / 499.8 MHz)
- Phase Stability (RMS): 0.007° @ 166.6 MHz, 0.02° @ 499.8 MHz
- 6 × RF direct-sampling channels (DC – 600 MHz) plus VM/REF monitoring channels
- Sampling clock generation from external clock or reference source
- Dual-loop clock generator with external VCXO and selectable internal/external VCO, enabling a flexible and configurable clock scheme



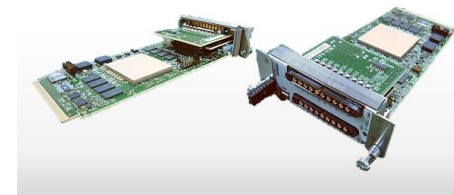
Direct Sampling Schemes with AMC Carrier

- High frequency analog signal transfer over Zone3 can lead to crosstalk between different channels
- Get rid of Zone 3 analog bandwidth limitations using carrier + FMC
- Many COTS components for GPS ADC and DAC



Other Direct Sampling Schemes

- High sampling rate digitizer using single-ended analog RTM connection (Class RF1.0)
- Zynq RF-SoC digitizer: highly integrated, more flexible, lower latency



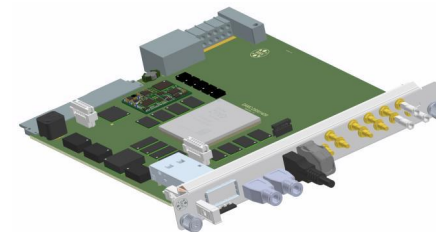
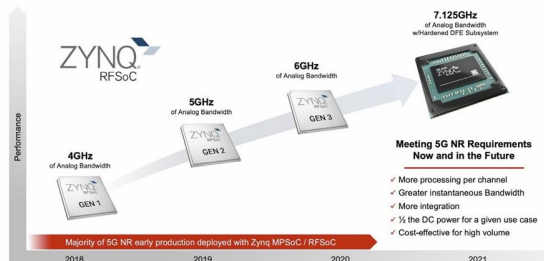
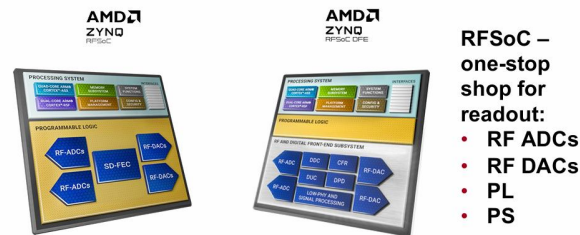
MMC-TRX02-B RF-SoC
12bit, Sampling: 4GSPS,
Bandwidth: 4GHz, Channels:
8ch



AMC576 RF-SoC
16 ADC (12-bit @ 2 GSPS)
16 DAC (14-bit @ 6.4 GSPS)



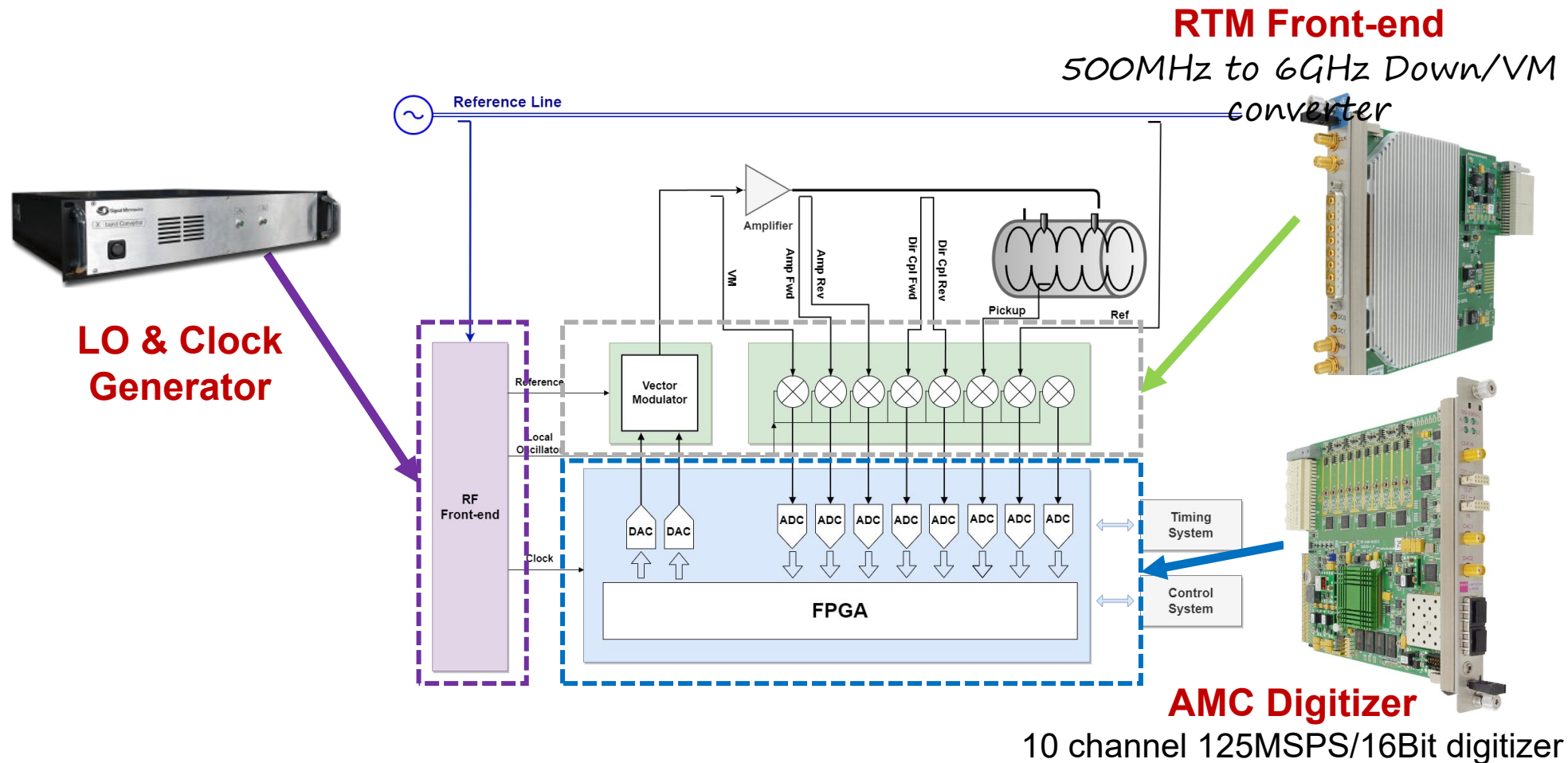
Similar to ZONE3 RF1.0
I can't find the its picture



DAMC-DS5014DR XCZU47DR
8ch 14 bits ADC, 5 GSPS, 6GHz analog BW
8ch 14 bits DAC, 10 GSPS, 4GHz analog BW

Down-conversion Schemes

- For L, S, C band LLRF, RF signal is typically down-converted in RTM front-end
- For higher frequency (X-band) LLRF, conversion between X, S or C out of crate may required



Down-conversion Schemes

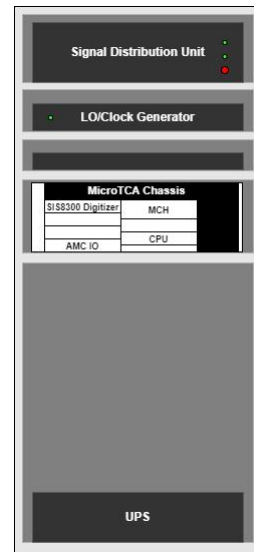
■ Down-Conversion Architecture for S-band LLRF at IHEP



HEPS 500MeV LINAC



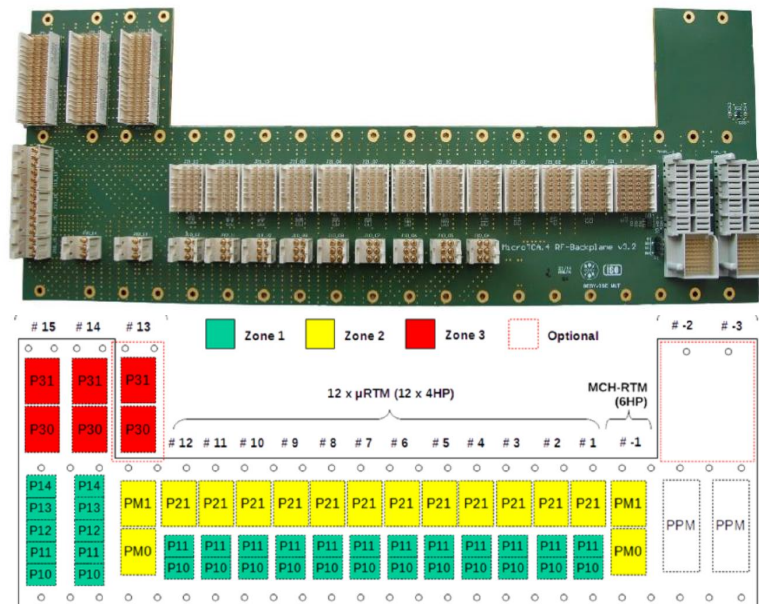
BEPCII 2.5GeV LINAC



- Mature Down-Conversion Architecture
 - Proven design with widespread deployment in HEPS and BEPCII Linac
- System Deployment
 - HEPS: 5 sets @ 2998.8 MHz
 - BEPCII: 22 sets @ 2856 MHz
- Hardware Configuration
 - Chassis: 3U / 9U
 - Control: 1 CPU / PS / MCH
 - Digitizer: 1 × SIS8300L2
 - Custom RTMs: wideband (650 MHz – 6 GHz)
 - 1 × Trigger Distribution AMC Board
 - 1 × SSA

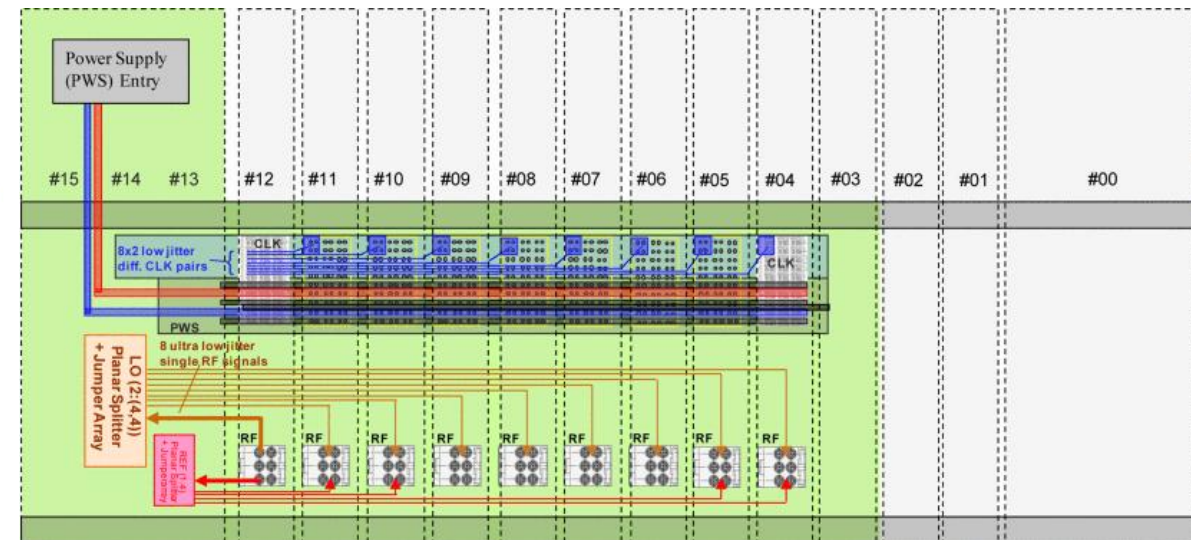
Down-conversion Schemes with RF Backplane

- RF backplane introduced in MicroTCA 4.1
- Extra slots for RF/clock signal generation and distribution modules, supports up to 3 extended RTMs (RTMs without AMC)
- Up to 2 power supply RTMs with low-noise, separated, analog, bipolar power distribution
- RF signal distribution over backplane, eliminates RF coaxial cable, more compact system, improves reliability



DRTM-LOG1300

Local Oscillator Generation



Cavity Tuning

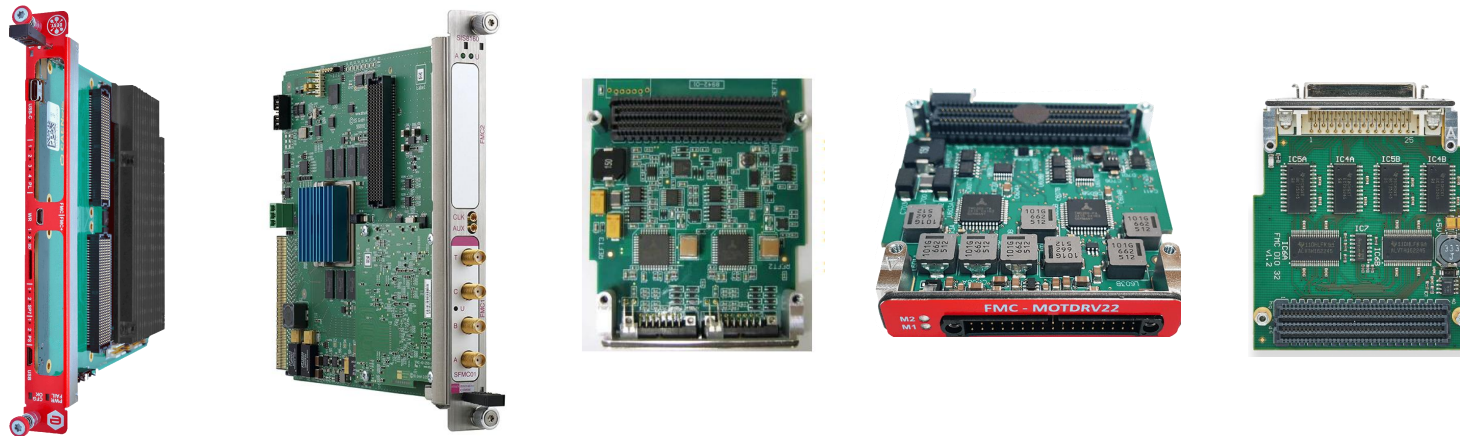
■ Piezo RTM



DRTM-PZT4

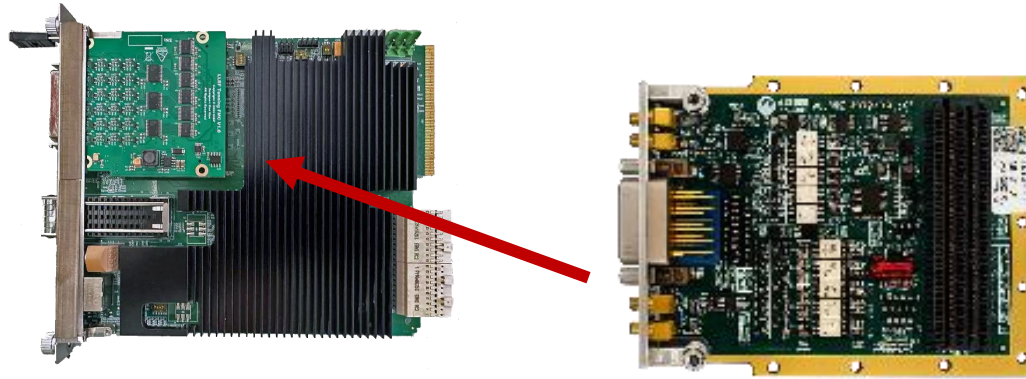
Output voltage range ± 80 V (bipolar); 0-80 V (unipolar)
 ± 80 V (bipolar); 0..80 V (unipolar)

■ Motor control



Cavity Tuning

■ LLRF Tuning and Piezo Control Solution at CSNS



Tuning FMC



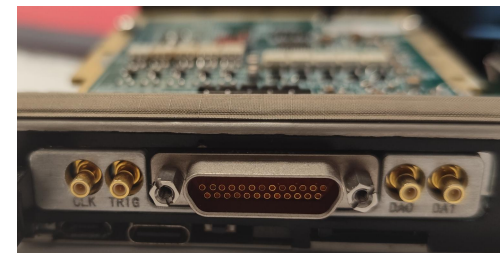
Step Motor Driver



Piezo Driver

□ LPC FMC

- 12 channel TTL/CMOS logic levels output 0~5V
- 10 channel TTL/CMOS logic levels input 0~5V
- 2 channel serial interface DACs with analog front-end(0~10V, $\pm 10V$ configurable)
- Synchronous clock:
1 ext. clock input / FMC CLK0_C2M
- 1 ext. trigger input

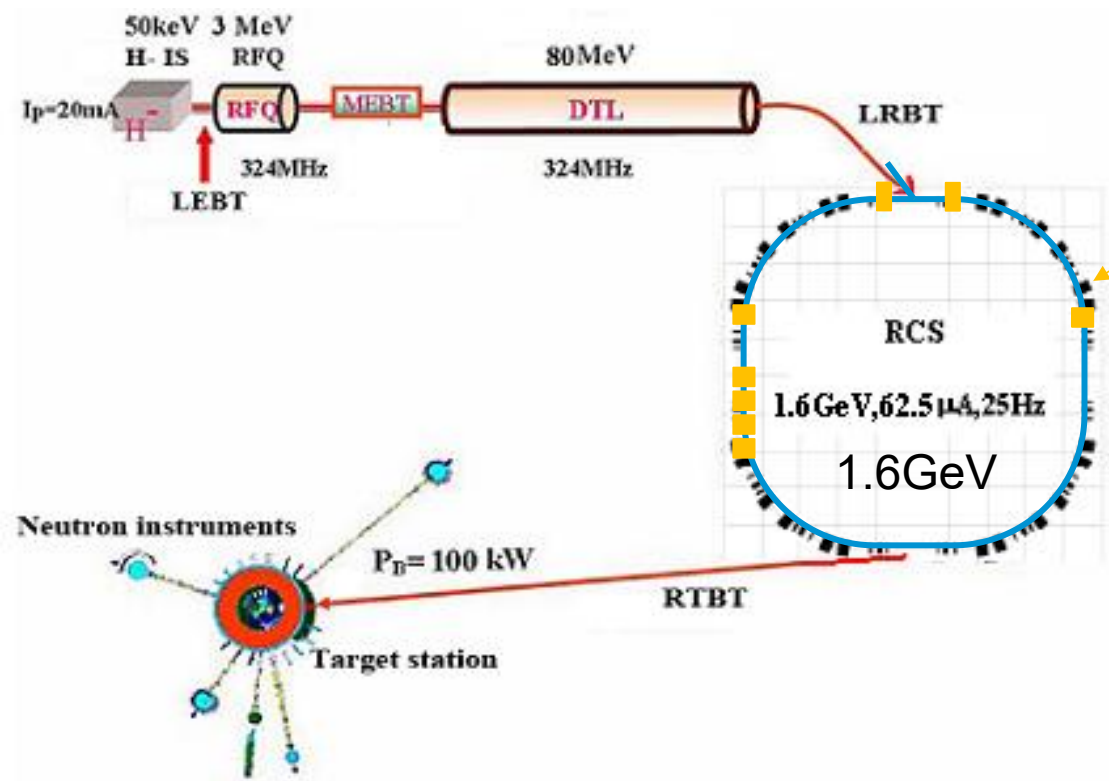


3

**Build a real LLRF
system with MTCA.4**

CSNS RCS LLRF

The CSNS RCS LLRF system is utilized to regulate the accelerating RF fields of eight ferrite-loaded cavities, which accelerate protons from an injection energy of 80 MeV to 1.6 GeV.



Ferrite-Loaded Cavity

RF Parameters	CSNS-II
RF frequency (MHz)	1.02-2.44
Number of RF cavities	8
Fundamental harmonic RF peak voltage (kV)	175
Repetition rate (Hz)	25

CSNS

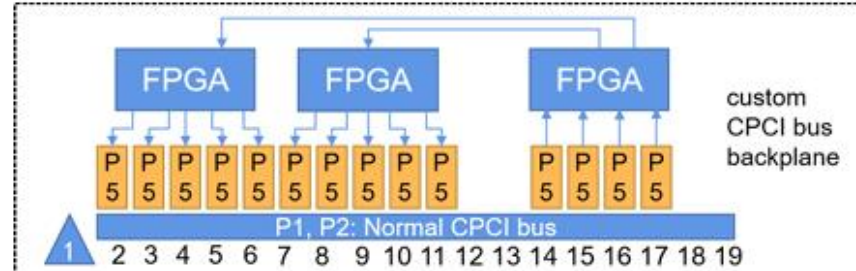
- CSNS RCS LLRF system operate mode:
- frequency-sweeping
 - pulsed mode

Why update?

CSNS-I RCS LLRF
Works very well



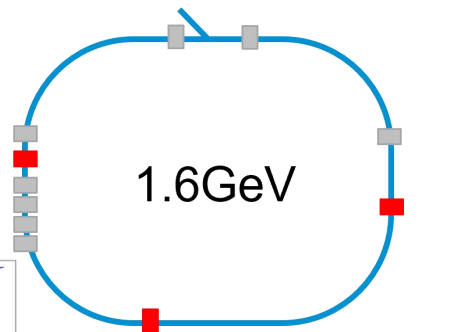
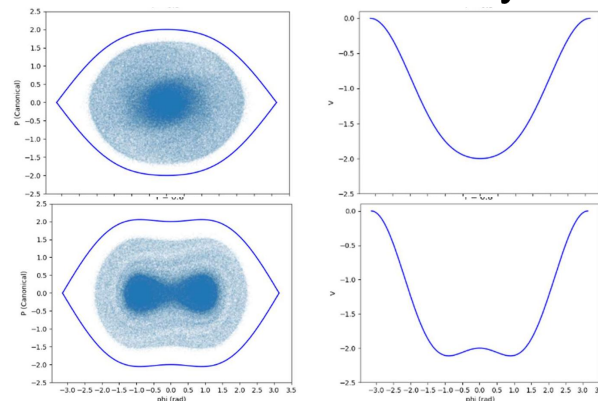
CPCI hardware platform



- 1 CPU (cpci6200)
- 8 LLRF controller for 8 Ferrite loaded cavity
- Timing + Beam signals (FCT, WCM, BPM)
- 10 Slots to receive Beam signals + 4 Slots to send

CSNS-II RCS **add 3 MA cavities**

- 1st harmonic cavity
- 2nd harmonic cavity



Flatten RF Potential
Uniform Distribution
of Particles

1. Not enough slots
2. **EOL of Legacy parallel CPCI bridge ICs & CPCI-6200**, make long-term maintenance difficult

RF Frequency range

CPCI-I RCS: 1.02-2.44MHz

CPCI-II RCS: 1.02-4.88MHz

low Q MA cavity → higher-order harmonics

Suppress up to 6-th (14.64MHz)

Process and monitor more data
(1st, 2nd, 3rd, 4th, 5th, 6th)

3. Bandwidth limitation (MAX bandwidth: 264MB/s)
4. Limited CPU processing capability CPU utilization > 95%



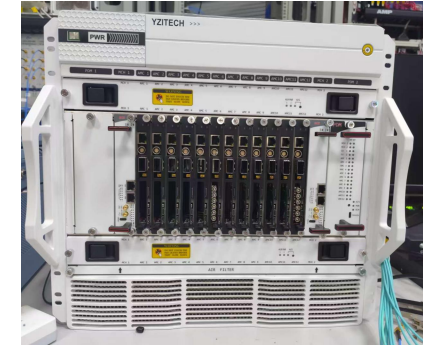
Why MicroTCA?

PXle: None standard of Field-replaceable PSU & fans

Strong commercial ecosystem. Few open source driver, Limited flexibility for deep customization

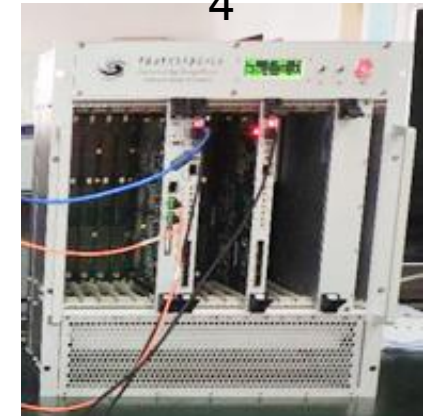
ATCA: Powerful, but Large, power-hungry, costly

	OpenVPX	MicroTCA.4
Backplane serial topology	Gigabit Ethernet; PCIe Gen3; SRIO; SAS/SATA: Available, but not standardized	Gigabit Ethernet; PCIe Gen3; SRIO; SAS/SATA
Redundancy	Available, but not standardized	High levels of redundancy across the PSU & CU, Fabrics
Hot swap	Not supported	Strongly supported
Board size	6U (160 × 233.35 mm)	148.5 × 181.5 mm
RTM	Highly flexible I/O configuration Application-dependent design Limited interoperability	Zone 3 standard Better interoperability
HEP & Accelerator Ecosystem	Mainly adopted in defense & aerospace	More proven applications Experience sharing & technical collaboration
Cost	More expensive rugged platform	Cost-effective



MicroTCA.

4



VPX

What's we need?

The maximum annual beam power delivery time exceeds 5,200 hours, with a peak device operation efficiency of over 97%.

High Reliability & Availability

Stable and reliable year-round operation

Redundant power and cooling modules

Hot-swappable individual modules for rapid online replacement

Centralized hardware health management

Open, Transparent, and Deeply Customizable Architecture

No black-box

internal operation is visible and understandable

modify or configure according to application

Modular & General-Purpose Hardware Platform

not only one specific application/system

CSNS-II LLRF & Timing & BPM ...

- Independent functional modules
- Flexible system configuration
- (combination of diff modules)
- Easy replacement and expansion

High performance & High bandwidth & High-Density Integration

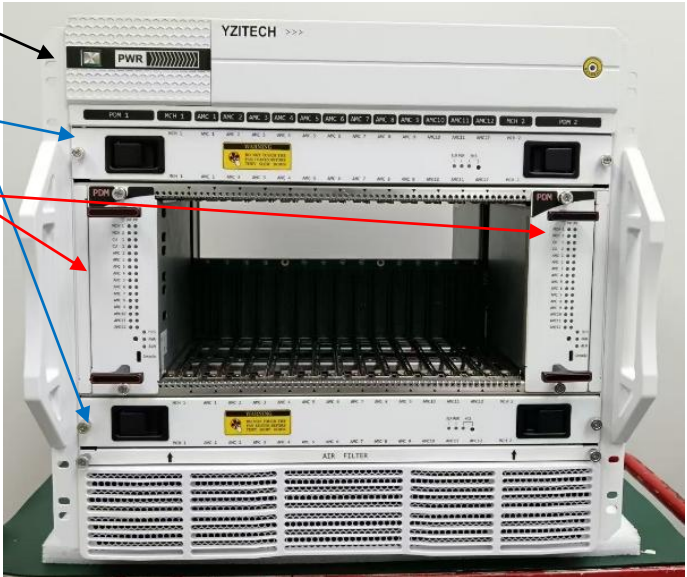
- High-Precision Clock Synchronization
- High-Speed RF Acquisition & Processing
- High-Performance ADC/DAC
- Real-Time Digital Signal Processing
- Real-Time Control Algorithms
- High-Bandwidth Data Transfer
- Network & Optical-Fiber Communications
- Remote Monitoring & Control

Hardware platform for CSNS-II RCS LLRF

12-slot chassis and backplane

2 Cooling unit

2 Power supply

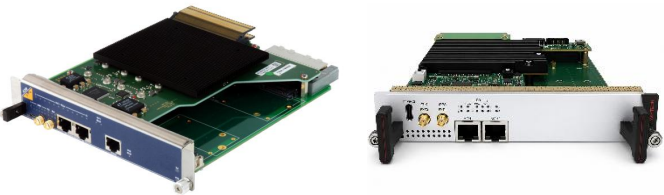
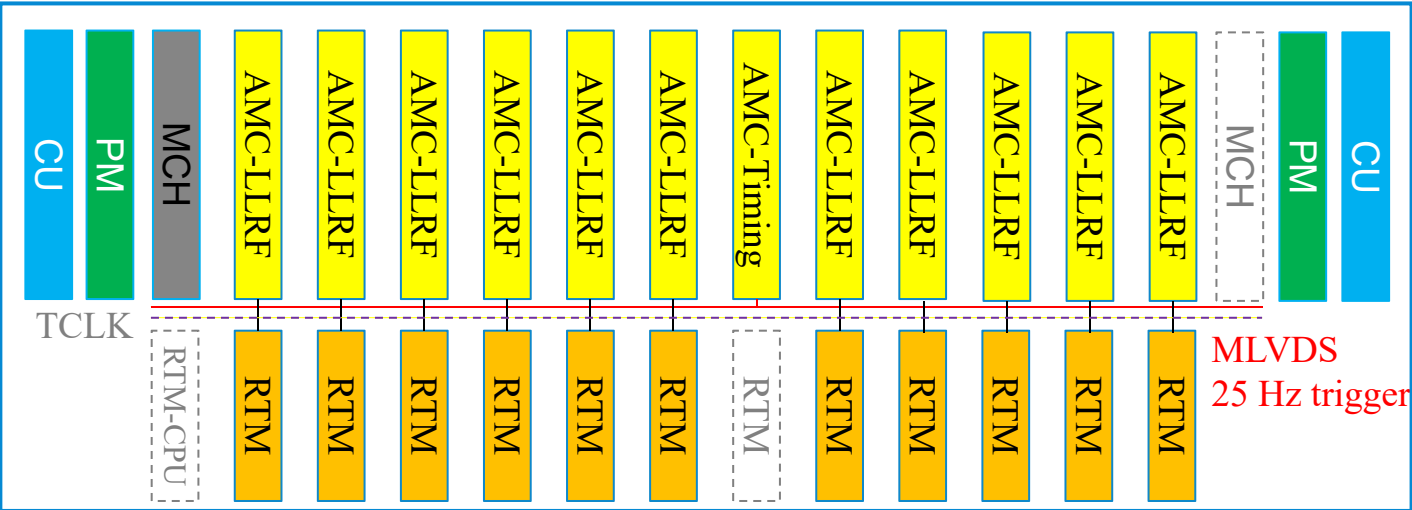


11 LLRF Controller:

- **AMC**
- **RTM** (Analog signals I/O and conditioning)

1 Timing AMC: 25Hz Timing Trigger

global synchronization among multiple RF cavities and other accelerator subsystems.

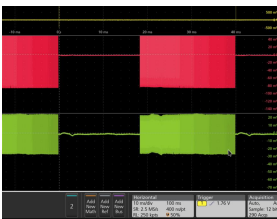


At least one MCH:

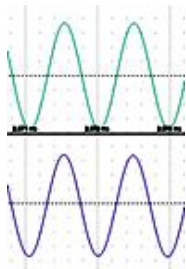
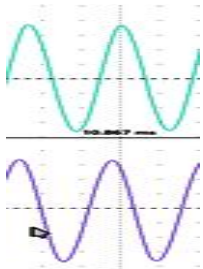
Centralized IPMI-based system management
High-speed data fabric switching
Synchronous Clock

Synchronous Clock

synchronizes the FPGA operating clocks
across all AMCs
TCLK or an External Clock Reference

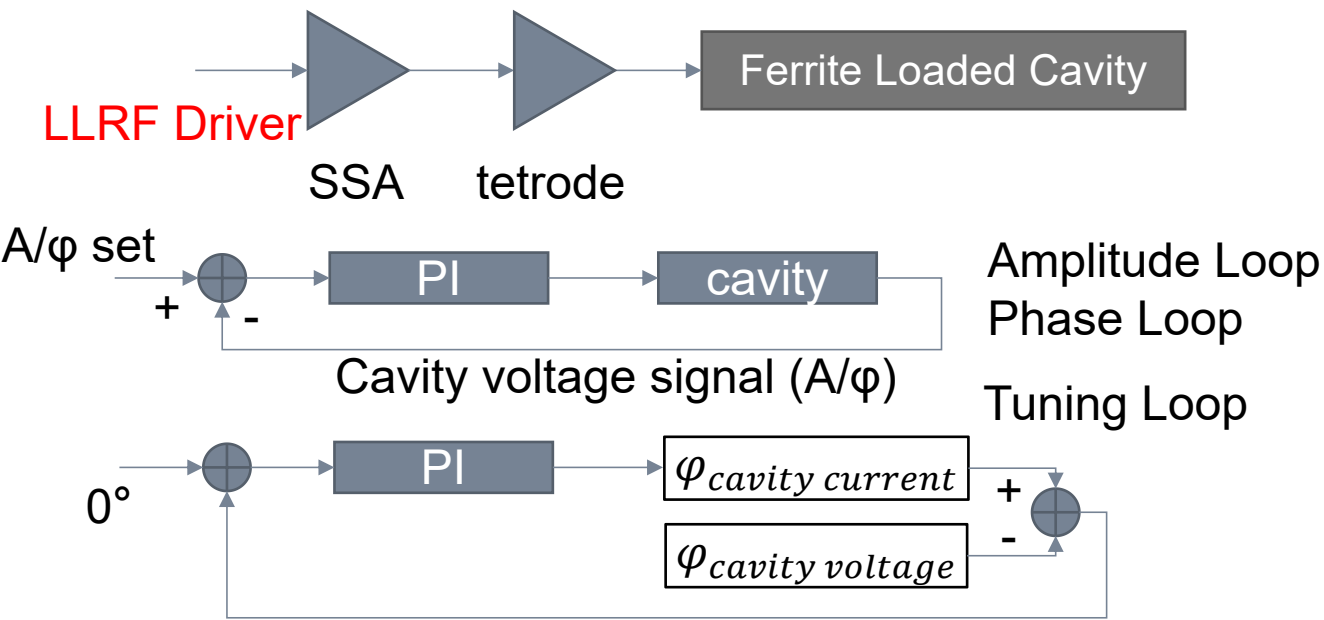


Without/With global trigger



Without/With synchronous clock

AMC Selection & Customization



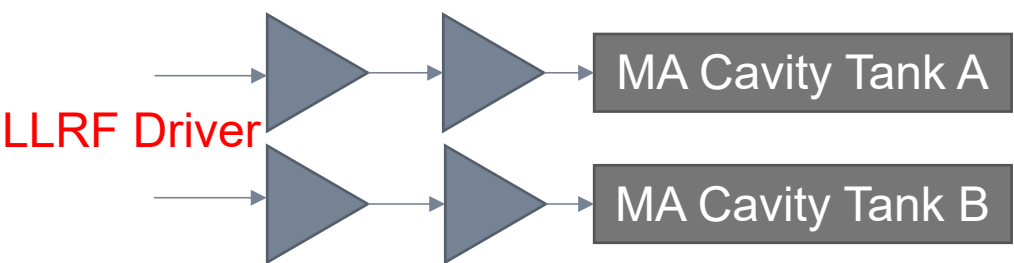
Cavity voltage Cavity current SSA voltage for Grid tuning Loop

3 ADC
1 DAC

3 optic
Ch

2 ADC
2 DAC

2 optic
Ch

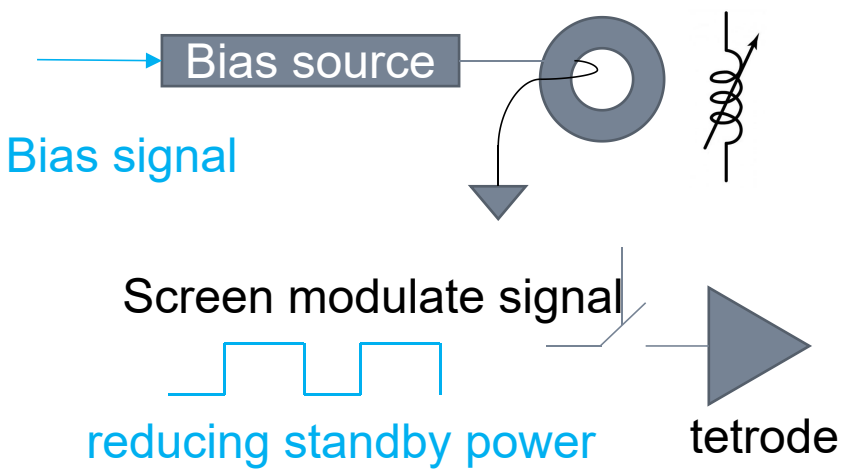


Only Amplitude & Phase Loops

(1st, 2nd, 3rd, 4th, 5th, 6th)

Each harmonic component has two loops

Driver A, Driver B
Cavity voltage A, Cavity voltage B



AMC Selection & Customization

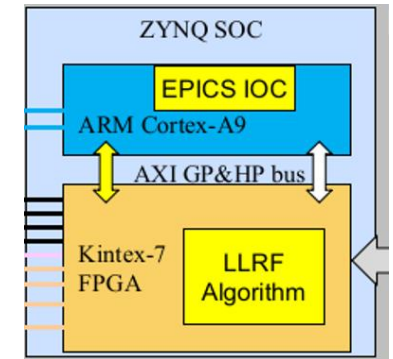
ADC Channels: ≥ 6

- 3/2 channels for RF signal acquisition
- 2 additional channels for system status monitoring & fault diagnosis (MA Cavity)
- 2 additional channels reserved for beam signals
(Suppression of Longitudinal Beam Oscillations, Beam Loading Compensation)

DAC Channels: ≥ 2 Ext Clock

Optic Channels: ≥ 3 but 2 is OK

Resource	Utilization	Available	Utilization %
LUT	129174	218600	59.09
LUTRAM	5572	70400	7.91
FF	111587	437200	25.52
BRAM	459	545	84.22
DSP	566	900	62.89
IO	179	362	49.45
GT	4	16	25.00
BUFG	8	32	25.00
MMCM	1	8	12.50



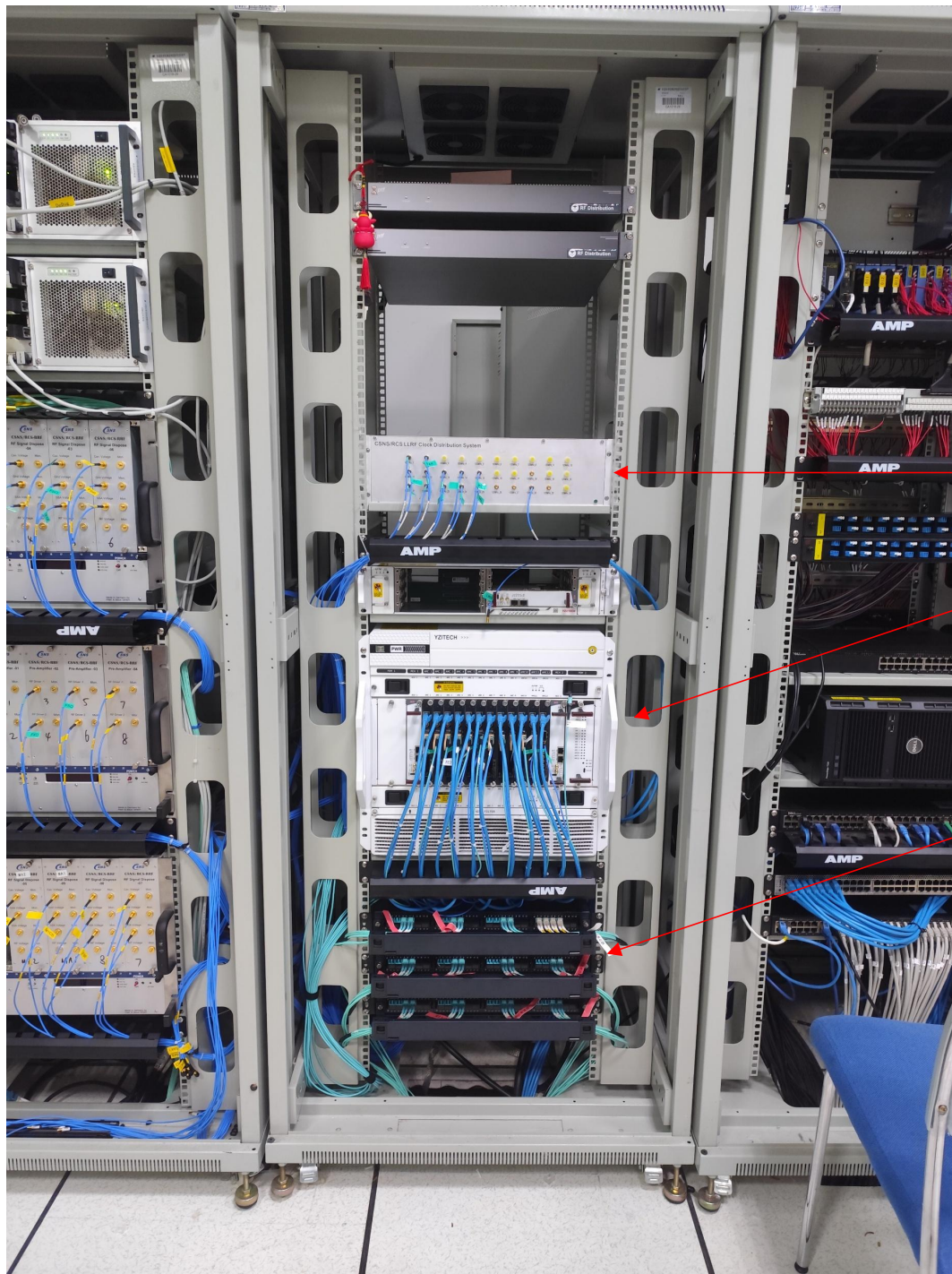
Reduce cost
integrate ARM CPU



SIS8300-KU



Custom-designed AMC

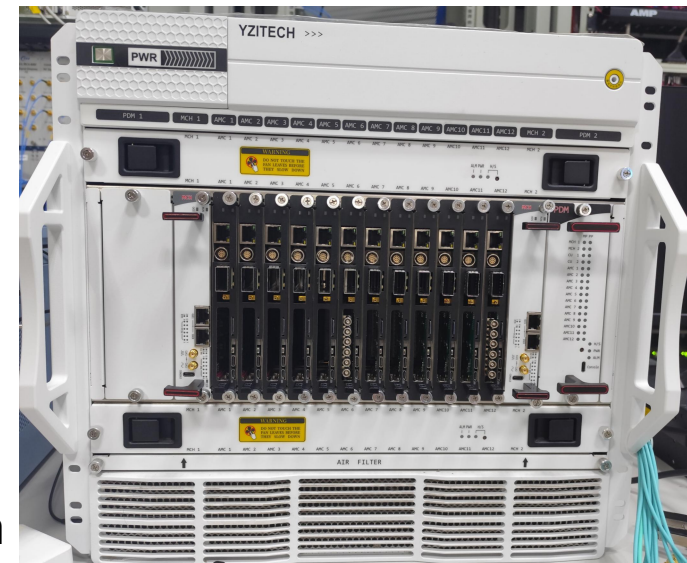


Front View

Ext Clock Distribution System

MTCA.4 LLRF hardware platform

QSFP to 4 SFP



Rear View

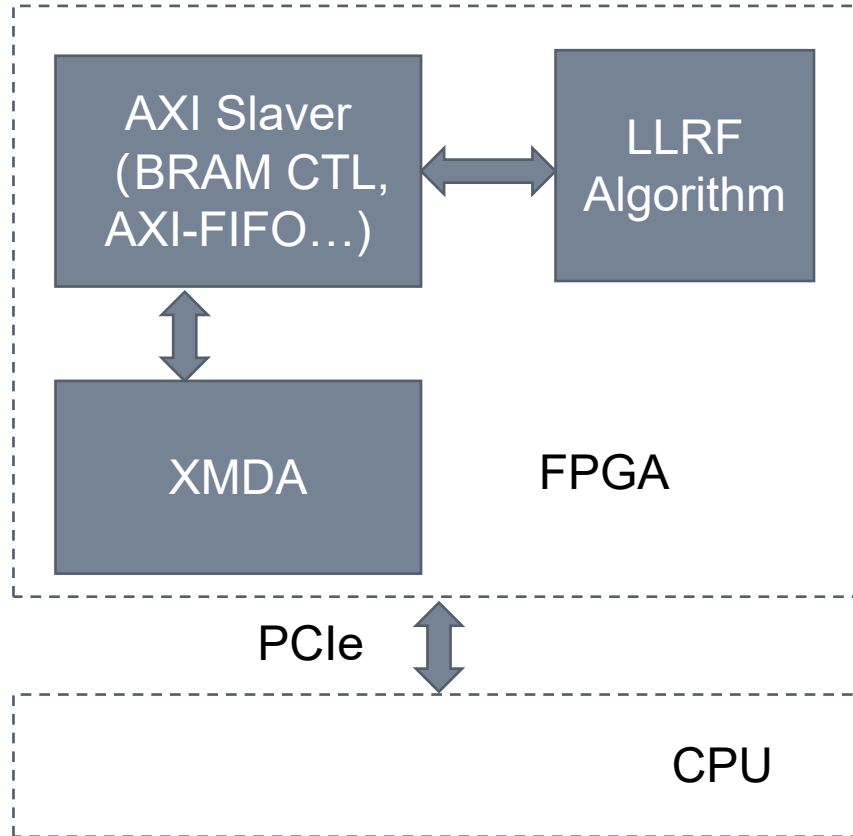


04

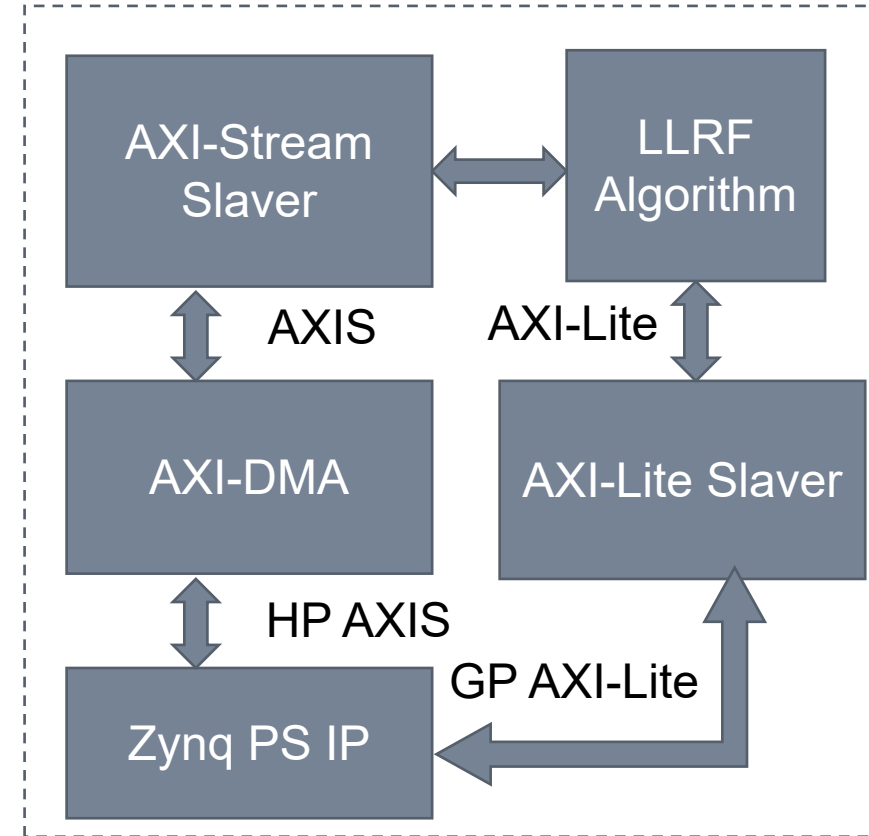
**FPGA Framework and
Software Implementation**

FPGA Framework

1. If you have a dedicated CPU module



2. Zynq SOC integrate ARM CPU



XDMA Device Driver

■ Official Driver:

https://github.com/Xilinx/dma_ip_drivers

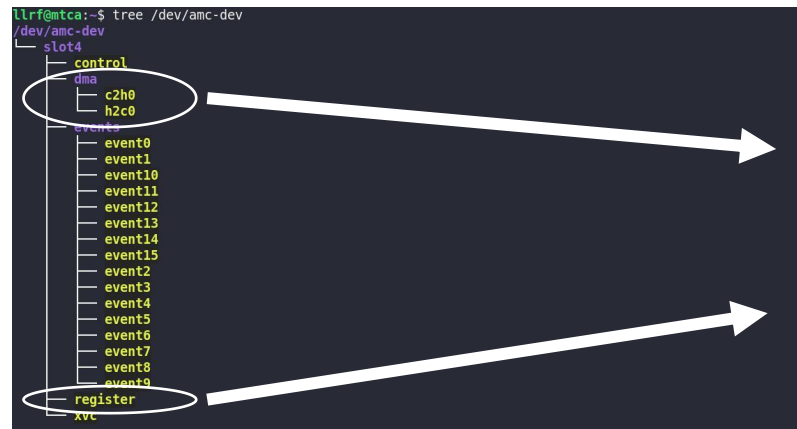
<https://xilinx-wiki.atlassian.net/wiki/spaces/A/overview>

■ Driver Customization:

- Board startup configuration support
- Crate slot mapping
- Driver installation script
- Udev rules and dkms support for the Xilinx XDMA driver, example:

<https://github.com/MicroTCA-Tech-Lab/xdma-metapackage>

■ User space character device structure :



C2H: AXI4 port (DMA from device)
H2C: AXI4 port (DMA to device)

Register: AXI4-Lite port

- Real-Time Linux
- ▼ Linux Drivers
 - Xilinx V4L2 HDMI 2.1 ...
 - > Xilinx DRM KMS HDM...
 - Xilinx Zynq UltraScale...
 - Linux I2S Driver
 - Linux Emaclite Driver
 - ZynqMP NAND
 - Linux CAN driver
 - Axi Watchdog
 - Linux SPI Driver
 - Linux ZynqMP GQSPI ...
 - ZynqMP Linux Reset-...
 - PS UART
 - ZynqMP Linux Pin Co...
 - > Linux AXI Ethernet dri...
 - Zynqmp RTC
 - Axi timer

User Space Driver

- Linux kernel driver for the general purpose DMA include Xilinx AXI-DMA

- Xilinx provides "DMA proxy" kernel driver

<https://www.xilinx.com/video/soc/linux-dma-from-user-space.html>

<https://github.com/Xilinx-Wiki-Projects/software-prototypes/tree/master/linux-user-space-dma>

- The drivers use the Linux DMA Engine subsystem and provide the ability for user to write their own Linux driver which uses the Xilinx driver in kernel space through the DMA Engine subsystem

- Other open source driver:

- A zero-copy, high-bandwidth Linux driver and user space interface library for Xilinx's AXI DMA and VDMA IP blocks:

https://github.com/bperez77/xilinx_axidma

- Linux Driver for the Zynq FPGA DMA engine

<https://github.com/bmartini/zynq-xdma>

User Space Driver

■ User space application/driver through the UIO framework

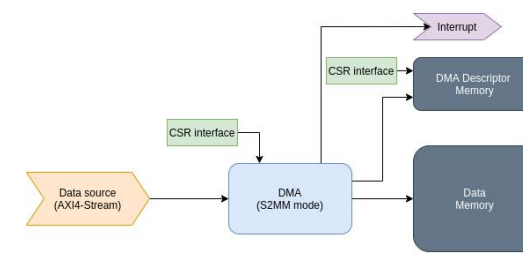
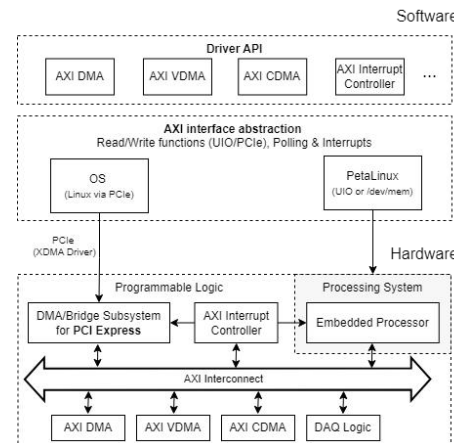
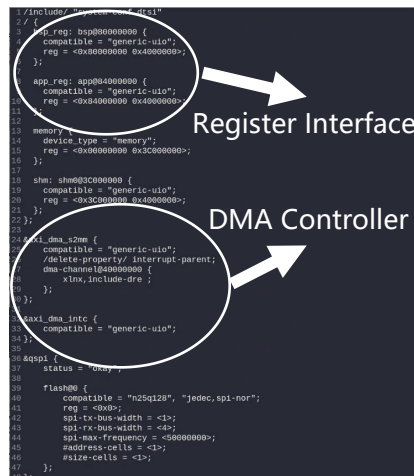
1. Add the UIO driver to the kernel
2. Setup IP core in the device tree to use the UIO driver
3. Develop API to access IP cores via UIO device
4. Add access to memory:
 1. reserved memory region in device tree
 2. u-dma-buf kernel driver: <https://github.com/ikwzm/udmabuf>
5. Control AXI DMA engine read from/write to memory space

S2MM for example

- Clear IRQs (S2MM_DMASR)
- Set config (S2MM_DMACR)
- Set Dst mem address (S2MM_DA)
- Set length (S2MM_LENGTH)

■ Example: libudmaio from MTCA Tech Lab

- <https://github.com/MicroTCA-Tech-Lab/libudmaio>
- Simplify the use of the Xilinx AXI DMA controller when used in S2MM (Stream to Memory-Mapped) mode
- Over PCIe with xdma driver
- From ARM over the Userspace I/O



***Thank you for
your attention!***