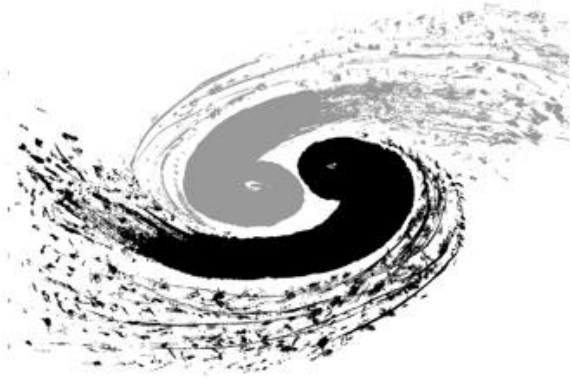


Status of MicroTCA.4 R&D&Run in IHEP Linac applications

MA Xinpeng (马新朋) , GAO Wenbin (高文斌) , GAN Nan (甘楠) ,
MU Yajie (牟雅洁) , MENG Cai (孟才) , LI Jingyi (李京祎)



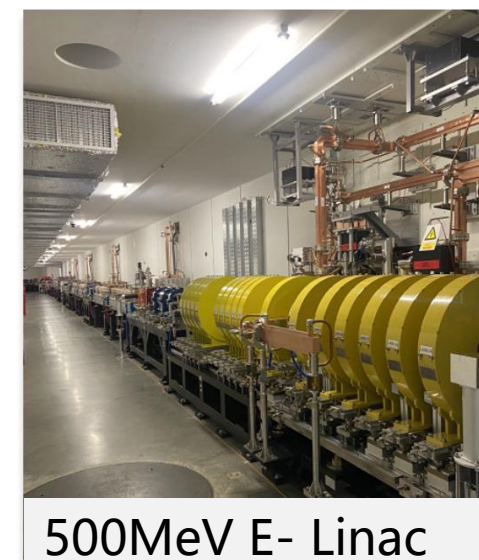
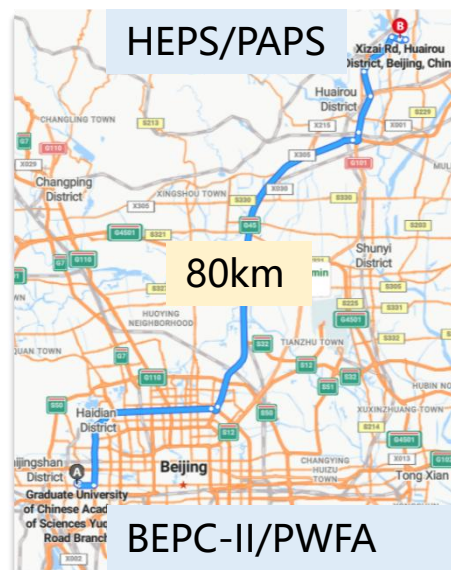
Institute of High Energy Physics
2026-9-15



Outline

- Introduction
- Status of R&D&Run
- Future plans

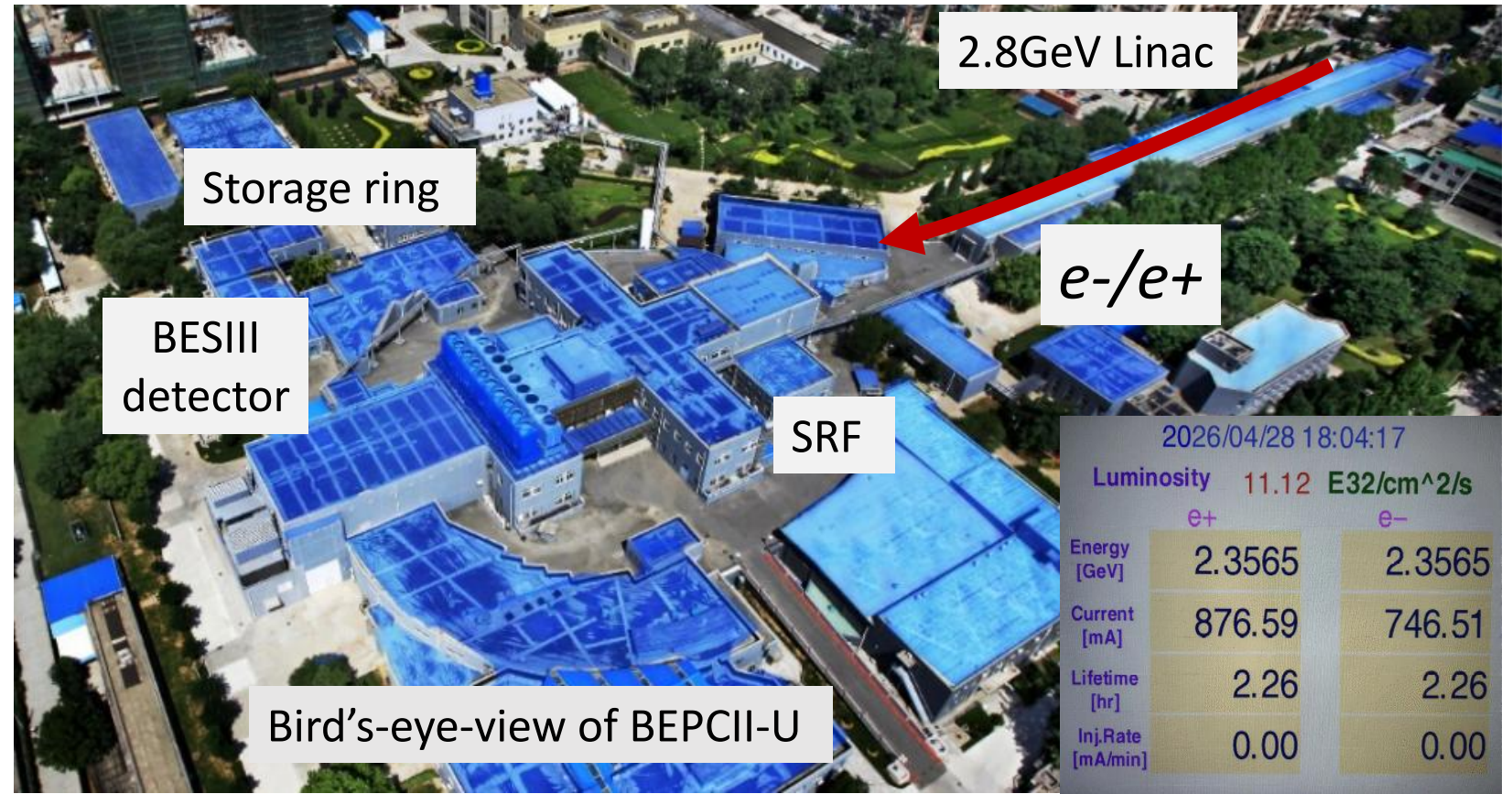
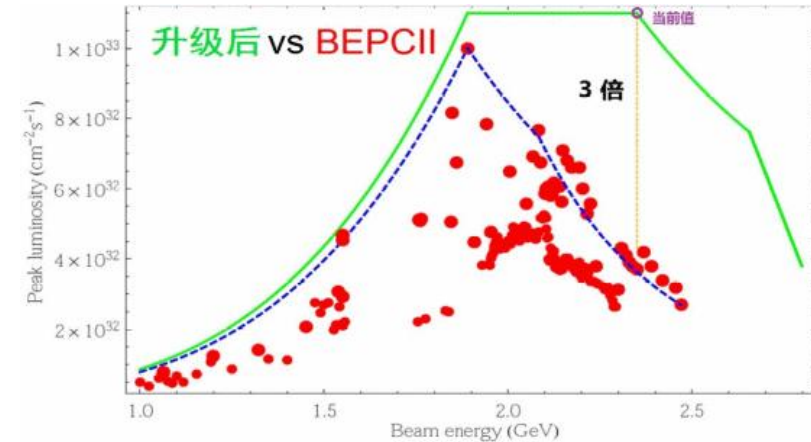
Introduction to facilities



BEPCII-Upgrade

BEPCII-Upgrade

- BEPCII-Upgrade project: completed at 2025, to increase energy from 2.5GeV to 2.8GeV, and 3 x higher collision luminosity broadening tau-charm energy region
- Linac upgraded (24 MicroTCA.4 digital LLRF)
 - 2 more SRF cavities
 - new IP magnets
 - upgrade in detectors ...

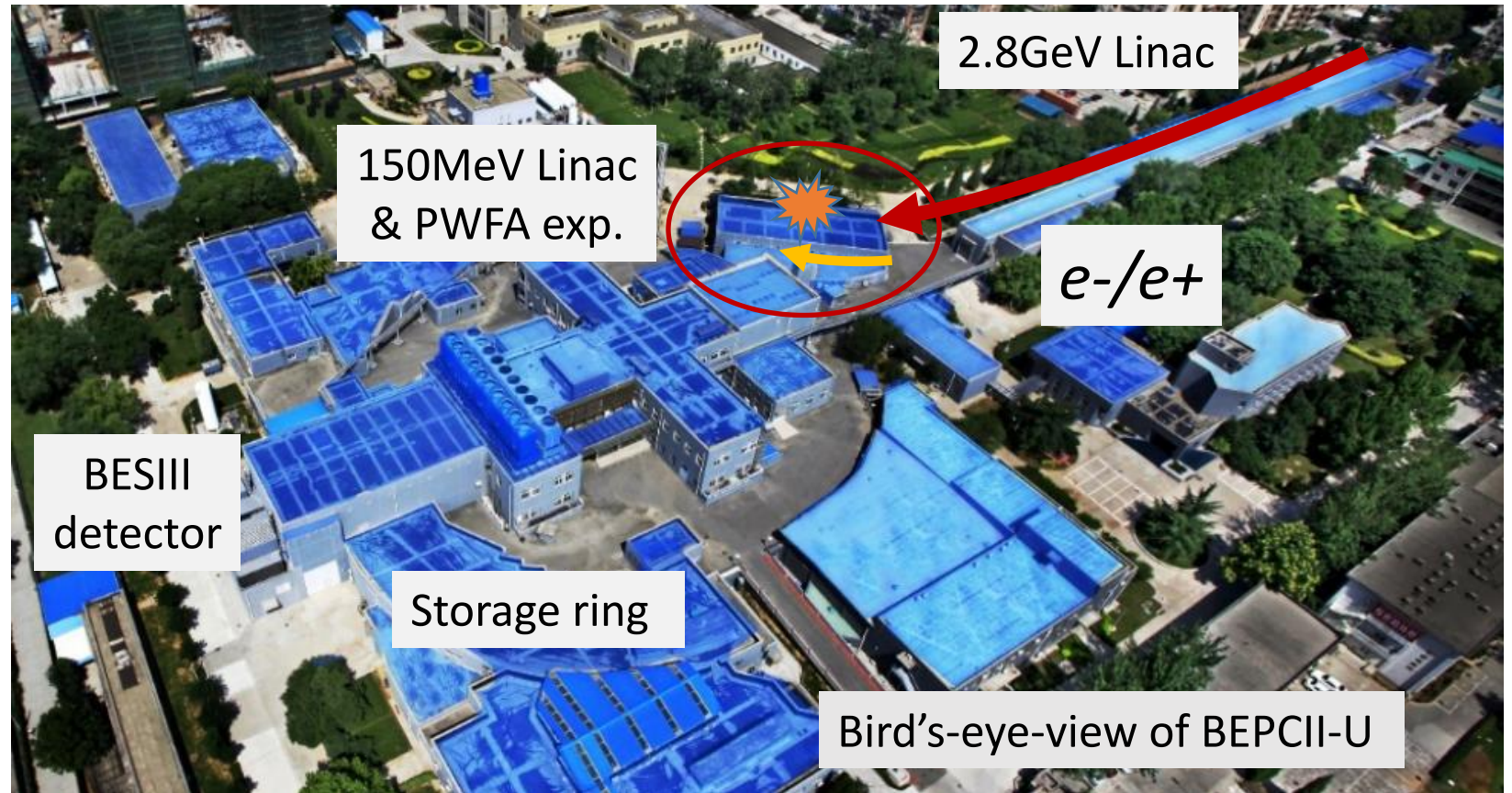


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Luminosity	11.12	$\text{E32}/\text{cm}^2/\text{s}$
	e^+	e^-
Energy [GeV]	2.3565	2.3565
Current [mA]	876.59	746.51
Lifetime [hr]	2.26	2.26
Inj.Rate [mA/min]	0.00	0.00

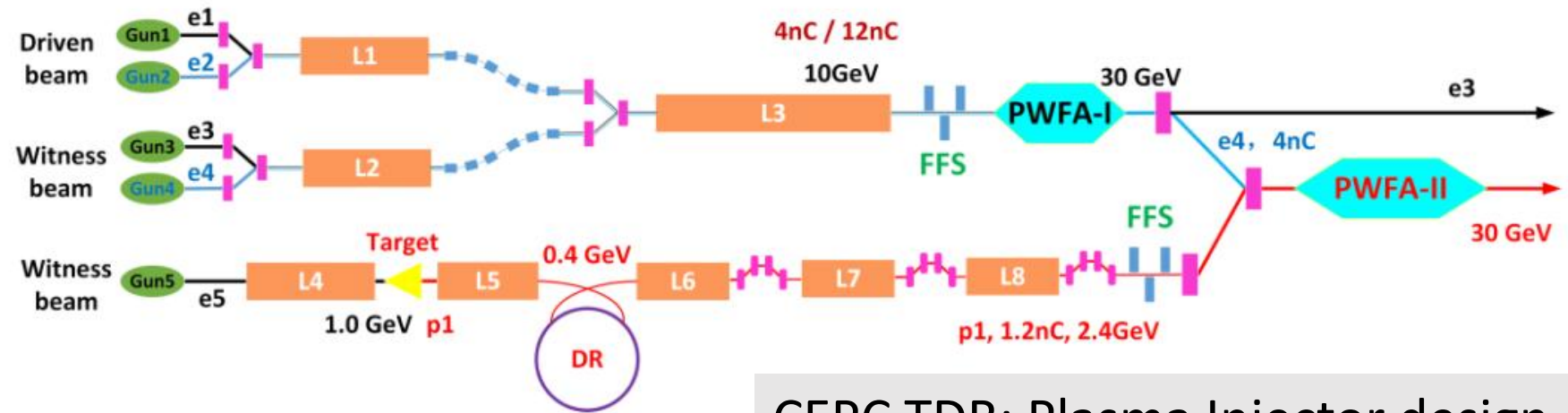
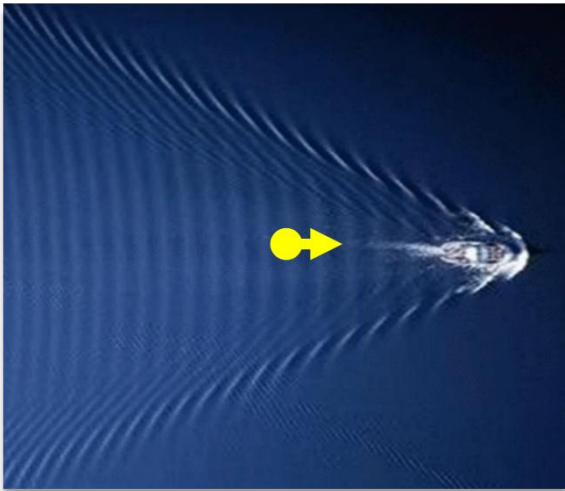
BEPCII-Upgrade and PWFA

- BEPCII-Upgrade project: completed at 2025, to increase energy from 2.5GeV to 2.8GeV, and 3 x higher collision luminosity broadening tau-charm energy region
- **New PWFA test facility:** new science and new engineering, a new 150MeV Linac in PWFA exp. hall (2024 -)



PWFA

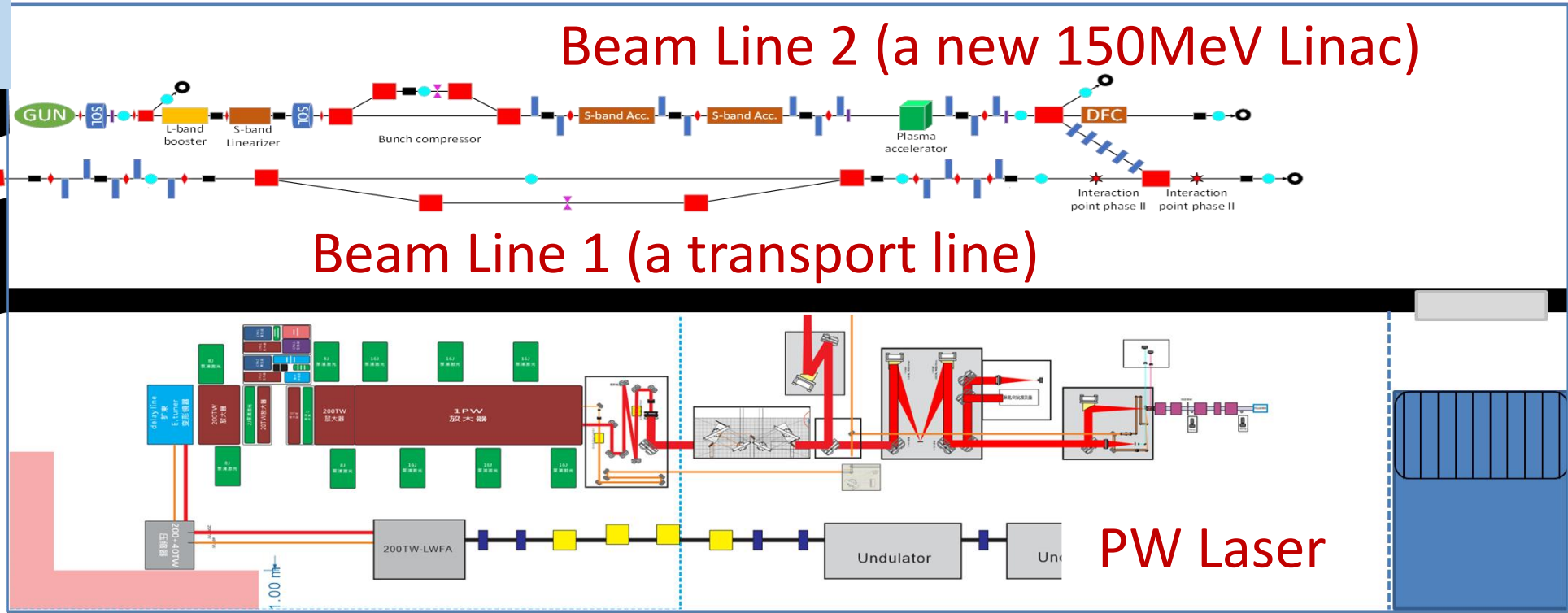
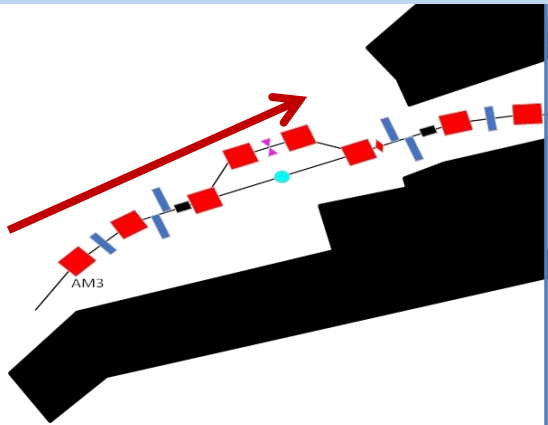
- PWFA (Plasma WakeField Acceleration) is a beam accelerated by another beam-stimulated wakefield when it pass through a plasma
- Pro: Very high acclerating gradient $>10\text{GeV/m}$!
- **High energy physics future:** Higgs factory needs e^-/e^+ collider, CEPC proposal is underway, but still too complex(100km) and expensive, PWFA is a candidate way for future collider and FEL



CEPC TDR: Plasma Injector design

PWFA station

e⁺/e⁻ from
BEPCII-U Linac



- Goals:
- (1) PWFA demonstration in new photon-cathode Linac. (BL2)
- (2) PWFA positron with new Linac and BEPCII-U Linac. (BL2+BL1)
- (3) Cascaded PWFA of e⁺/e⁻ by accelerated bunch together with BEPCII-U Linac based on (1) + (2). (BL2+BL1)
- (4) Laser Plasma Acceleration(LPA): PetaWatts Laser.

Frequencies of the new BL2 150MeV drive Linac

- Have to generate L band and 499.8MHz(for timing EVG) from BEPCII-U(existed 2856MHz)
- Those both L and S band machine, mostly from MO 1300MHz to 2856MHz
- Calculate from 2856MHz to near 1300MHz(because photon-gun been decided L band) , big enough common frequencies, near 1300MHz as gun can only be very few freq tuned
- Final solution is common frequency $14.28\text{MHz} = 1/200 \times 2856\text{MHz}$, L band 1299.48MHz referenced for both L band gun and driven laser

$$\frac{1300}{2856} = \frac{325}{714} = 0.45518207\ldots$$

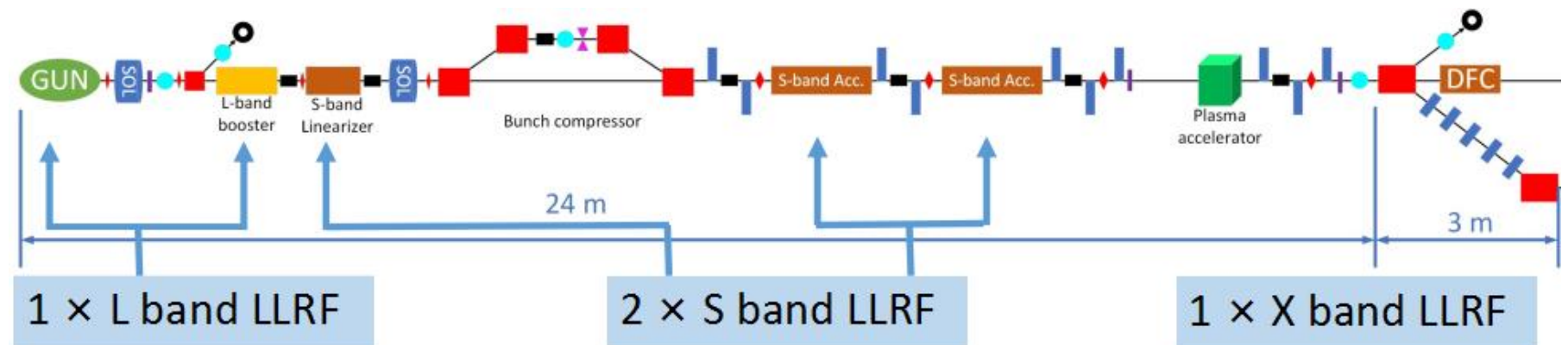
$$0.455 = \frac{91}{200}$$

$$0.455 \times 2856 = 1299.48$$

$$1/2 - 9/200: 1428 - 14.28 \times 9 = 1299.48$$

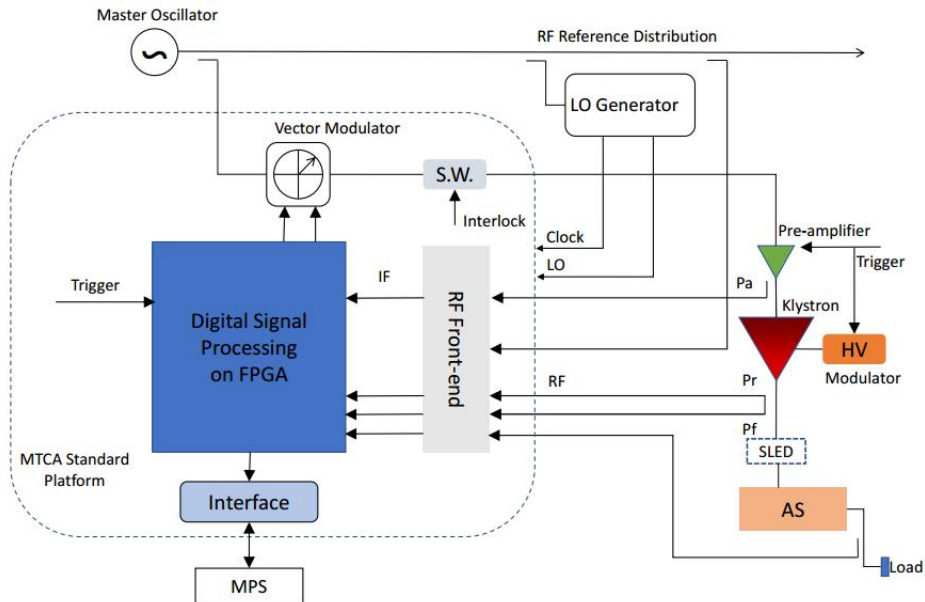
Common frequency: 14.28MHz

Beam line 2: new Linac, beam shall be sync-ed with beam from BEPCII-U Linac



LLRF for PWFA new Linac

- 3 MicroTCA.4 LLRF system, L band(1299.48MHz), S band(2856MHz), X band(11.424GHz)
- Upgrade MicroTCA hardware includes one new 2U local made chassis, DAQ-AMC/DWC-RTMs/CPU boards for L&S band, 1 Trig AMC board, NAT MCH
- Firmware/software kept same with BEPCII-U and HEPS
- 1Hz pulsed (us) klystrons for L + S high power systems



LLRF of L and S band



SSA: from Signal Microwave(时光微波)
Rack: from nVent(盈凡), water cooling
Chassis: from YZITech(源中)



LLRF upgrade on BEPCII-U Linac

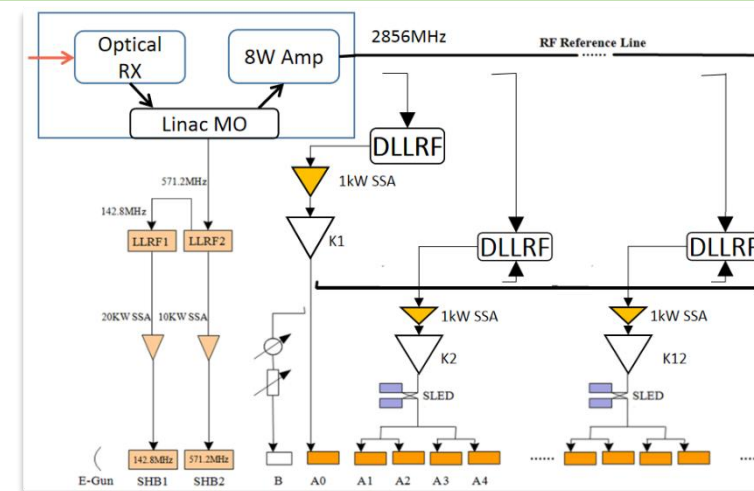
- BEPCII-U Linac: 202m, 2 more klystrons, 24 in total, full energy 2.8GeV for electrons and positrons
- Upgrade 22 + 2 new MTCA.4 LLRF 2856MHz system, 2x 142.8MHz and 571.2MHz bunchers system = 24
- Upgrade all MO signal module TEC-controlled $\pm 0.01\text{K}$

Frequency	2856 MHz
Pulse width	4 us
Klystron	50 MW
Repetition	1/12.5/25/50 Hz

PRL <- 8W PA
Phase monitor
Freq Multiply
Linac MSG
-> Optical Rx



Fully MTCA based modernized LLRF

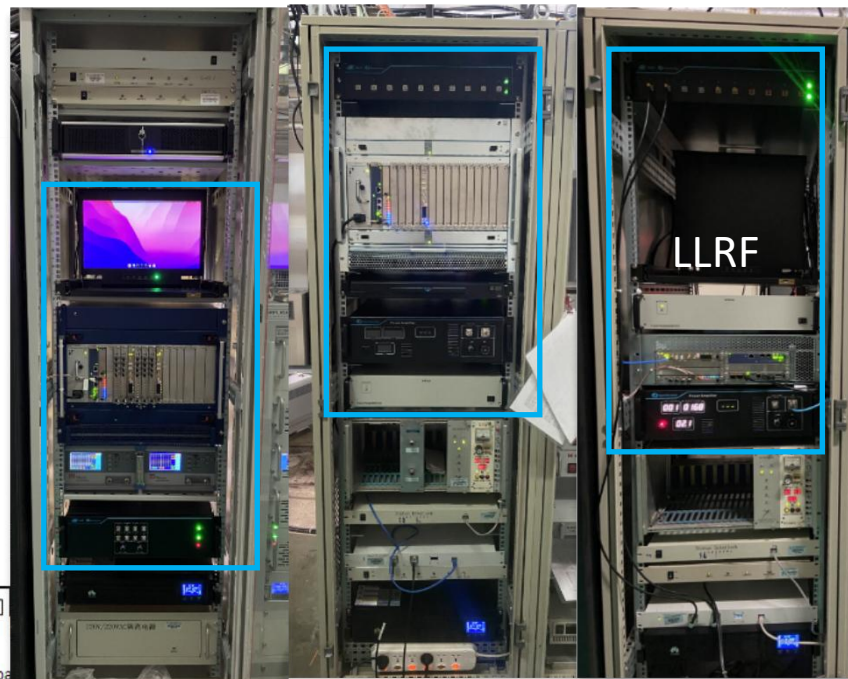
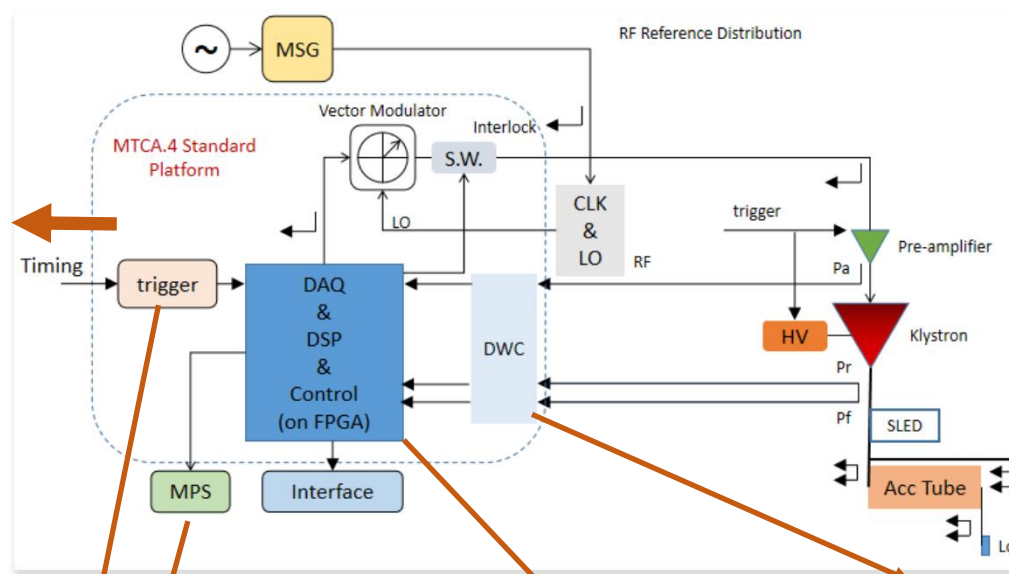


LLRF upgrade on BEPCII-U Linac

■ 24 MTCA hardwares:



MTCA chassis (3U/9U) :
nVent/ELMA...



In-house made
CPU AMC board



In-house made Trig/DIO



DAQ controller



In-house made
DWC RTM 2856MHz

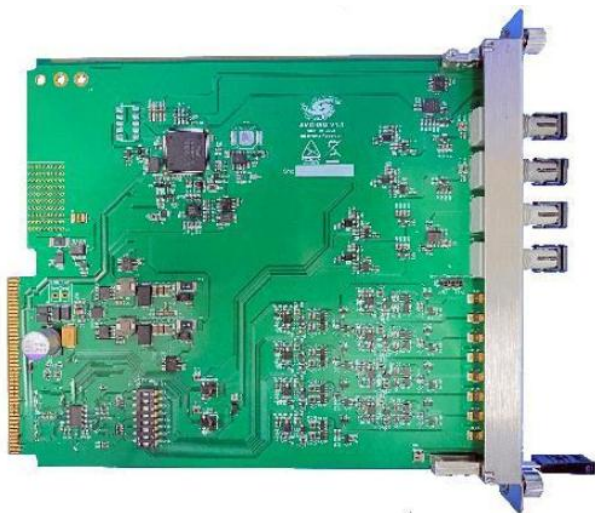


In-house made DS
RTM 142.8/571.2MHz

LLRF upgrade on BEPCII-U Linac

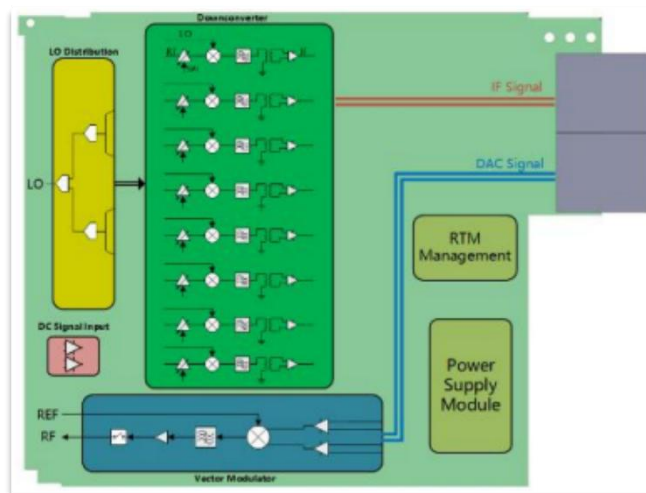
Timing/Digital I/O AMC

- ❑ Double width
- ❑ local timing and protection
- ❑ 8 channels TTL/LVTTL
- ❑ in/out direction configurable
- ❑ Impedance 50 Ohm/Hi-Z
- ❑ **Fanout through backplane**
- ❑ optical 2 in/2 out
- ❑ MMC by I2C: voltage, current, temperature monitoring



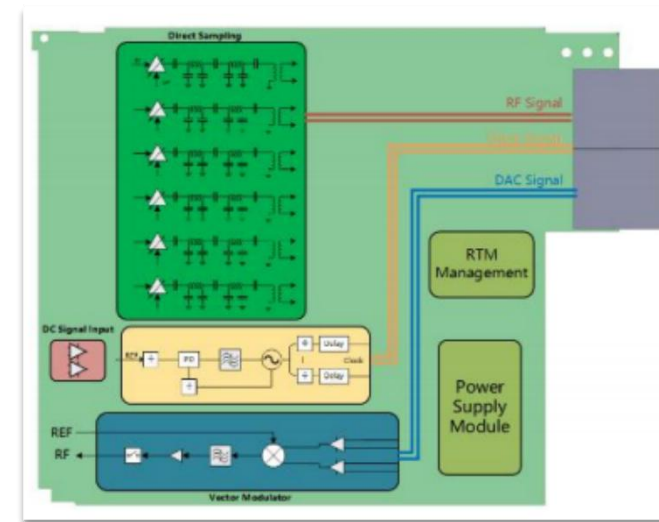
Downconverter RTM

- ❑ MicroTCA.4 RTM, Class A1.1
- ❑ 6 channels **600M-6GHz DWC**
- ❑ 6 IF 5-100MHz
- ❑ 1 channel VM UPC 50M-6GHz
- ❑ 2 channels DC input (MMCX)
- ❑ LO/REF power monitor
- ❑ adjustable in/output attenuation
- ❑ 4 channels TTL digital I/O
- ❑ connector: SMP



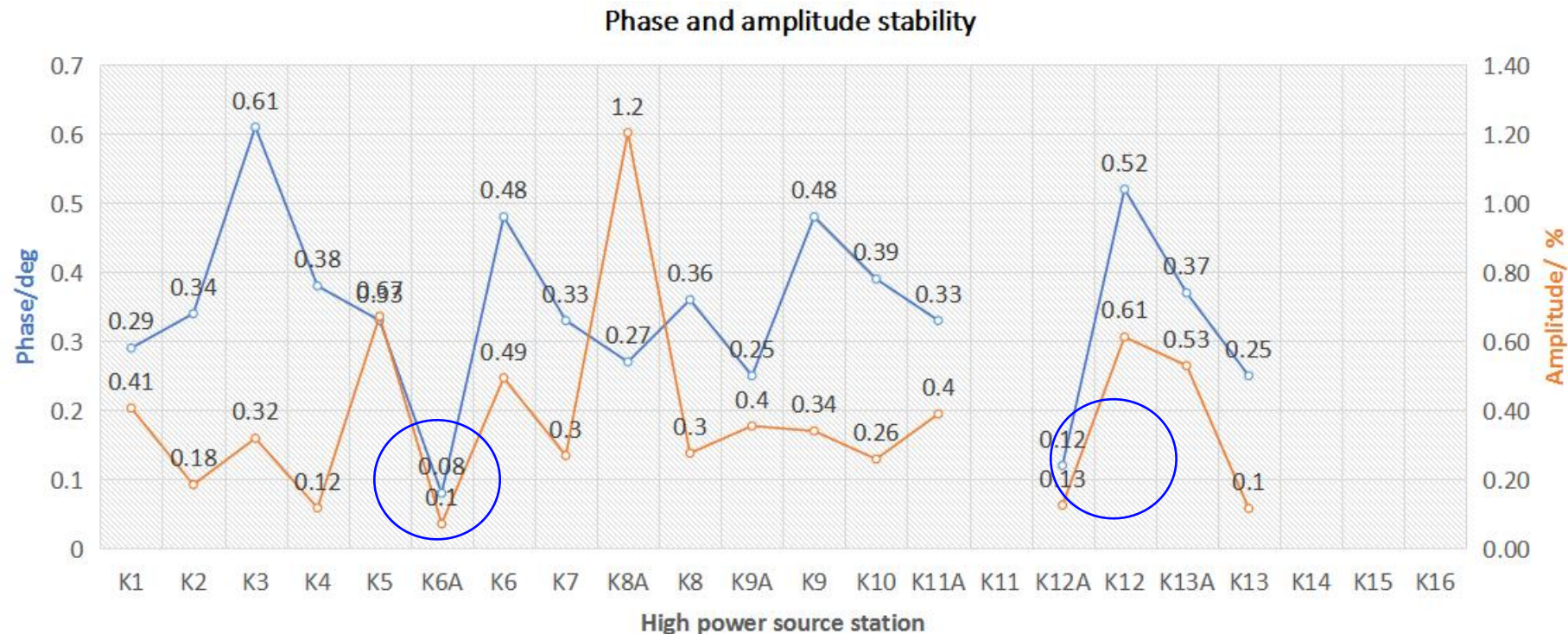
Direct-sampling RTM

- ❑ MicroTCA.4 RTM, Class A1.1
- ❑ 6 channels **DC-600MHz DS**
- ❑ 1 channel VM UPC 50M-6GHz
- ❑ dual-PLL, 100M-2GHz input
- ❑ LO/REF power monitor
- ❑ 4 channels TTL digital I/O
- ❑ connector: SMP
- ❑ I2C interface



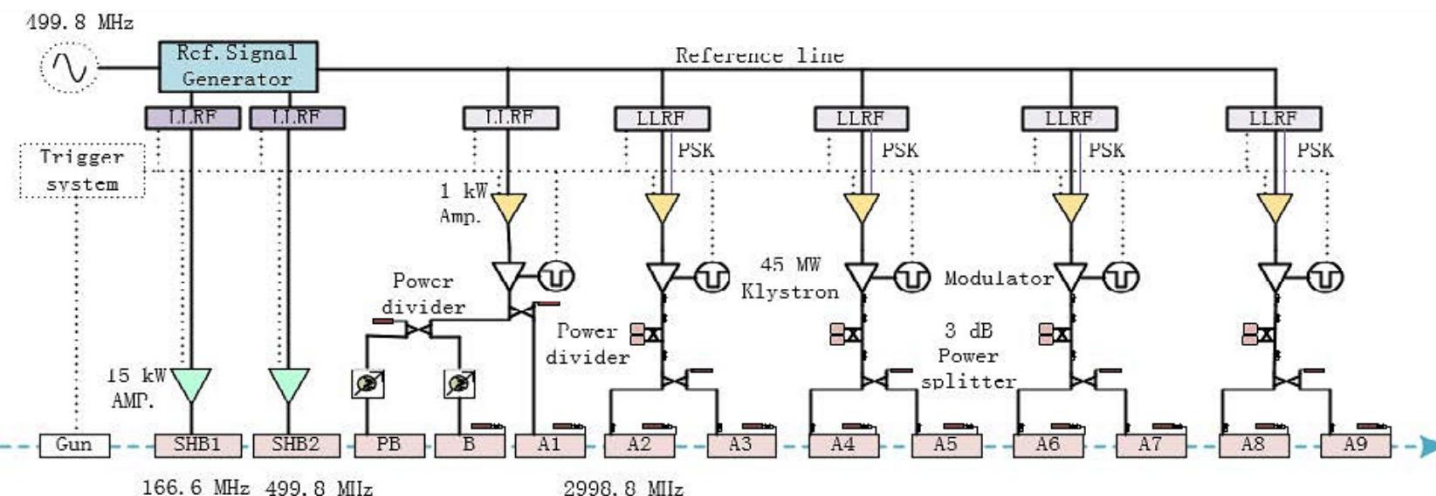
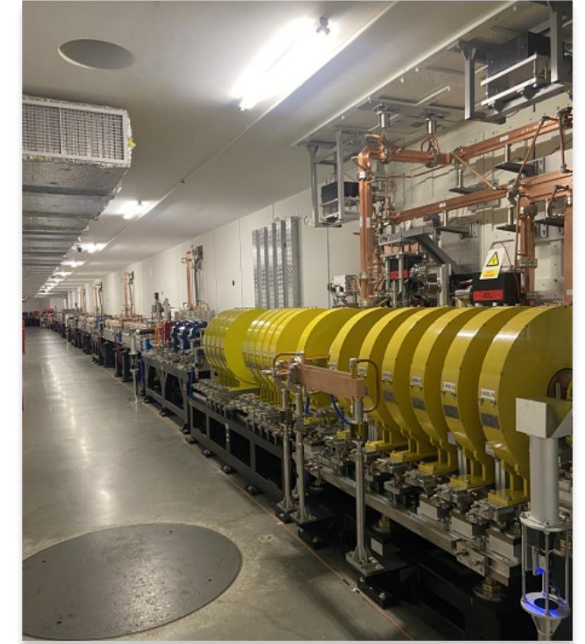
LLRF upgrade on BEPCII-U Linac

- **S-band LLRF Performance:** $\varphi < 0.6\text{deg(p-p)}$ and $A < 1\%(p-p)$, short term error **4 times reduction**, PFN type modulators used for klystrons.
- Two new K6A and K12A power sources are **solid state modulators**, stability are further improved, 0.08deg(p-p) and $0.1\%(p-p)$
- Linac beam arrival time jitter and energy stability much better, contributing **to PWFA!**



HEPS Linac

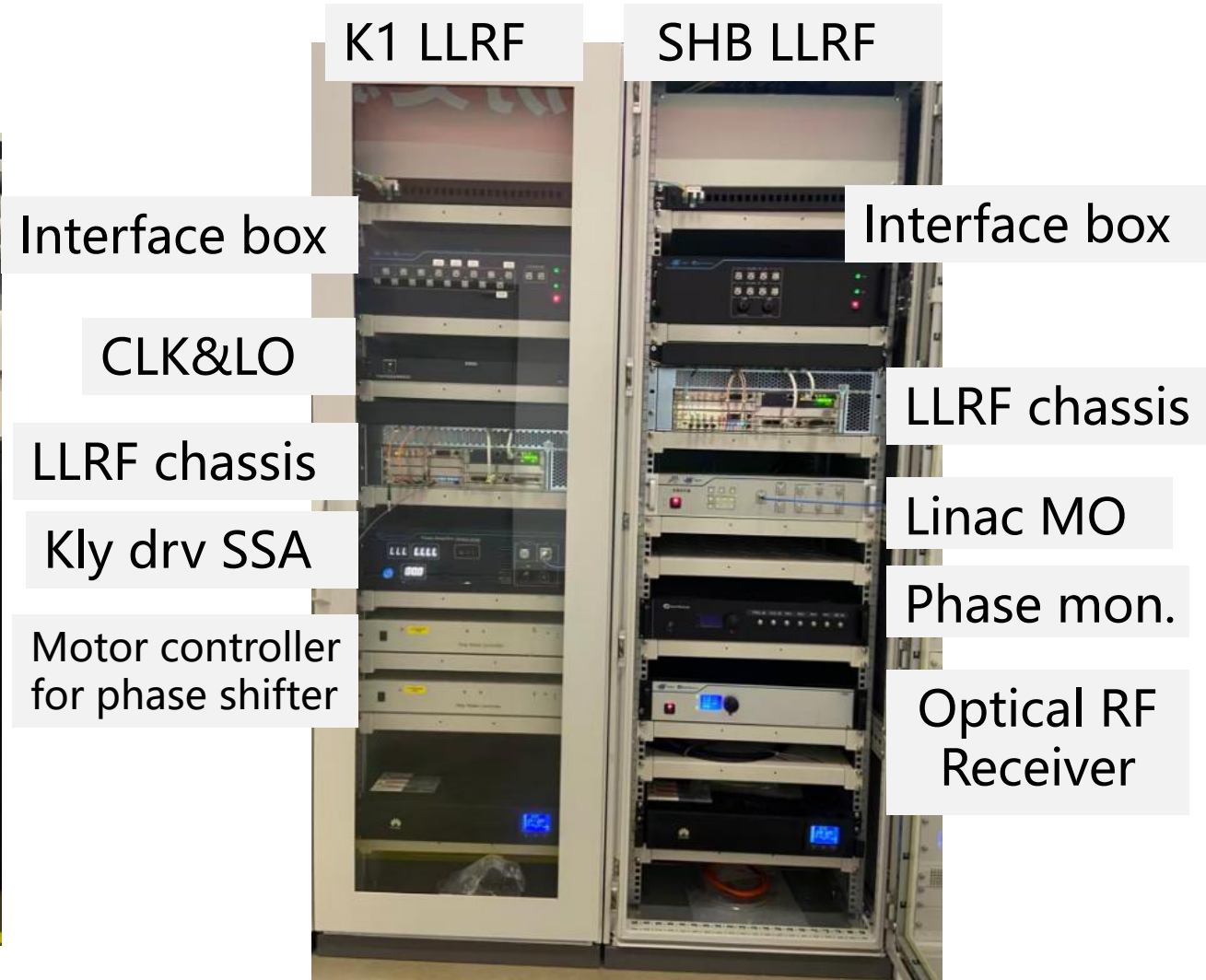
- 500MeV 4us pulsed E- accelerator;
- 1x166.6MHz, 1x499.8MHz SHB bunchers, 5x2998.8MHz 45MW klystrons for 9 accel. tubes;
- Rep Rate: 1-50Hz;



LLRF of HEPS Linac

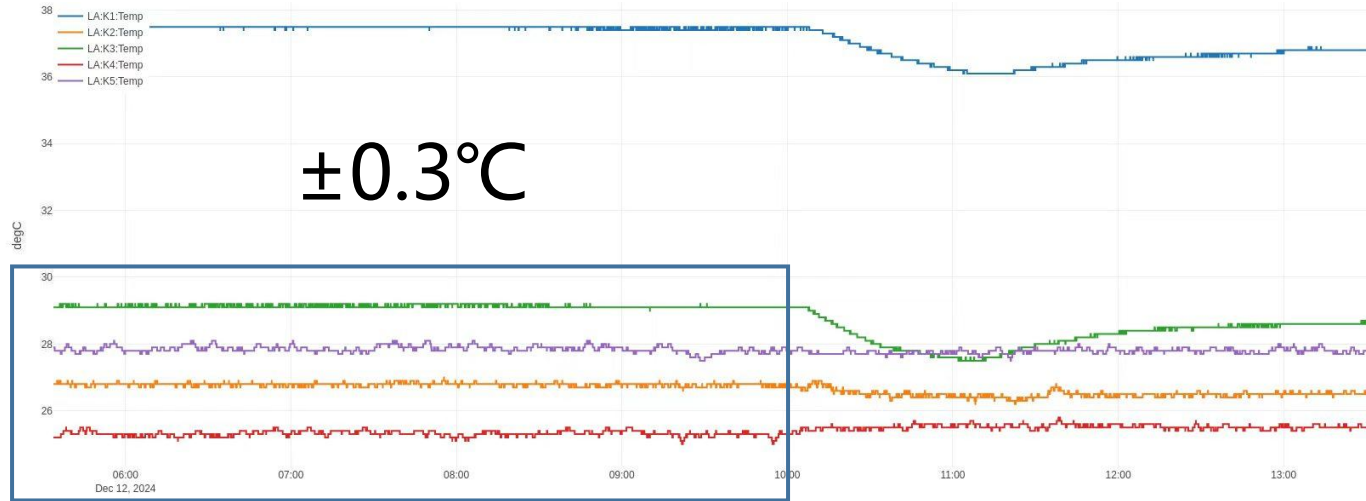
■ 6 LLRF racks

3 years run until now



LLRF of HEPS Linac

■ Temperature stability in the LLRF and environment



← wind blow →



■ Stability of LLRF accelerating gradient

No fault in one year round!
Still no much supervision!

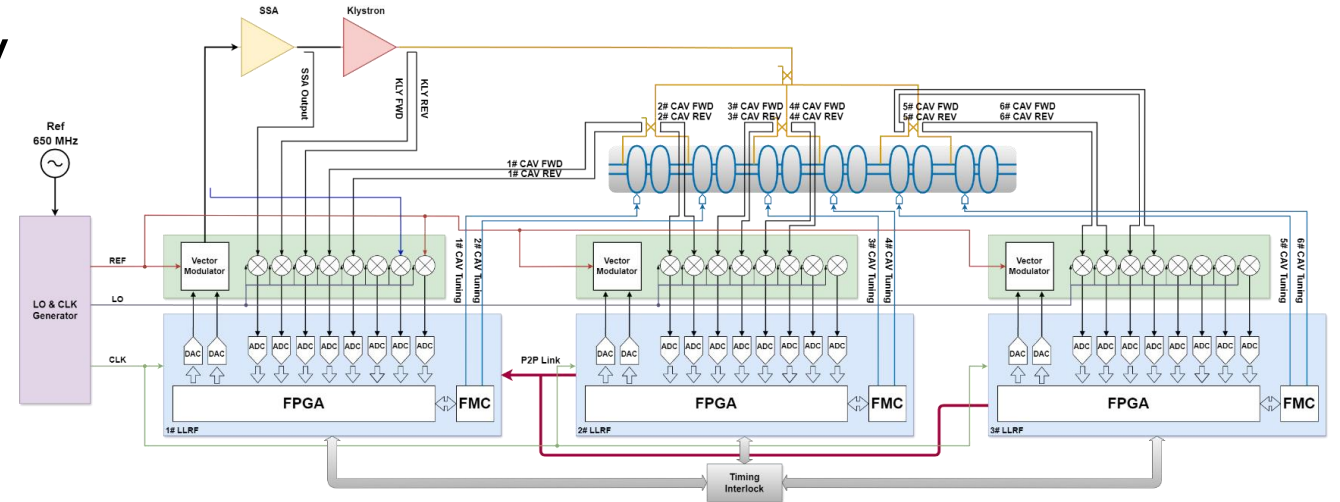


LLRF for superconducting cavities

LLRF for superconducting cavities

- CEPC prototype research - 650MHz and 1.3GHz SC cavities / cryomodules
- 650MHz 2-cell CM: 1 klystron - 6 Cavities
- 1.3GHz 9-cell: 1 SSA-1 Cavity

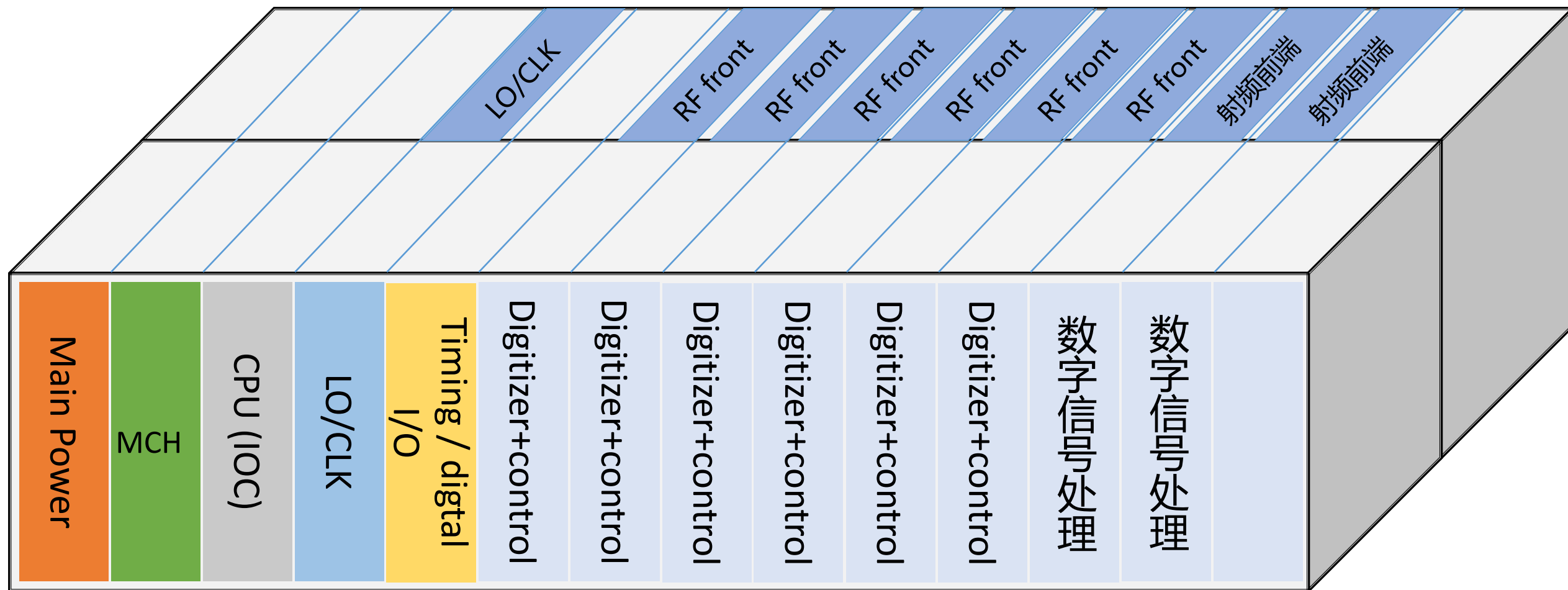
CEPC EDR Full-scale 650 MHz / 1.3GHz cryomodule



LLRF structure

19" MicroTCA.4 standard 9U/10U chassis

RTM: analog interface

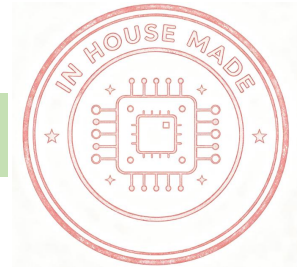


AMC front panel

LLRF structure (standard hardware)

- 1. MicroTCA.4 chassis(PS, fans...)
 - 2. LO/CLK module
 - 3. Digitizer AMC
 - 4. RF front-end RTM
 - 5. FMC (on AMC) for Frequency control
 - 6. CPU AMC
 - 7. Timing/Digital IO AMC
- Can be with EVR
 - Can be with MPS
 - Can be with interlock
 - Most cable in the rear

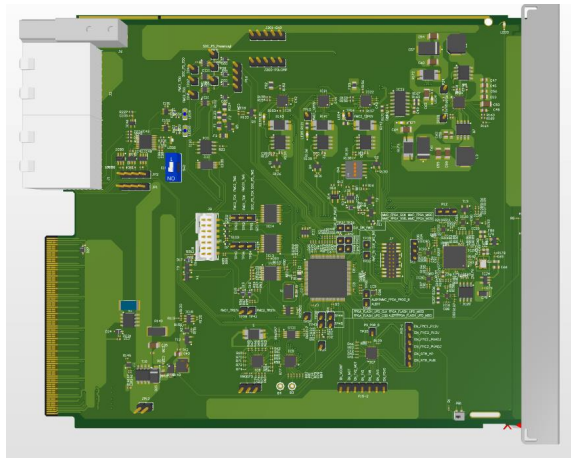
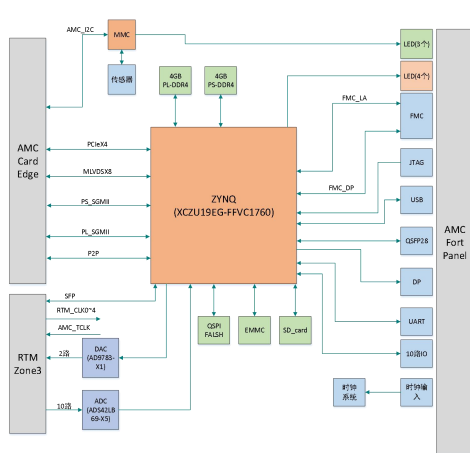
In-house made.



LLRF structure (upgraded digitizer & LO/CLK AMCs)

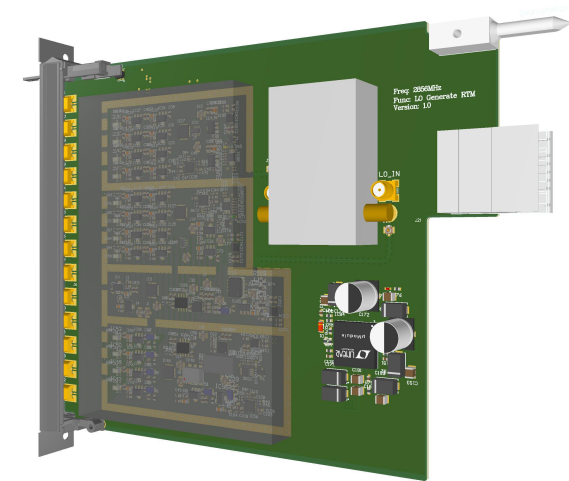
Zynq ultrascale based digitizer:

- Onboard 1 ZYNQ chip, model XCZU19EG-FFVC1760-2-I;
- 8-ch 16bit 250MSPS ADCs, 2-ch 16bit 500MSPS DACs
- The PS side of ZYNQ carries 1 set of DDR chips, with a capacity of 4 GB;
- The PL side of ZYNQ carries 1 set of DDR chips, with a capacity of 4 GB;
- The ZYNQ supports four boot modes: JTAG, SPI-Flash, eMMC, and SD card;
- The board includes 1 FMC connector;
- ZYNQ outputs one QSFP28 optical port to the front panel;
- ZYNQ outputs one DP interface to the front panel;
- The board edge connector (golden finger) supports PCIe x4;
- The board edge connector supports 2 Gigabit Ethernet interface;
- The board edge connector supports one P2P interface, with a data rate of 10 Gbps;



LO/CLK RTM Board – Key Specifications

- Compatible with MicroTCA.4 RTM, supported by MMC protocol with AMC
- 1 × RF reference input
- Generates 3 frequency types, each distributed to 4 output channels (supports up to 4 DWC applications)
- Reference RF frequency: 2856 MHz (prototype version)
- LO frequency: 2879.8 MHz
- CLK frequency: 95.2 MHz
- IF frequency: 23.8 – 26.775 MHz (typical 25 MHz, IF/CLK = 1/4)
- Input signal level: -10 to +10 dBm
- Output signal level: > 13 dBm
- Provides signal power and board status monitoring via I²C bus
- Includes LNA, power divider, IF band-pass filter (23.8 MHz LC), frequency divider
- LNA jitter performance example @499.8 MHz: 21.4 fs (10 Hz–10 MHz)
- PCB in production (Sep. 2025); Version 2 with temperature control and optimization planned for Q4 2025 – Q2 2026



LLRF structure (Universal digital I/O AMC)

- Stable timing and reliable protection are required for healthy run
- Universal digital I/O
 - Signal fanout through backplane
 - Multi-function: LLRF/BI digitizer, Timing EVR/EVG, interlock, frequency tuning
 - Instrumentation utilizing various of FMCs

Zynq Ultrascale based dual-FMC AMC:

- FPGA: Xilinx Zynq Ultrascale+ MPSoC(XCZU19EG-2FFVC1760)
- FMC1: LA/HA/HB,
- FMC2: LA/HA/HB,
- PCIe: PCIe Gen.3 x4
- 2x 1000M Ethernet: 1 to PS and 1 to PL
- 4GB DDR4 (2400 MT/s) to PS
- 4GB DDR4 (2400 MT/s) to PL
- RTM: DESY RTM D1.1 (42 LVDS I/O, 2 HS)



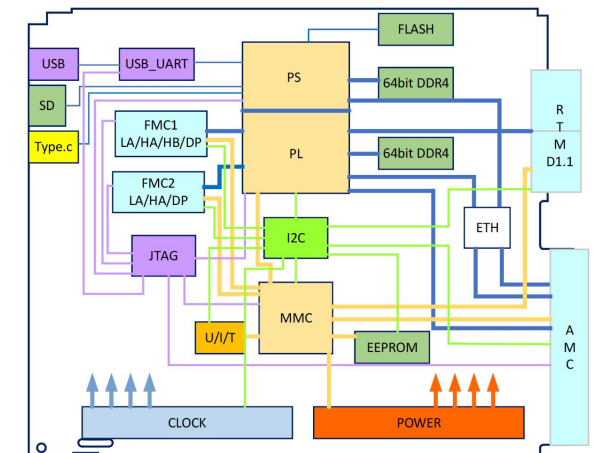
DIO V1.0



DIO V2.0

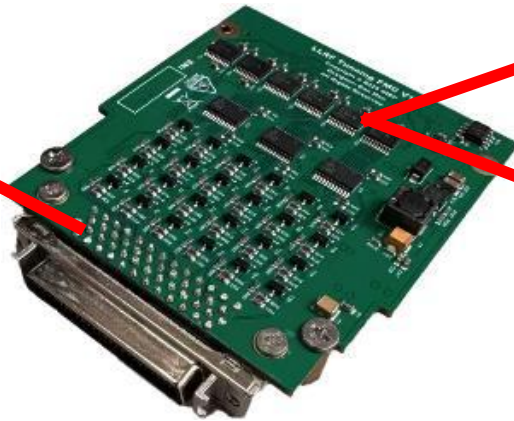
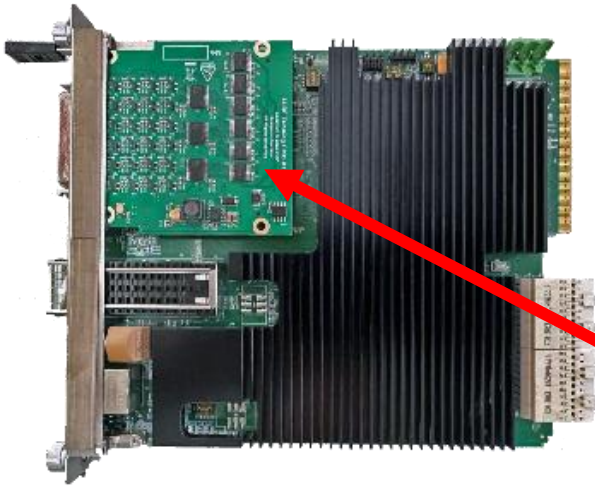


DIO V3.0



LLRF structure (SC Frequency control)

- LPC FMC for frequency control:
- 24 TTL IO for step motor
- 8 serial-output DAC: 0~5V, 0~10V for piezos
- Frequency control algorithm:
- detuning detection: phase error of forward and reverse RF
- Piezo fast compensation: PI + FF
- motor: large range sweep when beyond piezo limits
- mix of piezo and motor



Future plans

- Make more efforts on the firmware and software of new MTCA boards
- Extend and upgrade core-function boards
- System integration and applications

Thank you for your attention!