



中國科學院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

A High-Performance Digitizer for LLRF Systems Based on MicroTCA.4

Gan Nan

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目录
contents

- 1. Project & Board Overall Scheme**
- 2. Board Hardware Design**
- 3. Firmware & Software**

1

Project & Board Overall Scheme

1.1 Project Background

- **Background** — The AMC-ZU19EG digitizer board is developed specifically for digital Low-Level RF (LLRF) systems at IHEP.
- **Platform evolution** — in earlier IHEP projects, digital signal processing relied on the SIS8300L2 board (Virtex-6 FPGA); a digital board based on the Zynq-7045 was subsequently developed in-house.
- **Limitations of the existing platforms**
 - FPGA resources** — increasingly complex LLRF algorithms push resource utilization too high, and timing closure becomes difficult
 - Analog front end** — the ADC sampling rate of 125 MSPS is a limitation for direct-sampling LLRF architectures
 - Memory resources** — only 1 GB + 1 GB of DDR3; insufficient to buffer long multi-channel waveform records, with too little bandwidth for real-time processing and data streaming
- **Objective** — Upgrade the hardware platform to remove these bottlenecks



1.2 Board Overview and Key Specifications

- AMC ZU19EG board is designed as a high-performance processing platform for high-speed data acquisition, real-time signal processing, synchronization, and high-bandwidth data transmission in a MicroTCA.4 system.
- The board is based on a Zynq UltraScale+ MPSoC (XCZU19EG) and integrates an 8-channel 16-bit 250 MSPS ADC acquisition front end, a 2-channel 16-bit 500 MSPS DAC generation channel, dual 4 GB 64-bit DDR4 memory, a programmable clock and synchronization system, high-speed serial links (PCIe x4 Gen3, QSFP28, P2P, MLVDS x8), and a module management controller.
- Current status: Hardware development, functional validation, and firmware/software implementation are complete.

Item	Specification
ADC	4x ADS42LB69 (dual-channel) — 8 ch, 16-bit, up to 250 MSPS
DAC	1x AD9783 — 2 ch, 16-bit, up to 500 MSPS, analog to Zone3
Memory	PS DDR4 4 GB (64-bit) + PL DDR4 4 GB (64-bit)
Backplane	PCIe x4 Gen3 · 2x GbE · 8x MLVDS · P2P 10 Gb/s
Front panel	QSFP28 100G · Mini-DP · USB OTG · FT4232 JTAG/UART
Expansion	FMC LPC · Zone3 RTM (SFP, 5+1 clocks)
Boot	JTAG / QSPI 512 Mb / eMMC 32 GB / SD card
Management	hot-swap, power sequencing, monitoring

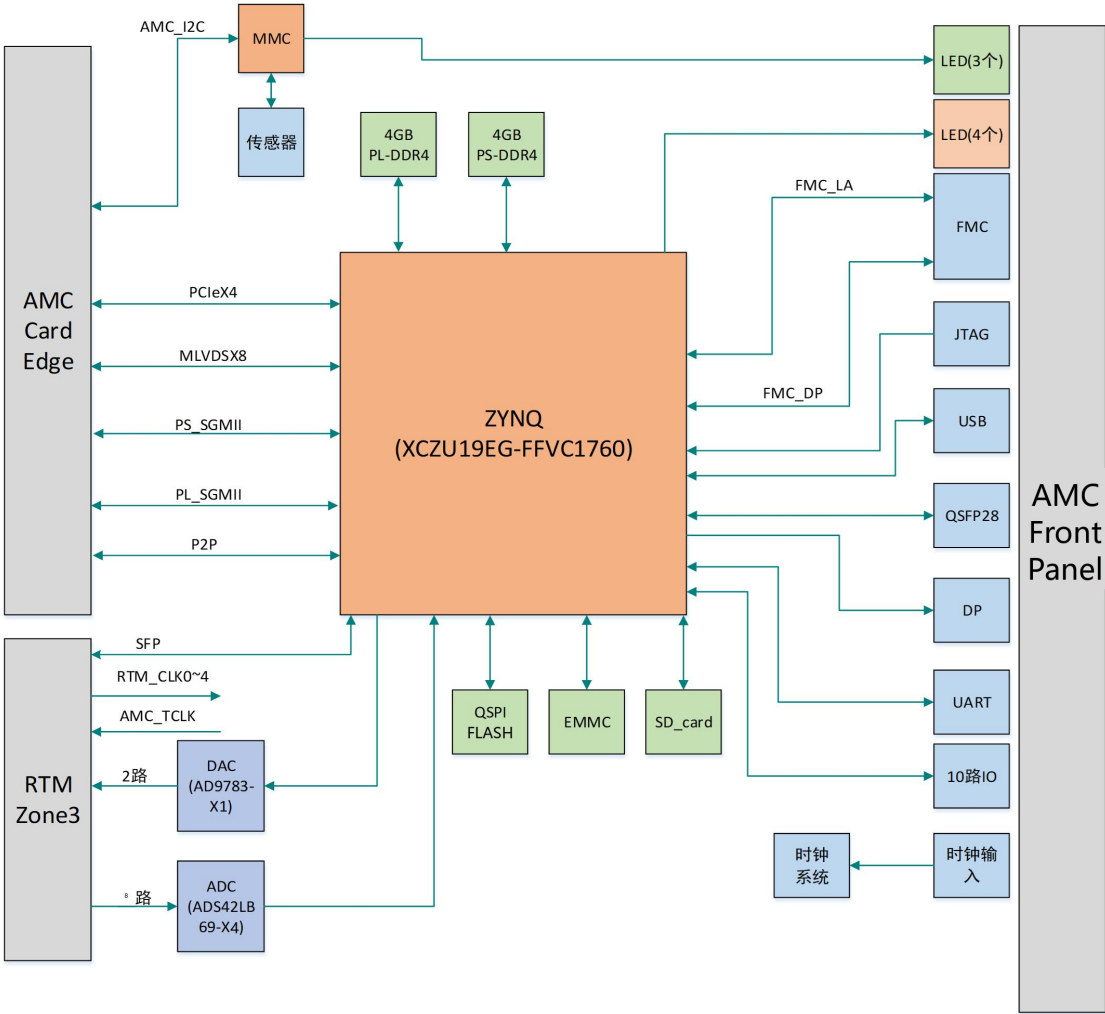


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1.3 System Architecture

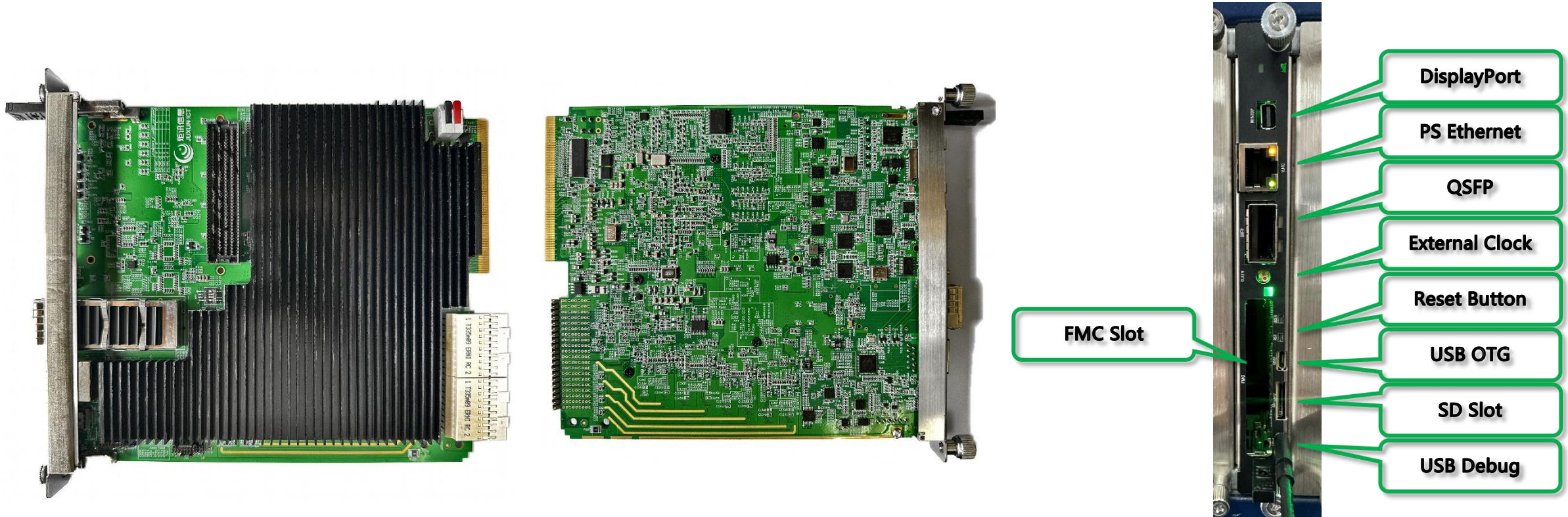


AMC port	Function
Port 0-1	PL SGMII — 1 GbE
Port 4-7	PCIe x4 (Gen3)
Port 12	P2P — 10 Gb/s
Port 17-20	MLVDS x8 — direction controlled by ZYNQ
TCLKA / TCLKB	Backplane clock inputs (2+2 differential)
FCLKA	PCIe reference clock

Front panel	Function
QSPF28	100 Gb/s optical (GTY bank 128)
Mini-DP	DisplayPort output (PS GTR)
USB OTG	Micro-USB host / device (USB3320 PHY)
UART / JTAG	Micro-USB via FT4232 (2x UART + JTAG + MMC ISP)
CLK IN	SSMB external reference clock
Others	Reset button · 2+2 LEDs (PS/PL) · SD slot

1.4 Mechanical Form Factor and PCB Layout

- **Form factor** — AMC double-width, mid-size 4 HP — 148.8 × 18.96 × 181.5 mm



2

Board Hardware Design

2.1 Component Selection (ZYNQ UltraScale+)

Selection Principles:

- 1.Prioritize ZYNQ UltraScale+ series chips with a larger number of configurable I/O ports to ensure the versatility and applicability of the AMC digitizer board.
- 2.Consider cost-effectiveness and availability in the Chinese market.
- 3.Ensure package portability for potential design adjustments.

AMD Zynq™ UltraScale+™ MPSoCs															
			ZU1	ZU2	ZU3	ZU3T	ZU4	ZU5	ZU6	ZU7	ZU9	ZU11	ZU15	ZU17	ZU19
Pkg Footprint ^(2,3)	Dimensions (mm)	Ball Pitch (mm)	PS I/Os ⁽¹⁾ , 3.3V HD I/O, 1.8V HP I/Os PS-GTR 6 Gb/s, GTH 16.3 Gb/s, GTY 32.75 Gb/s												
A494	9.5x15	0.5	170, 24, 58 4, 0, 0												
A530	9.5x16	0.5		170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A484	19x19	0.8	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0										
A625	21x21	0.8	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0										
C784 ⁽⁴⁾	23x23	0.8	214, 24, 156, 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 72, 52 4, 4, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
D784 ^(4,5)	23x23	0.8				214, 72, 52 4, 8, 0									
E784 ^(4,5)	23x23	0.8					214, 72, 58 4, 8, 0	214, 72, 58 4, 8, 0							
B900	31x31	1.0					214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0					
C900	31x31	1.0							214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		
B1156	35x35	1.0							214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		
C1156	35x35	1.0								214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0			
B1517	40x40	1.0										214, 72, 416 4, 16, 0		214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
F1517	40x40	1.0								214, 48, 416 4, 24, 0		214, 48, 416 4, 32, 0			
C1760	42.5x42.5	1.0										214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16
D1760	42.5x42.5	1.0												214, 48, 260 4, 44, 28	214, 48, 260 4, 44, 28
E1924	45x45	1.0												214, 96, 572 4, 44, 0	214, 96, 572 4, 44, 0

2.2 Zynq Resource and Interface Planning

- The XCZU19EG was selected not only for its programmable logic resources, but also for its extensive I/O and high-speed transceiver capability.
- The board requires simultaneous support for two DDR4 interfaces, multiple LVDS interfaces, FMC connectivity, PCIe, SGMII, QSFP28, P2P communication, DisplayPort, and RTM high-speed links. Therefore, device package selection and bank-level resource allocation were key design tasks.



Zynq Resource	Main Application
PS DDR Bank	PS DDR4
HP Banks	PL DDR4, ADC LVDS, MLVDS
HD Banks	FMC LA interfaces
PS GTR	PS SGMII, DisplayPort
GTH	PCIe, PL SGMII, FMC/JESD interfaces
GTY	QSFP28 and other high-speed links

2.3 Memory and Boot Configuration

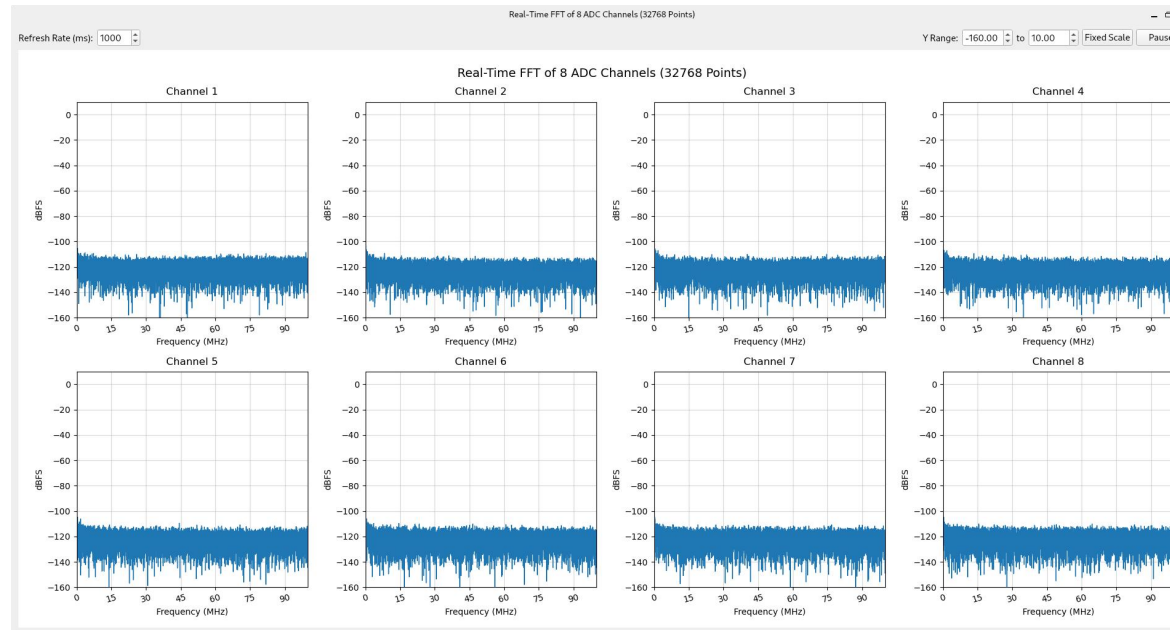
Device	Configuration
PS DDR4	4 GB, 64-bit — 4x MT40A512M (2400 MT/s)
PL DDR4	4 GB, 64-bit — 4x MT40A512M (2400 MT/s)
QSPI Flash	MT25QU512 — 512 Mb, dual-parallel
eMMC	MTFC32G — 32 GB
SD card	On-board slot (bottom side)

MODE[3:0]	Boot device
0000	JTAG
0010	QSPI Flash
0011	SD Card
0110	EMMC

Four boot options: JTAG for development, QSPI / eMMC for production, SD for field update. QSPI, eMMC and SD are served by the PS I/O peripherals (banks 500–504).

2.4 ADC Acquisition Channels

- **Devices** — 4x TI ADS42LB69 dual-channel ADC → 8 acquisition channels from Zone3 (RTM)
- **Performance** — **16-bit resolution, up to 250 MSPS per channel. Analog bandwidth extended from 650 MHz (AD9268) to 900 MHz, improving direct-sampling performance**
- **Data interface** — LVDS DDR/QDR links to ZYNQ HP banks 64–67
- **Sampling clock** — AD9512 #1/#2 — sources: on-board oscillator, front panel, backplane, FMC, RTM (via Si5394 / mux / fan-out)



Noise floor of 8 Channel ADC

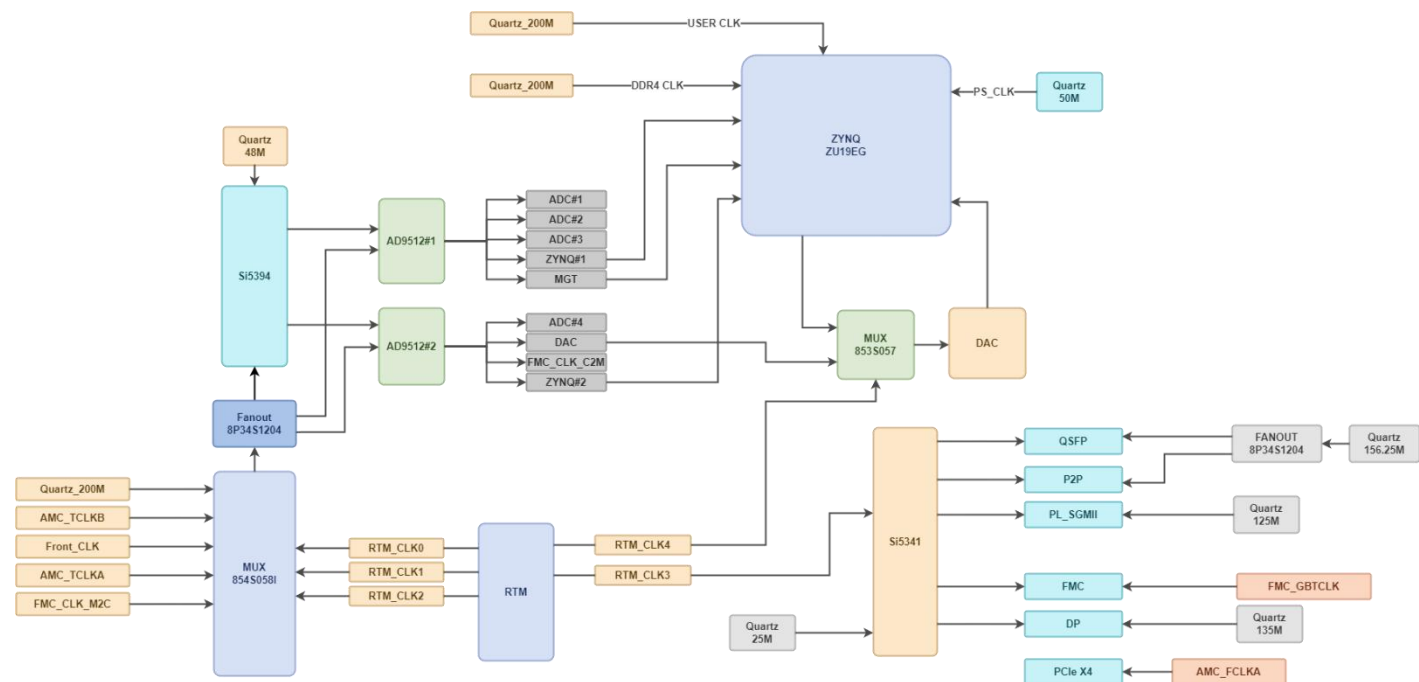
2.5 Clock and Synchronization Architecture

- A flexible multi-source clock architecture supports ADC/DAC sampling, Zynq system operation, high-speed transceivers, RTM/FMC interfaces, and precision synchronization.

Five major clock domains are considered:

1. ADC sampling clocks
2. DAC sampling clock
3. Zynq PS/PL system clocks
4. Zynq MGT reference clocks
5. External and synchronization clocks

- ADC sampling clocks may originate from the onboard oscillator, front-panel clock input, AMC backplane, FMC, or RTM.
- Clock multiplexers and fan-out devices route the selected source either directly to the AD9512 devices or through the Si5394 clock generator before distribution to the ADCs.

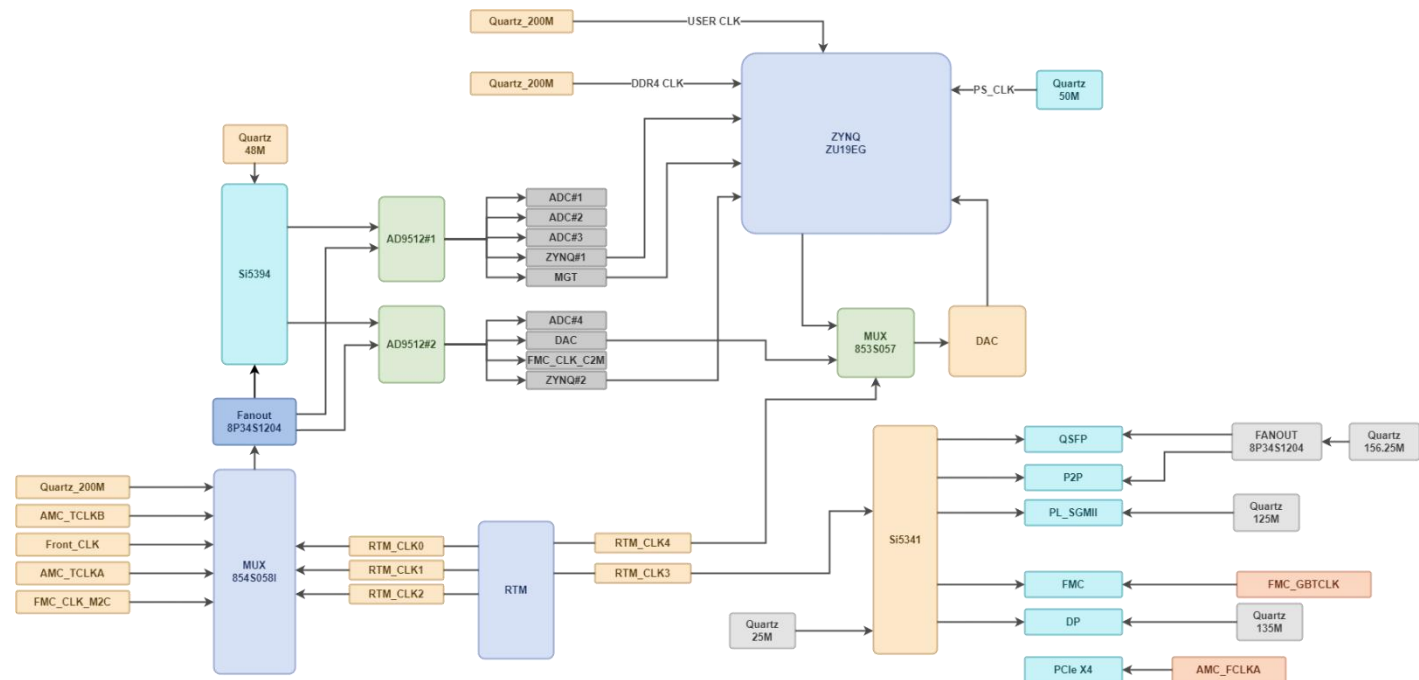


2.6 MGT Reference Clocks

- Independent reference-clock paths support PCIe, QSFP28, P2P, SGMII, FMC and RTM links while keeping transceiver timing separate from converter sampling clocks.

MGT Reference Clocks:

- **Si5341** — primary MGT reference: QSFP, P2P, PL/PS SGMII, FMC, RTM SFP, DP
- **PCIe** — reference from backplane FCLKA (per MicroTCA.4); backup from 100 MHz oscillator + 5V41234
- **Secondary refs** — 156.25 MHz oscillator fan-out (QSFP / P2P / FMC GBTCLK), 125 MHz (PL SGMII)
- **Control** — mux / fan-out (853S057 / 8P34S1204) from PL; RTM clock mux from MMC



2.7 MMC Functions and Board Monitoring

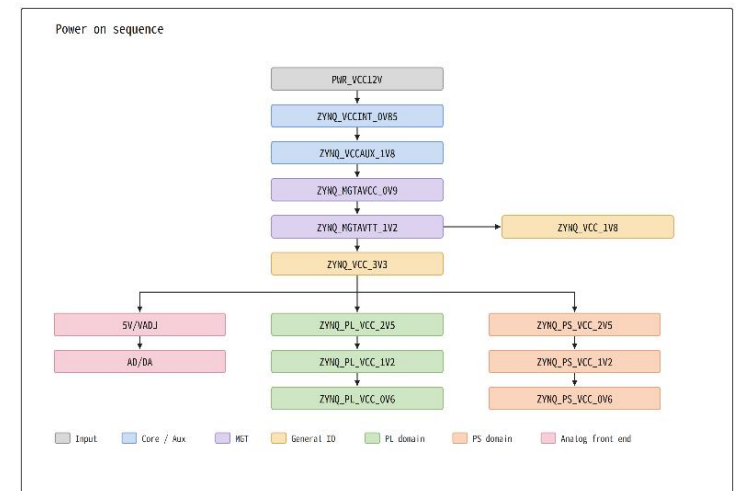
- Module Management Controller operates independently of the Zynq PS/PL. It is responsible for board management, power sequencing, hot-swap handling, system monitoring, and AMC/RTM management communication.

Management functions

- **Hot-swap & power** — AMC hot-swap management, 12 V power enable control (both standalone and in chassis)
- **Identification & bus** — GA[2:0] slot identification, AMC management I²C (IPMB)
- **RTM** — RTM presence detection (RTM_PS#), RTM management I²C
- **Config** — clock generator config on boot
- **Power Sequencing** — defines the order in which the board's supply rails must be established, from the 12V input through to the PL and PS domains, so the ZYNQ starts up reliably and without damage.

Board monitoring

- **Temperature** — MAX6604 and LM75, placed at the power converters, Zynq, ADC and DAC sections
- **Voltage/Current** — INA3221, 3-channel sampling, read by the MMC
- **Status reporting** — FRU information, sensors and hot-swap state reported to the MCH via IPMI



2.8 MMC Status in the MicroTCA Chassis

- Chassis tests confirm that the MCH enumerates both AMC modules, reads voltage/current and temperature sensors, and receives FPGA and PS status.

```
nat> show_fru

FRU Information:
=====
FRU  Device  State  Name
=====
0    MCH      M4     NAT-MCH-CM
3    mcmc1    M4     NAT-MCH-MCMC
5    AMC1     M1     CPU
7    AMC3     M4     AMC ZU19EG
9    AMC5     M4     AMC ZU19EG
40   CU1      M4     Cooling Unit
50   PM1      M4     PDM
60   Clock1   M4     MCH-Clock
61   HubMod1  M4     MCH-PCIE
=====
```

```
nat> show_sensorinfo 9
Sensor Information for FRU 9 / AMC5
=====
#   SDType  Sensor Entity Inst  Value  State  Name
=====
-   MDevLoc      0xc1 0x65      AMC ZU19EG
2   Compact  0xf2 0xc1 0x65 0x01    HOTSWAP AMC
3   Full      Voltage 0xc1 0x65 0.832 V  ok     ZYNQ 0V85
4   Full      Voltage 0xc1 0x65 0.624 V  ok     PL 0V6
5   Full      Voltage 0xc1 0x65 3.393 V  ok     ZYNQ 3V3
6   Full      Voltage 0xc1 0x65 11.904 V ok     AMC +12V
7   Full      Voltage 0xc1 0x65 0.000 V  ok     RTM +12V
8   Full      Voltage 0xc1 0x65 0.000 V  ok     FMC +12V
9   Full      Current 0xc1 0x65 2.976 A  ok     AMC +12V Curr
10  Full      Current 0xc1 0x65 0.000 A  ok     RTM +12V Curr
11  Full      Current 0xc1 0x65 0.000 A  ok     FMC +12V Curr
12  Full      Temp    0xc1 0x65 61 C    ok     ZYNQ TEMP
13  Full      Temp    0xc1 0x65 37.5 C  ok     BOARD TEMP 0
14  Full      Temp    0xc1 0x65 44.0 C  ok     BOARD TEMP 1
17  Compact  0xc0 0xc1 0x65 0x01    FPGA DONE
18  Compact  0xc0 0xc1 0x65 0x00    PS ERROR OUT
19  Compact  0xc0 0xc1 0x65 0x00    PS ERROR STATUS
20  Compact  0xc0 0xc1 0x65 0x00    INA CRITICAL
21  Compact  0xc0 0xc1 0x65 0x01    INA PV
22  Compact  0xc0 0xc1 0x65 0x01    INA TC
23  Compact  0xc0 0xc1 0x65 0x00    INA WARNING
24  Compact  0xc0 0xc1 0x65 0x00    TEMP ALERT
25  Compact  0xf0 0xc1 0x65 0x10    HS 009 AMC5
=====
```

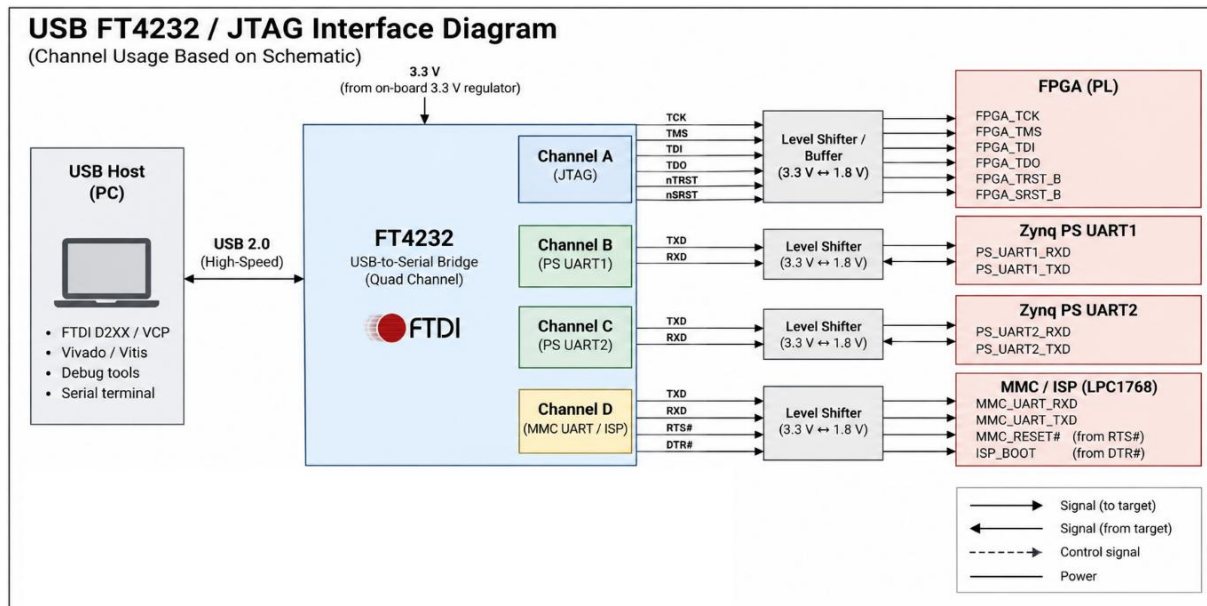
MMC status on NAT-MCH

- FRU enumerated - 2x AMC ZU19EG detected, hot-swap state M4
- Power status - FPGA core voltage
AMC/RTM Payload voltage/current
- Board temperatures and FPGA temperature monitored
- FPGA_DONE, PS system status and power-fault status reported to MCH

2.9 Debug and Configuration Interfaces

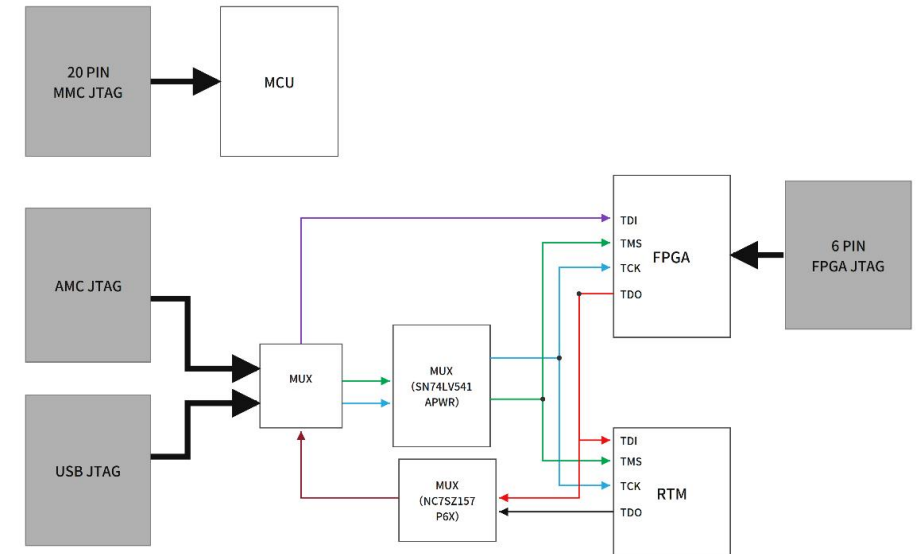
Debug channels & level shifting

- Single Micro-USB connector exposes four channels: PL JTAG, PS UART1/2, MMC UART/ISP
- Level shifters adapt the 3.3 V USB side to the 1.8 V FPGA banks
- Channel D drives MMC firmware update
- FTDI D2XX / VCP drivers — supported by Vivado / Vitis and serial terminals



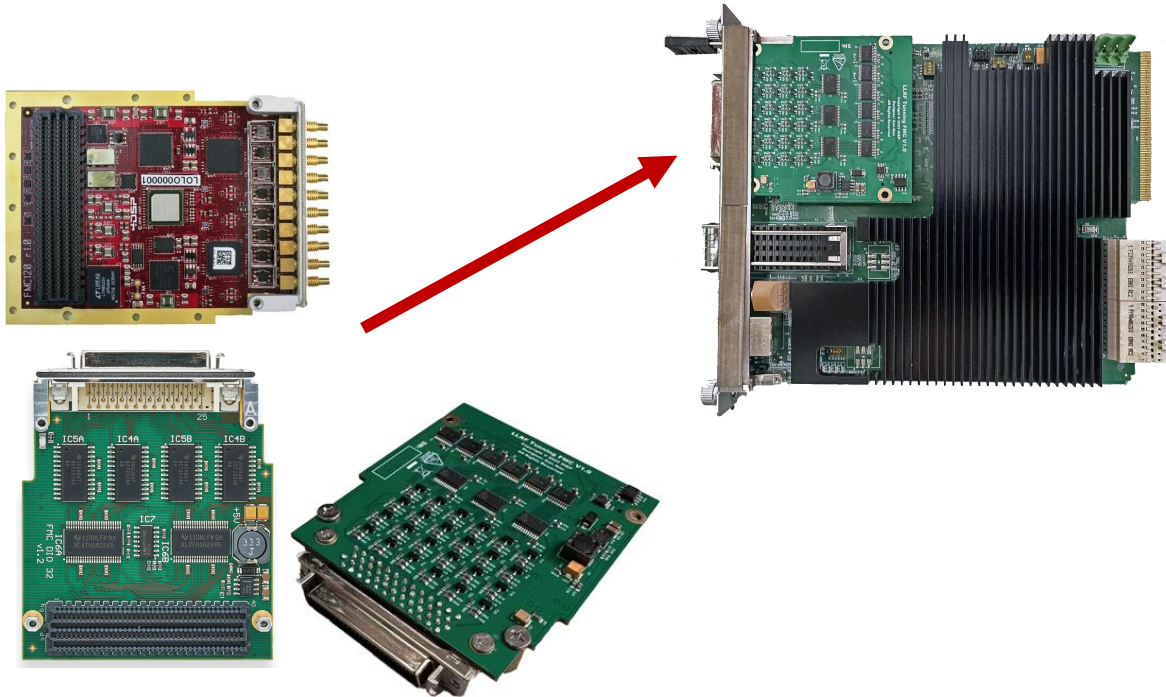
JTAG routing & headers

- Sources: on-board USB JTAG (FT4232 Ch A) or AMC backplane JTAG, selected by a MUX
- Buffered to the FPGA PL; TDO returned through a mux
- Chain extends to the RTM for rear-module programming
- Dedicated headers: 6-pin FPGA JTAG, 20-pin MMC (MCU) JTAG



2.10 FMC and Zone3 (RTM) Expansion Interfaces

- **FMC HPC:** 34 LA differential pairs → HD banks 90/91/93/94 · four bidirectional GTH lanes (DP0–DP3) → GTH bank 231 · GBTCLK0 reference from FMC
- **Zone3 (RTM)** — analog I/O: 10x ADC in / 2x DAC out · RTM clocks: 5 in / 1 out



Zone3	Signals
J31 (analog)	CH0–CH7 ADC inputs (TF: AC / PA: DC coupled) · DAC0/DAC1 outputs (current/voltage)
J30 (clk/SFP)	RTM_CLK0–4 inputs · AMC_TCLK output (TCLKA/B via MMC mux)
Note	TF = AC-coupled, PA = DC-coupled

3

Firmware & Software

3.1 Firmware Architecture

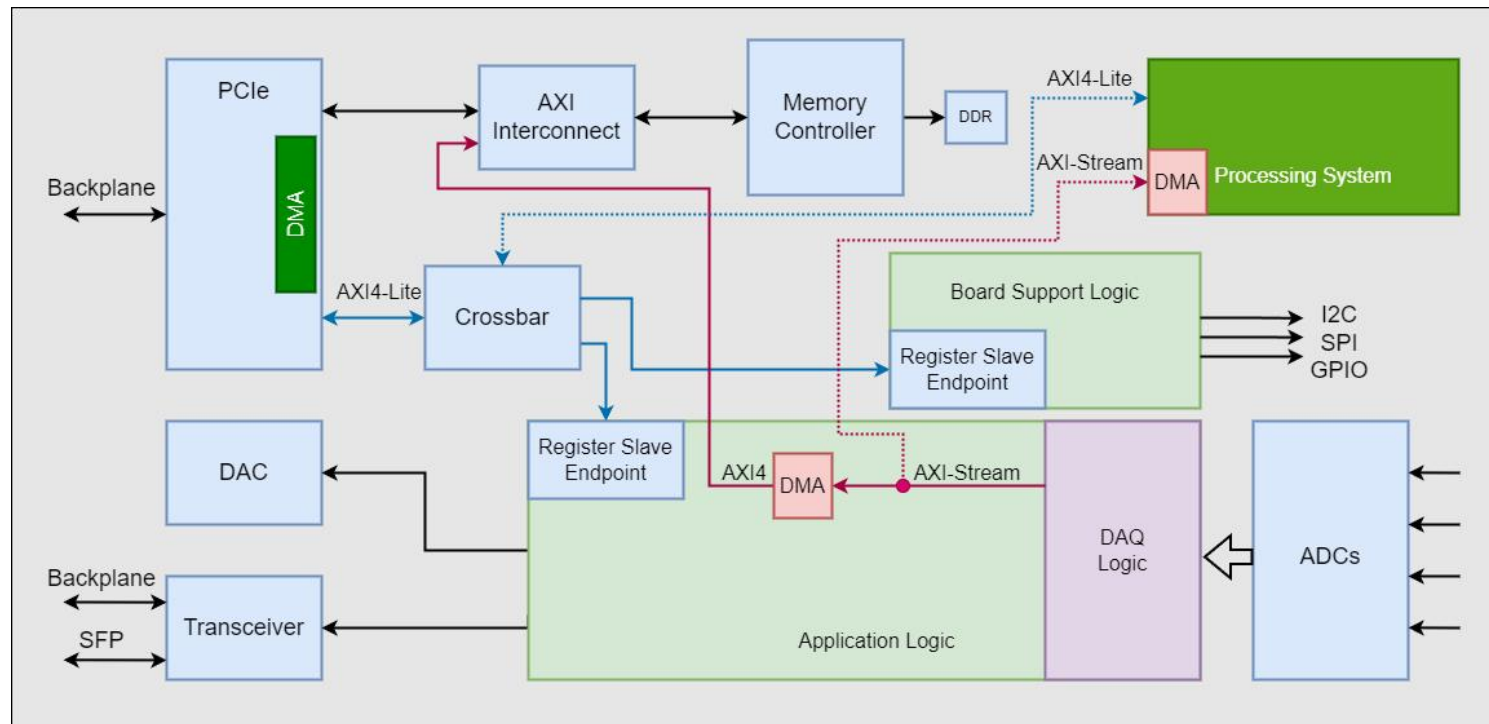
- The firmware top level has only two layers — a Board Support Package (BSP) that hides all board resources, and an application layer that carries the LLRF functionality:

- BSP

PCIe, DMA, DDR, configuration of peripherals on the board (clocks, I/O buffers, ADCs, DACs, etc.)

- APP

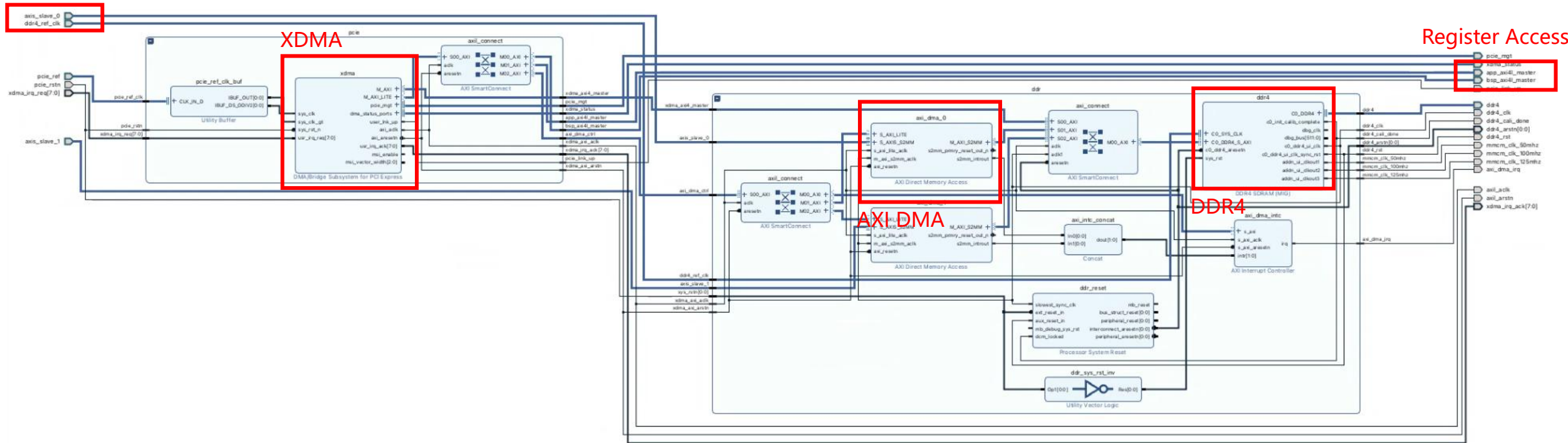
User specific algorithms (LLRF control , DAQ logic, etc.)



3.2 PCIe block design

- Xilinx XDMA provides register access and multi-channel DMA between the FPGA and host memory.
 - The open-source driver avoids project-specific kernel-driver development.
 - A 512-bit DAQ stream feeds the bulk-data path while AXI-Lite handles control registers.

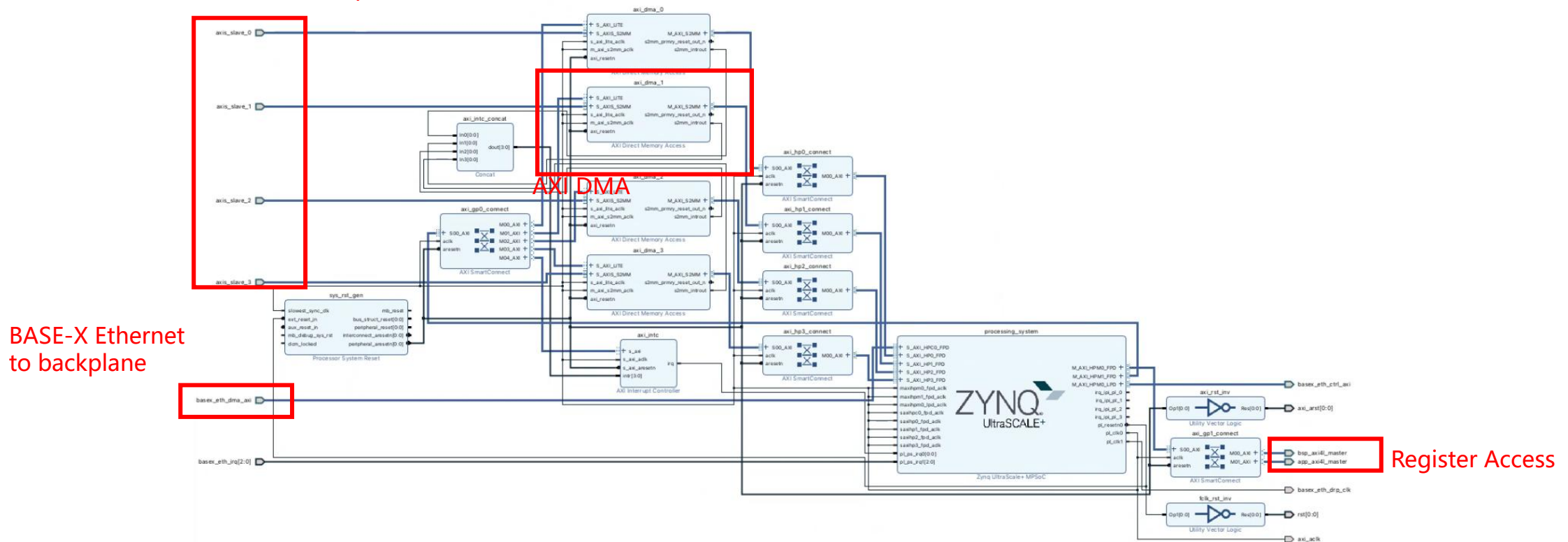
DAQ Stream Input (512bit width)



3.3 Processing system block design

- The processing-system path supports stand-alone acquisition and control without a host PC.
 - Four 128-bit acquisition streams feed AXI DMA and PS DDR4.
 - An embedded EPICS IOC provides control and data access over Ethernet.

DAQ Stream Input (128bit width each)



3.4 Software Stack and EPICS Integration

Layer	Role	Deliverable
Kernel driver (amc-dev)	XDMA PCIe devices: control, DMA, events, JTAG-XVC	/dev/amc-dev/slotN/*
User-space library (USpaceIF)	Register mapping, DMA threads, board identification	Static / shared library
EPICS IOC	Board support + LLRF system	Ilrf IOC, PetaLinux (aarch64)
Phoebus GUI	Operation panels	BOY/Phoebus displays

- **One code base, two boards** — the IOC selects AMC-7Z045 / AMC-ZU19EG at start-up; installation builds a source-free, relocatable runtime package
- **Control paths** — registers via PCIe (host) or PS Linux (stand-alone operation); waveform data via DMA to both PCIe host and PS DDR4

4.1 Firmware Resource Utilization

Resource	Utilization	Available	Utilization %
LUT	166035	218600	75.95
LUTRAM	5519	70400	7.84
FF	183072	437200	41.87
BRAM	151.50	545	27.80
DSP	440	900	48.89
IO	286	362	79.01
GT	5	16	31.25
BUFG	26	32	81.25
MMCM	2	8	25.00
PLL	3	8	37.50
PCle	1	1	100.00

7Z045 target: LUT 76% · FF 41.8% · BRAM 27.8% · DSP 48.9% · GT 31.25%

Resource	Utilization	Available	Utilization %
LUT	236533	522720	45.25
LUTRAM	12253	161280	7.60
FF	281629	1045440	26.94
BRAM	247.50	984	25.15
DSP	444	1968	22.56
IO	371	512	72.46
GT	18	48	37.50
MMCM	1	11	9.09
PLL	3	22	13.64
PCle	1	5	20.00

ZU19EG target: LUT 45.3% · FF 26.9% · BRAM 25.2% · DSP 22.6% · GT 37.5%

- **Resource headroom** — the same LLRF design that occupied ~76% of the Zynq-7045 LUTs fits in 45.3% of the ZU19EG (522,720 LUTs, $\approx 2.4\times$) — the resource bottleneck that motivated the redesign is resolved
- **GT channels 18 / 48** — $4\times$ QSFP + $4\times$ P2P + PL BASE-X ethernet + FMC GT;
- **DSP & BRAM** — 444 DSP ($\approx 23\%$) for CORDIC / PID / mixers, 247.5 RAMB36 ($\approx 25\%$) for DAQ buffering; PCIe hard block 1 / 5

5. Summary

- **Hardware:** XCZU19EG, eight 16-bit 250 MSPS ADC channels, two 16-bit 500 MSPS DAC channels and 8 GB of DDR4 form the core digitizer platform.
- **Integration:** MicroTCA.4 backplane links, FMC/RTM expansion, multi-source clocking and independent MMC management are integrated on one AMC.
- **Software:** A shared BSP and EPICS IOC support both PCIe host operation and stand-alone PS operation.
- **Current status:** Board bring-up and functional validation have been completed.
- **Next step:** Deploy and evaluate the board in the existing LLRF system.

A grayscale image of a spiral galaxy, viewed from an angle that shows its three-dimensional structure. The galaxy's core is a bright, dense central region. From this core, numerous spiral arms emerge, each composed of many individual stars and interstellar dust. The arms are more densely packed in some regions than others, creating a complex, swirling pattern. The overall image has a high-contrast, almost ethereal quality.

THANKS