



An Ultra-Low-Latency ATCA-Based Processing Platform for Fast Protection at CSNS-II

Peng Zhu

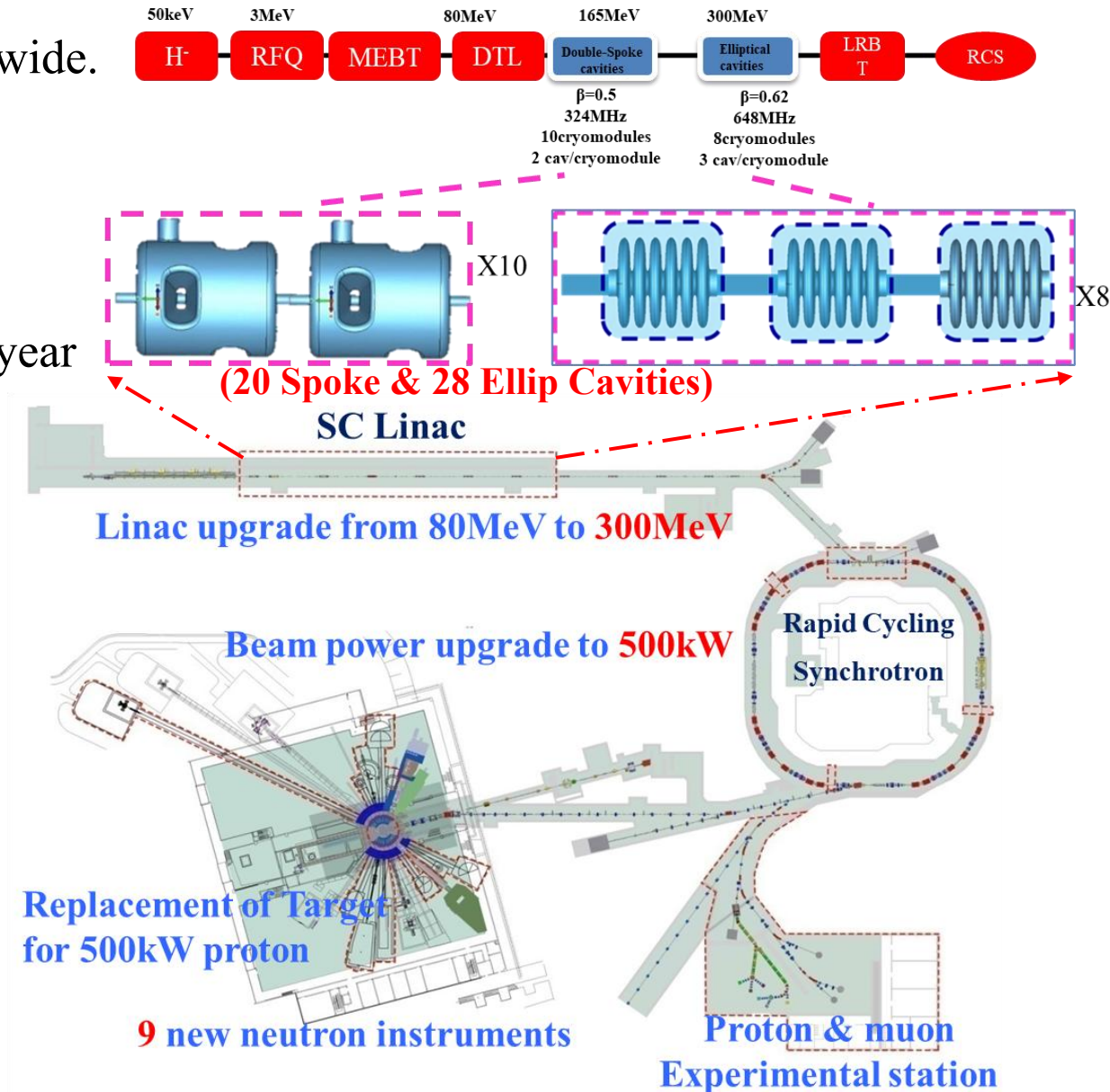
**The MicroTCA/ATCA International Workshop For Large Scientific Facility Control
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- **Background & Requirements**
- **Design and Implementation of ATCA-Based Hardware**
- **Experimental Validation of the DBCM Prototype**
- **Future Work**
- **Summary**

Overview of the Linac

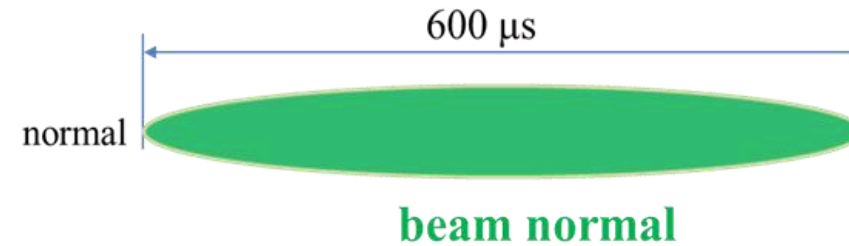
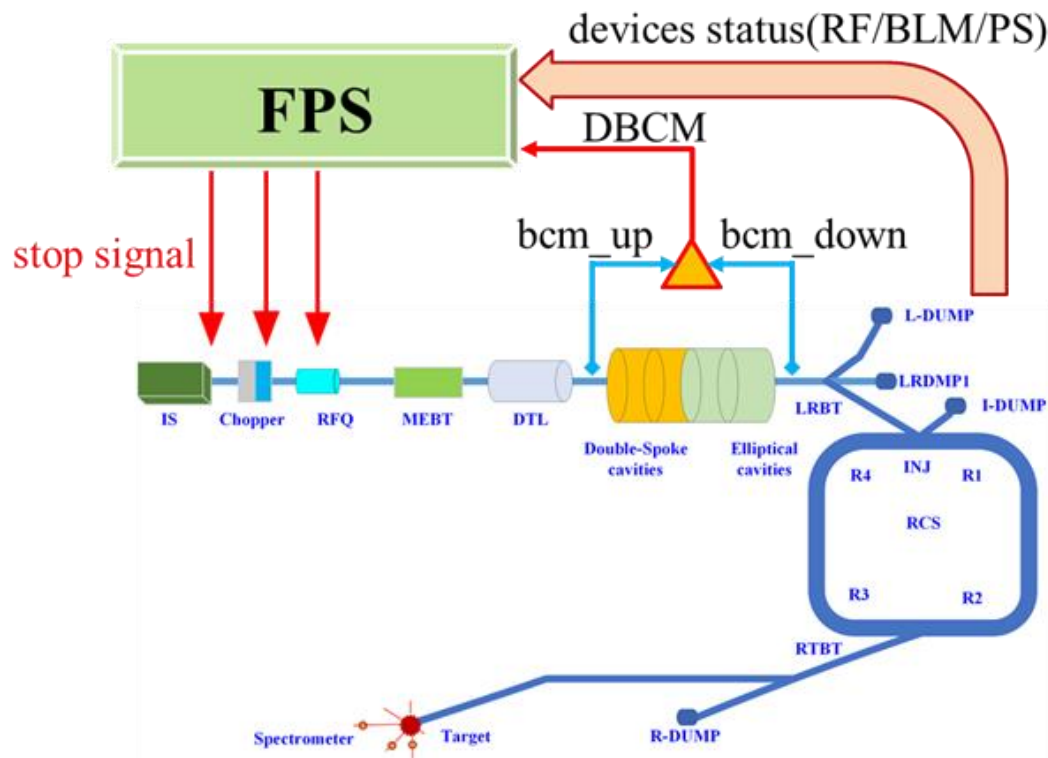


- The fourth pulsed spallation neutron source worldwide.
- National acceptance on August 23, 2018.
- Operating efficiently and stably for seven years.
- Upgrade approved in 2024, with an estimated six-year construction period.
 - Phase I: 80 MeV, running now.
 - **Phase II: 300 MeV, preparation.**

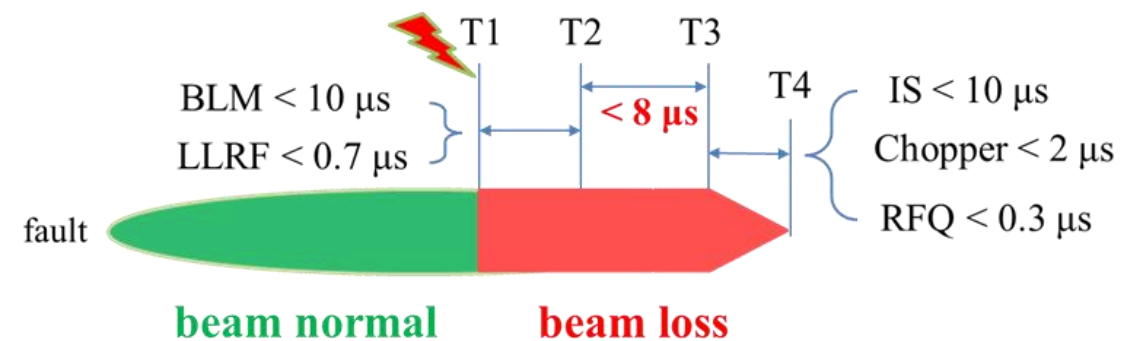


Objectives and Performance

- **Objectives :** High availability, high reliability, and high efficiency, ensuring the long-term stable and safe operation.

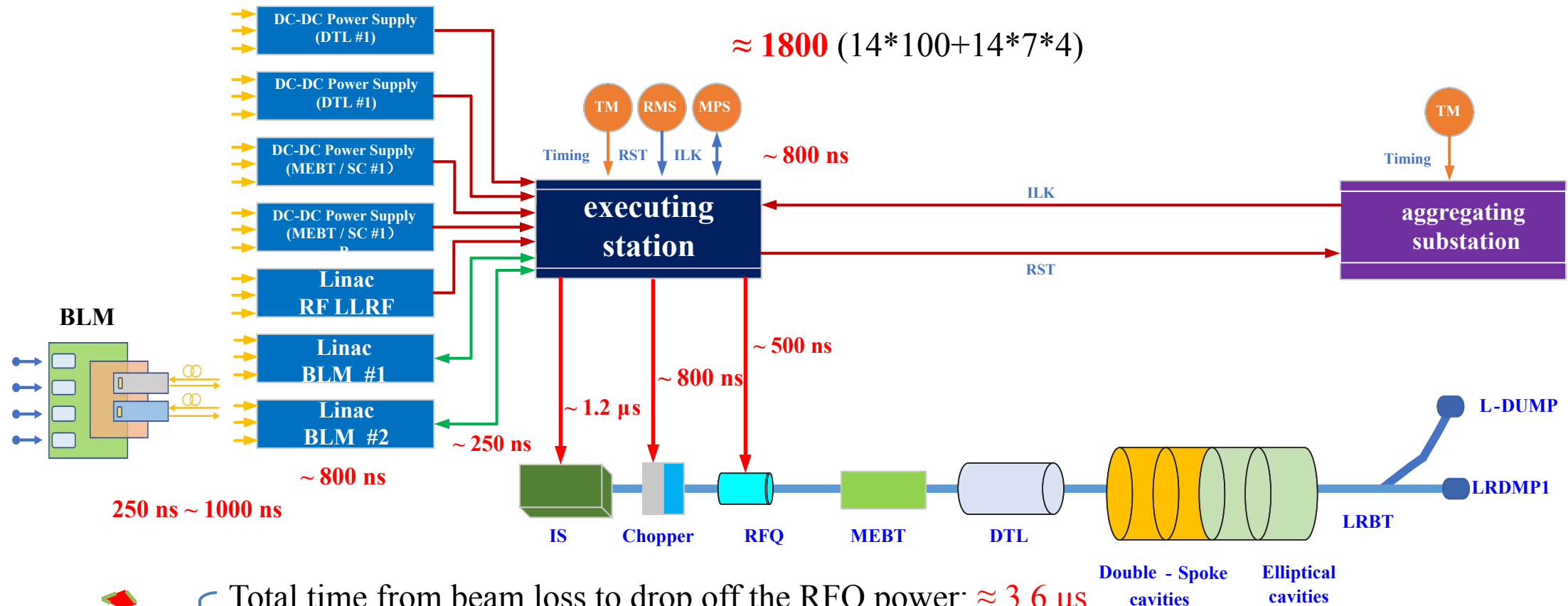


- T1: fault occurs
- T2: receive from detector
- T3: send to the front of terminal
- T4: no beam hazard



- **Metrics :** Must be controlled within 8 μ s, including fiber-optic transmission delay, intrinsic device delay, and interlock signal debouncing.

- **The FPS for Linac** (Distributed System, A key component of the accelerator)
 - Each substation independently connects to 100 interlocking signals.
 - Each Rocket IO channel processes 16 signals, and the maximum number of signals that the master station can handle:



Total time from beam loss to drop off the RFQ power: $\approx 3.6 \mu\text{s}$ Double Spoke cavities Empirical cavities
 Total time from beam loss to shutdown timing of the chopper: $\approx 4 \mu\text{s}$
 Total time from beam loss to shutdown timing of the ion source extraction power supply: $\approx 4.5 \mu\text{s}$

Function for ATCA-based Processing Platform

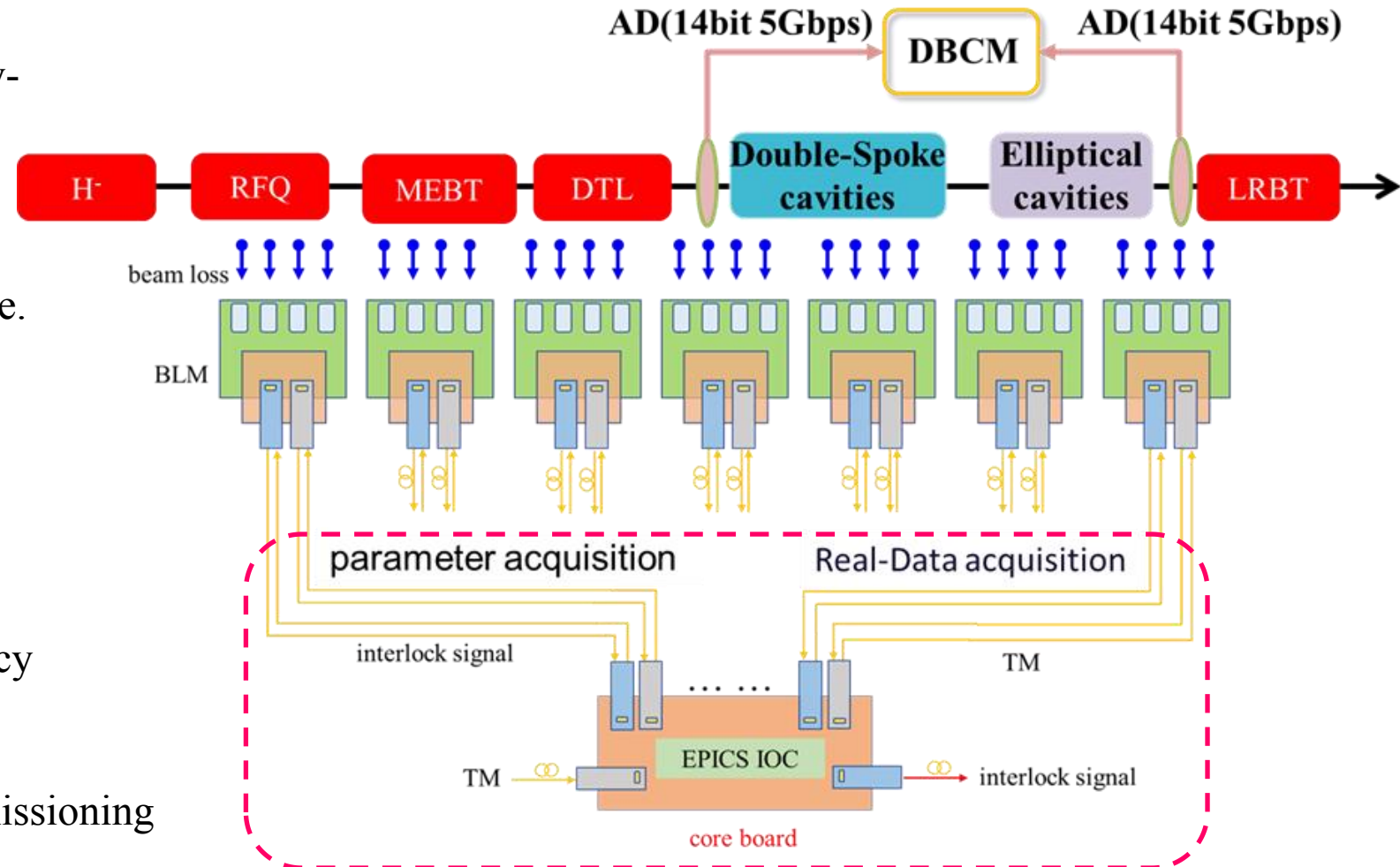


- **Integrate FPS & TM:** Provide real-time beam data with high-precision timestamps for beam commissioning and machine studies.

- ✓ Synchronously acquire bunch-by-bunch beam data.
- ✓ Perform real-time analysis and decision-making to minimize machine protection response time.
- ✓ Utilize Edge AI to determine the optimal timing for beam stop.

■ Challenges

- Ultra-high reliability and accuracy
- High-precision timestamps
- Signal integrity and beam commissioning



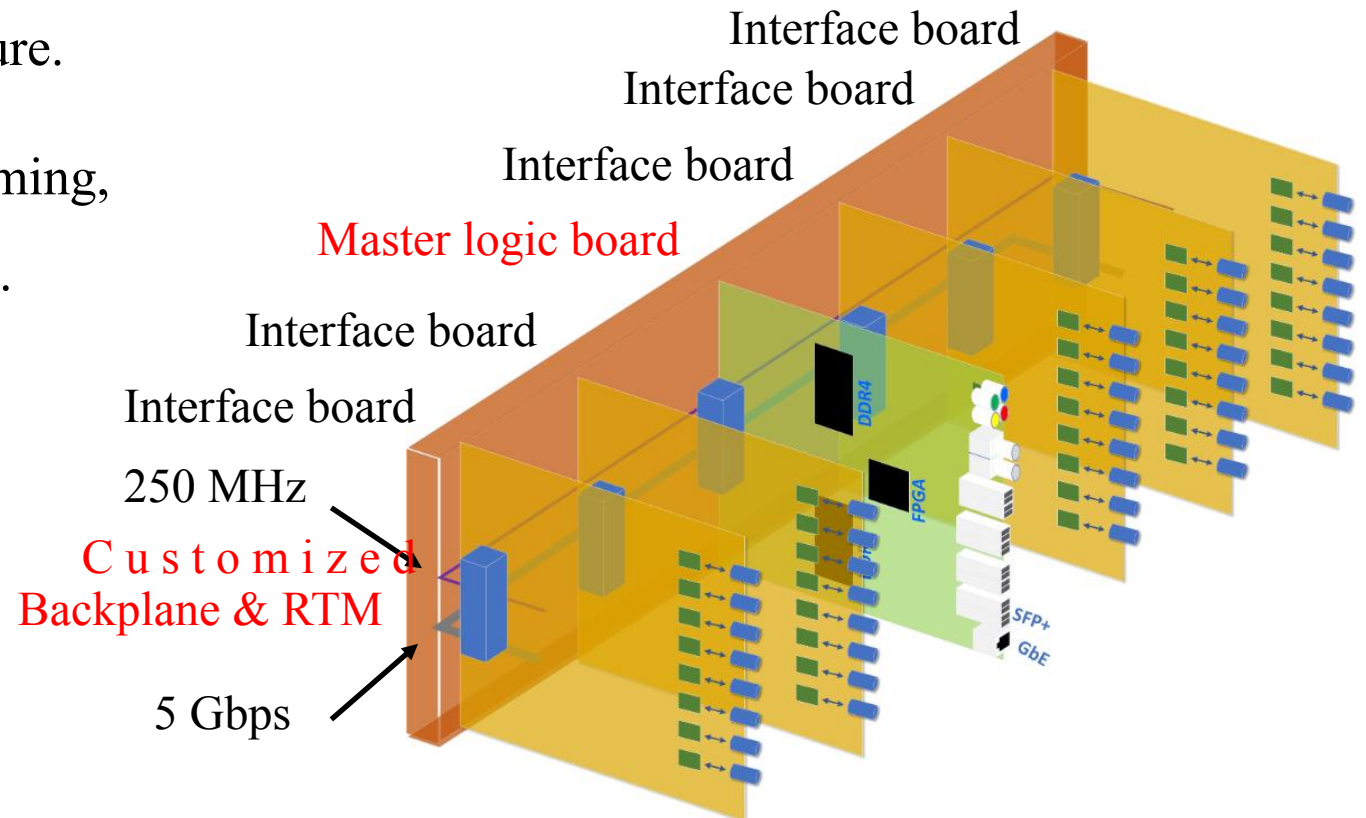
Hardware for ATCA-based Processing Platform



- **Motivation:** (1) VME --> xTCA.
(2) demo FPGA --> RAM + Linux + EPICS (**Embedded IOC**).
(3) distributed data --> Associated data with high-precision timestamps (**EVR**).

- **Approach: ATCA + FPGA + Rocket I/O**

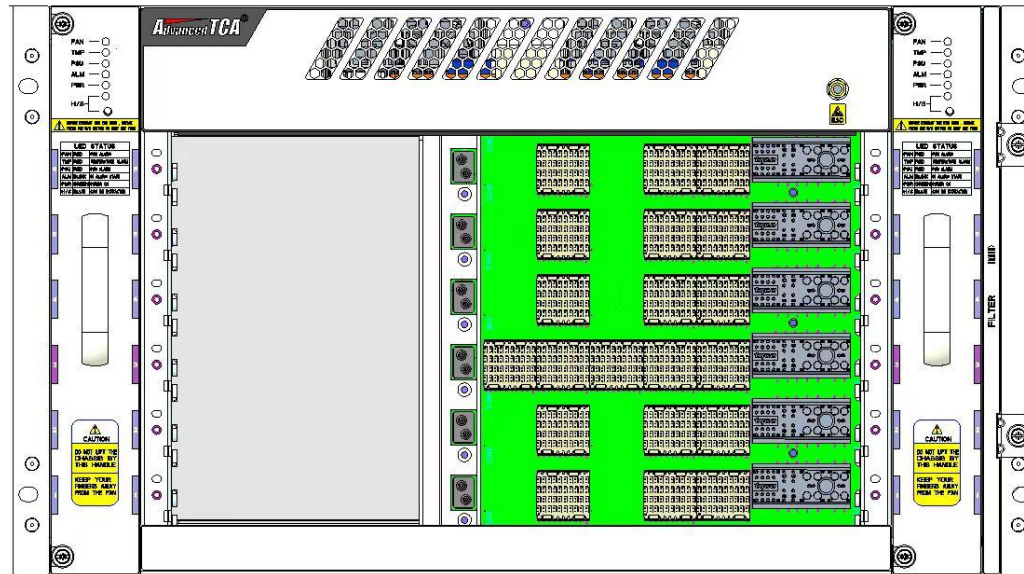
- ✓ Based on the ATCA mechanical architecture.
- ✓ Integrating functions of fast protection, timing, beam loss configuration, and data readout.



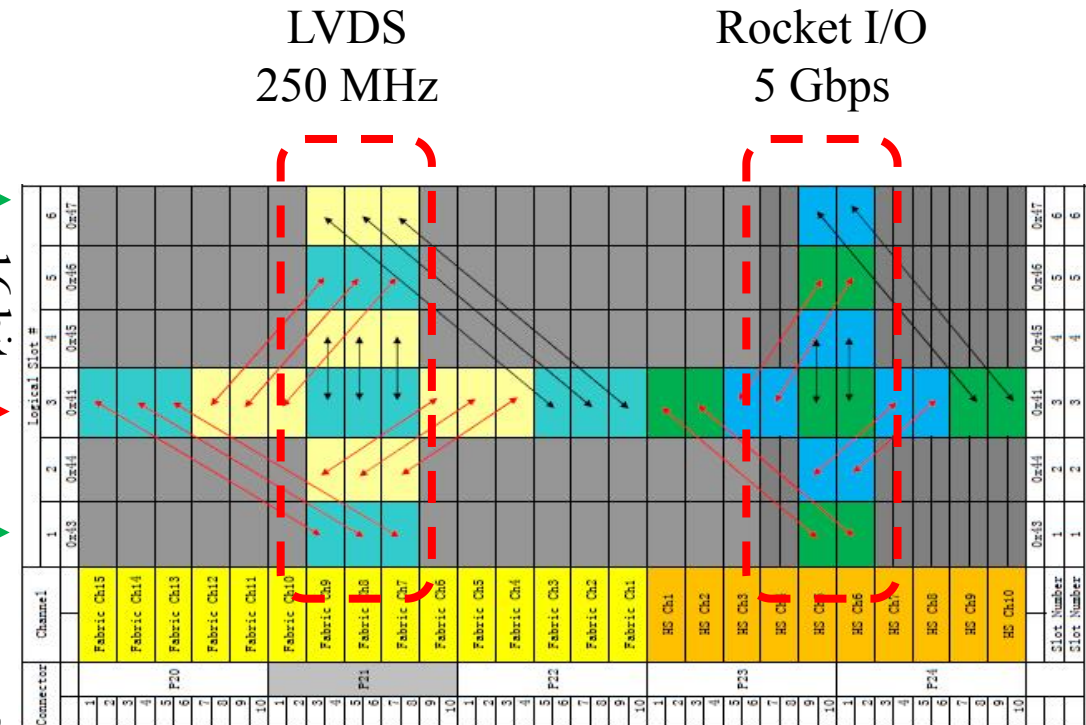
Hardware for ATCA-based Processing Platform



■ Self-developed backplane with signal interfacing



6# slot
24 bit
16 bit
3# slot
1# slot



- ✓ **Master:** slot #3, while slave: slots #1, #2, #4, #5, and #6.
- ✓ **Master slot** handles logical processing, parameter configuration, status readback, and on-board IOC.
- ✓ **Slave slots** handle external signal input and internal signal output.
- ✓ Master slot is directly connected to each slave slot via **32 pairs of high-speed differential signals through pin-to-pin routing** on the backplane.

Hardware for ATCA-based Processing Platform



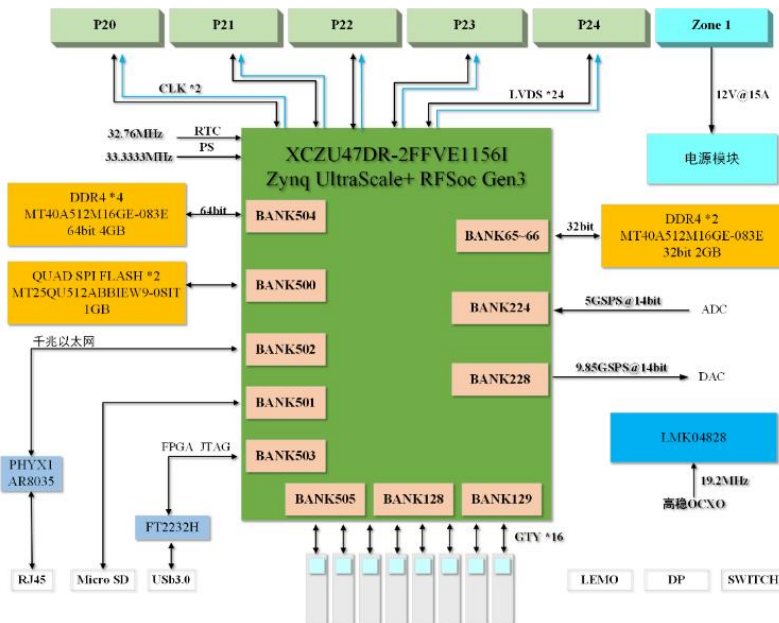
■ System Components: Master logic board, Self-developed backplane, and Interface boards

➤ Master logic board: Acquisition & Signal processing & Interlock logic

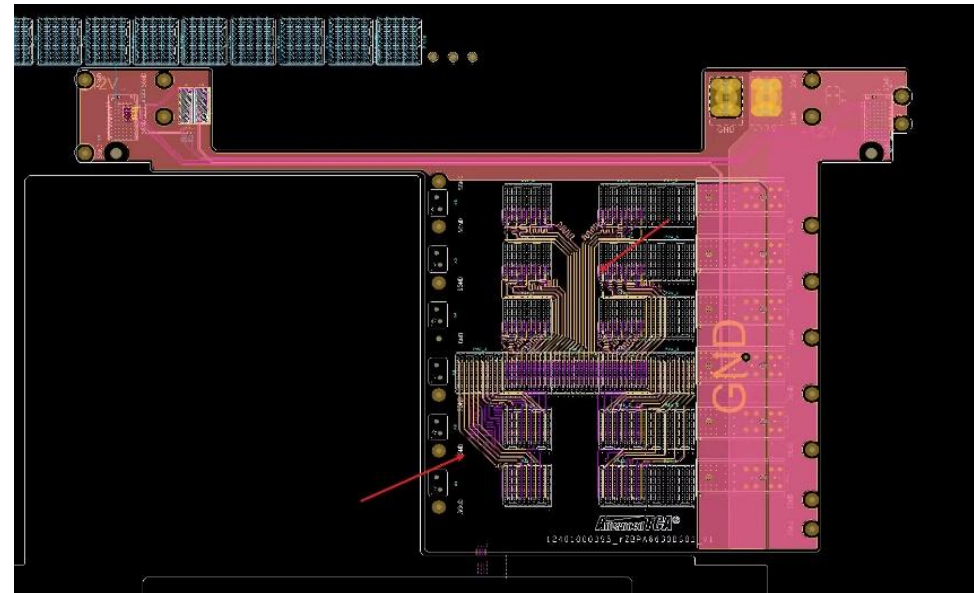
- ✓ RF SoC: real-time ADC acquisition and beam signal processing.
- ✓ KU060: interlock logic and beam abort via point-to-point links to interface boards.

32-bit LVDS parallel bus
RF SoC interface with KU060

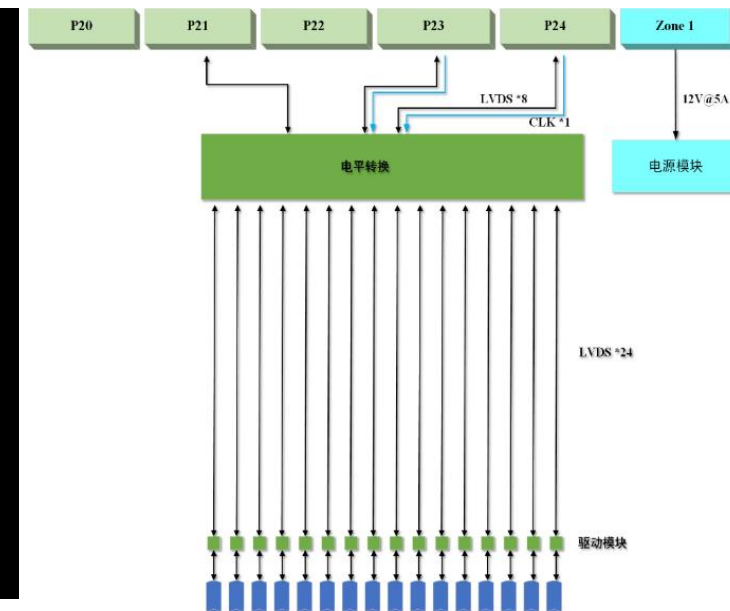
➤ Interface boards: Signal I/O with external subsystems



RF SoC (Master logic board)



Self-developed backplane
(no logic chip, just point-to-point links)



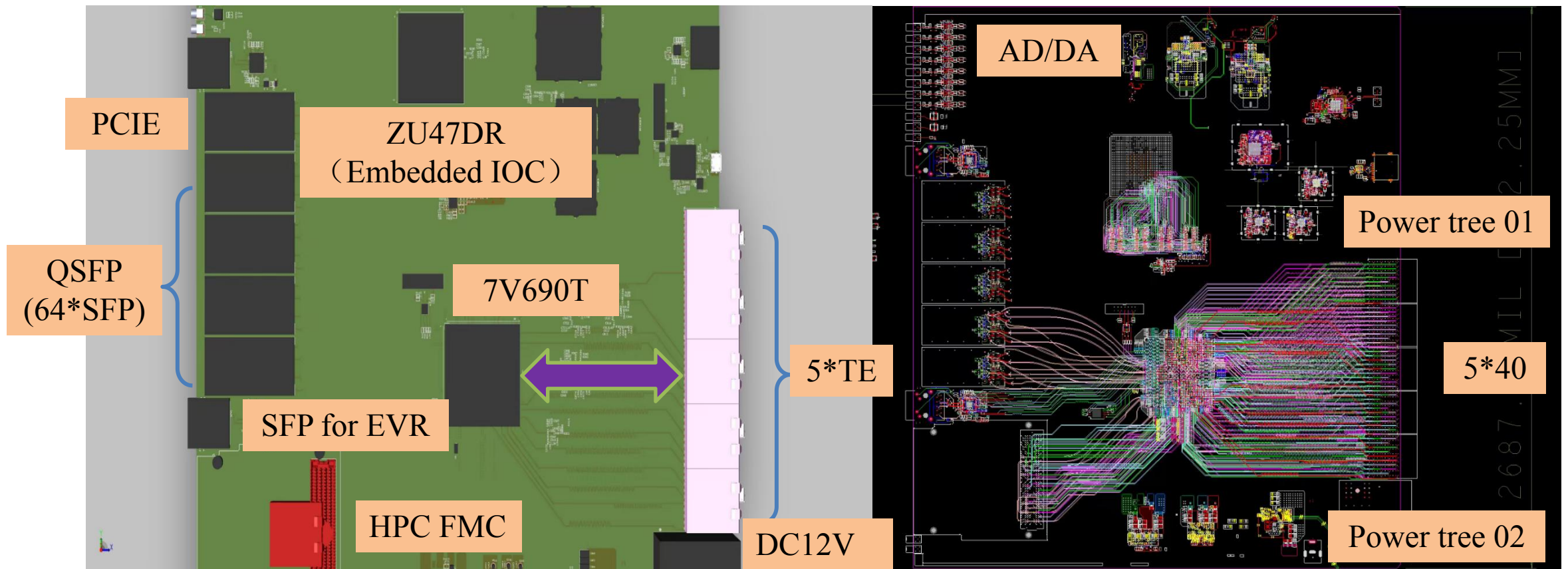
Interface board
(no logic chip, just basic Functions)

Hardware for ATCA-based Processing Platform



■ **Master logic board:** Completed schematic and PCB design, plus functional debugging of the 6U ATCA core master logic board.

- 4 QSFP + 1 PCIE
- Event timing support
- HPC FMC
- 8 x 14 bits **ADC**, **5 GSPS**, **6GHz** analog BW
- 8 x 14 bits **DAC**, **10 GSPS**, **4GHz** analog BW
- Megtron-6, 24 Layer



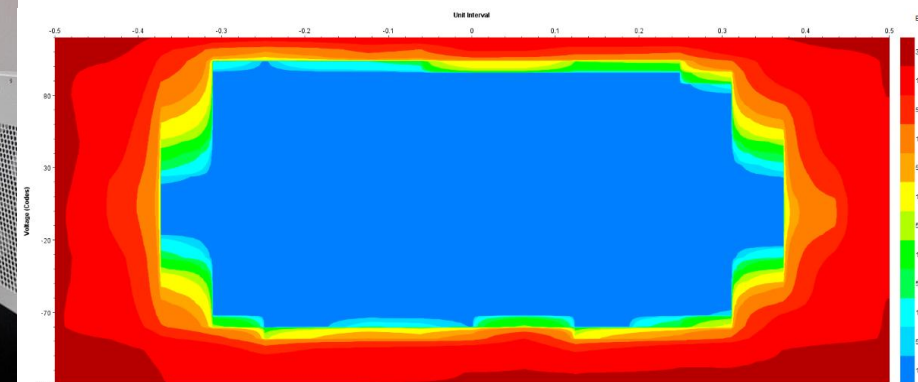
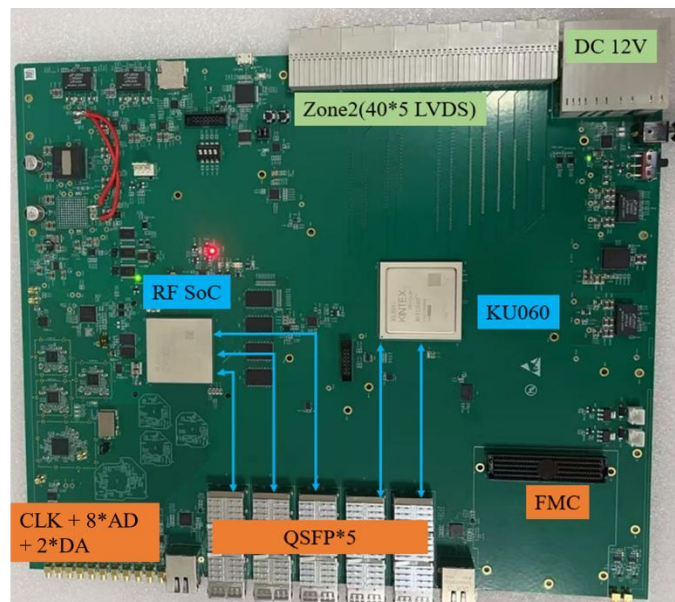
3D view

Layout

Hardware for ATCA-based Processing Platform



- **Master logic board:** Achieved error-free 5 Gbps high-speed transmission across 16 channels.



16*5 Gbps

Tcl Console Messages Serial I/O Links x Serial I/O Scans ? _ □ ✕																			
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DfE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mo
Ungrouped Links (0)																			
Found Links (8)																			
Auto detected link 0	Quad_228/MGT_X1Y16/TX (xc ku060_0)	Quad_227/MGT_X1Y12/RX (xc ku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 1	Quad_228/MGT_X1Y17/TX (xc ku060_0)	Quad_227/MGT_X1Y13/RX (xc ku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 2	Quad_228/MGT_X1Y18/TX (xc ku060_0)	Quad_227/MGT_X1Y14/RX (xc ku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 3	Quad_228/MGT_X1Y19/TX (xc ku060_0)	Quad_227/MGT_X1Y15/RX (xc ku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 4	Quad_227/MGT_X1Y12/TX (xc ku060_0)	Quad_228/MGT_X1Y16/RX (xc ku060_0)	5.014 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 5	Quad_227/MGT_X1Y13/TX (xc ku060_0)	Quad_228/MGT_X1Y17/RX (xc ku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 6	Quad_227/MGT_X1Y14/TX (xc ku060_0)	Quad_228/MGT_X1Y18/RX (xc ku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 7	Quad_227/MGT_X1Y15/TX (xc ku060_0)	Quad_228/MGT_X1Y19/RX (xc ku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (000000)	0.00 dB (000000)	950 mV (1100)	✓	Inject	Reset	Reset	Locked	Locked	None

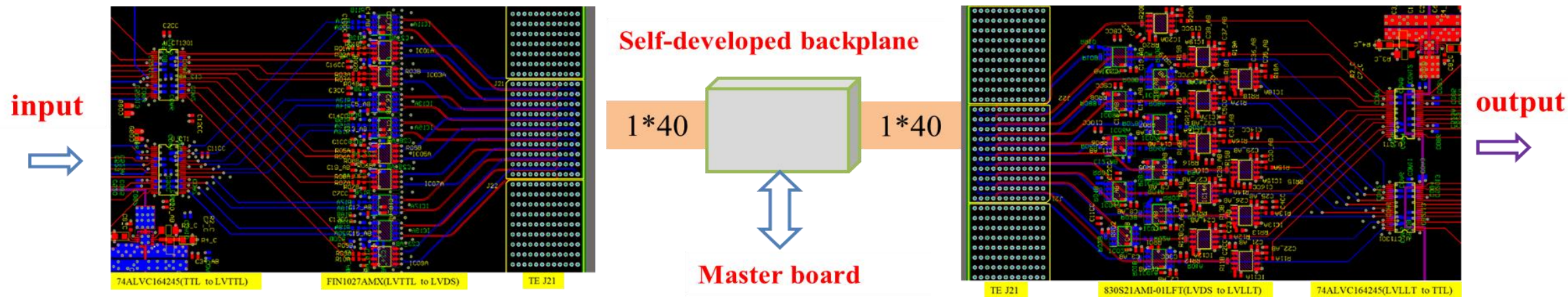
Hardware for ATCA-based Processing Platform



■ Interface board: Optical-type & PLC-type to cover different application.

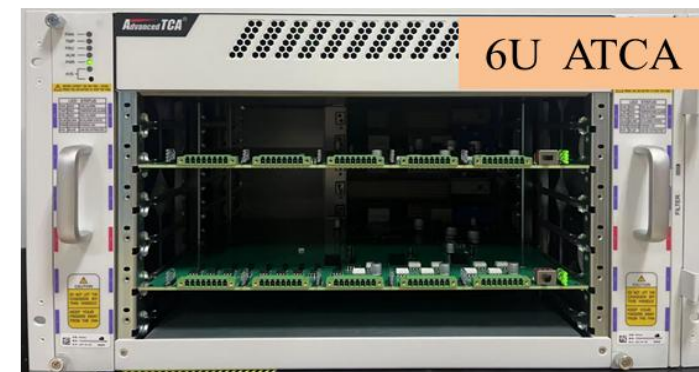
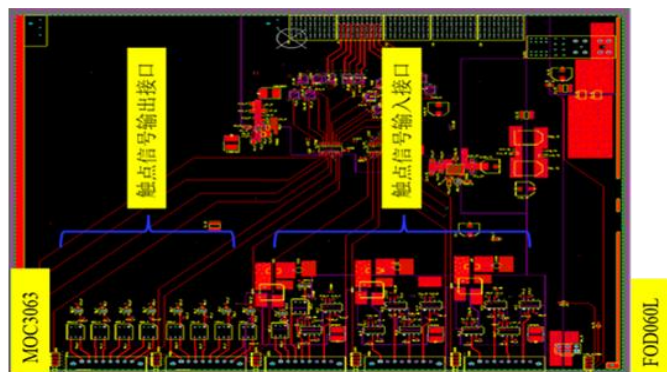
➤ **Opt-type input :** HFBR2412T => 74ALVC164245 => FIN1027AMX(LVTTL to LVDS) => TE

➤ **Opt-type output :** TE => 830S21AMI-01LFT(LVDS to LVLLT) => 74ALVC164245 => HFBR1414T



➤ **PLC-type input :** phoenix => FOD060L => 74ALVC164245 => FIN1027AMX(LVTTL to LVDS) => TE

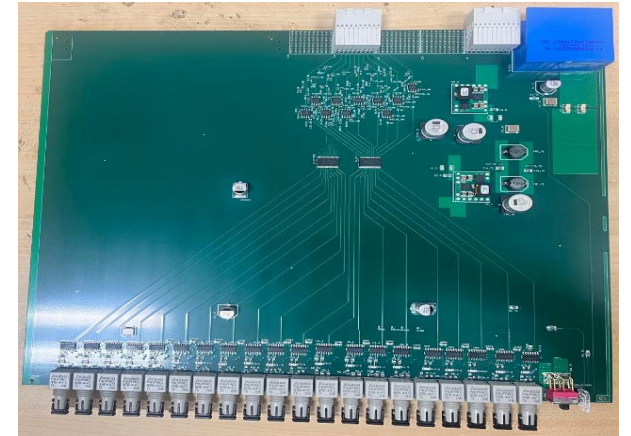
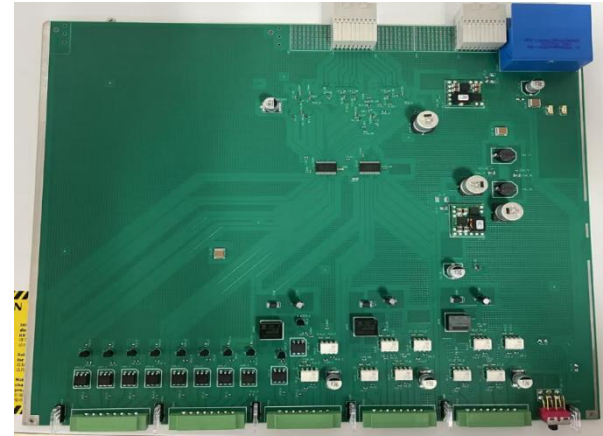
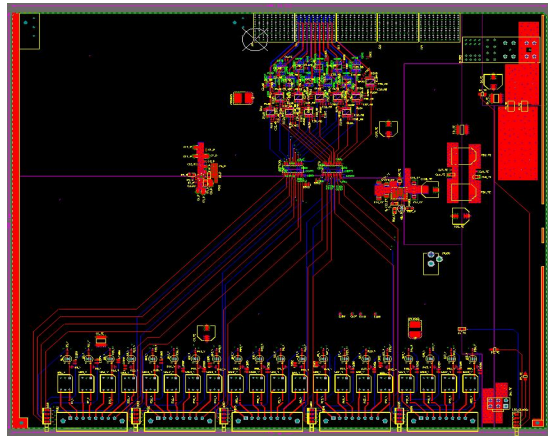
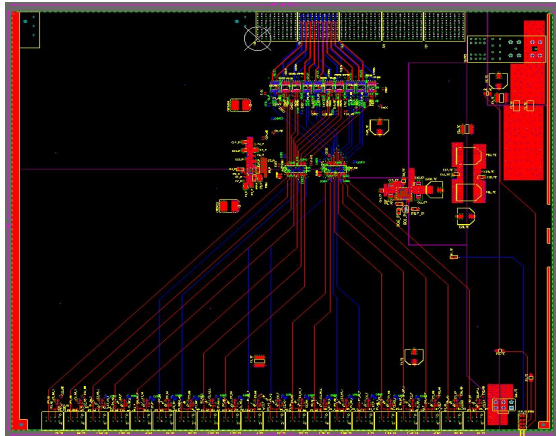
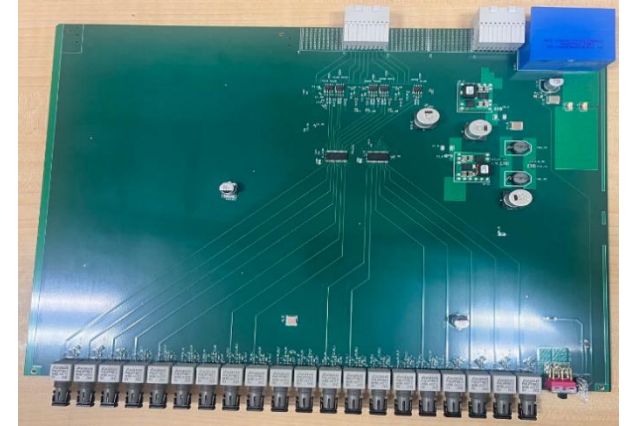
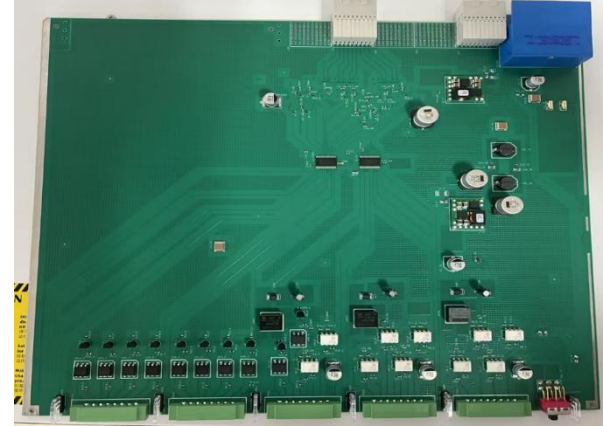
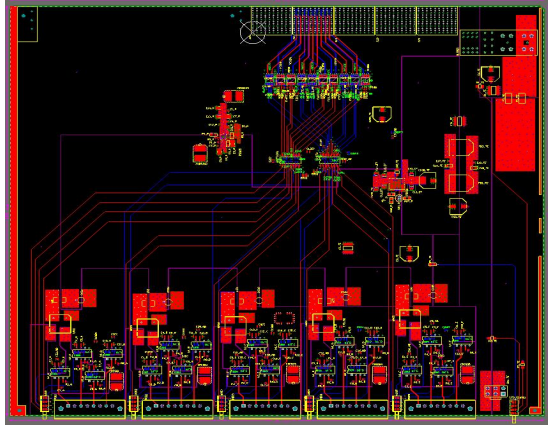
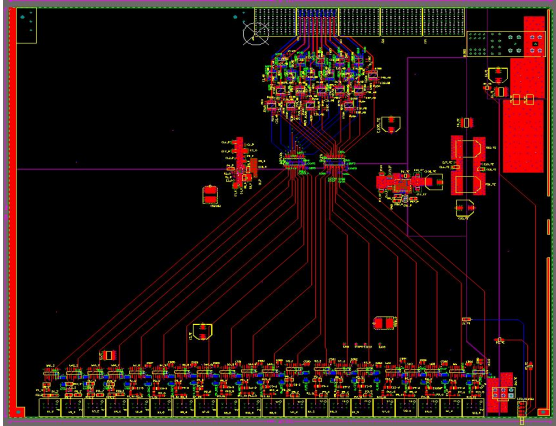
➤ **PLC-type output :** TE => 830S21AMI-01LFT 74ALVC164245 (LVLLT to TTL) => MOC3063 => phoenix



Hardware for ATCA-based Processing Platform



- **Interface board:** Optical-type & PLC-type to cover different application.

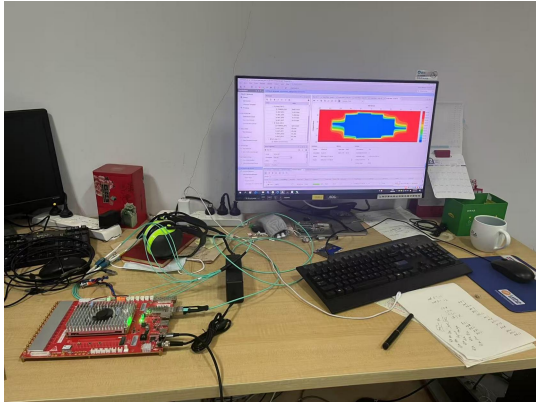


The four types of interface boards have successfully completed system-level internal testing and are currently pending equipment-level joint testing.

Hardware for ATCA-based Processing Platform



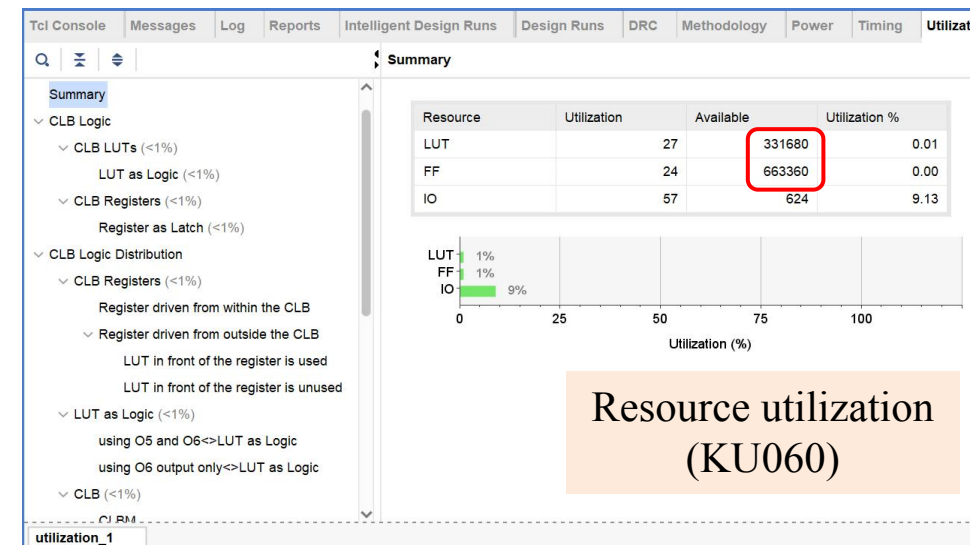
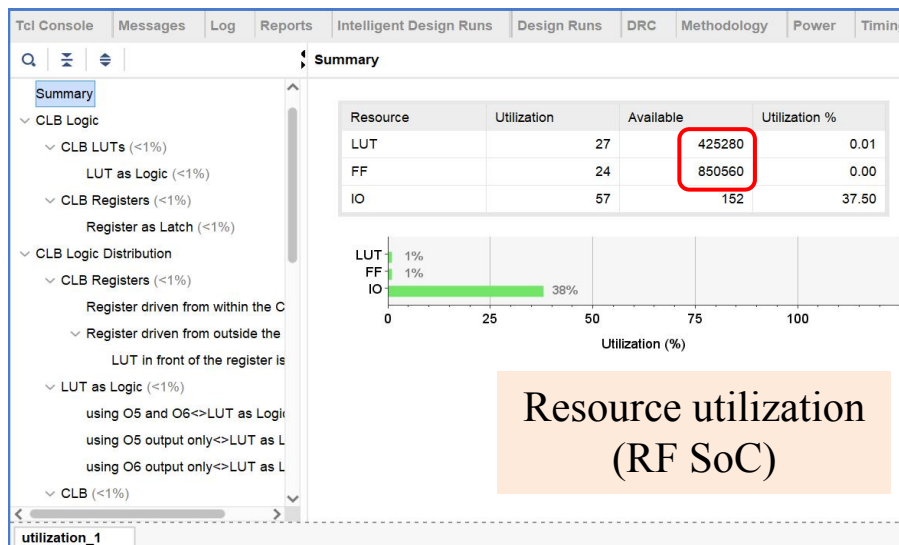
■ **Current Status:** Porting of Fast Protection Firmware for online operation.



Implementation	Summary
Status:	✓ Complete
Messages:	⚠ 3 warnings
Active run:	impl_1
Part:	xcku060-ffva1517-2-i
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

Implementation	Summary
Status:	✓ Complete
Messages:	⚠ 3 warnings
Active run:	impl_1
Part:	xczu47dr-ffve1156-2-i
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

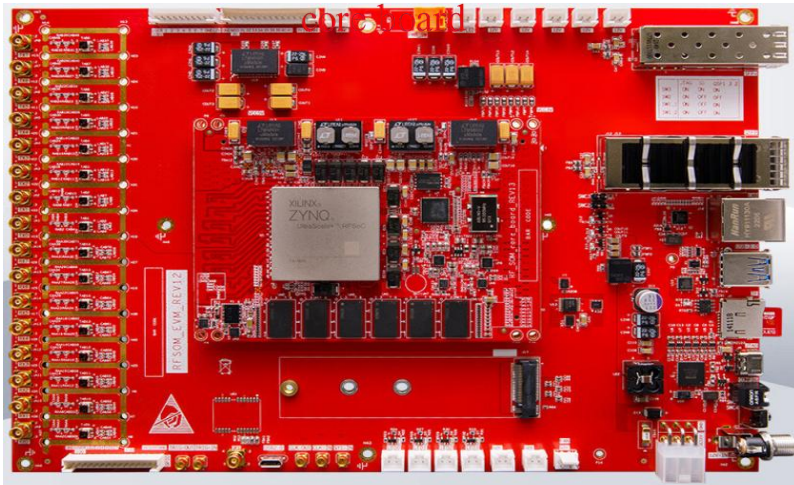
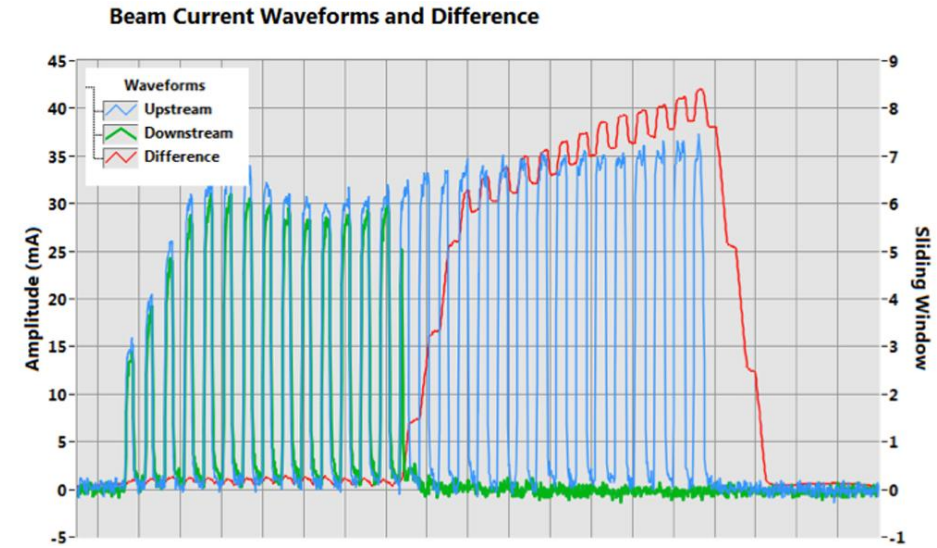
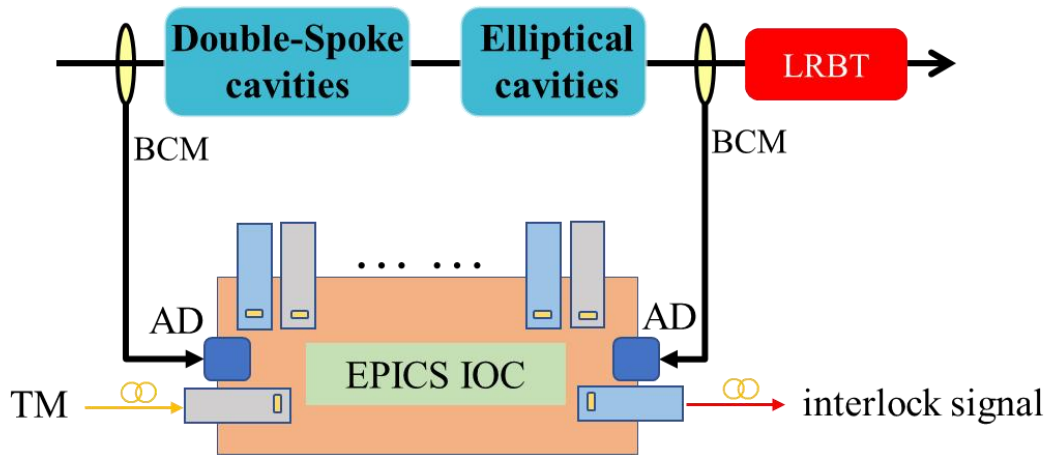
Both chips are fully integrated, with online beam commissioning targeted for early 2027.



- **Background & Requirements**
- **Design and Implementation of ATCA-Based Hardware**
- **Experimental Validation of the DBCM Prototype**
- **Future Work**
- **Summary**

Experimental Validation of the DBCM Prototype

- A prototype was developed to validate the RF SoC-based DBCM solution for real-time beam monitoring



RF SoC Development Board Physical Diagram

- ✓ Seamless integration of ADC and ARM processors into a single chip.
- ✓ Supports high-speed signal acquisition up to 5 GHz, with highly efficient I/Q signal generation required for demodulation.
- ✓ Supports embedded Linux and upper-layer application development.

Experimental Validation of the DBCM Prototype



■ Signal Processing Architecture (No multi-device cascading & Low latency)

FCT → RF-ADC → Demodulation → Differential Calculation → Decision-making → Protection Output

➤ Signal Acquisition and Processing (PL)

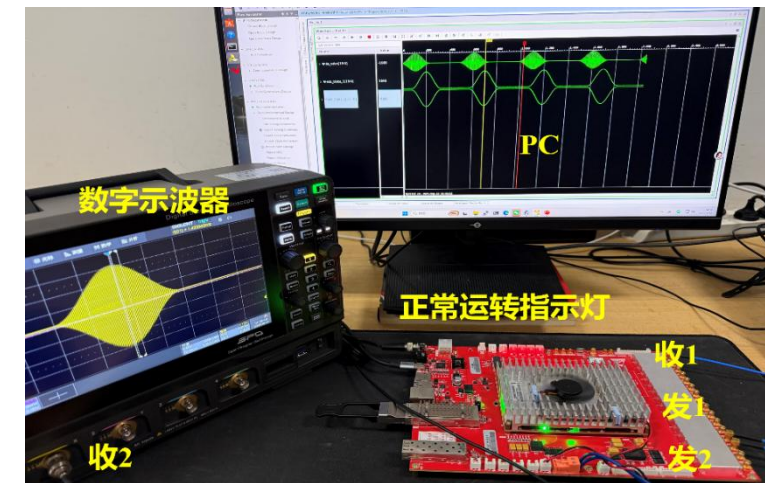
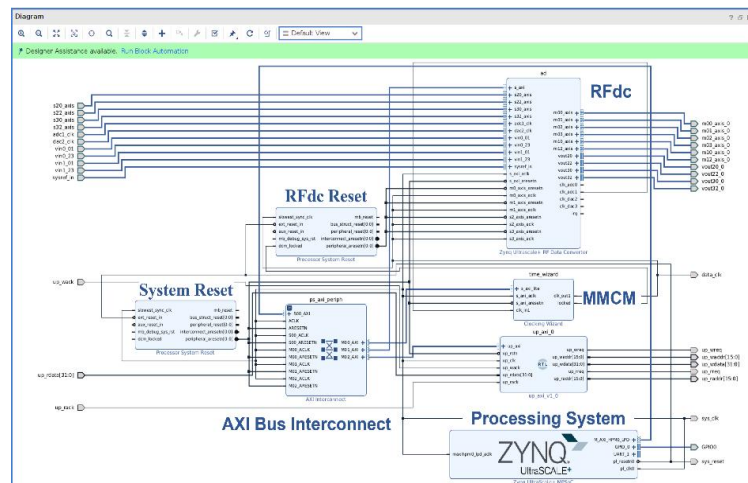
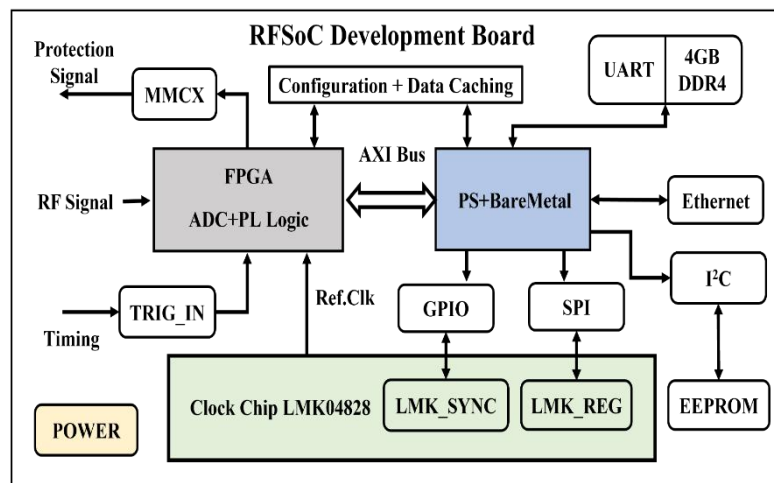
- ✓ Digitize incoming ADC signals.

➤ Real-time Processing (PL)

- ✓ Process the sampled data in real time to generate protection signals. Meanwhile, the data or status information is transmitted to the PS side via the AXI bus.

➤ Control and Communication (PS)

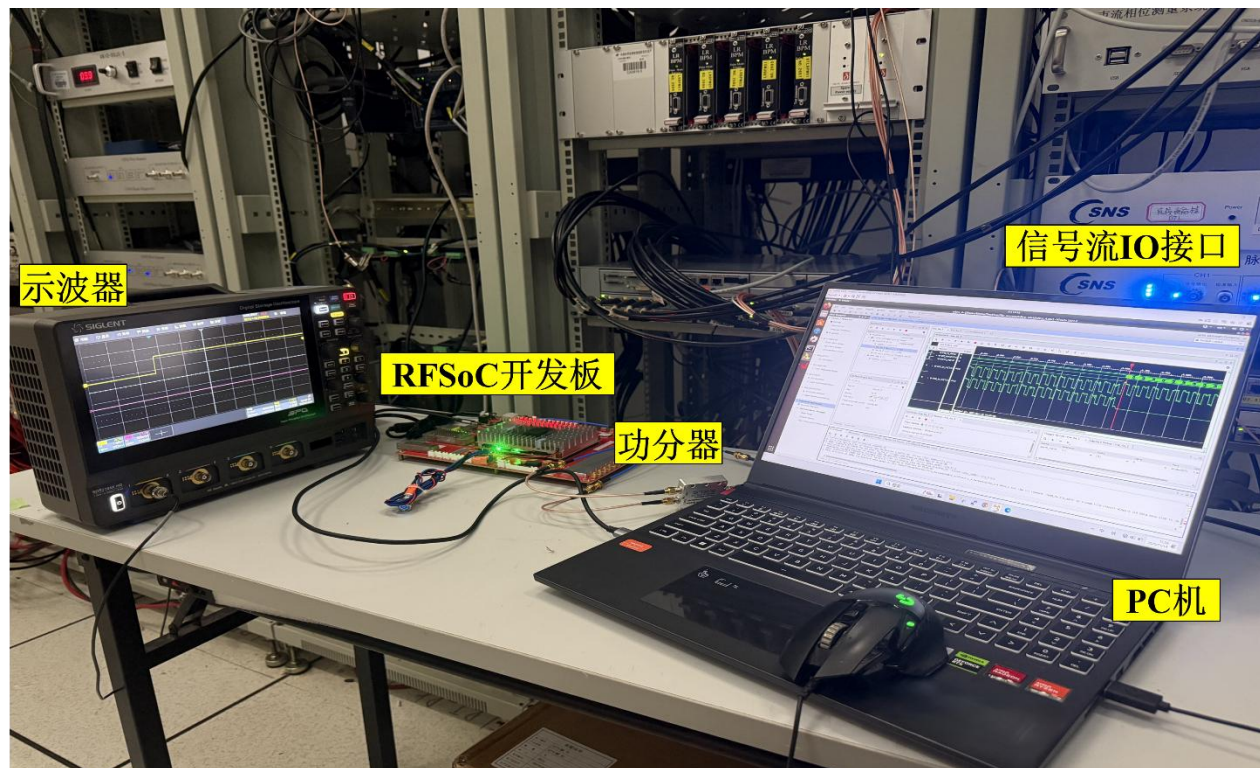
- ✓ A Linux application to handle system configuration and data buffering.
- ✓ Communicates with the host computer via Ethernet and storage devices via GPIO.



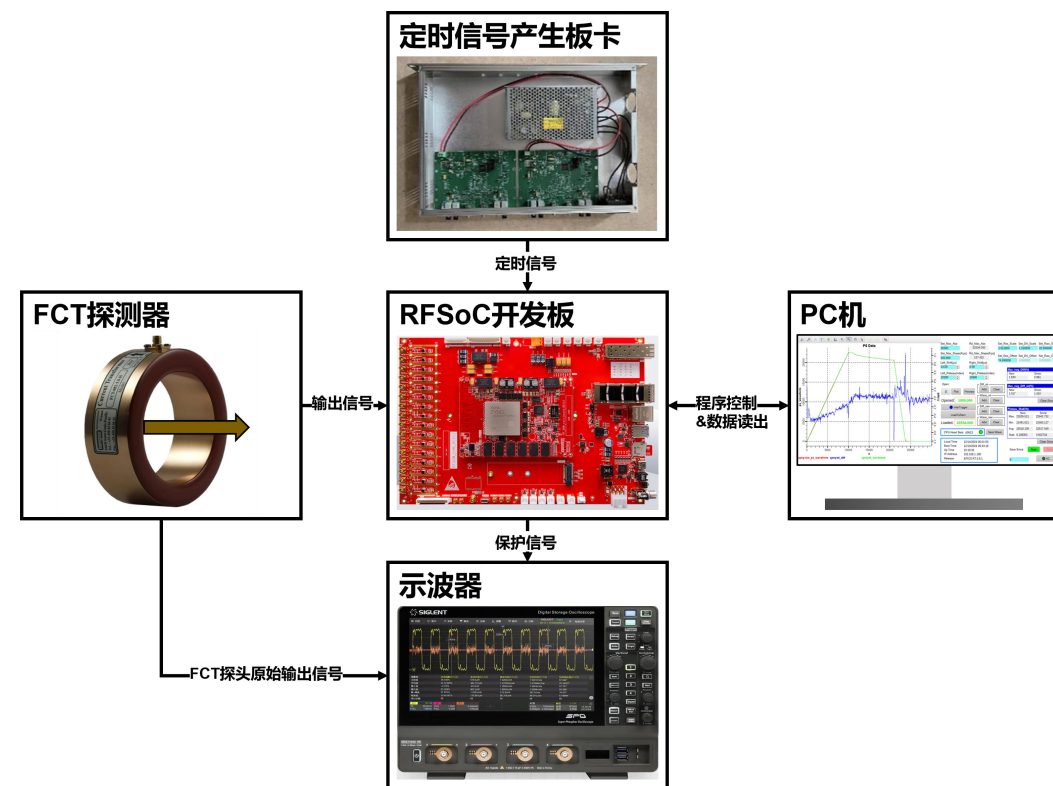
Experimental Validation of the DBCM Prototype



- **Test Setup:** Due to the availability of only a single FCT testing device, a power splitter was employed to divide the FCT output into two identical signals, which were then fed into the development board for dual-channel comparative processing.



Field Test Scenario



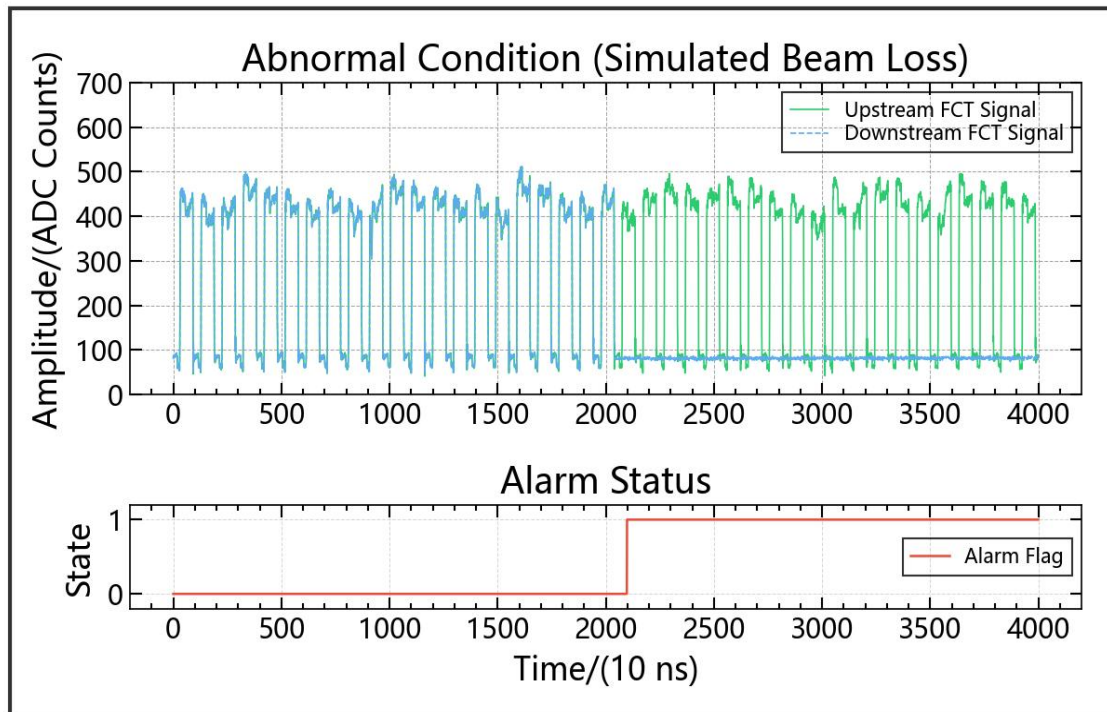
Equipment Connection Block Diagram

Experimental Validation of the DBCM Prototype

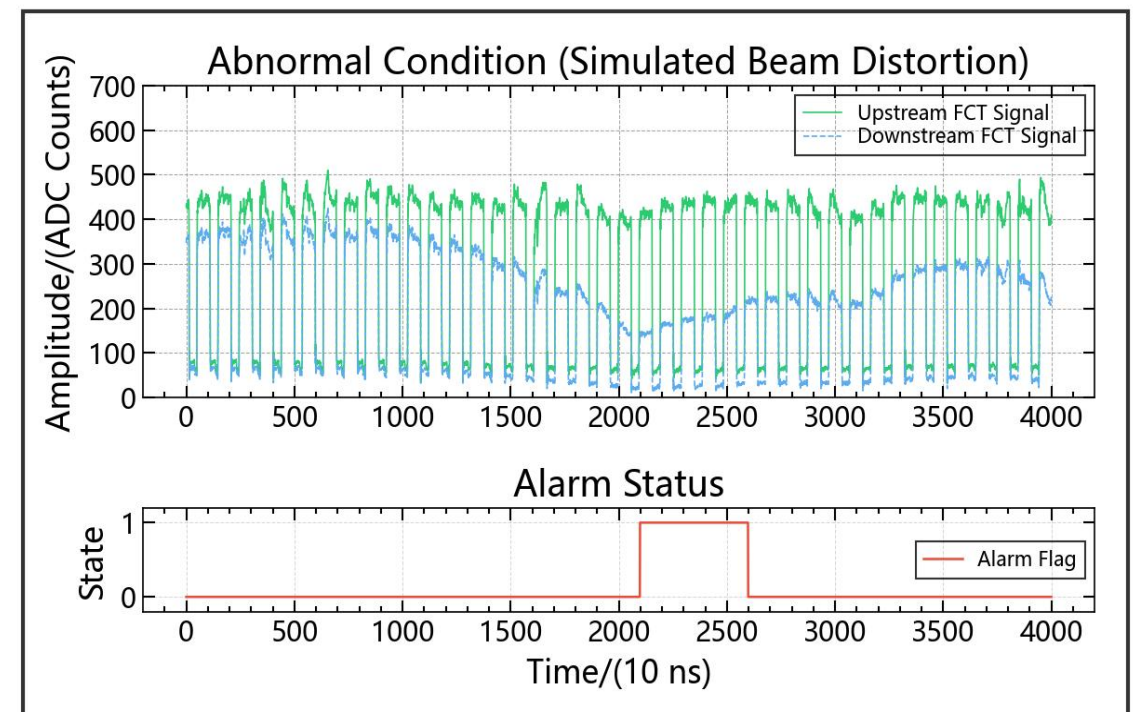


■ Validation under Abnormal Conditions (Simulated Beam Loss/Distortion)

- Under the normal beam mode, the waveforms of the two channels were consistent, and no alarm was triggered.
- When simulating two abnormal conditions, **bunch loss and waveform distortion**, the system immediately initiated a protection response once the signal difference exceeded the alarm threshold.



Simulating downstream beam loss

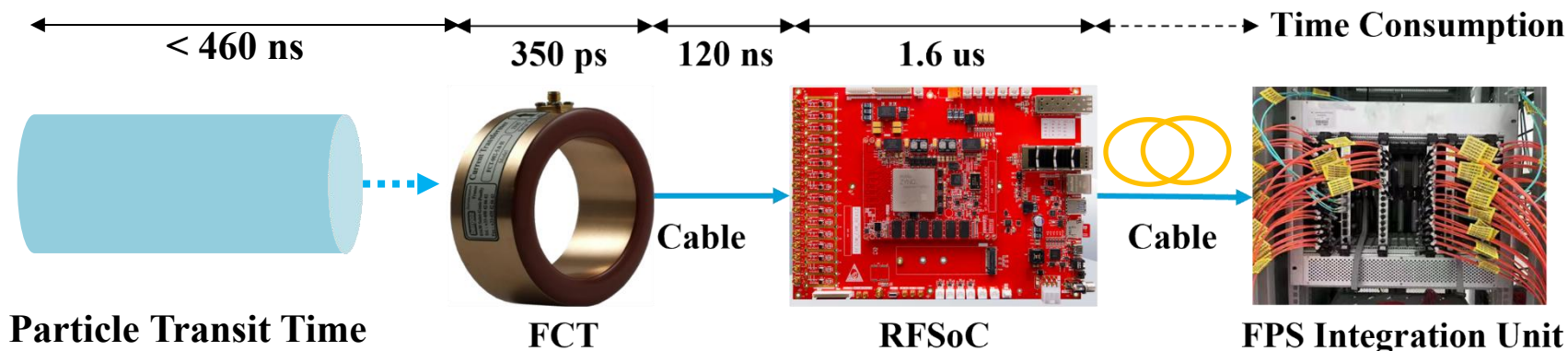
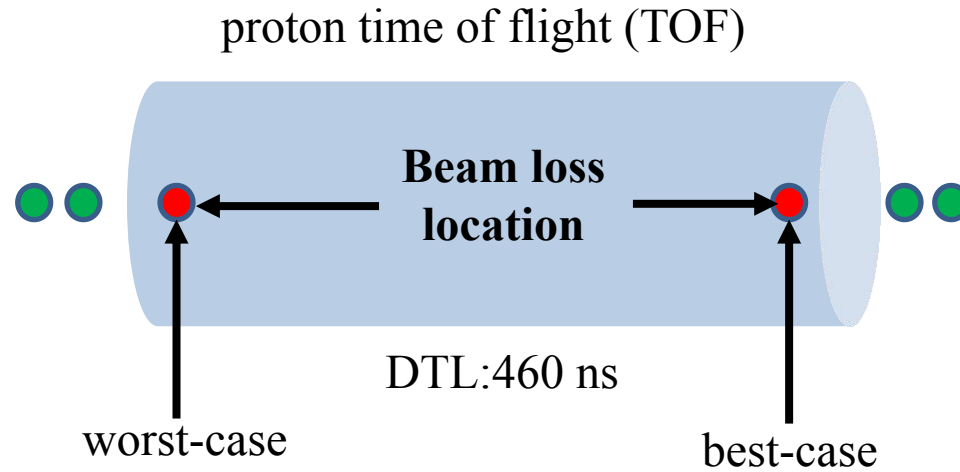
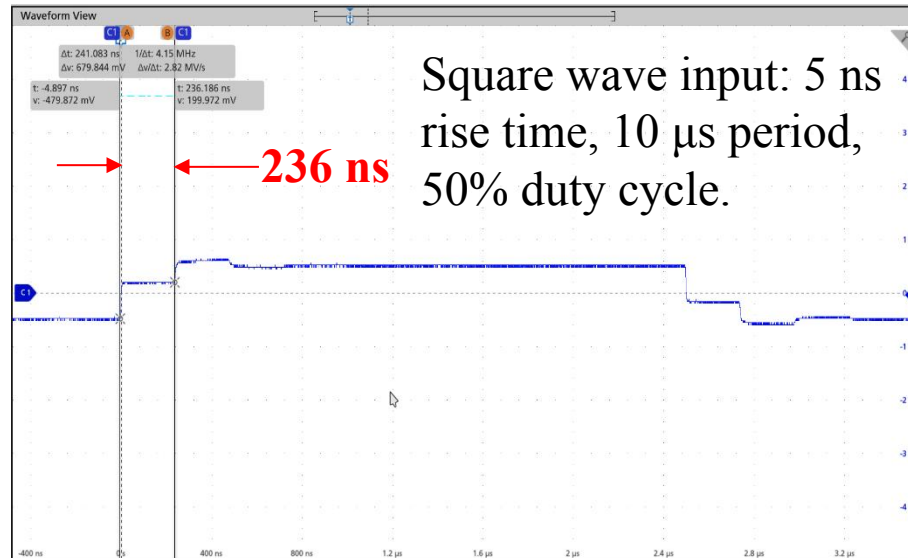


Simulating downstream beam waveform distortion

Experimental Validation of the DBCM Prototype



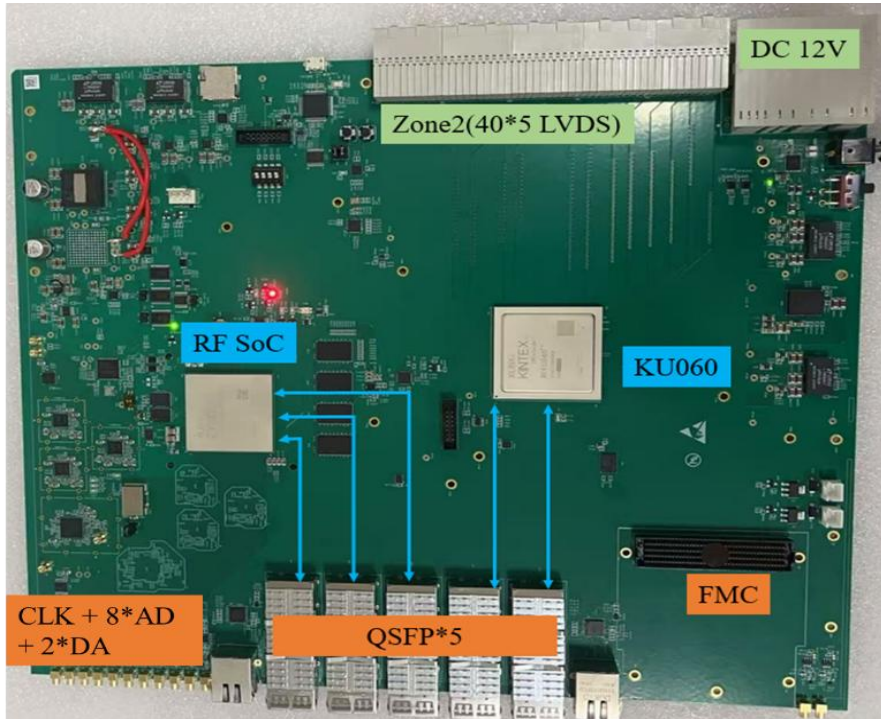
- **System Latency Evaluation:** The DBCM logic takes $\sim 1 \mu\text{s}$. Including $\sim 2.5 \mu\text{s}$ of cable delay and $\sim 1.5 \mu\text{s}$ of beam propagation time (TOF), the overall system latency is approximately $5 \mu\text{s}$.



Estimated overall system latency: $5 \mu\text{s}$, meeting the protection requirements for future superconducting cavities.

■ Active Protection Mechanism:

From "Triggering" to "Prediction"



- **Real-time processing:** Sliding average filtering & baseline subtraction
- **Edge AI deployment:** 1D-CNNs / Autoencoders via hls4ml
- **Pipelined inference:** Triggered at fixed beam-cycle intervals.

Built on a self-developed advanced hardware data processing platform featuring “RF SoC + KU060”.

- Adopt ATCA architecture based on a **customized backplane and self-developed front boards** as the solution.
- Using one main logic board (**Embedded IOC**) and four types of interface boards to cover most applications.
- Combining **DBCM with AI** in the linear superconducting section is expected to further enhance the performance.
- Integrating BLM and the FPS into a unified platform is challenging, and the real-time data with high-precision timestamps is worthwhile to explore (**EVR function**).

zhup@ihep.ac.cn



Thank you for
your attention!

