

DESY MicroTCA Ecosystem and Digital Hardware Platforms for Scientific Applications

2026 MicroTCA/ATCA Workshop for Large Scientific Facility Control

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MSK Accelerator Beam Controls - Digital Hardware Team

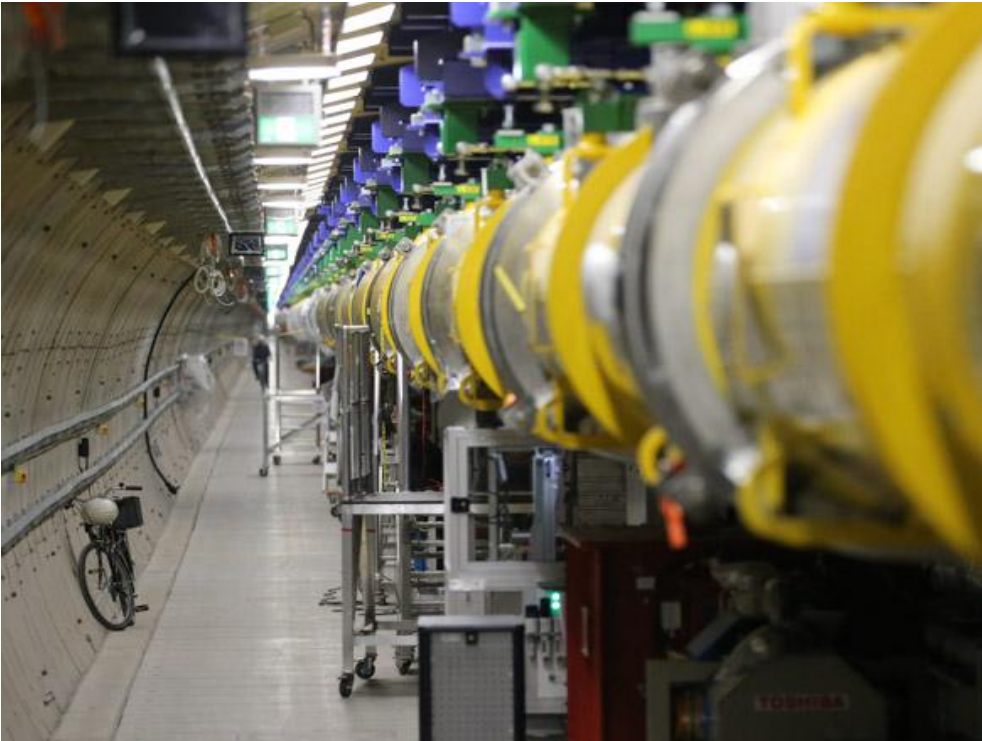
Huairou, Beijing, China - Sep.14-17, 2026

Agenda

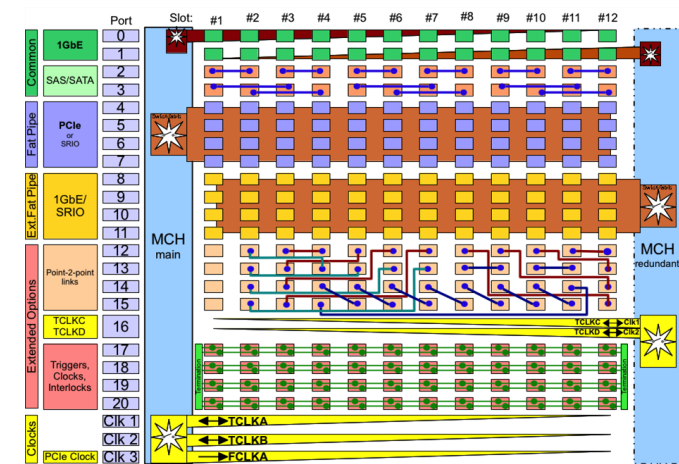
MicroTCA: Ecosystem and Licensing
From History to New Developments
What We Bring to the Community

Background

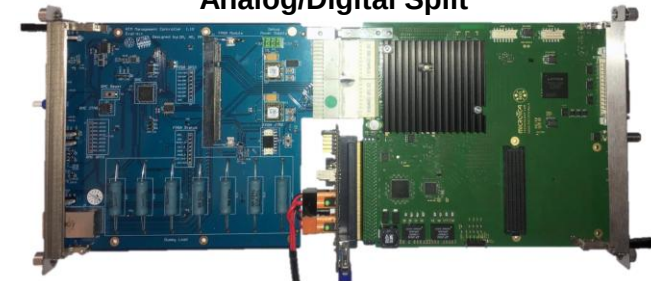
- **DESY MSK = Accelerator Beam Controls**
- Responsible for LLRF electronics of large FLASH and XFEL (and other) accelerators:
 - As part of large DESY team: concept, design, installation, operation and maintenance
 - 100% end-to-end development in-house: hardware (schematics, board, test), firmware and software 10 years+ of electronics life time (hostile environment), 24/7 operation, limited access to electronics



Powerful Backplane (PCIe, Triggers, P2P)

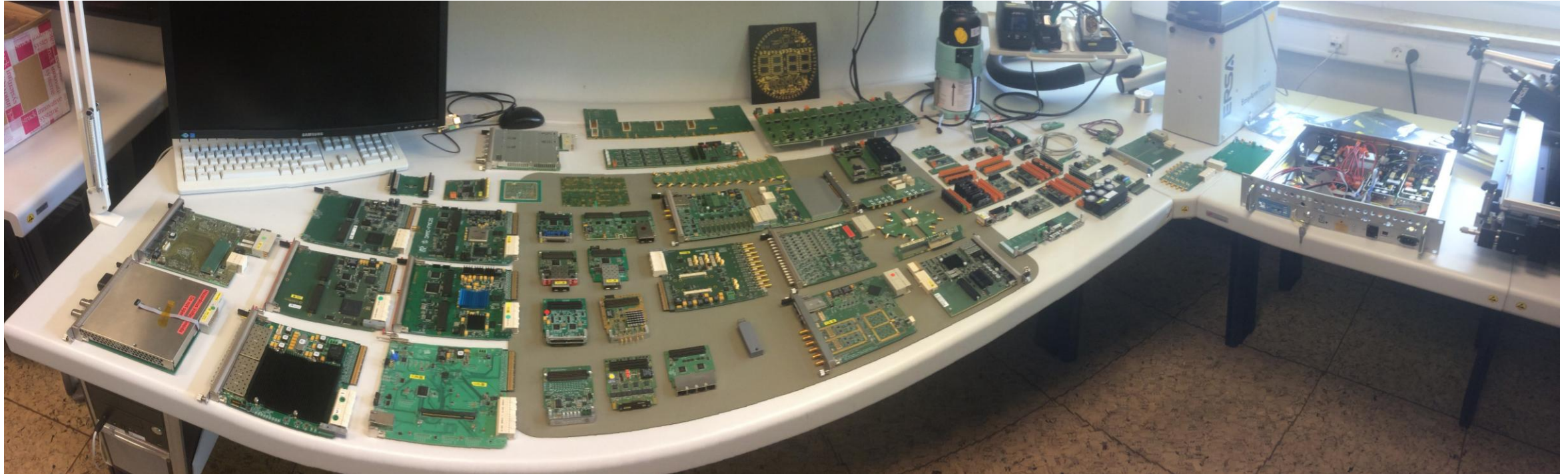


Analog/Digital Split



Main responsibility

We develop and maintain digital electronic boards



AMC

DAMC-FMC20
DAMC-FMC25
DAMC-FMC2ZUP
DAMC-FMC1Z7IO
DAMC-TCK7
DAMC-MOTCTRL
DAMC-DS812ZUP
DAMC-MMCB breakout
DAMC-Template
DAMC-AMCTest
DAMC-StarterMMC
DAMC-MMCNEEDLETEST
DAMC-UNIZUP
DAMC-X3TIMER
DAMC-DS5014

FMC

DFMC-AD16
DFMC-DS800
DFMC-MD22
DFMC-SFP4
DFMC-SIO
DFMC-TC4
DFMC-TestAdp
DFMC-UNI-IO

LISA

~ 5 Boards

RTM

DRTM-PZT4
DRTM-MXC
DRTM-AD84
DRTM-PZT4
DRTM-DS812FT
DRTM-CLKFT
DRTM-Template
DRTM-VM2

eRTM

DRTM-HVPM

19-inch boxes

X2 Converter Box
LDD (Mezzanine, Carriers)

19-inch components

FRED, FredFan, FredFanPWM (MO)
H-Bridge Driver
Redundancy Controller 4P
Redundancy Controller 3P+1N
ZMX Connection Module
TMCB2
GPIO Test
PowerSeqPatch
REFMOPT patch
Patchpanel (Uni-IO)

Eval Boards

DS8XX DC/DC Eval. Loop Eval.
Motion Controller DCDC Eval.
Coaxipack2 Eval

Development Support

RTM Standalone Driver
AMC Bringup Adapter
DFMC-Extender
FMC Test Carrier
SE2DIFF Adapter
Breakout MD22
Breakout AD16

Stand-Alone

DMMC-STAMP
RadCon
ZMX Test Board
NoiseEater

Company Support

Struck (MMC)
CAENels
Piezotechnics, Eicsys (PZT4)
Techlab
Embeck, Hitachi,
7Solutions, D-TACQ,
CEA

- Photo is 7 years old: Underlined Boards are not shown on picture
- *Italic* Boards are not developed by us, but maintained by us

Licensing Strategy

- We promote an ecosystem
- DESY has licensed almost all developments: components are available for us **and** for third parties
- Strategy: Concentrate on the application; purchase all “unexciting” infrastructure

AMC

DAMC-FMC2ZUP

Zynq Ultrascale+ MPSoC based Dual FMC/FMC+ Carrier Board with D1.1 RTM support



DAMC-FMC1Z7I0

Cost-Optimized IO Controller Board with one FMC socket

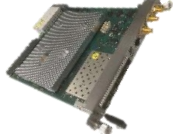


DAMC-TCK7

AMC Data Processing and Telecommunication Module



DAMC-UNIZUP



ADVANCED MEZZANINE CARDS

AMC boards (Advanced Mezzanine Card) are the key components of a MicroTCA system. Within the MicroTCA.4 crate, AMCs are placed in the front of the crate. They are connected by a high-speed backplane that carries serial links, power and management data. Every AMC card is monitored and managed. This allows hot-plug, hot-swap, health monitoring and thermal management of the modules.

There are six standard sizes of AMCs: single and double width as well as compact, mid-size and full-size height. Every combination of width and height is valid. The power consumption of an AMC is divided into 3.3V management power plus 12V payload power.

AMC boards are used for digital processing. On every AMC board there is a controlling unit called MMC (Module Management Controller). Plugging in the AMC board to the MTCA crate connects the board to the backplane of the crate. The backplane ensures the connection of the AMC boards with every other AMC board in the crate. Plus, every AMC board is connected to the MCH (MicroTCA Carrier Hub), which is the overall management card of the MTCA system. The MCH gives management power to the AMCs first. This power is used to check if everything is ok with the AMC. If the MMC, the managing unit on the AMC detects no problems on the board, the MCH gives payload power to the AMC.

Clustering of AMCs in the system is possible.

DAMC-FMC25

AMC Dual HPC-FMC Carrier



DAMC-FMC20

AMC Dual FMC Carrier Board



X2TIMER

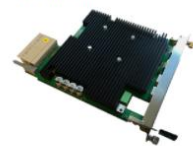
AMC Fast Timing System



RTM

DRTM-MXC

Mobile GPU Carrier



DRTM-AD84

RTM 8Ch ADC, 4Ch DAC



DRTM-PZT4

RTM 4 Channel Piezo Driver



REAR-TRANSITION-MODULES

RTMs, the rear-transition-modules, are extension boards that are placed in the back of the MTCA.4 crate. They directly connect to the front AMCs via the Zone 3 connector. The possibility to separate analogue and digital functions by moving sensitive analogue electronics to the RTM is one of the key strengths of MicroTCA.4.

DRTM-DWC8VM1

RTM 8 Channel Down-Converter 1 Channel Up-Converter



DRTM-LOG1300

eRTM Local Oscillator Generation



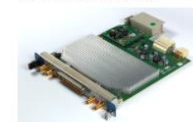
DRTM-VM2LF

RTM 2 Channel Vector Modulator Low Frequency



DRTM-DWC10

RTM 10 Channel Down-Converter



DRTM-DS8VM1

RTM 8-Channel Direct Sampling 1-Channel Vector Modulator



DRTM-VM2HF

RTM 2 Channel Vector Modulator High Frequency



DESY MMC Stamp



FMC

DFMC-DS800

FMC Direct-Sampling A-D Converter



DFMC-AD16

FMC 16-channel A-D Converter



DFMC-TESTADP

FMC Loopback Adapter



FPGA MEZZANINE CARDS

FPGA Mezzanine Card (FMC) is a standard defining I/O mezzanine cards and corresponding carrier boards. Huge ecosystem of carrier boards, both in MicroTCA format and standalone boards, provides a good prototyping platform, suitable for experimental physics and industrial applications. The FMC mezzanine format provides additional degree of modularity for a lot of I/O applications, such as ADC and DAC boards, or communications boards.

DFMC-MD22

FMC 2 channel stepper motor driver



DFMC-SFP4

FMC 4-Channel SFP+ Adapter



DFMC-UNI-IO

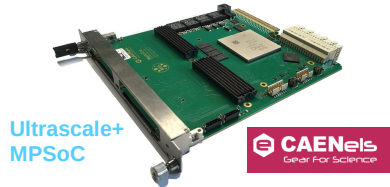
FMC Multi-Purpose I/O Board



All SoC developments of the last few years

Similarity 1: Boards are all based on DMMC-STAMP

DAMC-FMC2ZUP (Supercarrier)



(DMMC-STAMP)



DAMC-FMC1Z7IO



DAMC-DS812ZUP



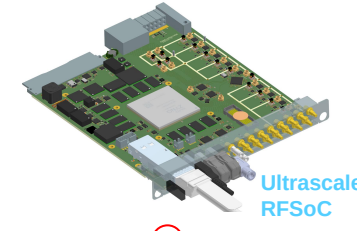
DAMC-MOTCTRL



DAMC-UNIZUP



DAMC-DS5014DR
(RFSoc-based)



DAMC-X3Timer



2019

2020

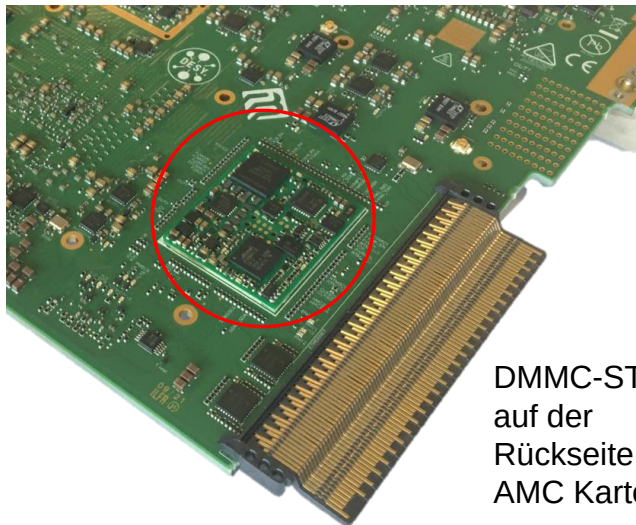
2021

2022

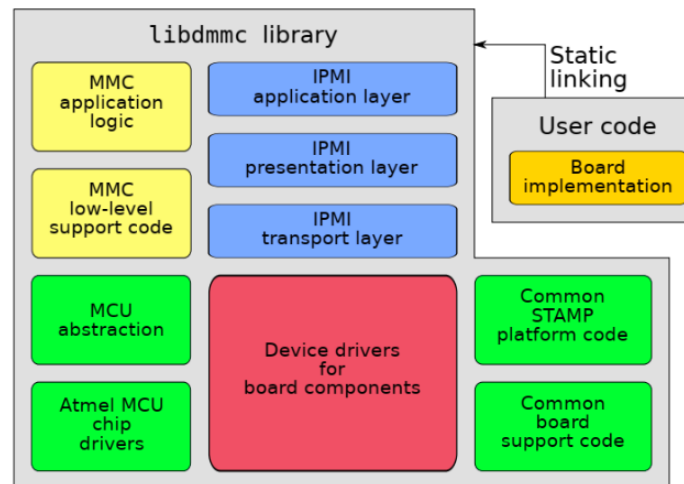
2023

2024

2025



DMMC-STAMP
auf der
Rückseite der
AMC Karte



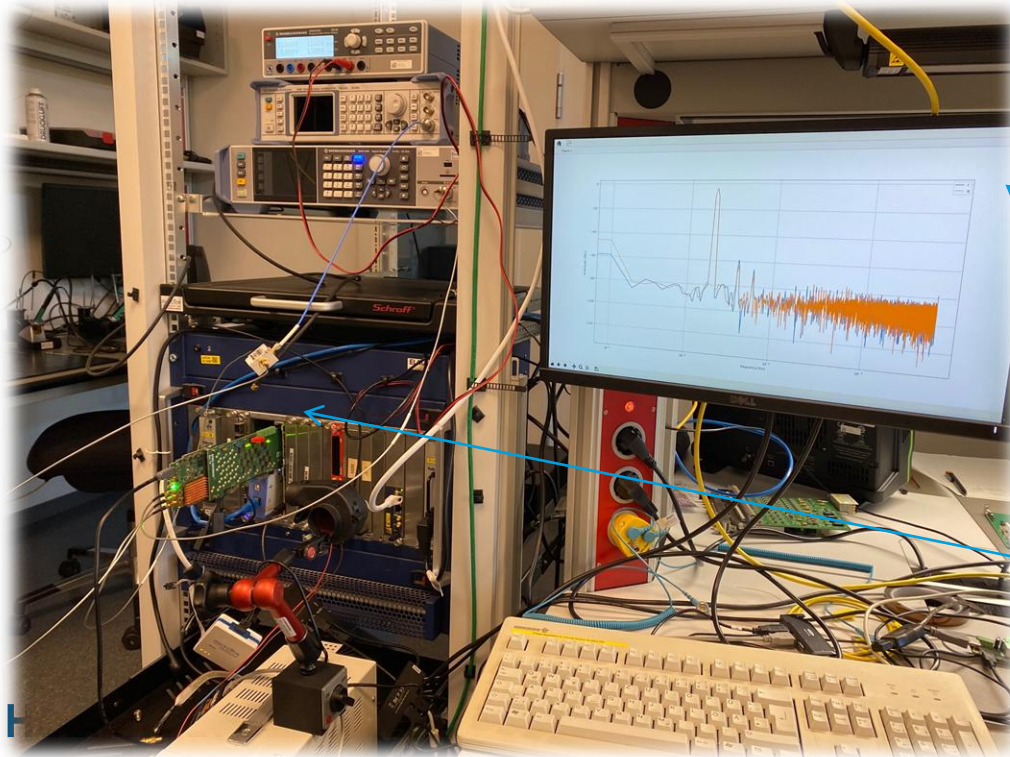
- DMMC-Stamp handles MicroTCA Management
- Complete software framework
- 95% re-use
- Compatibility with all MCHs we know of
- In-system update (from MMC and FPGA)
- Serial-over-IPMI (remote access to the FPGA and MMC UART)
- 2024: over 1000 pieces produced
- used by 30 partners
- 100% test in the needle test adapter



Why MPSoC?

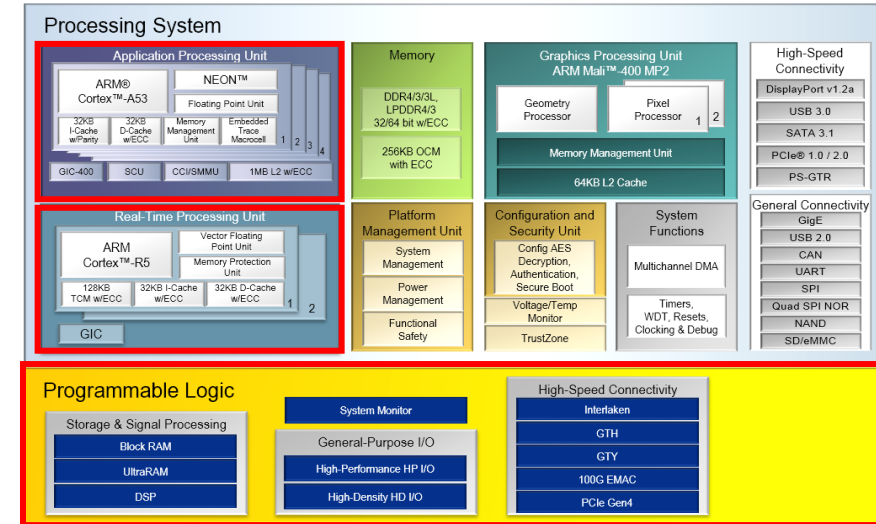
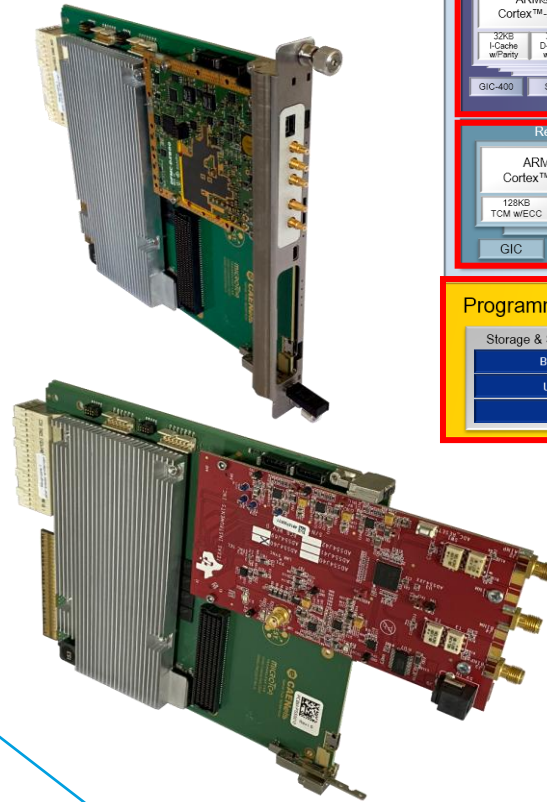
Similarity 2: Processor inside FPGA

- Everything is SoC-based
- Processor-centric approach (“Raspberry Pi in FPGA”)
- Changed development method towards: “on-the-fly”, “re-use”, “modular” and “low-code”
- Keywords: IP modules, Linux, Python



Courtesy of J. Marjanovic and S. Farina

DESY DAMC-FMC2ZUP Board

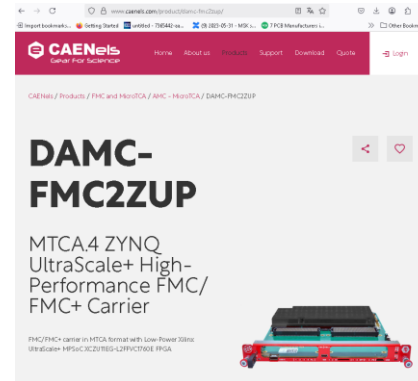


- DAMC-FMC2ZUP board runs graphical **Linux desktop** (Displayport)
- Additionally: **Web server** with Jupyter
- DAMC-FMC2ZUP collects data from FMC-DS500; Output via **Python** Mathplotlib



High performance processing MPSoC-based FMC carrier

DAMC-FMC2ZUP

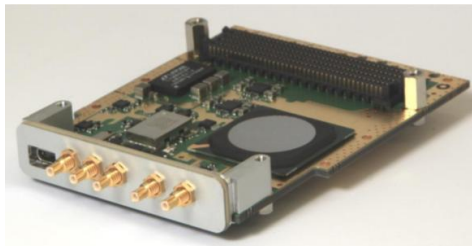


“Working horse”, very powerful, very flexible FMC carrier - is part of a family of boards.

Main Features:

- High-performance FPGA: Zynq UltraScale+ **ZU11EG or ZU19EG**
- Full Backplane and RTM D1.1 connectivity
- **FMC/FMC+** mezzanine support (**28 Gbps**)
- Quad-Core ARM Cortex-A53 @1.5 GHz, Dual-Core ARM-R5 RT @600 MHz and Mali-400 MP2 graphics
- PCIe x4 (**x8** option on supported systems); Gen.3 supported
- **USB type-C Alternate Mode Display Port** for standalone operation (no need for additional AMC CPU Module)
- Flexible clocking scheme and front panel connector for external clock input and **White Rabbit support**
- Supported by all Xilinx development tools (e.g. Vivado HLx)

DFMC-DS800



DFMC-MD22

FMC 2 channel stepper motor driver

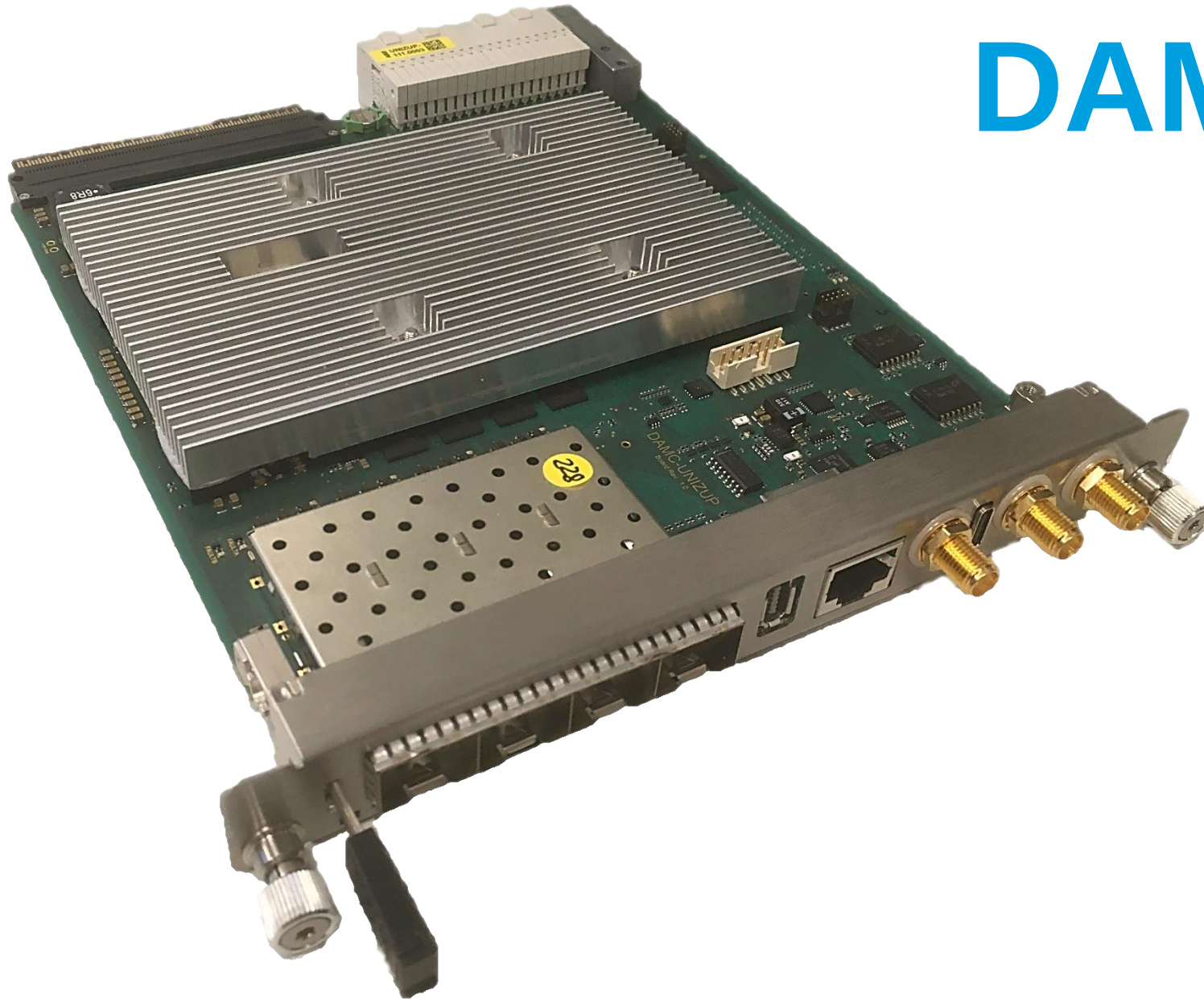


DFMC-AD16

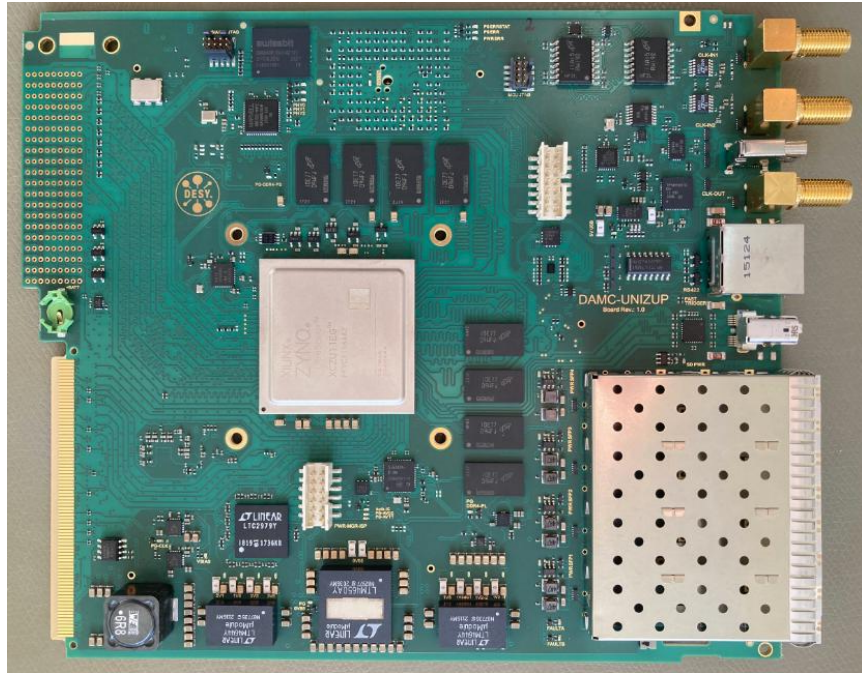
FMC 16-channel A-D Converter



DAMC-UNIZUP



DAMC-UNIZUP



“Little Sister” of DAMC-FMC2ZUP

- Lower-cost-board with smaller FPGA: hundreds of units will be needed at Petra IV
- 14 instead of 16 layers, 0402 components, (only 0201 capacitors)

Facts

- Board inherits the **technology of DAMC-FMC2ZUP**
- Universal MPSoC board with high-performance **RTM connectivity**
- Large FPGA (in smaller package):
Zynq Ultrascale+ **ZU7CG...ZU11EG**

New:

- **2 x 64bit wide** DDR4 interfaces (in total 8GiB RAM)
- **4 integrated SFP+** slots with 16.375 Gbps (not 28 Gbps GTY)
- Connectors for “**slow trigger**” (RS485 for machine protection) and “**fast trigger**” on Front Panel
- 2 Front panel clock inputs via SMA, 1 Output



INSTRUMENTATION
TECHNOLOGIES

Inherited features:

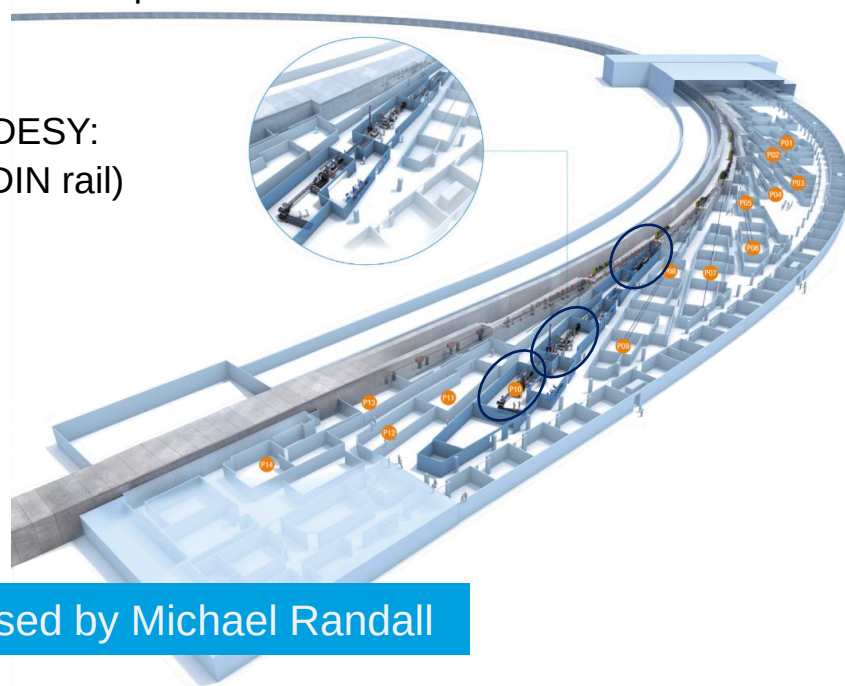
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Motion Controller

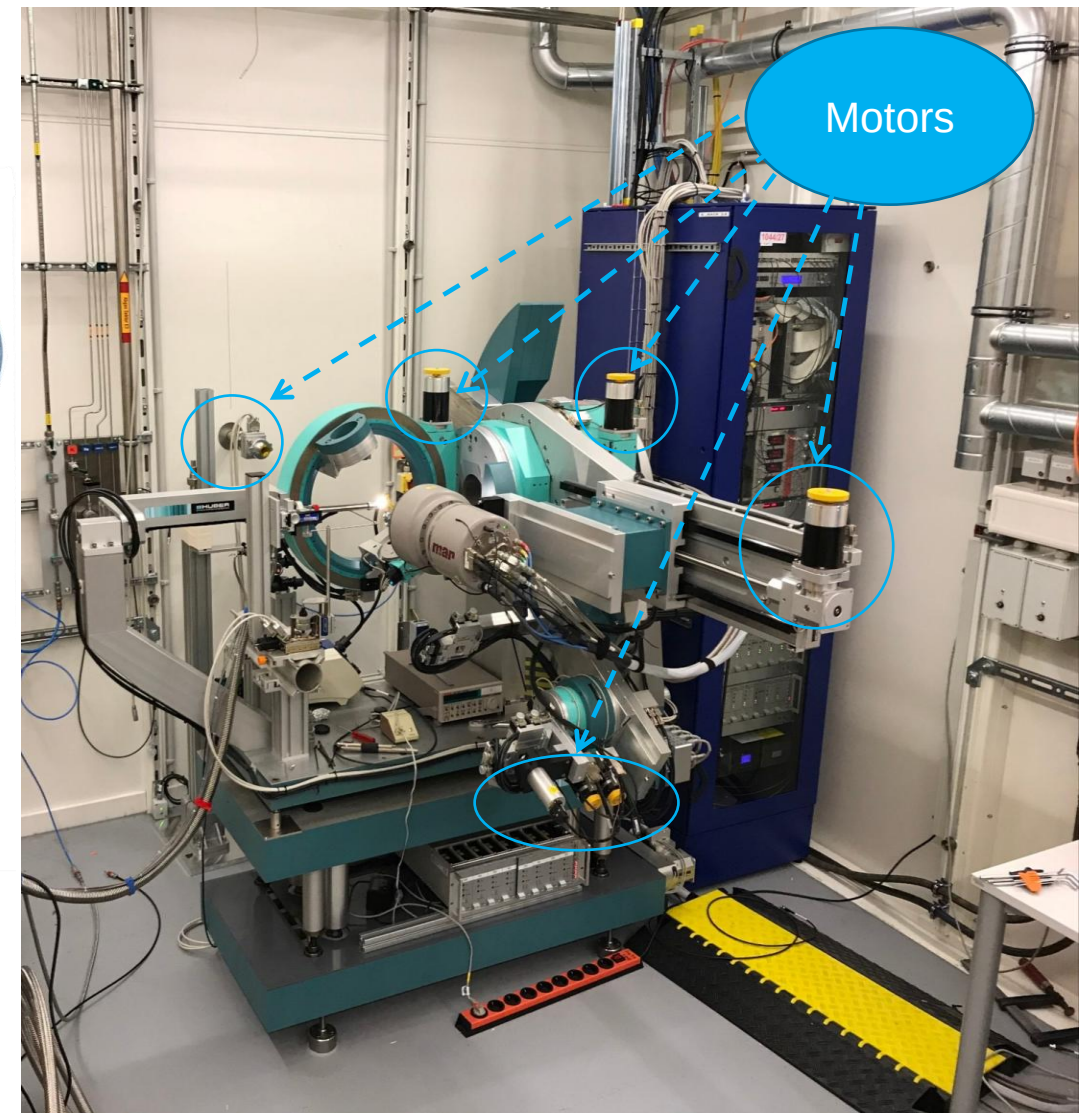
- DESY needs to move motors in experiments

- Popular motion control at DESY:
 - Beckhoff EtherCAT (DIN rail)
 - OMS MAXv (VME)



Already discussed by Michael Randall

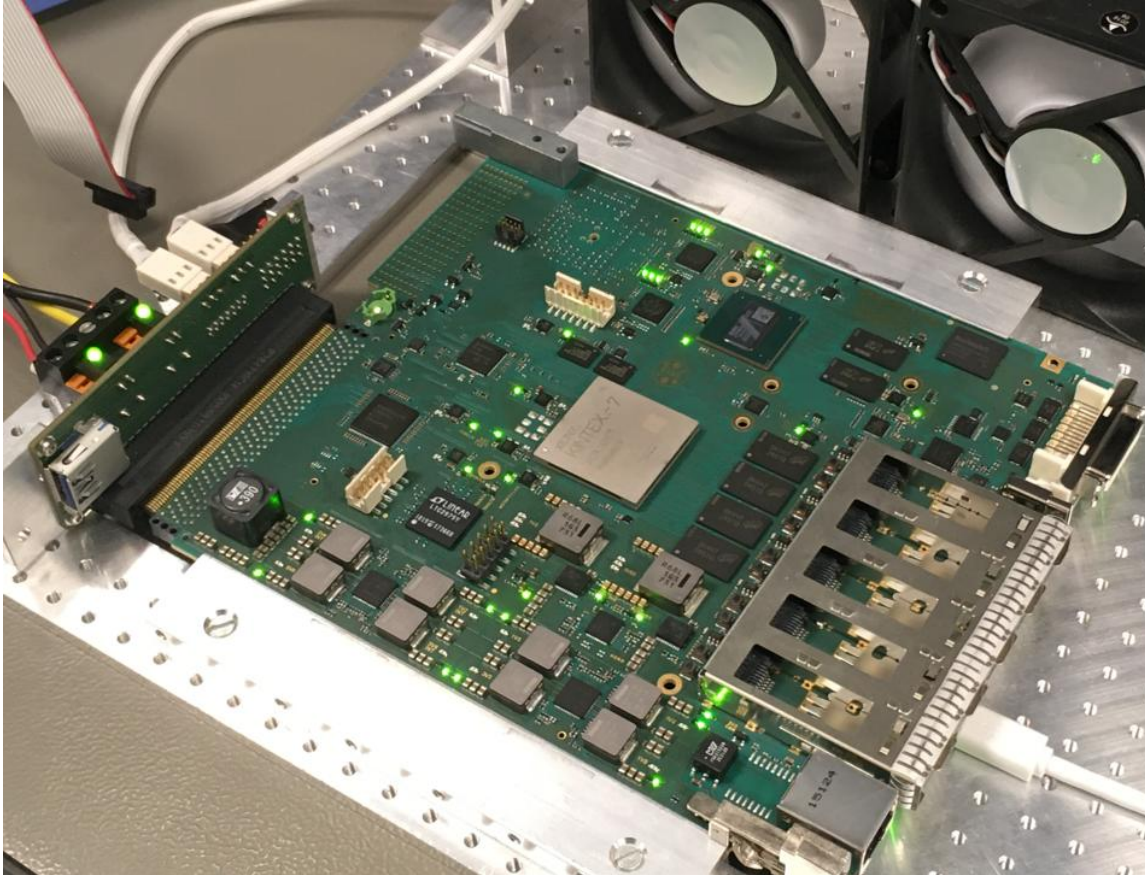
- MicroTCA infrastructure is planned for upcoming Petra IV
- A replacement for VME systems is required
 - to overcome limitation of 8 motors per card,
 - to provide (long-desired) card-to-card communication
- DAMC-MOTCTRL:
 - Controls (min.) 48 motors/axis per card (FW depended)
 - Scalable interconnection of several cards in the crate and campus-wide
 - Position-triggered data acquisition with other MicroTCA cards
 - Focus on competitive cost factor (licensing planned)



Diffractometer at Beamline
(Martin Tolkiehn)

Hardware Plattform

Hardware Plattform



- Board is fully running in Rev. A
- No single patch wire.



- **Heterogeneous Approach**
 - MPSoC (2GB DDR4) and FPGA (4GB DDR3)
 - Kintex-7: real-time control
- **MPSoC:**
 - Raspberry Pi“ inside the FPGA (runs Yocto Linux)
 - responsible for non-realtime tasks
 - communication to other cards
- 5 SFP+ ports (1Gbps to 10Gbps)
 - e.g. 3x Motor interfaces, 2x Ring topology
- HW Support: CAN EtherCAT, SERCOS
- Backplane Ethernet
- 26-pin connector: 3.3V /5V IO
- Monitor/Keyboard interface via USB-C

DAMC-DS812ZUP

8-Channel Giga-sample Digitizer

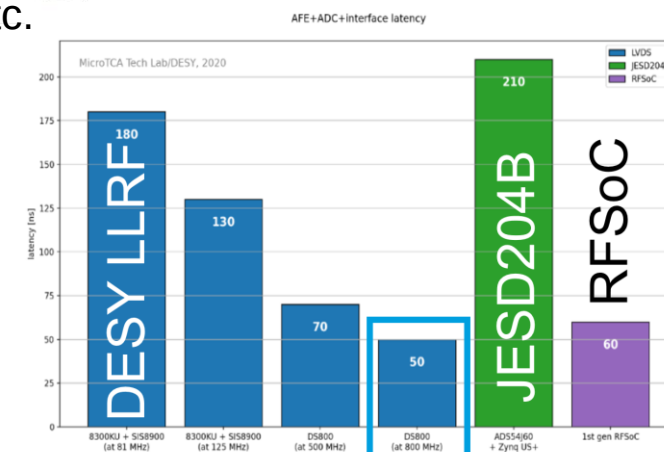
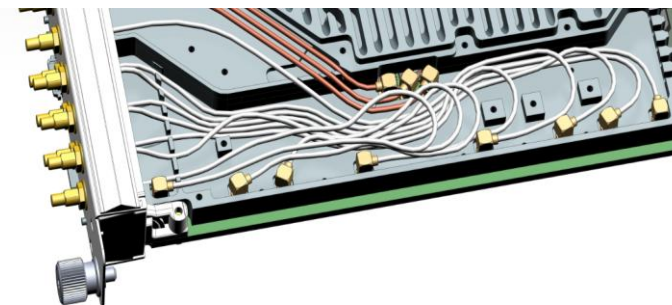
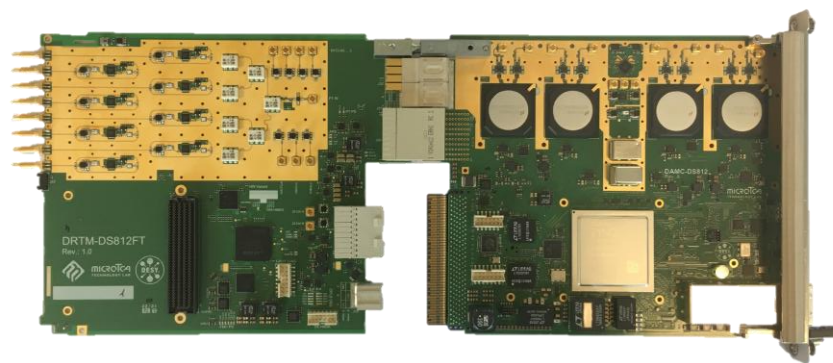


Modes of operation:

- 8-Channel 800 MSPS digitizer or 4-channel 1600 MSPS

New:

- Coaxial Zone-3 connection “RF1.0”
- Front panel/ RTM swapping concept using semi-rigid coaxial RF cables
- Front Panel: oscilloscope-like application and board bring-up
- RTM: space for signal conditioning, filters, etc.



Main Features:

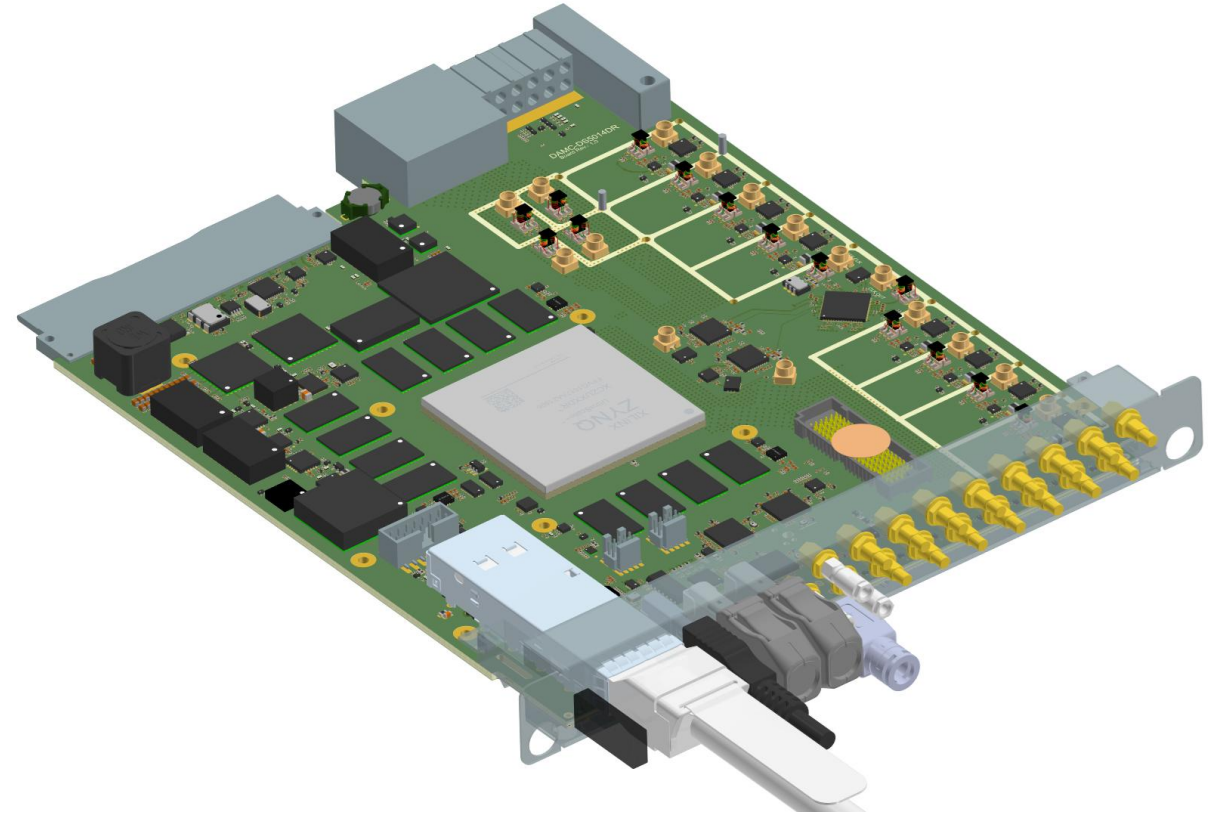
- 2.7GHz input BW, 12bits, 8-channels (Amplifier Bandwidth: 4.8 GHz)
- 50ns end-to-end latency
- **Coaxial analog Zone 3 RF1.0 Class**
- RF input from front panel or RTM: 800 MSPS / 1600 MSPS
- On-board PLL: 14fs jitter



DAMC-DS5014DR- High-speed Digitizer

Main Features

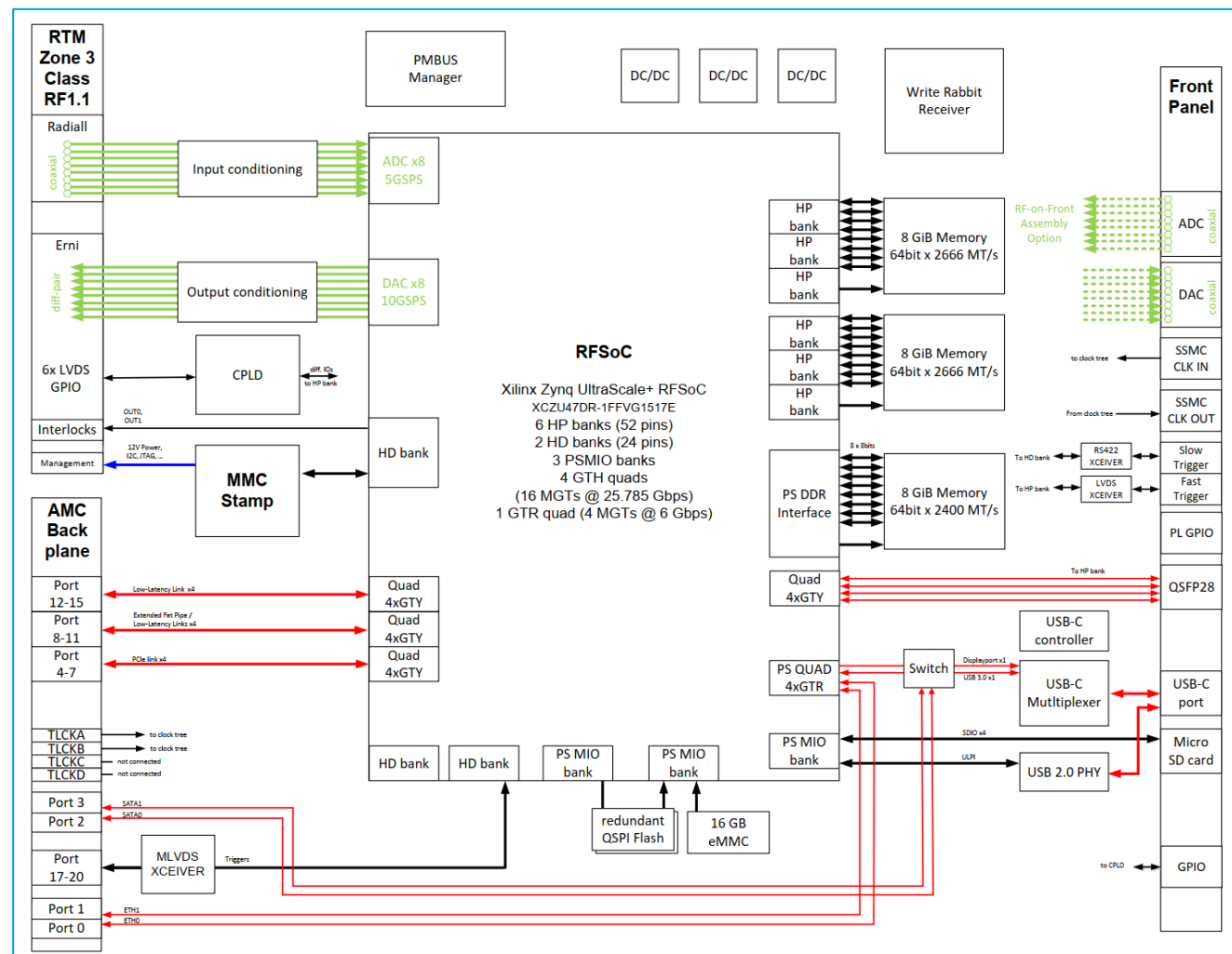
- 6.0 GHz analog bandwidth (-3 dB)
- Single-ended analog RTM connection (Class RF1.1)
- 8 analog inputs and 8 analog outputs via RTM
- Alternatively up to 8 analog inputs and/or outputs on front panel via coaxial SSMC connector
- 5.0 GSPS per channels ADC sampling rate
- 3x DDR4 banks with up to 24 GB DRAM
- Dual-Loop Low-Jitter PLL On-Board
- 9.85 GSPS per channels DAC data rate
- 4 front-panel Trigger channels (input/output)



DAMC-DS5014DR- High-speed Digitizer

Main Features

- FPGA: AMD Ultrascale+ RFSoc XCZU47DR-1 (default)
- Analog signal range 1 Vpp (± 0.5 V)
- AC or DC coupling, depending upon assembly variant
- Internal or external clock reference and ref. output
- White Rabbit support
- Event timestamp
- 24 GB onboard memory (>6 Gsamples storage capacity for 14-bit ADC data with a 16-bit timestamp).
- PCIe Gen.3 x 8 and 100G Ethernet data interfaces (PCIe Gen.4 would be available with speed grade -2 FPGA only)
- Fully customized firmware code available for fast data processing
- FPGA open for custom application (open-source BSP)
- Yocto Linux support
- Standalone mode (can run without AMC CPU module)



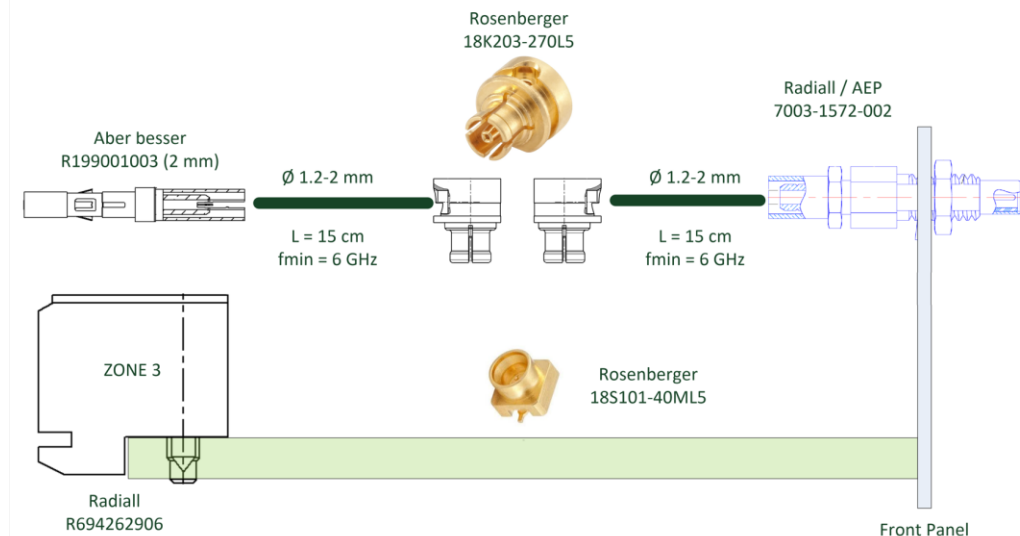
ZONE 3 Interface

ERNI and Radiall Connectors

208	Zone 3 Interfaces with RTM (Class RF1.1)	Pin Assignment	Pin Number	I/O	Description	
209	J30 ERNI Connector	PWRA1, PWRA2, PWRB1, PWRB2	1a, 2a, 1b, 2b	I	RTM supply voltage (12 V, 30 W max.)	
210		PS#	1c	O	RTM present signal (connected to GND on RTM)	
211		SDA, SCL	1d, 2d	I/O	I2C management interface to- RTM (level 3.3 V)	
212		TCK, TDI, TDO, TMS	1e, 2e, 1f, 2f	I/O	JTAG interface to RTM	
213		MGT-RX±	3a, 3b	I/O	Gigabit receiver, not implemented	
214		DAC0±, DAC1±, DAC2±, DAC3±, DAC4±, DAC5±, DAC6±, DAC7±	3a, 3b, 3e, 3f, 4c, 4d, 5a, 5b, 5e, 5f, 6c, 6d, 7a, 7b, 7e, 7f	O	Differential DAC outputs, DC coupling	
215		D0-CC±, D1±, D2±, D3±, D4±, D5±, D6±, D7±/OUT0± D8±/OUT1±	3c, 3d, 4a, 4b, 4e, 4f, 6a, 6b, 6e, 6f, 7c, 7d, 9c, 9d, 9e, 9f	I/O	LVDS (Vcm 1.2V, Vdiff 350mV, 100R), connected to the PL HP bank (1.8V) Note: This interface is intended to carry a differential SPI Bus with LVDS levels. A CPLD on the RTM can fan out these signals into standard SPI and I2C busses.	
216		RTM-CLK±	8a, 8b	I	LVDS/LVPECL clock input from RTM to the RF synthesizer	
217		RF-CLK0±, RF-CLK1±, RF-CLK2±, RF-CLK3±	10a, 10b, 8c, 8d, 10c, 10d,8e, 8f	I	RF-CLK0± is connected to the ADC(Tile3) RF-CLK1± is connected to the DAC(Tile0) Not implemented	
218		AMC-TCLK±	9a, 9b	O	LVDS/LVPECL clock output to RTM derived from TCLK	
219		OUT0/D6±, OUT1/D7±	9c, 9d, 9e, 9f	I/O	LVDS (Vcm 1.2V, Vdiff 350mV, 100R) trigger, interlock or user IO connected to the PL HP bank (1.8V)	
220		AMC-CLK±	10e, 10f	O	LVDS/LVPECL output clock to RTM from RF synthesizer	
221						
222						
223		J31 Radiall Connector	DAC-OUT0, DAC-OUT1, DAC-OUT2, DAC-OUT3	1a, 1b, 2a, 2b	O	Single-ended DAC outputs, AC coupling
224			ADC-IN6, ADC-IN7	3a, 3b	I	Single-ended ADC inputs, AC coupling
225						
226						
227		J32 Radiall Connector	ADC-IN0, ADC-IN1, ADC-IN2, ADC-IN3, ADC-IN4, ADC-IN5	1a, 1b, 2a, 2b, 3a, 3b	I	Single-ended ADC inputs, AC coupling
228						

		Digital Clock I/O	Digital Fixed I/O	Digital Clock Input		Digital User I/O	Differential DACs			MTCA.4 Management		
J30		10	9	8		7	6	5	4	3	2	1
-	f	AMC-CLK-	OUT1-/D8-	RF-CLK3-		DAC7-	D5-	DAC4-	D2-	DAC1-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D8+	RF-CLK3+		DAC7+	D5+	DAC4+	D2+	DAC1+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D7-	RF-CLK1-		D6-	DAC5-	D3-	DAC2-	D0-CC-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D7+	RF-CLK1+		D6+	DAC5+	D3+	DAC2+	D0-CC+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-		DAC6-	D4-	DAC3-	D1-	DAC0-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+		DAC6+	D4+	DAC3+	D1+	DAC0+	PWRA2	PWRA1
Single Ended Analog Signals												
J31		3	2	1								
	B	ADC-IN7	DAC-OUT1	DAC-OUT3								
	A	ADC-IN6	DAC-OUT0	DAC-OUT2								
J32		3	2	1								
	B	ADC-IN1	ADC-IN3	ADC-IN5								
	A	ADC-IN0	ADC-IN2	ADC-IN4								

Zone 3 – Class RF1.1 pin assignment J30, J31, and J32 Connector, AMC side View.



We invite everybody to be part of the MicroTCA ecosystem

What we can offer...

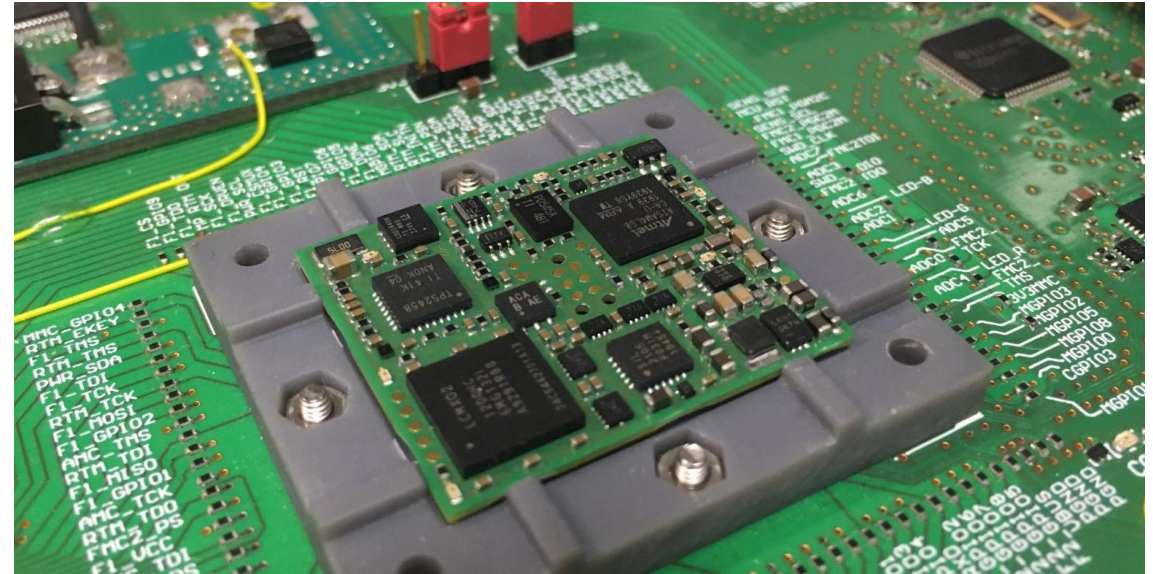
Creative Commons License



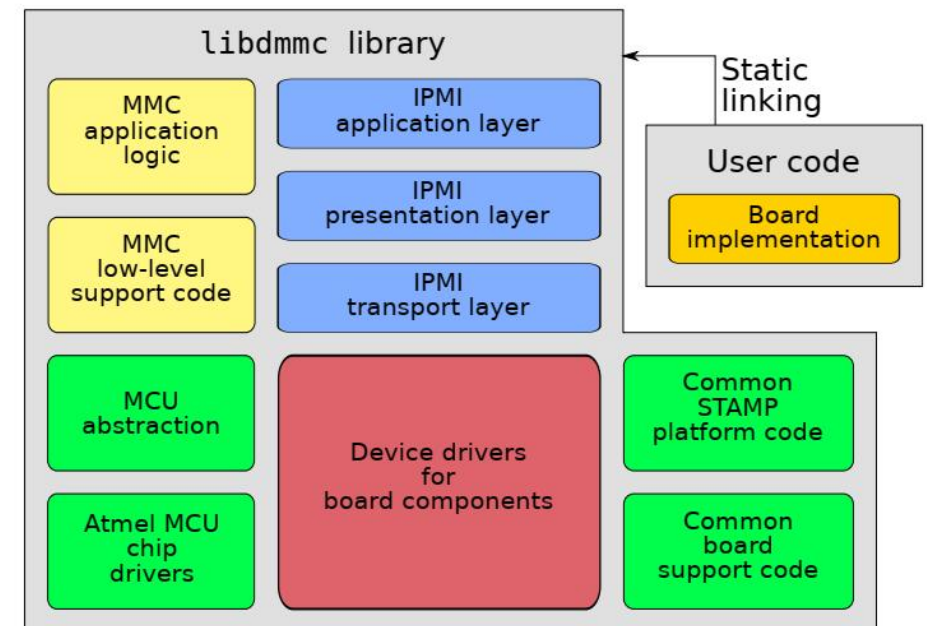
DMMC-STAMP: A complete Management solution for MicroTCA

- ▶ System on Module (SoM)
 - ▶ 25.5 x 29.5 x 2.3 mm
 - ▶ Pre-programmed firmware
 - ▶ Evaluation board available (BoB)
- ▶ Software Development Kit (SDK)
 - ▶ MMC firmware customization
 - ▶ DESY MMC Software Library (libdmmc)
 - ▶ Example implementations (BoB, DAMC-FMC2ZUP)
- ▶ Open Source Tools and Templates
 - ▶ AMC and RTM Altium Designer Templates
 - ▶ mmcterm: serial over IPMB
 - ▶ bin2hpm: create HPM files for IPMI upgrade
 - ▶ frugy: read and write FRUs
 - ▶ cpld-img-tools: bitstream conversion for Lattice CPLDs

Patrick Huesmann



Post-Production test of DMMC-STAMP



MicroTCA.4 Template

Community Support

Idea: Jump-Start with MicroTCA as you would with any other board

Fully MicroTCA compliant “empty” board

- Already “fully functional”
- Start with correct mechanical shape
- AMC and RTM “only” get power
- All the management is done on DMMC-STAMP

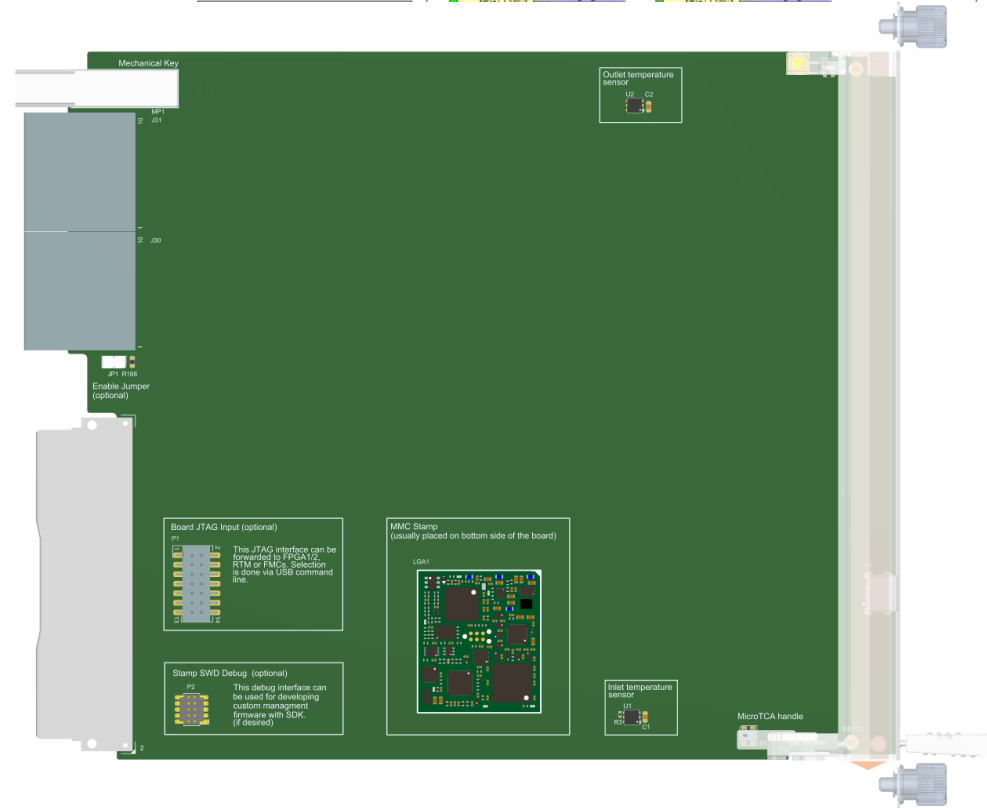
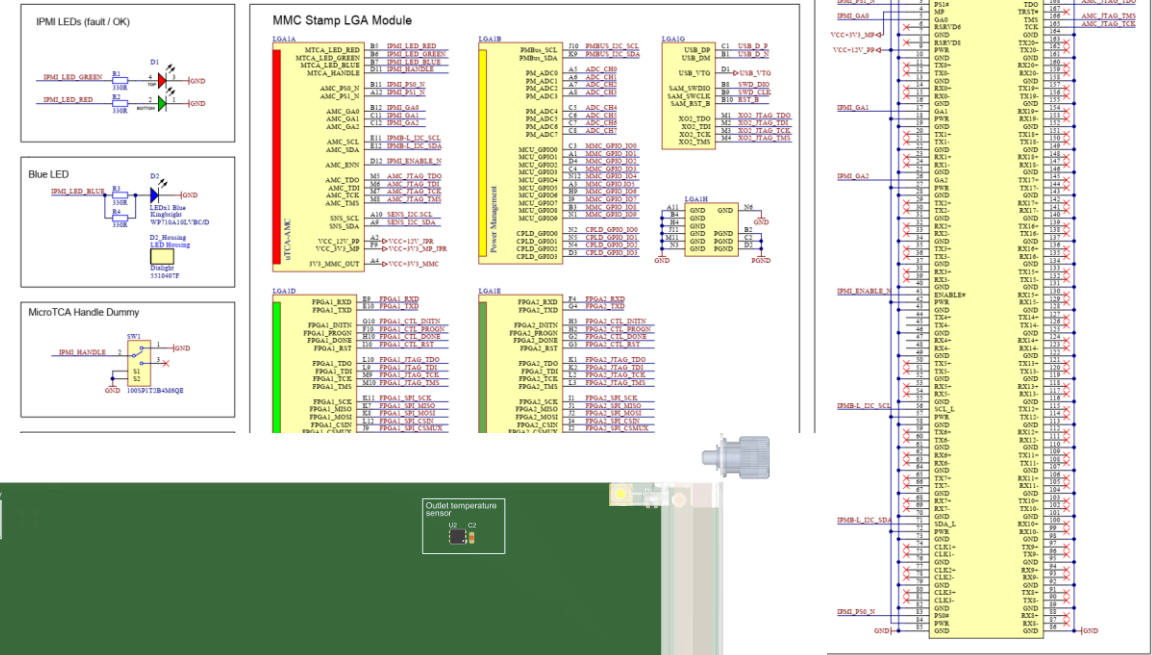
Purpose: facilitate development

- Allows design migration (e.g. from VME)
- Source design files (Altium Designer) are provided
 - Schematics
 - PCB

Components:

- MMC SoM, LEDs, Connectors, Temperature Sensors
- USB Interface for management and status

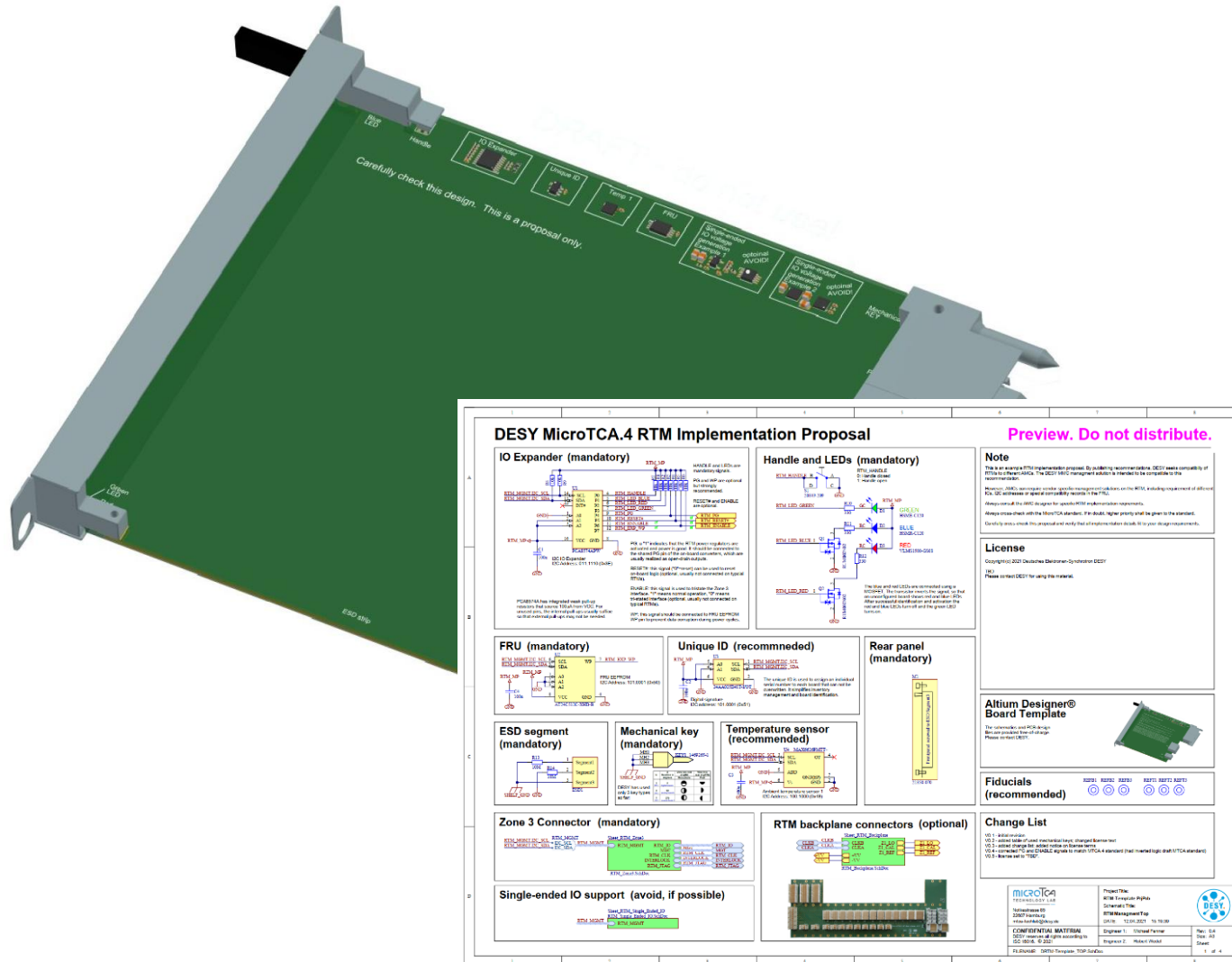
Mandatory Components on AMC Card



 microTCA EChNOLOGY LAB Holtstraße 10 2007 Hamburg desy-technik@desy.de		Project Title: DMMC-STAMP-BreakOut.C.PyPCB		
		Schematic Title: Mandatory Components		
		DATE: 15.12.2019 01:53:40		
		Engineer 1: Michael Fenner		
CONFIDENTIAL MATERIAL DES.Y reserves all rights according to IEC 10016. © 2019	Engineer 2: S. Chytkov / J.Zink		Rev: B	
			Size: A3	
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L.ENSURE: Mandatory SchDoc				

RTM Template

Community Support



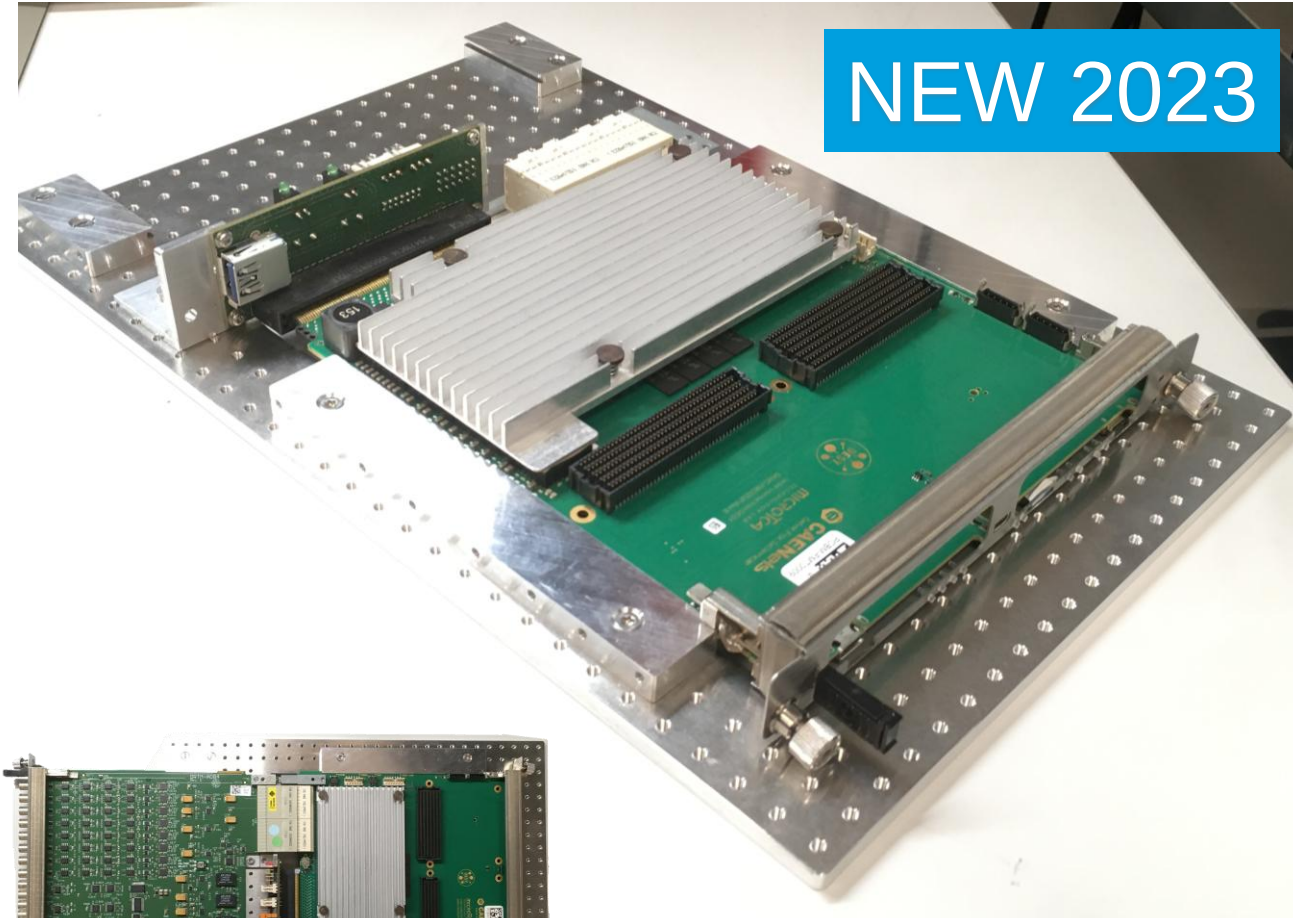
- We also provide a RTM Template
- Complete guide and “empty board” for own MTCA RTM designs ☐ Altium Designer Template
- MTCA Standard leaves freedom for RTM interface implementation (vendor-specific) ☐ risk of non-interchangeable AMC-RTM pairs
- DESY has a “class concept” ☐ Interchangeable boards
- DESY collected and documented best design practices beyond the standard



Benchtop Setup - Typical Bring-Up environment

NEW 2023

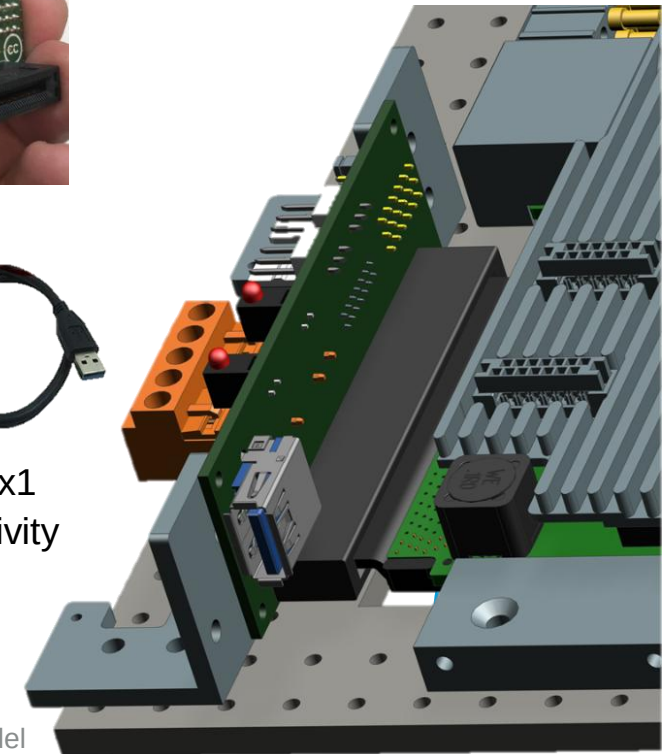
- We have flexible lab development tools
- DESY provides them on request:
 - Aluminum frame production files
 - Bring-up PCB production files



With RTM Support...



Adapter brings out PCIe x1
Gen. 3 (8Gbps) connectivity
„on the lab desk“



Typical Lab bring-up Setup



- Flexible and handy development tools
- DESY provides them (Creative Commons)
 - bring-up PCB production files
 - Aluminium frame production files

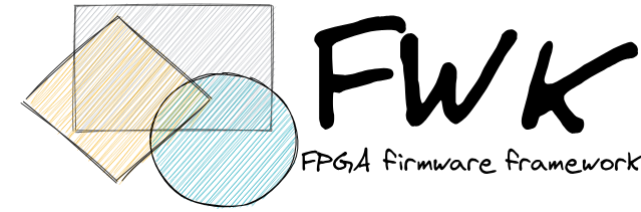


Write an email to me if you are interested in these designs.



FWK: The Swiss Army Knife of FPGA development

- MSK Firmware group maintains a large open-source repository for FPGA development. It contains:
 - BSPs, IPs,
 - FWK, Scripts, Tools, Example Designs in Vivado
 - Documentation
 - Is actively used in DESY's accelerators
- FWK: FPGA development toolkit written in Tcl for large FPGA projects
- Create and implement FPGA project using various vendor tools (including Vivado)
- Handle versioning
- Combine multiple IPs and create address mapping for each register
- Create documentation of the IPs
- Package an IP
- Create an IP using Higher-Level-Synthesis (eg. Xilinx HLS)
- Embedded Linux Creation with Yocto Flow



FPGA firmware

Group ID: 45 [Leave group](#)

The MSK FPGA firmware framework with projects and their components.

Go to [MSK Firmware documentation site](#) for more details.

Subgroups and projects Shared projects Archived projects

> A	Applications and Scripts ⓘ High level software applications and scripts used to operate firmware
> L	Libraries ⓘ VHDL libraries
> M	Modules ⓘ RTL modules (IPs) sources
> P	Projects ⓘ Master projects
> S	Software ⓘ Software that runs on FPGA. Bare metal or OS applications.
> T	Tools ⓘ
> Y	Yocto ⓘ
📄	Documentation ⓘ The main firmware documentation module. Default on Antora generated site.
📁	Firmware Framework ⓘ The main firmware framework project

Visit now!

gitlab.desy.de/fpgafw

Documentation:

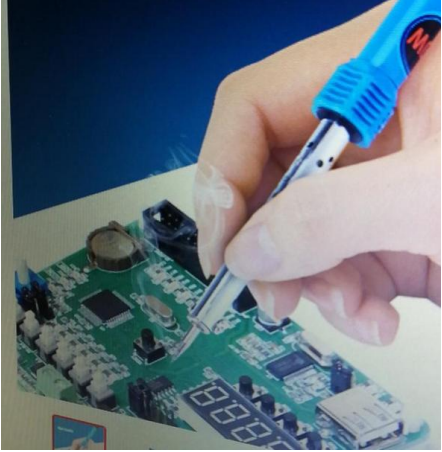
fpgafw.pages.desy.de/docs-pub/doc/



Summary

- **Overview:** DESY's MSK Digital Team develops and maintains FPGA- and SoC-based MicroTCA platforms for accelerator beam control, focusing on reliability, modularity, and full in-house hardware/firmware/software development.
- **Ecosystem & Licensing:** DESY has licensed nearly all of its developments, making the components accessible both internally and to external partners. The strategy is to focus on application-specific solutions while sourcing standard infrastructure from external suppliers.
- **Key Hardware:** The DMMC-STAMP ecosystem standardizes MicroTCA management, allowing for significant hardware/firmware reuse (95%), supporting in-system updates, and has been adopted by over 30 partners due to its open licensing strategy. Boards like DAMC-FMC2ZUP (high-performance MPSoC carrier), DAMC-UNIZUP (cost-optimized version), and DAMC-MOTCTRL (motor controller) enable scalable, processor-centric, "Raspberry Pi inside FPGA" solutions for data acquisition and control. High-speed digitizers: Includes 8-channel gigasample digitizers (DAMC-DS812ZUP), RFSoc-based converters (DAMC-DS5014DR).
- **Development Support:** DESY provides open-source FPGA tools (FWK), Altium design templates for AMC/RTM boards, and lab bring-up setups under Creative Commons to encourage community collaboration and rapid prototyping.
- **Future Outlook:** Next-generation MTCA efforts focus on PCIe Gen 5, 100 GbE, higher power per AMC (up to 220 W), and lower latency to meet the demands of future large research facilities.

Thank you!



-> https://www.reddit.com/r/electronics/comments/d62qwi/karen_hold_it_like_you_were_soldering/

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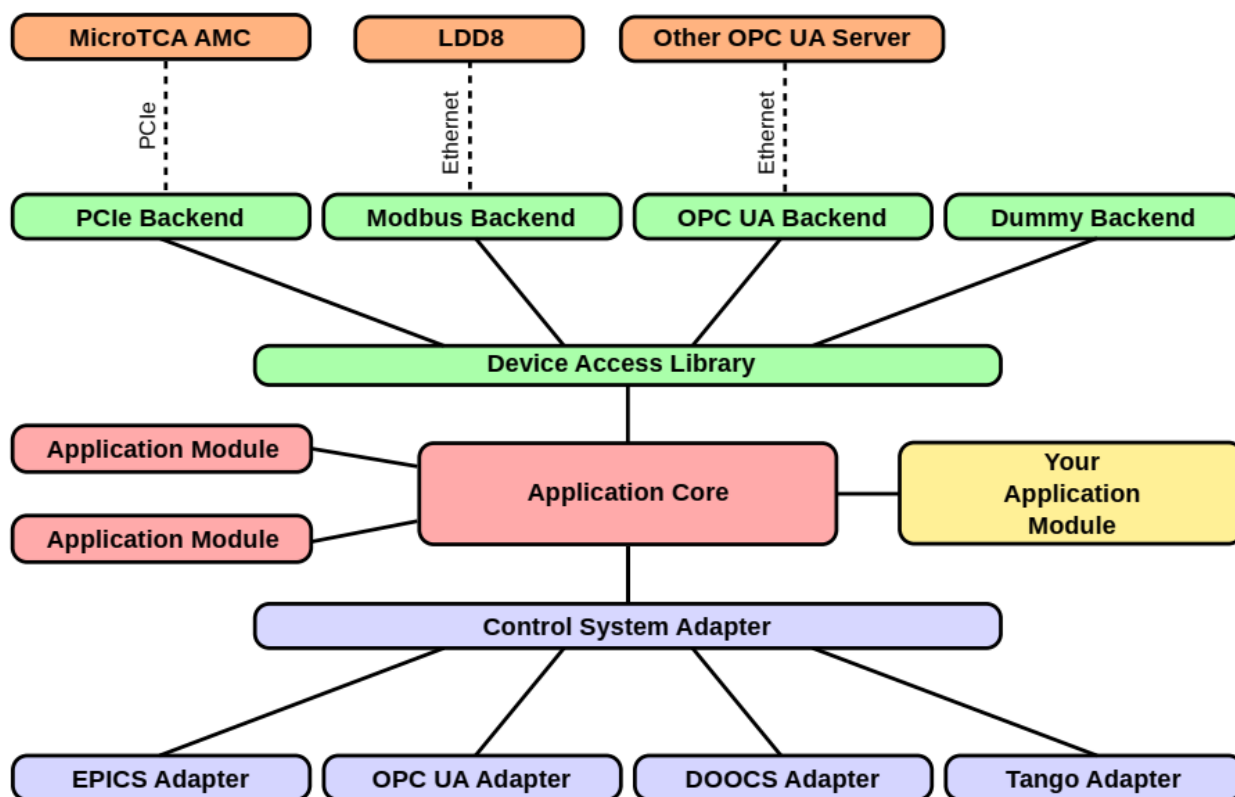
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Thank you!

ChimeraTK – A software tool kit to facilitate control application development



DeviceAccess

- Common API for different backends
- Seamless integration with FWK
- Improved device abstraction
 - Named registers → process variables
- C++ (native)
 - Python bindings
 - Matlab bindings
 - Command line interface
 - Graphical user interface

ApplicationCore

- Model data flow with process variables
- Small self-contained modules
- Modern multi-threading

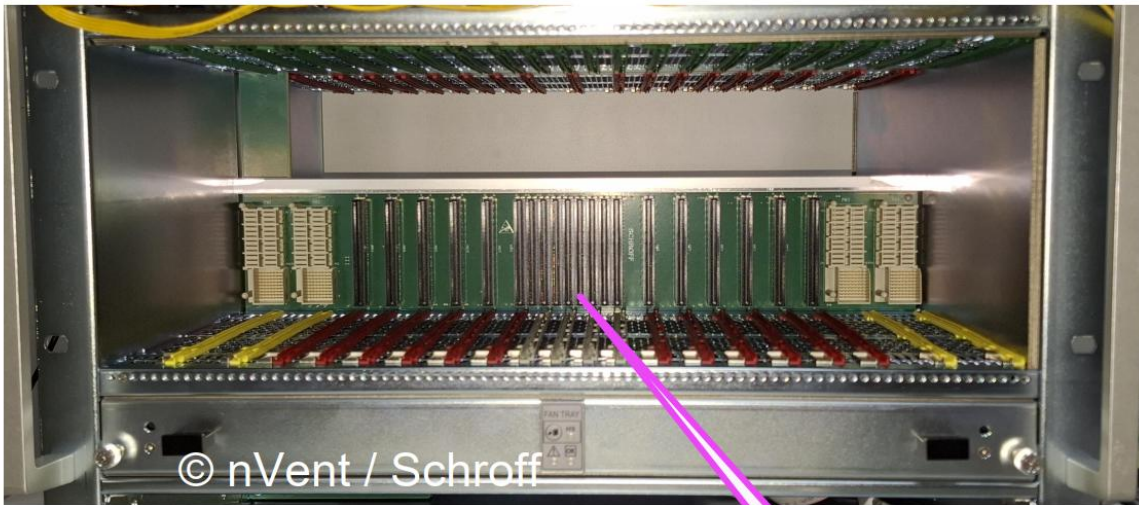
ControlSystemAdapter

- Native integration into control systems
- Publish process variables

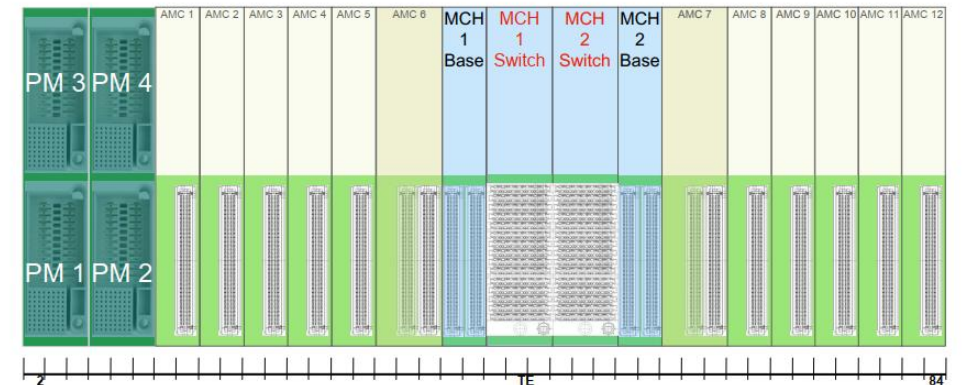
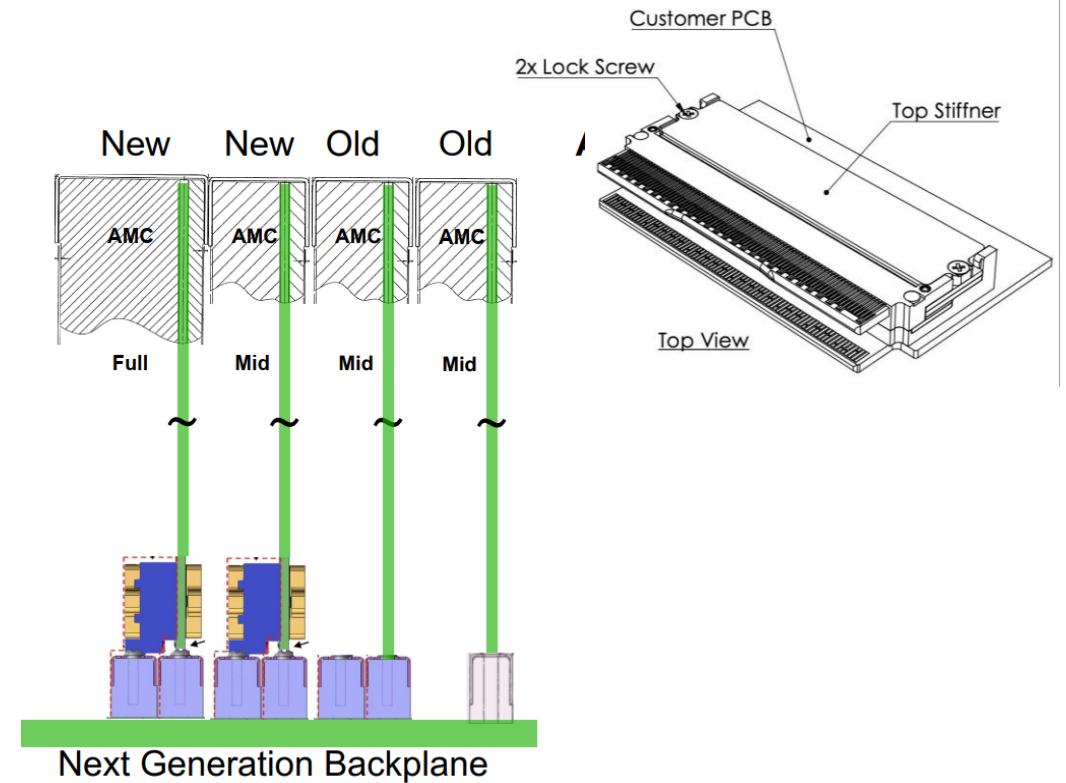
Next Generation MTCA

Community Support

- PCIe Gen. 5 and 100 GbE → 32 Gbps → lower latency
- Power: up to 220 W per AMC, more power on RTM
- Crate power ≥ 2 kW
- Split MCH



Redundant MCH in center of crate
to achieve 32 Gbps in all slots



Courtesy of Kay Rehlich