



STRUCK MTCA. 4 Board-Level and System Integration Solutions

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[muTCA/ATCA product page \(struck.de\)](http://www.struck.de/muTCA/ATCA)

Outline

- First MTCA.4 Digitizer AMC → SIS8300 (2011)
- First MTCA.4 RTM → SIS8900 (2011)
- 125 MSPS Digitizer Evolution
 - SIS8300-V2,
 - SIS8300-L2 (2014)
 - SIS8300-KU (2016)
- SIS8325 250 MSPS Digitizer (2015)
- Sidetrack on Export Control
- Digital I/OAMCs (2015, 2018)
- More Rear Transition Modules
- SIS8160/SFMC01 FMC Carrier/Digitizer FMC (2017)
- SIS8172 FMC Carrier (2022)

SIS8300-KU

10 channel 125 MSPS 16-bit digitizer (250 MSPS 14-bit stuffing option)

SIS8300

SIS8300-L

SIS8300-L2

SIS8300-KU

SIS8325

- History
- Virtex 5 based
 - 2010 SIS8300 initial development, first MTCA.4 board worldwide
 - 2011 SIS8300 V2 > 370 units in field (in part 8 channel 250 MSPS 14-bit BPM)
- Virtex 6 based
 - 2014 SIS8300-L > 150 units in field
 - 2015 SIS8300-L2x > 930 units in field (L2S, L2D,...)

SIS8300-V1/2 Digitizer Properties

- MTCA.4
- 4 lane PCI Express → 640 MB/s readout
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel
- AC and DC input stage
- Two 250 MS/s 16-bit DACs for fast feedback implementation
- High precision, flexible clock distribution logic
- Internal, front panel, RTM and BP clock sources
- Programmable delay of twin ADC groups
- Gigabit Link Port implementation to backplane
- Double SFP cage for high speed system interconnects
- Virtex-5 FPGA
- Up to 32 MSample DDR2 Memory per channel
- Additional point to point links over backplane
- In field firmware upgrade

Motivation: Joined DESY-Struck ZIM Project targeted at XFEL



SIS8900 Single Ended Input RTM

- 10 LEMO 00 connectors (FBM option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- analog signals can be routed to AC and DC input stage
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- two metric on board pin headers for 6 LVDS input/output signals each

Original Motivation: Test Board for SIS8300



SIS8300-L2 Digitizer Properties

SIS8300 w. new FPGA family
and new IPMI

- XC6VLX130T-2FFG1156C FPGA
- DDR3 Memory
- DESY MMC1.0

Central Motivation:
Higher Point to Point Link throughput

→ XFEL Working Horse



SIS8300-KU Properties

- 10 Channels **125 MS/s 16-bit** or **250 MS/s 14-bit** ADC
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- White Rabbit Clock Option for SFP+ Ports
- Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
- XCKU040-1FFVA1156C Kintex Ultrascale FPGA
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual FPGA Configuration Flash
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- Vivado Project for Custom Firmware Development
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible



Central Motivation: ISE → Vivado, FPGA Lifespan, ESS/Lund initiated

DWC8VM1

8 Channel Downconverter

One Channel Vectormodulator*

Model	$f_{\min}$ in MHz	$f_{\max}$ in MHz
DWC8VM1LF	350	500
DWC8VM1	500	3500
DWC8VM1HF	3500	6000

DWC8VM1 Overview Table

*under license from DESY



DS8VM1

8 Channel Direct Sampling

One channel vectormodulator*

SIS8300-KU/DS8VM1

as single cavity LLRF solution
covering 5 MHz to 500 MHz

Application Examples

UNILAC

NICA

ELBE

CERN PS

*under license from DESY



SIS8325 Properties

(Helmholtz Validation Fund Project)

Basically higher sampling speed version of SIS8300-L2

- 10 Channels **250 MS/s** **16-bit** ADC

Central Motivation:

- Sampling of shorter pulses,
- Faster availability of feedback data
- Slightly changed clock distribution scheme (HMC987LP5E replacing 2x AD9510 for improved jitter < 50 fs)

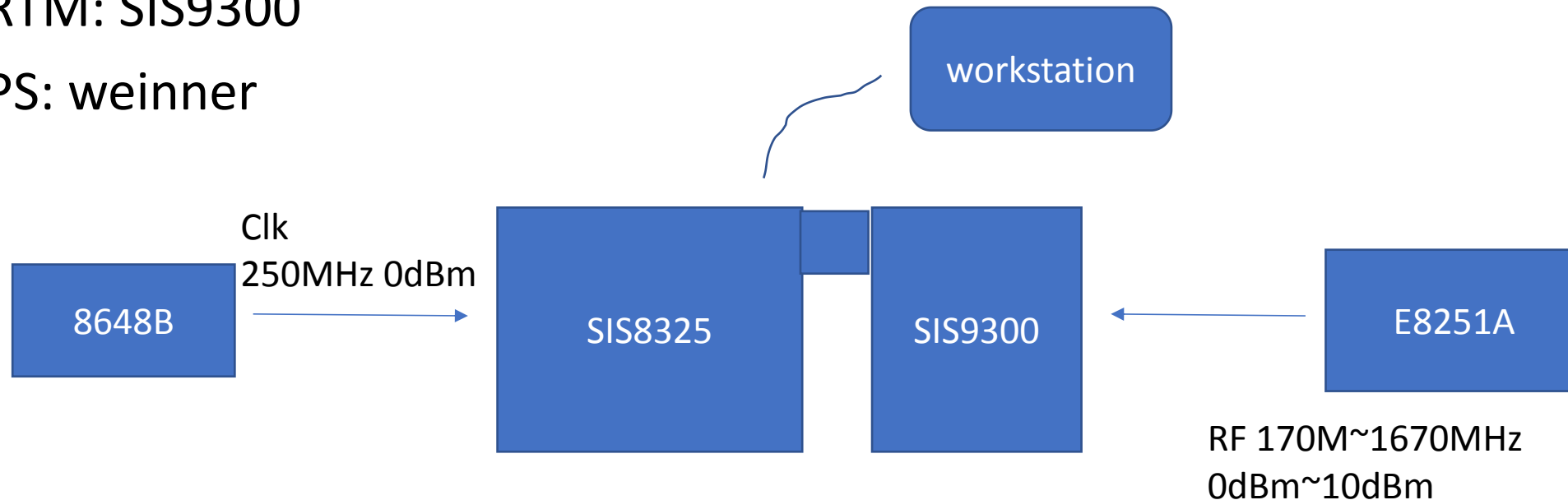
Tradeoff I: Historically still Virtex-6 based

But: SIS8300-KU in 250 MSPS 14-bit has almost the same number of effective bits

Tradeoff II: 16-bit > 180 MS/s → export control

Test setup

- Clock: 8648B 250MHz 0dBm
- RF: E8251A
170MHz,420MHz,670MHz,920MHz,1170MHz,1420MHz,1670MHz
- CPU,MCH: NAT
- RTM: SIS9300
- PS: weinner



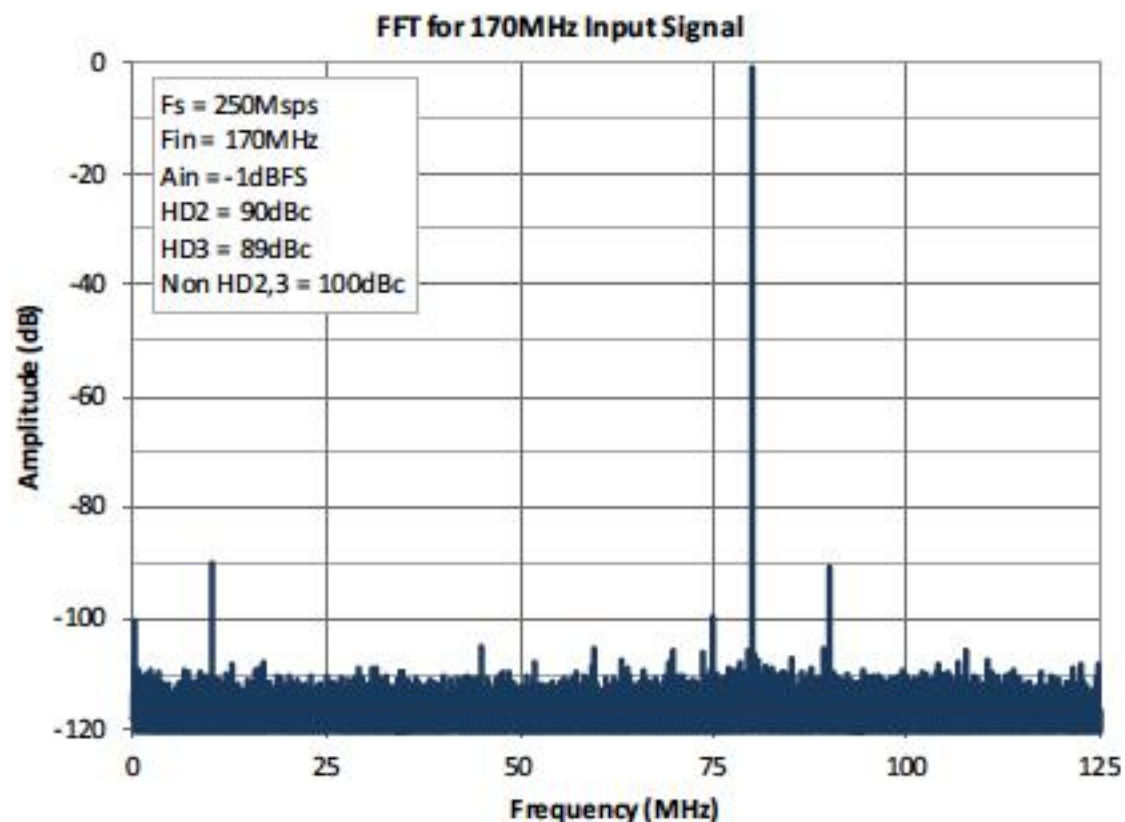
results

Input=open: noise floor~-100dB 19digit rms

Input=170MHz sine +10dBm @ clock=250Msps: noise floor~-85dBc

2017.01.30 ohshima

- TI ADS42LB69: SNR
73.2dBFS@170MHz 2Vpp



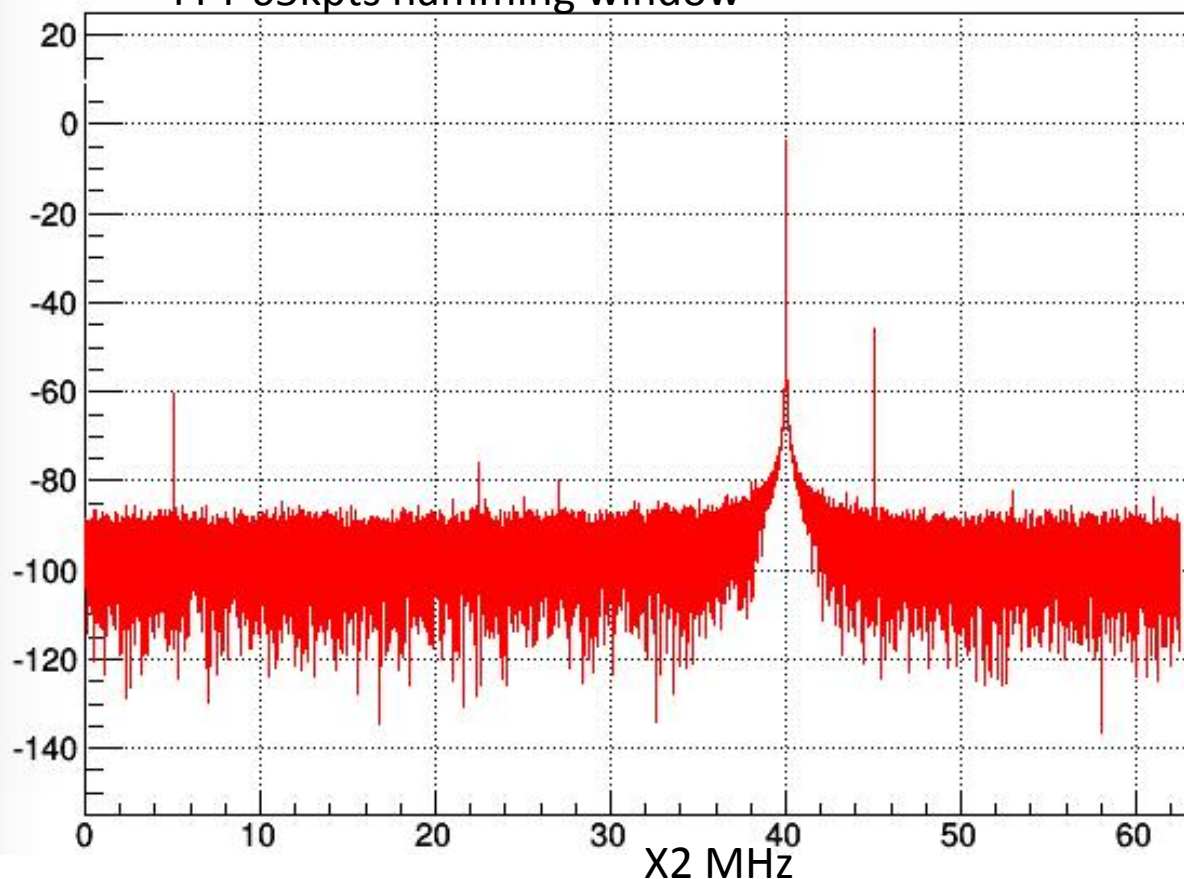
SIS8325

Fs=250Msps Fin=170MHz

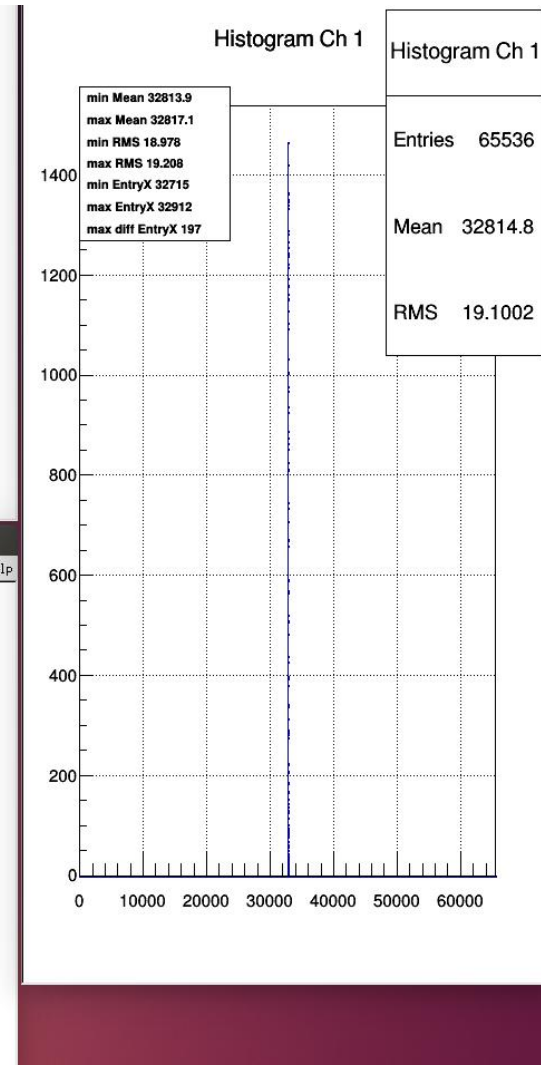
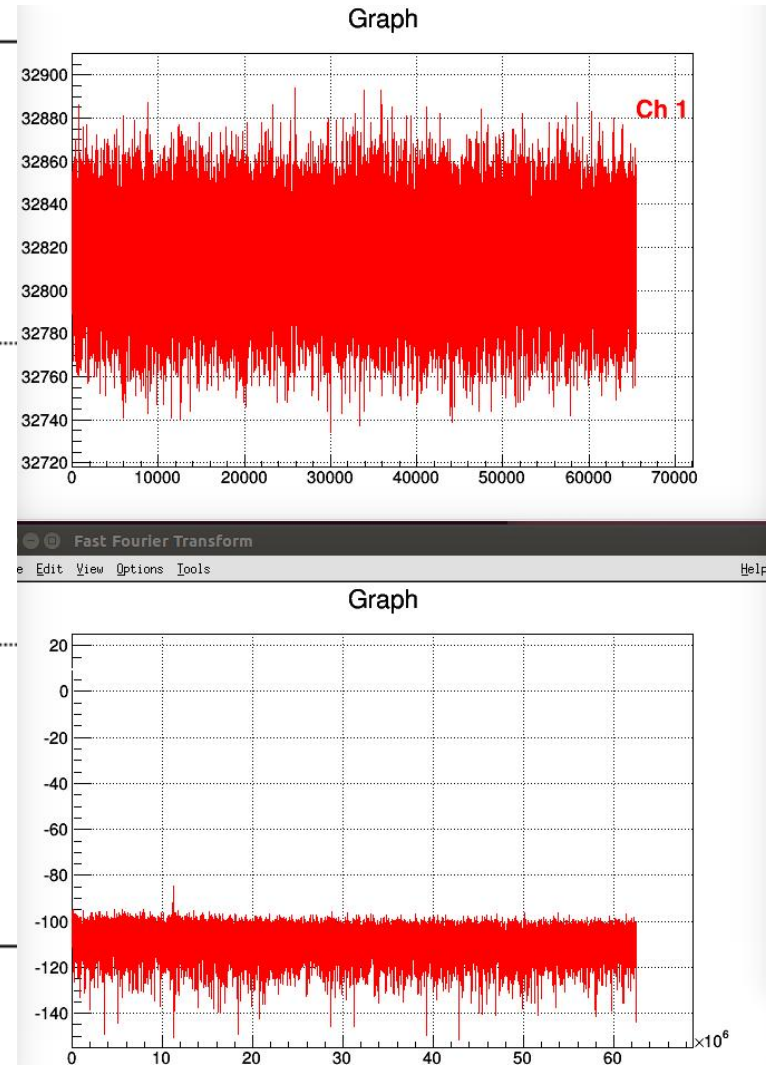
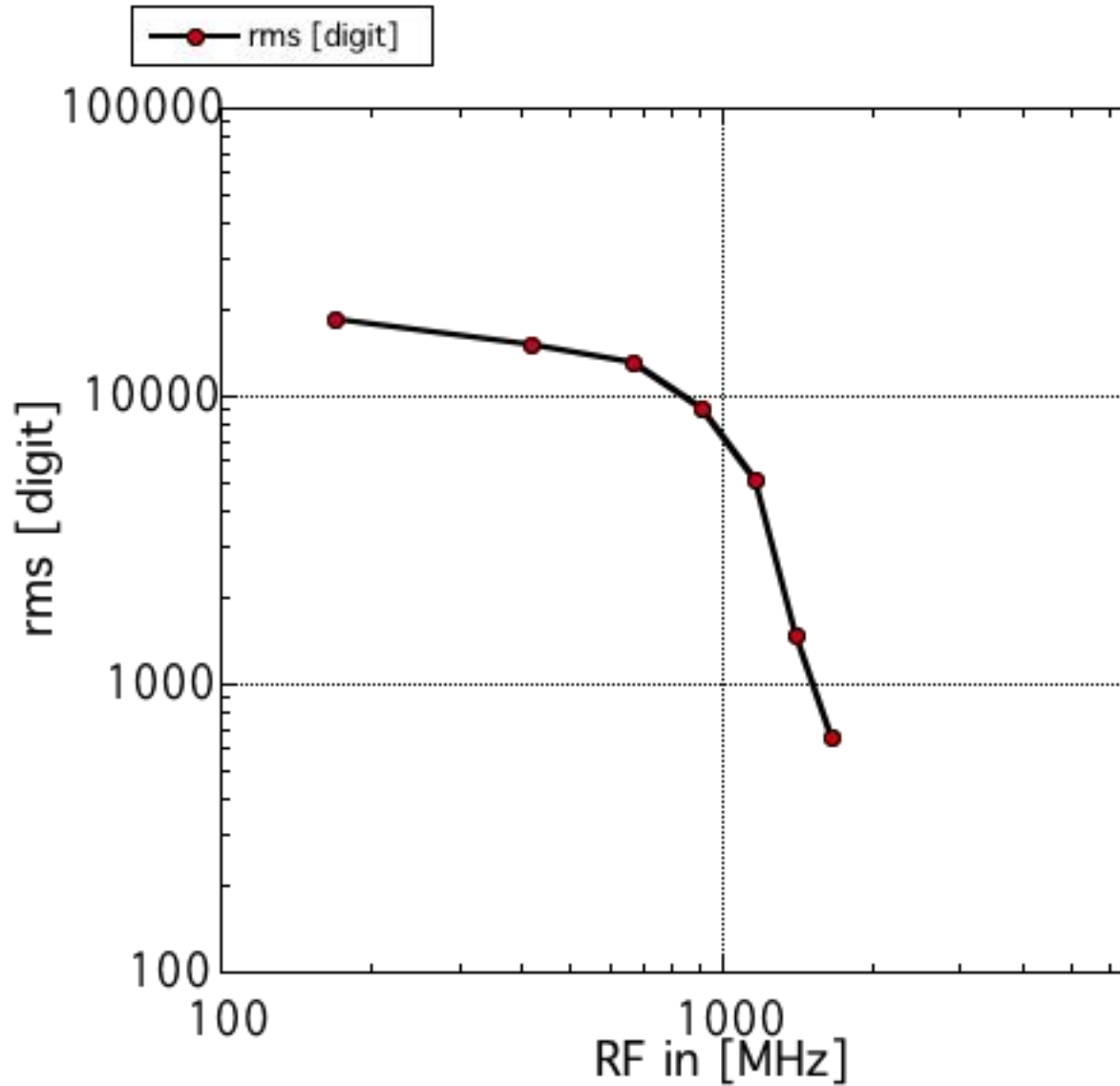
FFT 65kpts hamming window

Carrier ~ -5dB

Noise floor ~-85dB



- Frequency response (include response of SIS9300)
- FFT & time signals with input open



Export Control (Digitizers)

Dual use: Commission delegated regulation (EU) 2020/1749

3A002h h. "Electronic assemblies", modules, or equipment, specified to perform all of the following:

1. Analogue-to-digital conversions meeting any of the following:

	From #Bits	To # Bits	MSPS	Struck Boards
a	≥ 8	<10	> 1300	-
b	≥ 10	< 12	> 1000	SIS3305 (2 x 5 GSPS interleaved, VME)
c	≥ 12	< 14	> 1000	SIS1332 (PCIe)
d	≥ 14	< 16	> 400	SFMC01
e	≥ 16		> 180	SIS8325

General Equal Treatment Act (AGG) No. EU001

Australia, Island, Japan, Canada, New Zealand, Norway, Switzerland including Liechtenstein, UK and the USA

Export Control (FPLDs, FPGAs)

so far of no concern for Struck
to be checked with new products anyway

3A001.a

7. Field programmable logic devices having any of the following:

- a. A maximum number of single-ended digital input/outputs of greater than 700; or
- b. An 'aggregate one-way peak serial transceiver data rate' of 500 Gb/s or greater;

Note: 3A001.a.7. includes: — Complex Programmable Logic Devices (CPLDs) — Field Programmable Gate Arrays (FPGAs) — Field Programmable Logic Arrays (FPLAs) — Field Programmable Interconnects (FPICs) NB: For integrated circuits having field programmable logic devices that are combined with an analogue-to digital converter, see 3A001.a.14.

Note: Encryption and other features may come on top

Keep an eye on: Sanctions Lists, Embargo Countries, Military Goods List, Nuclear Suppliers Group, ...

SIS8800 Multi Purpose Scaler

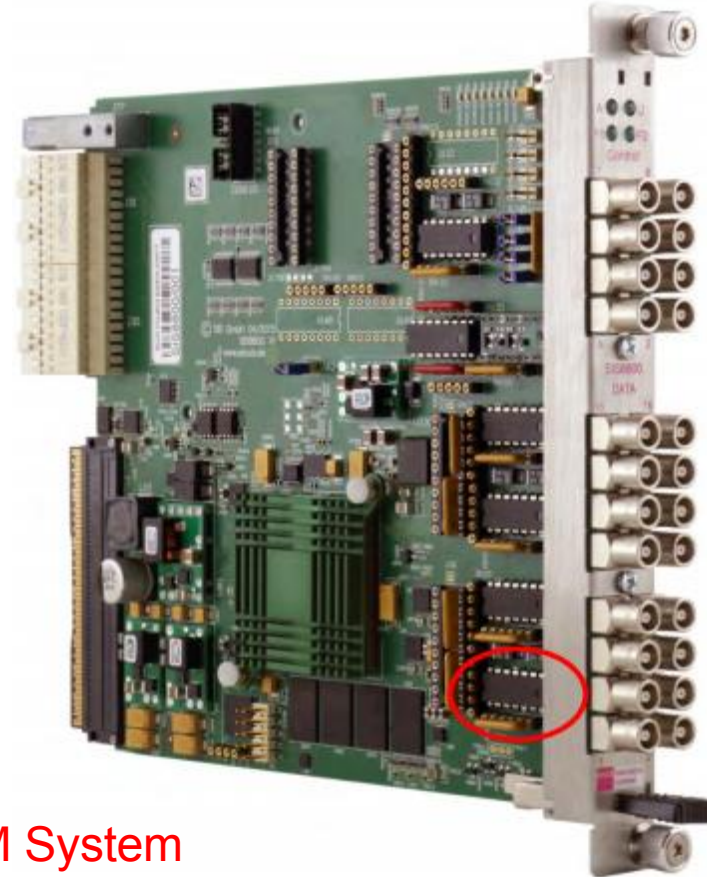
Functionality

- MTCA.4 AMC
- 4 Lane PCI Express connectivity
- XC6VLX130T-2FFG1156C Xilinx
- Dual FPGA Configuration Flash
- Redundant PCIe implementation
- 2 GByte DDR3 memory
- 16 front inputs NIM or TTL/LEMO, TTL,ECL or LVDS/flat cable
- 200 MHz count rate (NIM/ECL)
- 4 control in-/4 control front outputs
- Zone 3 Class D1.1 compatible
- MMC 1.0 under DESY license LV91

Original motivation for development: FAIR LASSIE BLM System

→ good fit for SRI (Synchrotron Radiation Instrumentation) also

Note: NIM/ECL suffers from discontinuation of MC10H124 and MC10H125



SIS8864 64 channel LVTTTL Digital I/O AMC

- Machine cycle dependent & generic output pattern with digital input
- Alternative to OHWR FMC carrier and two I/O FMC's
- Ready to run firmware
- Application specific firmware adaptations



SIS8160 Dual FMC Carrier AMC



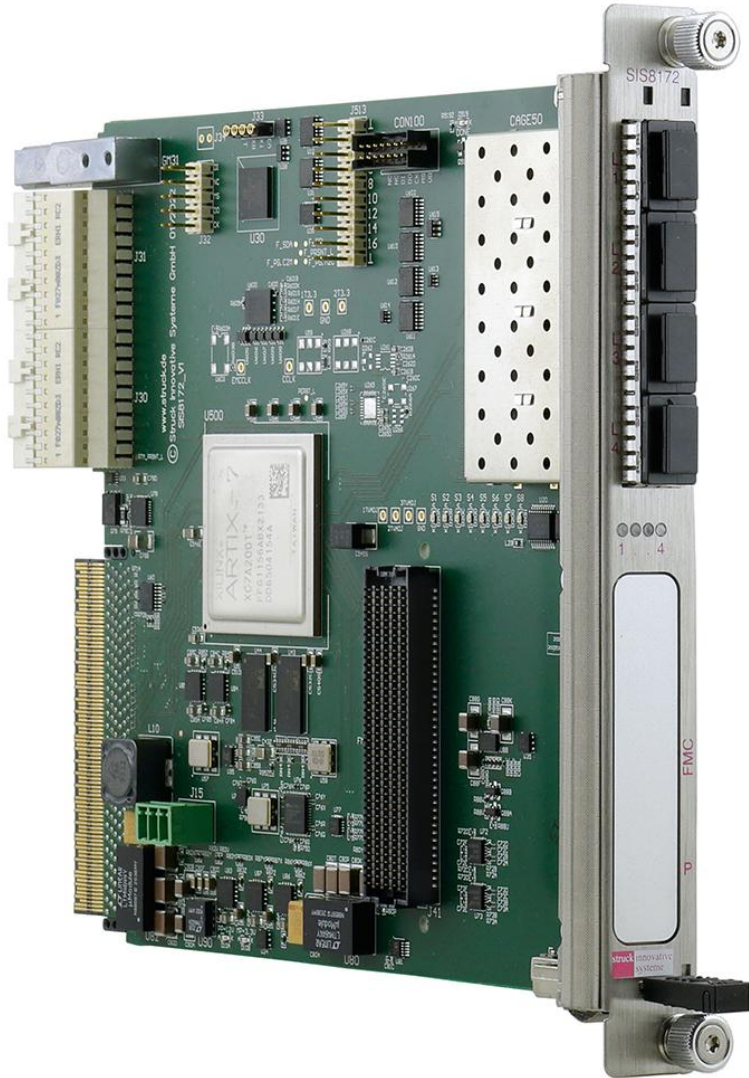
- 4-lane PCI Express Gen3 Connectivity
- Xilinx XCKU40- or XCKU060-1FFVA1156C Kintex Ultrascale FPGA
- Dual Boot
- Front Panel MMCX Clock Input
- Front Panel MMCX Digital In-/Output (HW Configuration)
- Point to Point Links
- 4 MLVDS μ TCA Ports (AMC Ports 17-20) $\rightarrow$ 8 MLVDS lines
- 2 HPC FMC Sites
- Variable FMC VADJ (1,0V - 1,8V)
- Low Jitter Clock Generation and Management
- 2 x 2 GByte DDR4 Memory with two Memory Controllers
- White Rabbit Option (over FMC 2)
- StandAlone Operation Option
- **MMC1.0 under DESY LV91**

SIS8160 Industrial Byproduct Avionics Simulation-/Testbench



Note:
Monolithic front panel rather
than FMC bezel solution (EMI)

SIS8172 Artix-7 Based FMC Carrier Block Diagram



- MTCA.4 AMC with Double Width Mid-Size Form Factor
- Mid cost FPGA (XC7A200T-2FFG1156C)
- 256 M x 32 Bit DDR3 Memory (Artix-7 Limitation)
- 4 Lane PCIe Gen2 (Artix-7 Limitation)
- Dual FPGA Configuration Flash
- Quad SFP+ Cage
- HPC FMC Site
- Zone 3 Class D1.0 Implementation
- 4 Point to Point Link Backplane Interface
- 4 AMC Ports MLVDS (8 MLVDS lines)
- White Rabbit Timing Option
- Module Management Controller ATxmega128A1U, IPMB-L Interface
- **DESY MMC1.0 (under LV 91)**

SIS8890 Discriminator RTM for SIS8800 Multi Purpose Scaler

Functionality

- MTCA.4 RTM
- 16 Discriminator Inputs, Connector Type MMCX
- Leading Edge
- 50 Ω Input Termination
- 14 Bit Threshold DAC for each Channel, 0.4 mV/Step
- 16 Outputs to Zone 3 (to Scalers on SIS8800)
- 16 Front Outputs, Connector Type MMCX
- Programmable Pulse Width 10 ns -250
- Zone 3 Class D1.1 Compatible
- MMC1.0 Compatible



Possible SIS8172 Target Applications

RTM/Zone 3 Applications

- Beam Loss Monitor (BLM)
- Machine Protection System (MPS)
- PETRA 4 HF Movement Monitor
- PZT4 Piezo Controller (Low Level Radiofrequency)

...

FMC Applications

- DOSIMON (Dosimetry, XFEL MPS)
- MOTDRV22 (Low Level Radiofrequency)
- Analog Input (Synchrotron Beamline Spectroscopy)
- Digital I/O (Synchrotron Beamline Multiscaler)

...

In General: AMC for Cost Sensitive Applications

Supply Chain Issues

ARTIKEL 05784 - XCKU040-1FFVA1156C KINTEX ULTRASCALE						
Dispositionsbestand		Dispositionsbestand (Woche)		Produktion	Verkauf	
Datum	Einkauf	Verkauf	Produktion	Bestand	Basisme	
					41	Stk
06.05.2027	24	0	0	65	65	Stk
20.05.2027	24	0	0	89	89	Stk
17.06.2027	72	0	0	161	161	Stk

 **XCKU040-1FFVA1156C** € 1.853,640
:1; No.of User I/Os:520I/O S; Process Technology:-; Ic Mounting:Surface Mount Rohs Compliant: Yes |Amd Xilinx XCKU040-1FFVA1156C
AMD

[Datenblatt](#) [CAD-Modelle](#) [Herstellerseite](#) [Zur BOM hinzufügen](#)

Vertriebspartner	SKU	Stock ±	Min.	Verpackung	Staffelpreise	1 ±
★ Farnell	XCKU040-1FFVA1156C	0	1		EUR	1.810
★ DigiKey	122-2090-ND	9	1	Tray	EUR	1.911
★ Avnet	XCKU040-1FFVA1156C	0	1		EUR*	*1.691
★ Newark	XCKU040-1FFVA1156C	0	1		EUR*	*1.785
★ Mouser	217-KU040-1FFVA1156C	3	1		EUR	1.920
★ Microchip USA	XCKU040-1FFVA1156C	155	1	Tray	EUR*	*1.292

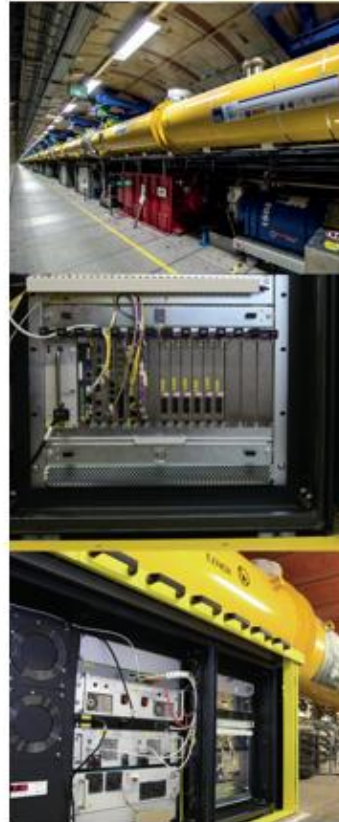
- Xilinx ↑ ↑ ↑
- Analog Devices
- Texas Instruments
- Schroff
- Skyworks/SiLabs
- Harting
- EMS house
- ...

→ Grey Market risk paired with 10-fold price not unusual

MTCA Electronics for Beam Instrumentation & Controls



10 channel
125 MSPS 16-bit
250 MSPS 14-bit
DigitizerAMC
Kintex Ultrascale



2/4 channel
2.5 GSPS 14-bit
DigitizerAMC
Kintex Ultrascale



RTMs
DC - 6 GHz
Direct Sampling
Downconverter
Vectormodulator *

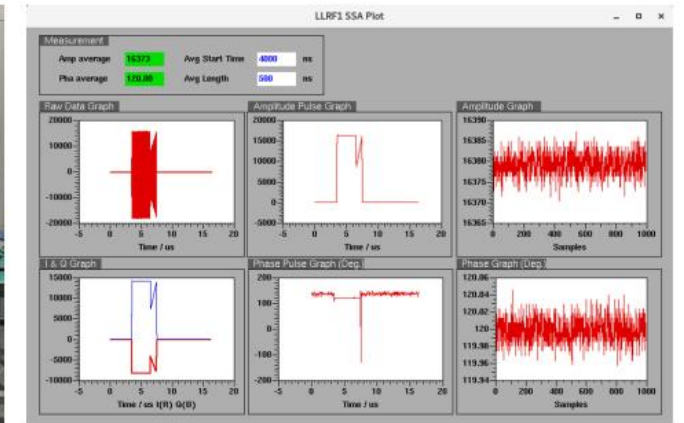


Digital I/OAMCs
16/64 Channels
DiscriminatorRTM
16 Channels

*in part under license from DESY

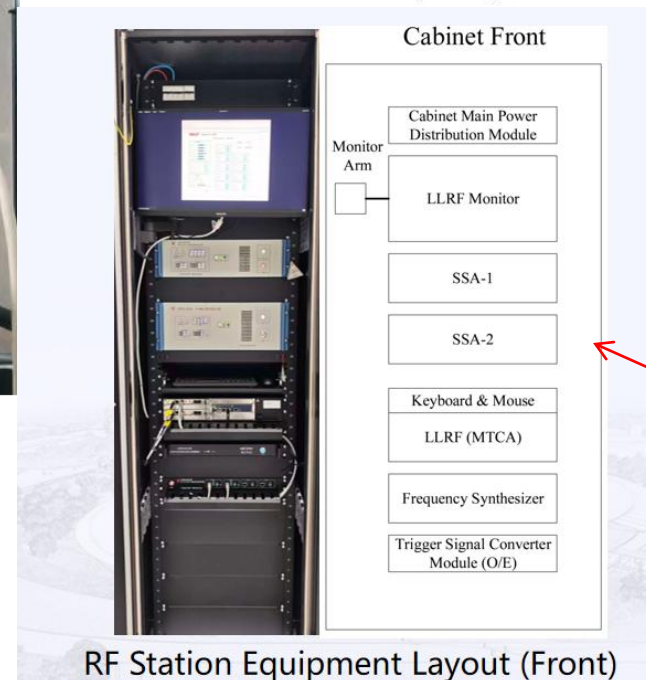
System Integration Examples

Courtesy Junqiang Zhang (UTEF)



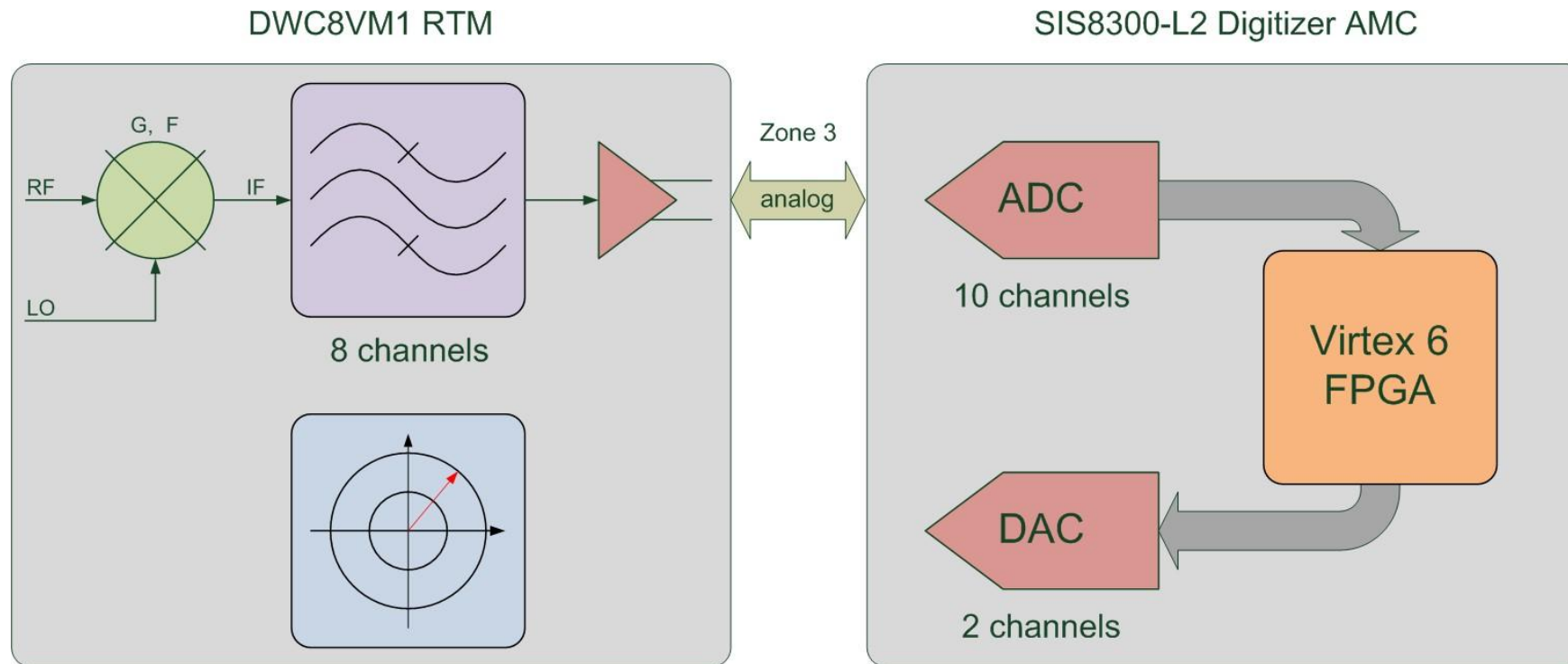
Desktop testing

A/P stabilities(rms): 0.01%, 0.01°



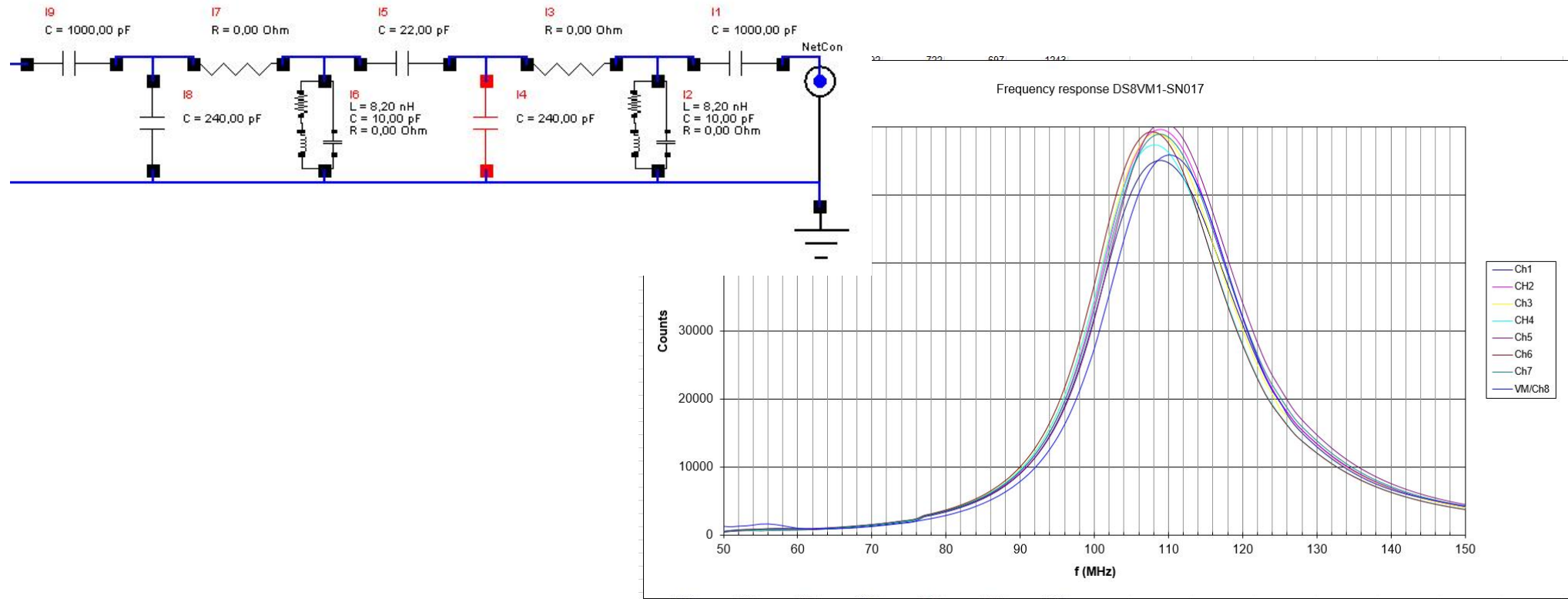
Courtesy Yuchen WANG (NSRL)

SIS8300-x/DWC8VM1 as single cavity LLRF solution covering 350 MHz to 6 GHz



Current combination: SIS8300-KU Kintex Ultrascale Digitizer and DWC8VM1

DS8VM1 GSI 108 MHz Input Filter and Input Response



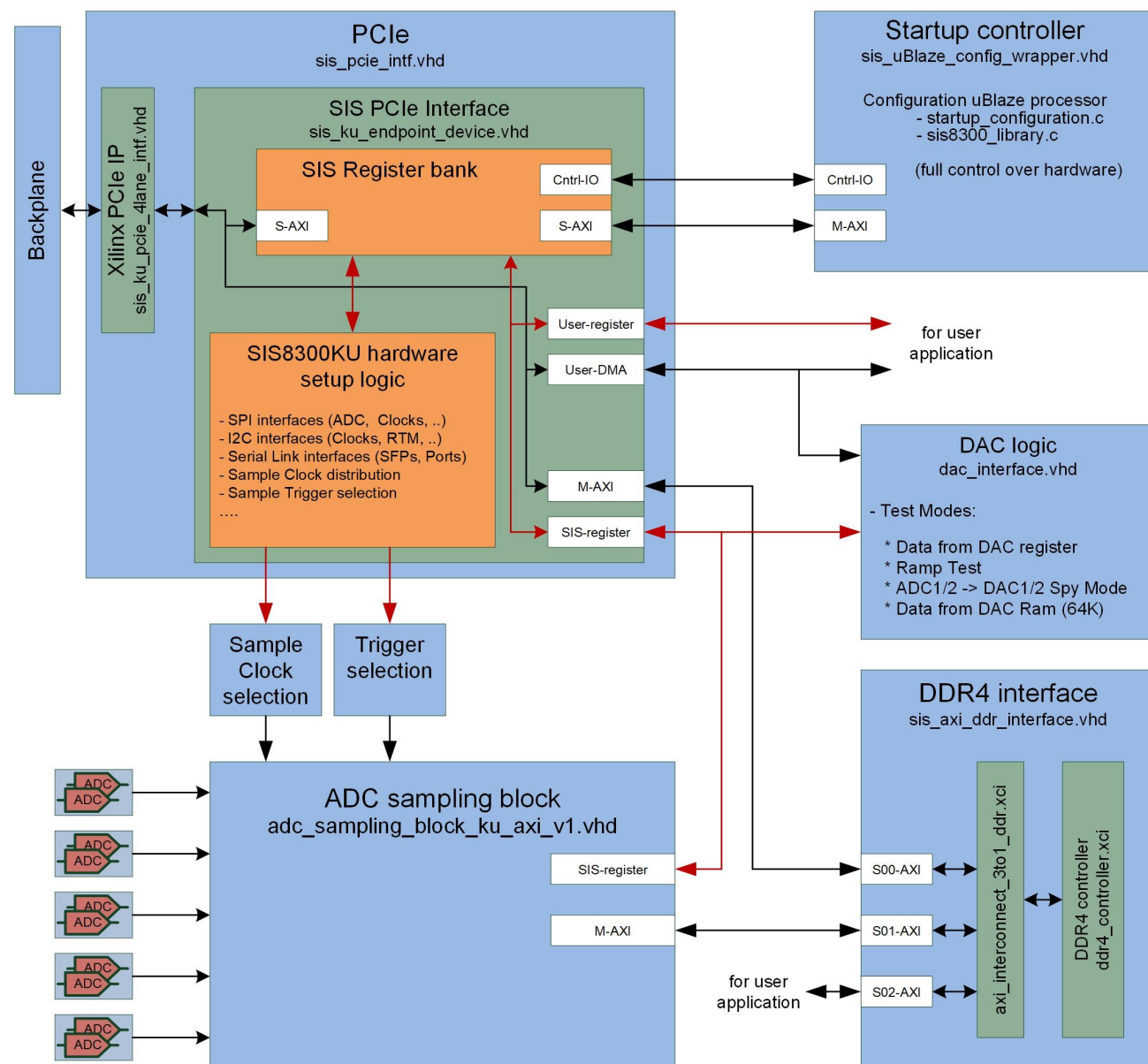
Jens Zappai et. al. LLRF2017

SIS8300-KU

AXI Based VIVADO Project

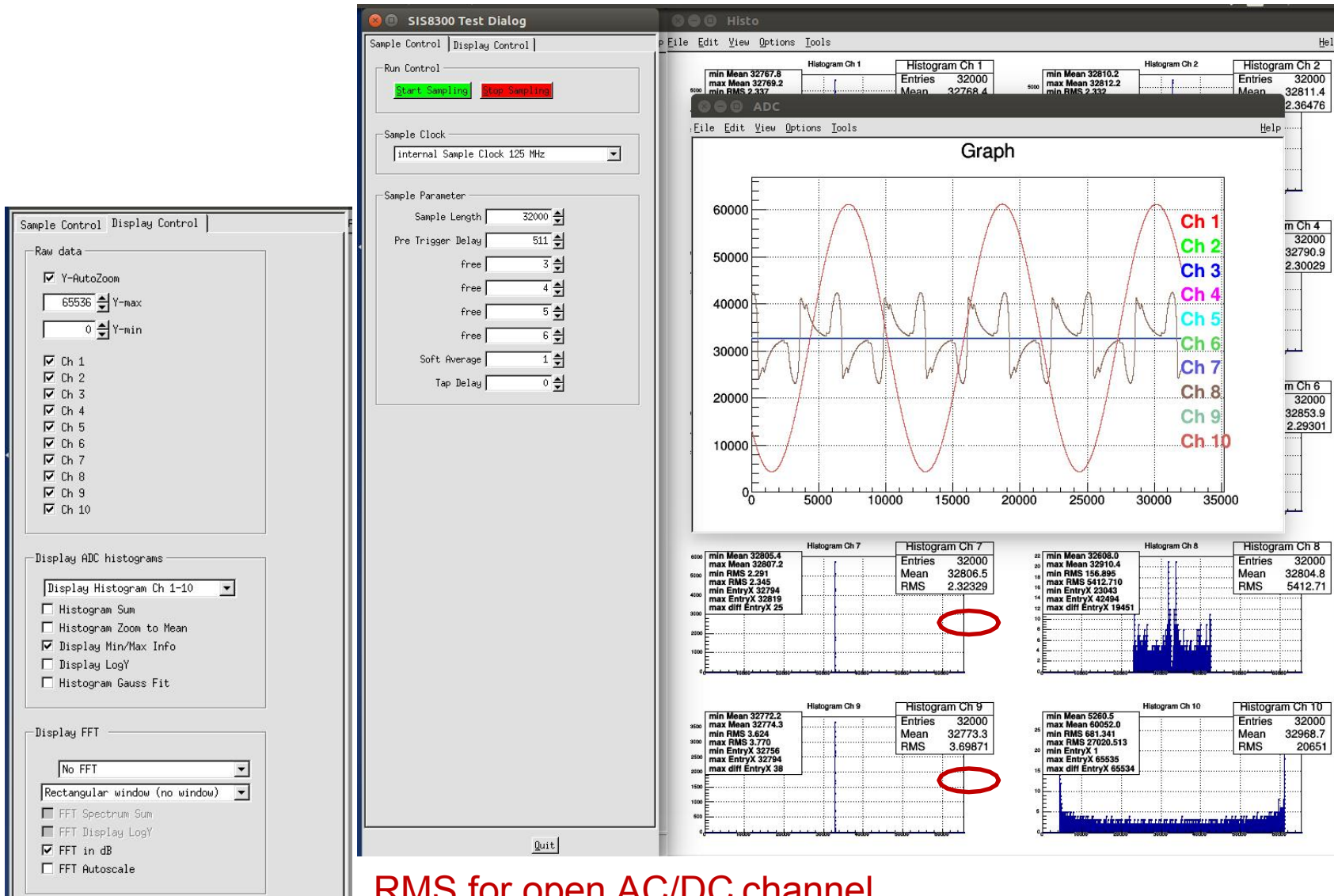
- Cooperation Lund University/ESS/Struck
- To Meet ESS/ERIC Firmware Specs
- ESS Version → COSYLAB EPICS
- Struck Version available to all users

Struck SIS8300-KU AXI-Based Xilinx FPGA Framework



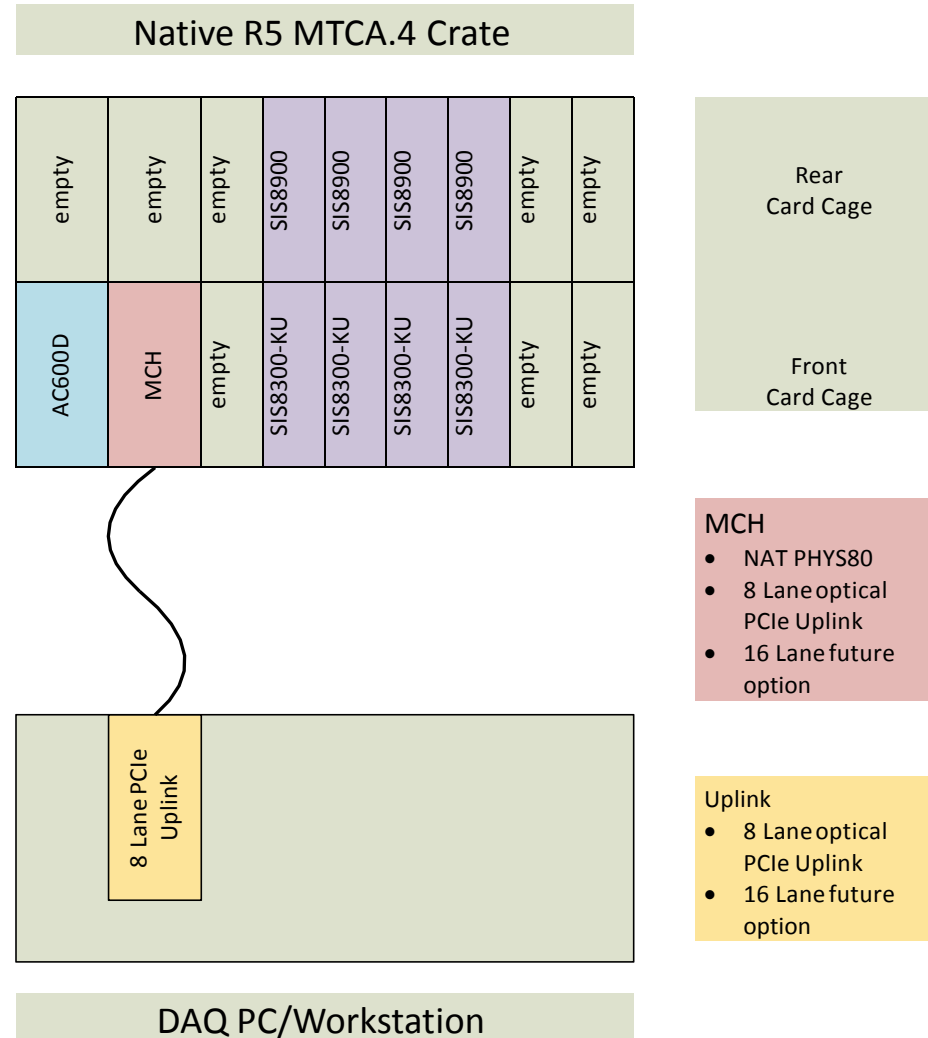
SIS8300-x ROOT GUI

SIS8300-KU 8AC2DC with SIS8900 RTM



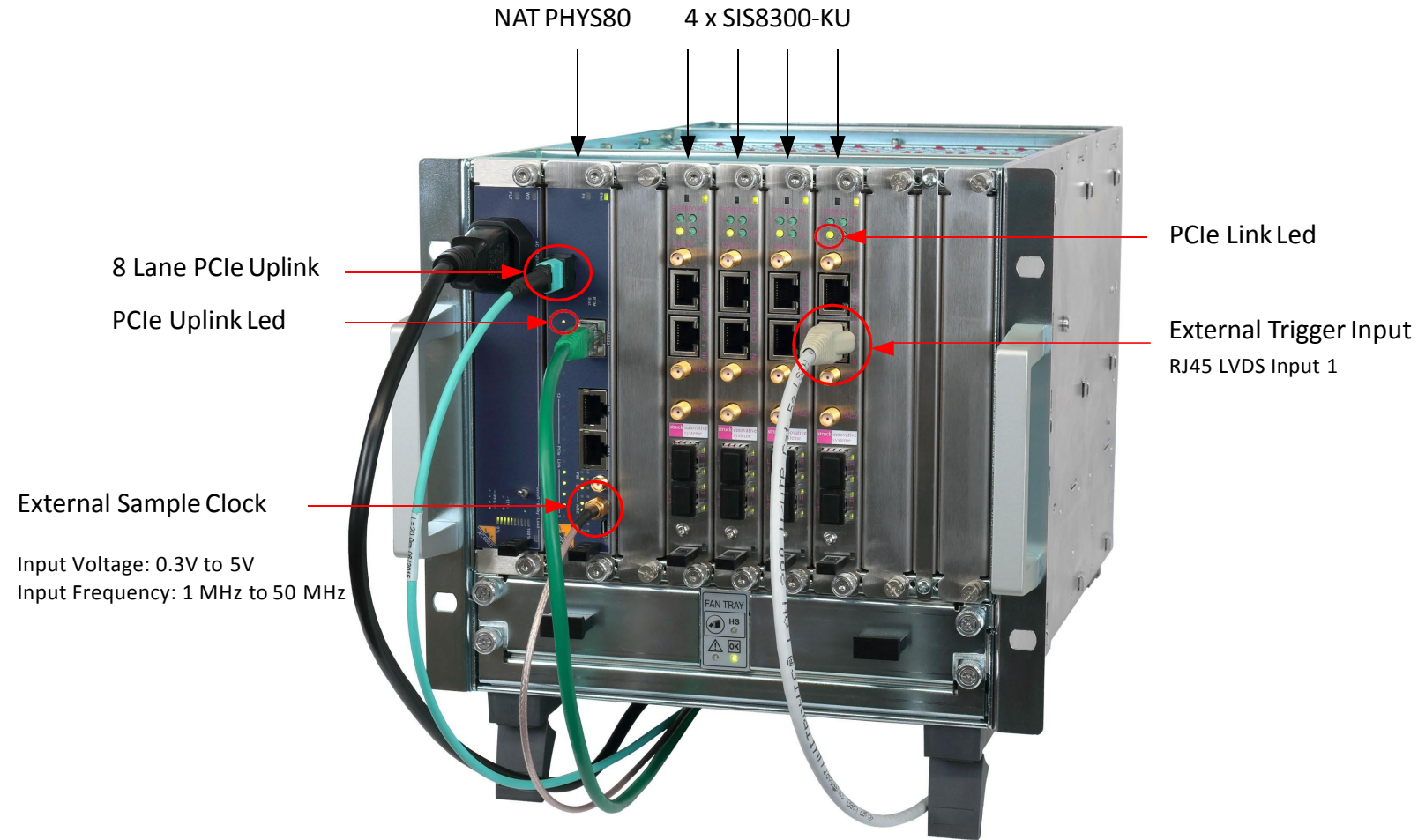
SIS8300-KU Wendelstein X7 Application

40 Channel Streaming System



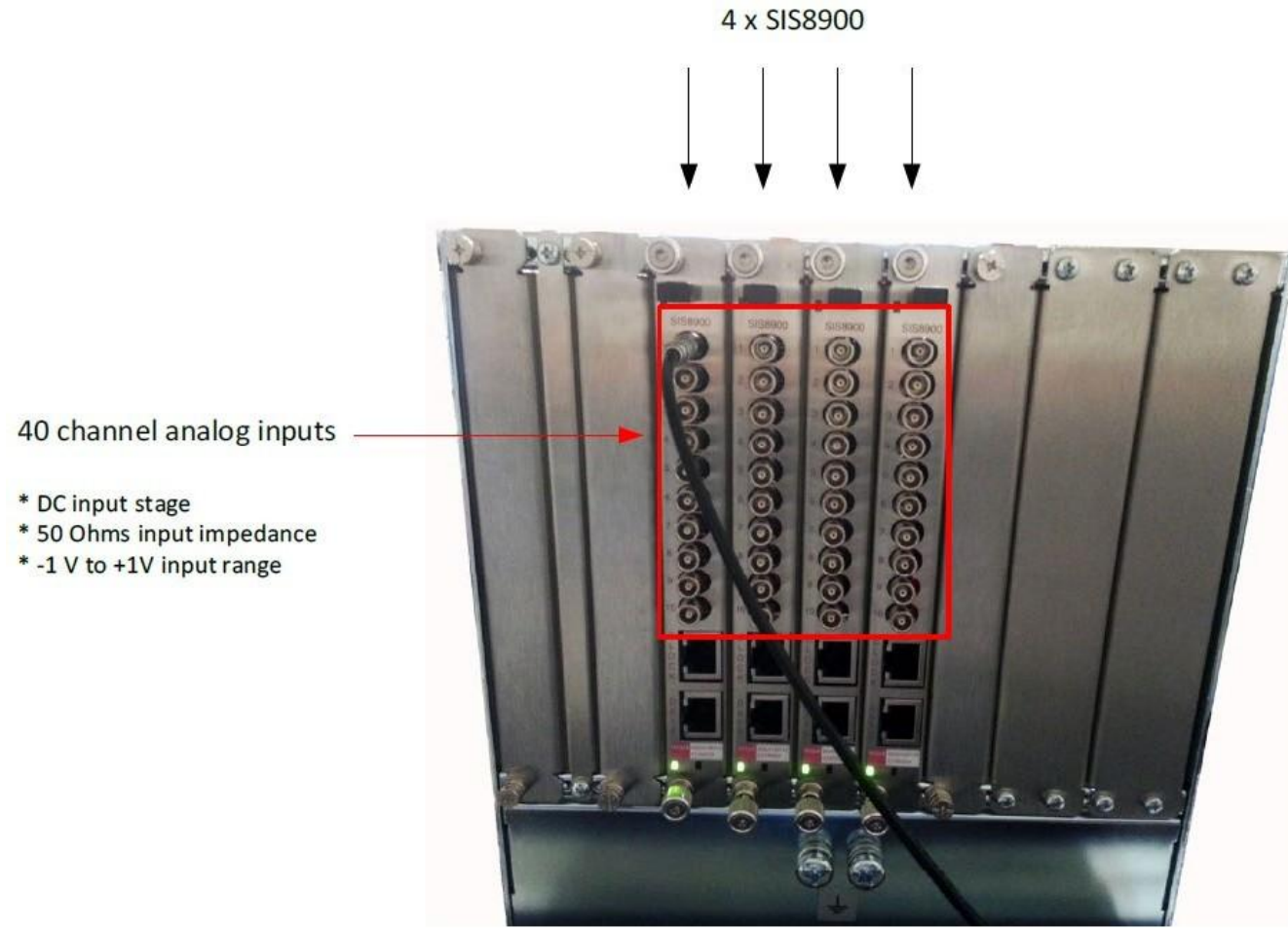
SIS8300-KU Application Example

40 Channel Streaming System (Front)



SIS8300-KU System Example

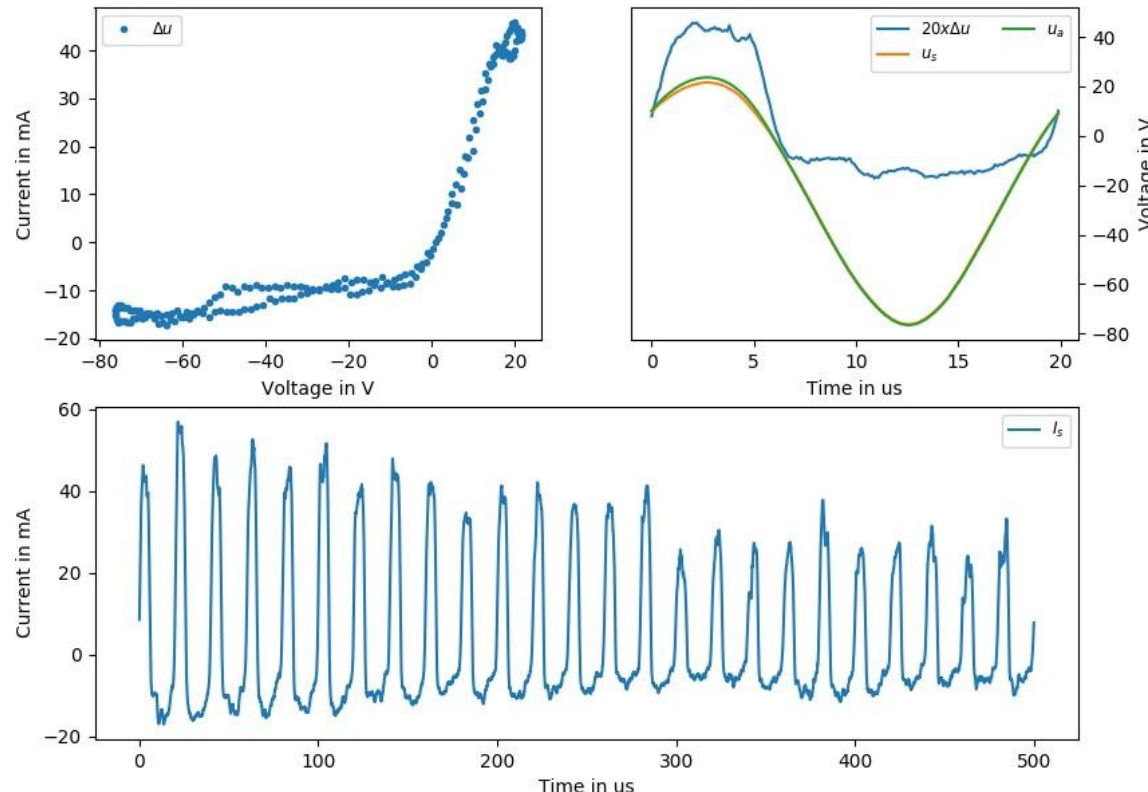
40 Channel Streaming System (Rear)



Fast Langmuir Probes on Wendelstein 7-X



- **Wendelstein 7-X is a nuclear fusion experiment in Greifswald, Germany at the Max-Planck-Institute for Plasma Physics**
- **Langmuir probes measure plasma density and temperature**
- **Fast probes can resolve turbulence**
- **40 ADC channels with 16b at 10 MS/s**
- **Synchronised with ~50 other systems**
- **In operation for ~500 experiments of up to 100s**



Courtesy Lukas Rudischauser, IPP

SIS8300-x BPM Application

PAL FEL

144 Stripline BPMs SIS8300 V2
in 8 channel 250 MSPS configuration

SLAC RTM

56 Cavity BPMs SIS8300-L2/SLAC RTM

DESY FLASH

SIS8300-L2/DESY Interleaving RTM

ESS

SIS8300-KU/DWC10LF

MTCA.4 Relevance, current Struck user base

AU	Australian Synchrotron
BR	LNLS
CH	CERN
CN	IHEP, SINAP, USTC, CIAE, CSNS, IMP, DLS, IASF, PKU, THU, CQU, ...
CZ	ELI (Inst of Physics, Praha)
DE	DESY, HZDR, PTB, MPG, KIT, HZB, GSI, DESY Zeuthen, HMI
ES	ESS Bilbao, GMV
FR	ITER, Saclay
GB	Diamond, STFC
IN	TIFR
JP	KEK, SPring-8
KR	PAL
RU	ITER, JINR (Techlab/Bevatech)
SE	ESS, Lund University
TR	TARLA
TW	NSRRC
US	SLAC, NSCL/FRIB, ANL, ORNL



Conclusion/QA/&thanks



It's truly inspiring to see how fast the MTCA community is growing here in China. With the support of DESY and global partners, we're witnessing so many fantastic local designs coming to life.

As a global partner, we see our role as a two-way bridge. We can do more than just bring international technology to China—we also want to help the brilliant local innovations reach the global market. And the best way to achieve that is by staying closely aligned with international standards. Great localization shines brightest when it speaks a global language.

At the end of the day, we are **all building this ecosystem together**. Let's keep the communication open, support each other, and grow this community across borders. Thank you for a wonderful workshop, and let's win together!

partner

Beijing DAQ Technology Co. Ltd.

