



Research and Implementation of Dynamic Loading Technology for RFSoc

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01 Functions and Principles

02 Multiple-Bitstream Flash Loading

03 Ethernet Loading

04 PCIe Loading

05 Demonstration





/01

**Functions and
Principles**



Functions and Principles

The PS coordinates PL function updates while the board is running.

Three approaches address storage and transfer needs: Flash, Gigabit Ethernet and PCIe.

DDR buffers bitstreams. QSPI Flash provides persistent storage. Gigabit Ethernet and PCIe transfer data to the board.

01 Multiple-Bitstream Flash Loading

Upload and store bitstreams in Flash, then select a saved file to load.

**PC → Ethernet (TCP/IP) → DDR
→ QSPI Flash**

QSPI Flash → DDR → PCAP → PL

02 Ethernet Loading

Start PL configuration after receiving the complete bitstream file.

**PC → Ethernet (TCP/IP) → DDR
→ PCAP → PL**

03 PCIe Loading

XDMA writes the bitstream to DDR. Control registers hand the request to the PS to update a predefined reconfigurable partition.

**PC → XDMA → DDR → PCAP
→ Reconfigurable partition**

Standalone (bare-metal) and Linux implementations address different application requirements

Functions and Principles



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Conceptual Levels

Six Bitstream Levels and Their Processing Mechanisms

1	.bit File Header	File metadata parsed by software, outside the PL configuration protocol	File Structure
2	Device Programming Data	Complete configuration stream beginning at 0x7A in this example	
3	Configuration Word	Basic data unit: 32 bits, assembled from four bytes	Data Format and Protocol
4	Configuration Packet	Type 1 or Type 2 header followed by data words	
5	Configuration Frame	Smallest addressable configuration unit: 93 × 32-bit words on this device	Hardware Storage and Resources
6	Programmable Resources	Configuration bits control LUTs, routing, BRAM and I/O	

Functions and Principles

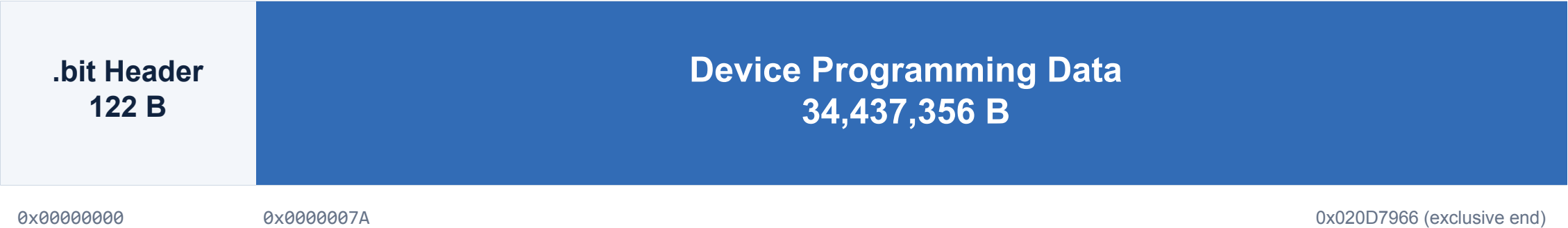


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.bit File Structure

The .bit File Contains a Header and Device Programming Data

Example .bit file for the target RFSoc device: 34,437,478 byte



Region	Contents	Handled By	Result
File Header	Design, device, date, time and programming-data length	PS software / configuration library	Locate programming data and determine its length
Programming Data	Preamble, sync word, packets, frame data and startup commands	Transfer path and PL configuration logic	Transfer words and execute the PL configuration protocol

Software processes the file header. The configuration stream begins at 0x7A in this file.

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File Header

The fields a-e in this .bit file header

The original header bytes in this .bit file

```
00000000 00 09 0F F0 0F F0 0F F0 0F F0 00 00 01 61 00 32
00000010 64 65 73 69 67 6E 5F 31 5F 77 72 61 70 70 65 72
00000020 3B 55 73 65 72 49 44 3D 30 58 46 46 46 46 46 46
00000030 46 46 3B 56 65 72 73 69 6F 6E 3D 32 30 32 31 2E
00000040 31 00 62 00 16 78 63 7A 75 34 37 64 72 2D 66 66
00000050 76 65 31 31 35 36 2D 32 2D 69 00 63 00 0B 32 30
00000060 32 36 2F 30 39 2F 30 32 00 64 00 09 31 35 3A 30
00000070 31 3A 30 35 00 65 02 0D 78 EC FF FF FF FF FF FF
```

Fields

a

0x0D–0x41

b

0x42–0x5A

c

0x5B–0x68

d

0x69–0x74

e

0x75–0x79

Field	Tag / Length	Content Offset and Value
a	0x0D / 0x0E–0x0F = 50	0x10–0x41: design, UserID, Vivado version
b	0x42 / 0x43–0x44 = 22	0x45–0x5A: xczu47dr-ffve1156-2-i
c	0x5B / 0x5C–0x5D = 11	0x5E–0x68: 2026/09/02
d	0x69 / 0x6A–0x6B = 9	0x6C–0x74: 15:01:05
e	0x75 / 0x76–0x79 = 4 B	0x020D78EC: programming-data length

a–d: 1 B tag + 2 B big-endian length + content. e: 1 B tag + 4 B big-endian length. Data starts at 0x7A.

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Header Processing

Locate and Validate the Programming-Data Boundary

1 Read Fixed Prefix Skip the prefix: 2-byte length 9, 9 fixed bytes, then 2-byte marker 0x0001

2 Parse Fields a–d Read the 1-byte tag, 2-byte big-endian length and content

3 Parse Field e Tag 0x65 at 0x75. The next 4 bytes give length 0x020D78EC

4 Locate Data Start After the e length field, the next byte is at offset 0x7A

5 Check Boundary $0x7A + 34,437,356 = 0x020D7966$ (exclusive file end)

Output for this file: programming-data offset 0x7A and length 34,437,356 B

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Programming Data

Device Programming Data and Its Internal Structure

Definition

File range 0x0000007A–0x020D7965
Length 34,437,356 B
Word format 4 bytes per configuration word

Device programming data is the complete configuration stream: preamble, synchronization, packets, frame data, integrity checks and startup control.

Internal Structure

Category	Project Example	Function
Preamble	Dummy words Width detection pattern	Padding and interface detection pattern
Synchronization	AA995566 (sync word)	Enable configuration-packet parsing
Packets	Type 1 / Type 2	Specify operation, target register and word count
Frame Writes	Frame address, WCFG and frame data	Address configuration frames and write their contents
Finalization	CRC, startup and end commands	Check integrity, start user logic and end synchronization

Dummy pads with 0xFFFFFFFF. NOP is a no-operation packet after sync. Neither carries user frames.

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32-bit Words

Configuration Words and 32-bit Byte Order

Basic Unit

Programming data starts at 0x7A. Each group of four bytes forms one configuration word. For word index n, starting at 0:

$$\text{offset}(n) = 0x7A + 4n$$

A word may represent synchronization, a packet header, register data or frame data. The PL parser state determines its meaning.

Example: Sync-Word Bytes and Logical Value



Processing Step	Result
Word Boundaries	Group four bytes at a time from programming-data offset 0x7A
Byte-Order Detection	Use the synchronization pattern to identify file byte order
Endian Adaptation	Software or DMA adjusts the byte order of each 32-bit word
Logical Value	PL configuration logic receives sync value 0xAA995566

Endian adaptation changes the byte layout in memory while preserving the protocol value of each configuration word.

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Configuration Port

PCAP Definition, Hardware Location and Responsibility

Definition

PCAP
Processor Configuration Access Port

Location CSU configuration path in the PS

Port Width 32-bit configuration data interface

Input connects to SSS. Output connects to dedicated PL configuration logic.

PCAP Interface Boundary

Input

Receive the 32-bit stream from SSS

Output

Connect to dedicated PL configuration logic

Function

Enable the path and transfer configuration words

Parsing

PL configuration logic parses and executes the data

PCAP transfers 32-bit words from PS to PL. Dedicated PL configuration logic parses and executes the stream.

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Chip Architecture

RFSoc

PS: Processing System

Receive load requests and start configuration

CSU: Configuration Security Unit

Move data
Control PCAP

PCAP

Config. Port

Config.
data

PL

Dedicated Configuration Logic

Parse headers and execute register operations

Parser

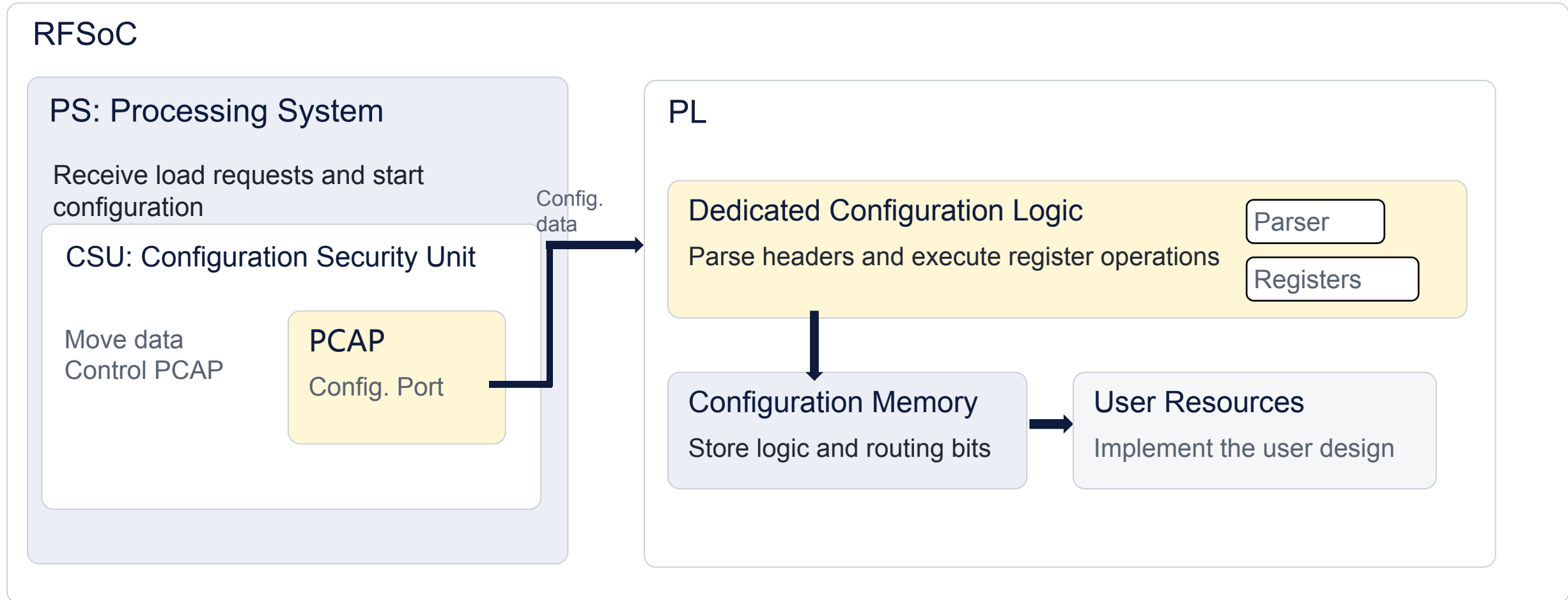
Registers

Configuration Memory

Store logic and routing bits

User Resources

Implement the user design



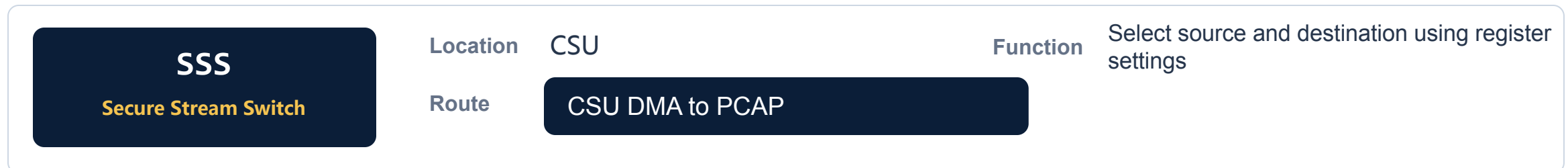
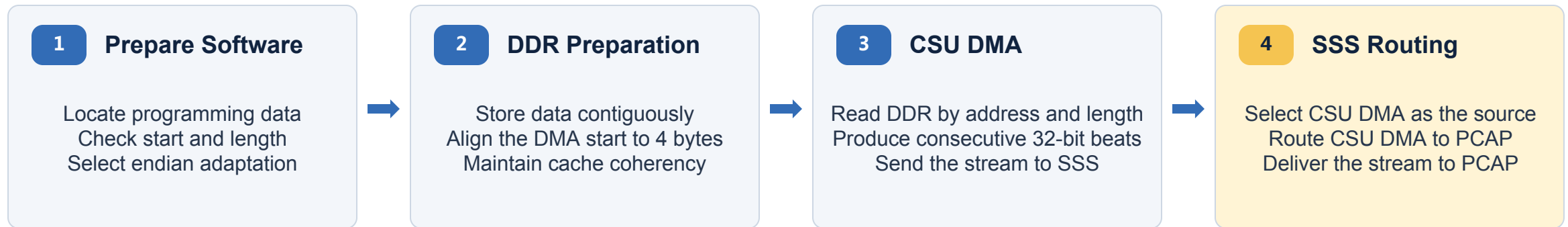
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Before PCAP

Programming-Data Preparation and Transfer to PCAP



Software or the configuration library locates the data and prepares byte order and memory coherency. CSU DMA reads DDR and sends 32-bit words to PCAP through SSS.

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PCAP Transfer

PCAP Transfer of 32-bit Configuration Words

PCAP Control Path

Direction	Select configuration writes from PS to PL
Enable	Release PCAP reset and enable the data path
Status	Report busy, idle, transfer and error status
Completion	Distinguish transfer end from PL configuration completion

PCAP Data Path

Stage	Handling of the Current 32-bit Word
Input Handshake	Accept the word when input is valid and the interface is ready
Data Transfer	Send the word as one 32-bit beat to the PL configuration input
Backpressure	Hold the data beat and stall upstream DMA while downstream is blocked
Order Preservation	Preserve the logical word value and transfer order
PL Handoff	Deliver the word to dedicated PL configuration logic

PCAP preserves word values and order during transfer. PL configuration logic parses and executes the words.

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Receive / Parse

PCAP Reception Conditions and PL Synchronization

Transfer: PCAP Interface Readiness

Reception depends on the enabled write path, interface readiness, downstream backpressure and error status. The sync-word value does not determine interface acceptance.

Parsing: PL Synchronization State

The preamble contains dummy words and a bus-width detection pattern. After detecting AA995566, PL logic parses configuration packets. PCAP transfers fixed 32-bit words.

Key words shown below. Two additional dummy words occur between the detection sequence and sync word.



Preamble and sync both pass through PCAP. PL logic parses packets after detecting AA995566.

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Packet Parsing

Type 1 and Type 2 Packet Headers and Parsing Rules

Type 1 Header



OP (opcode): 00 = NOP, 01 = read, 10 = write, 11 = reserved

Type 1 Parsing

Latch OP, target register and COUNT.
For a write with COUNT > 0, consume data words.
When COUNT reaches zero, parse the next header.

Type 2 Parsing

[31:29]=010 [28:27]=OP [26:0]=COUNT

Type 2 inherits the target register from the preceding Type 1 header. Its 27-bit COUNT specifies the long transfer length.

OP selects the operation. REGISTER selects the target. COUNT bounds the data. Type 2 inherits the Type 1 target register.

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Registers / CMD

Configuration Registers and Control Commands

FAR **Frame Address Register**

Select the configuration-memory address for the next frame

CMD **Command Register**

Receive control commands such as WCFG, START and DESYNC

WCFG **Write Configuration Data**

Writing WCFG to CMD enables the configuration-data write state

FDRI **Frame Data Register Input**

Stream frame data to the configuration address selected by FAR

CRC **Cyclic Redundancy Check**

Accumulate CRC during configuration to detect data errors

START / DESYNC **Startup / End Synchronization**

START requests startup. DESYNC ends the synchronized packet session

OP selects the packet operation. CMD receives WCFG. FAR selects the frame address. FDRI receives frame data.

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Packet Sequence

FDRI Continuous Write Sequence and Hardware Processing

1 Configuration Commands

2 Frame Writes

3 Resource Settings

4 CRC and Startup

File Offset	Word	Parser / Hardware Action	Resulting State
0x176	30002001	Parser: write FAR, one following data word	Next word goes to FAR
0x17A	00000000	FAR: latch frame address 0	Current frame address = 0
0x17E	30008001	Parser: write CMD, one following data word	Next word goes to CMD
0x182	00000001	Controller: execute WCFG	Enable frame-data writes
0x18A	30004000	Parser: select FDRI for a write, COUNT = 0	FDRI is the write target
0x18E	50835C38	Parser: write operation, COUNT = 8,608,824	Load the long word count
0x192	FDRI DATA...	Frame-write logic: receive following FDRI data	Write until COUNT = 0

FAR sets the frame address. WCFG enables writes. Type 2 bounds FDRI data until COUNT reaches zero.

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Frame Writes

FDRI Frame Assembly and Configuration-Memory Writes

1 Configuration Commands

2 Frame Writes

3 Resource Settings

4 CRC and Startup

1 Receive Words

```
buffer[index] = word  
CRC = update(CRC, word)  
index++  
remaining--
```

Store each FDRI word in the frame buffer. Update CRC and decrement the remaining count.

2 Write a 93-word Frame

$$93 \times 32 \text{ bit} \\ = 2,976 \text{ bit} = 372 \text{ B}$$

Write the 372-byte frame to configuration memory at the address selected by FAR.

3 Advance FAR

FAR fields: block type, row, column and minor

Advance FAR through the device-defined valid frame addresses, then receive the next frame.

The 8,608,824 FDRI words equal 92,568 frame-length units. The stream may include padding or dummy frames.

Frame data reaches configuration memory at the locations selected by FAR.

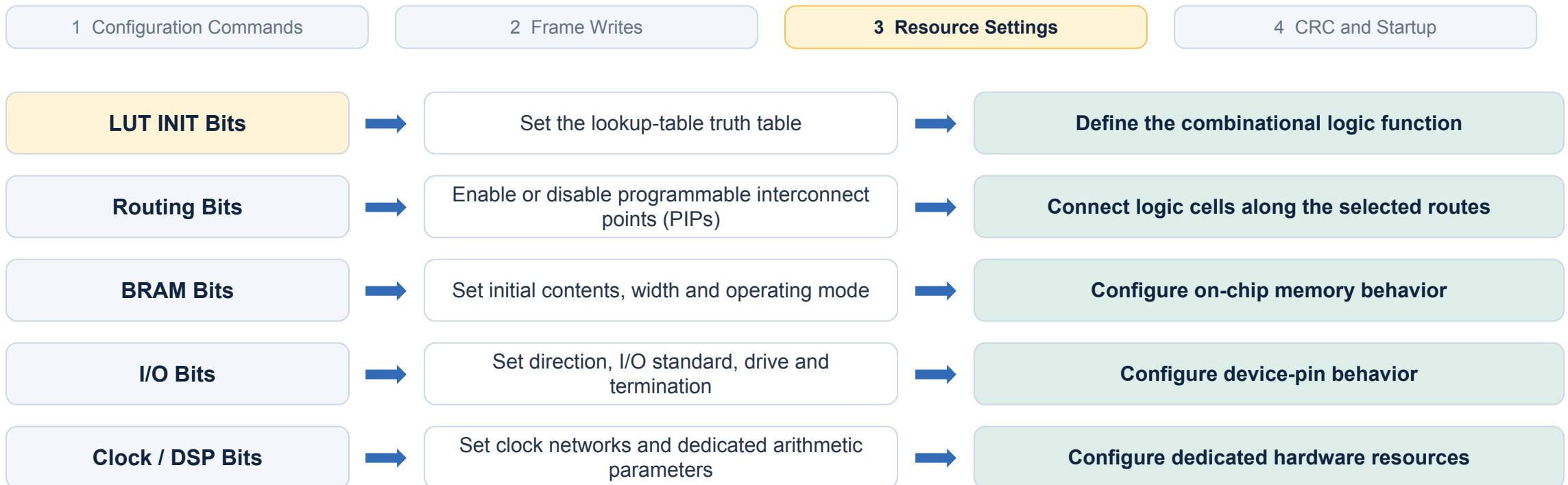
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PL Resources

Configuration Bits Control PL Resources and Routing



Configuration memory now holds the design. Startup control still governs user I/O and sequential resources.

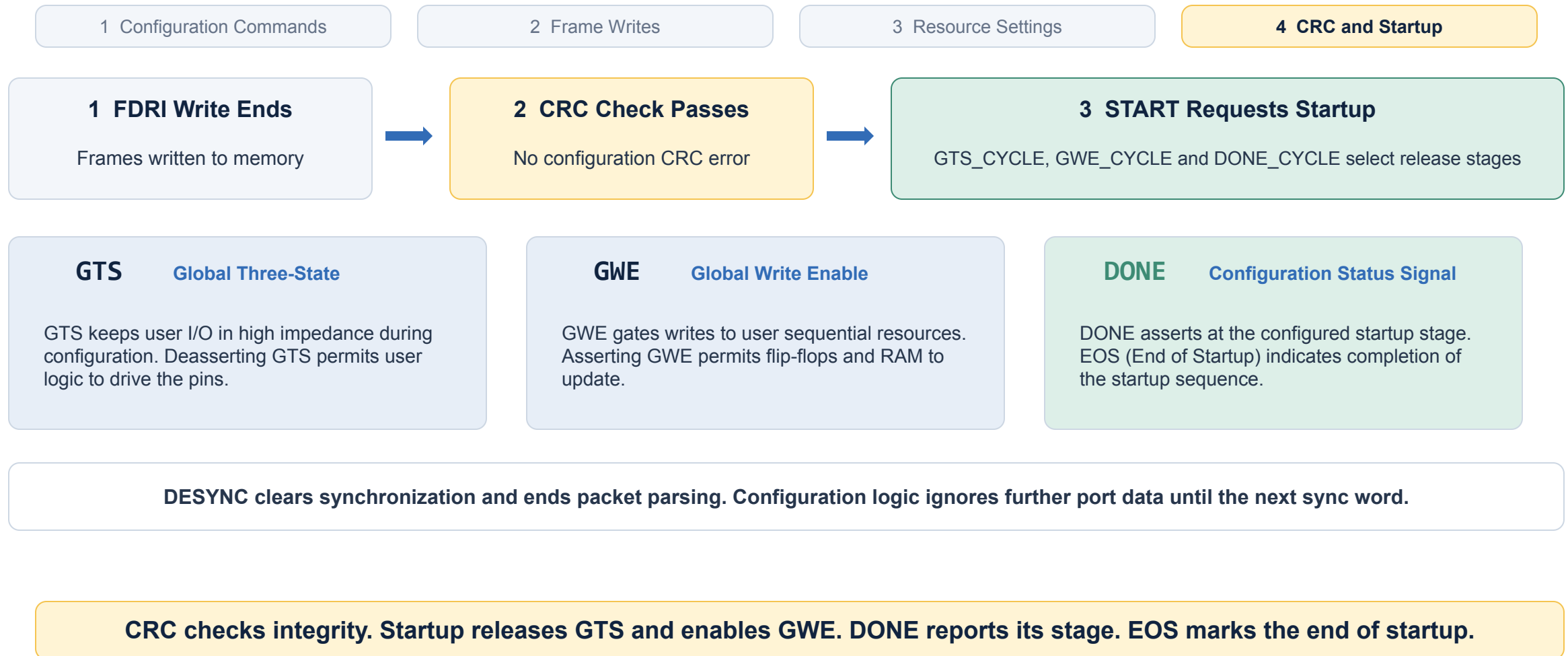
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CRC and Startup

Configuration Integrity and User-Circuit Startup





/02

Multiple-Bitstream Flash Loading

Flash Loading: Standalone Storage Layout



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Storage Layout

Flash adds persistent storage and bitstream selection to the common PL configuration mechanism. Each Flash device contains two software-defined 48 MB bitstream slots. Each slot contains a file record and one .bit file.

Flash Chip 0 128 MB

Bitstream Slot 0 48 MB	Bitstream Slot 1 48 MB	Unused 32 MB
0x00000000	0x03000000	0x06000000 0x08000000

Flash Chip 1 128 MB

Bitstream Slot 2 48 MB	Bitstream Slot 3 48 MB	Unused 32 MB
0x00000000	0x03000000	0x06000000 0x08000000

Inside Each 48 MB Slot

File Record 64 KB

Bitstream starts at slot base + 0x00010000

Chip select distinguishes the two devices. Maximum bitstream size per slot: 0x02FF0000 bytes (47.9375 MB).

Records store length, CRC, validity and filename. After reading the selected file, reuse the common configuration mechanism.

Flash Loading: Linux Partition Layout



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MTD Partitions

MTD (Memory Technology Device) provides partition and offset access for raw Flash reads, writes and erases. The device tree defines the partitions. Each 48 MB bitstream partition serves as one logical slot, while file records occupy a separate region.

256 MB Logical Address Space

System 23.25 MB	Slot 0 48 MB	Slot 1 48 MB	Slot 2 48 MB	Slot 3 48 MB	Records 0.5 MB	Unused 40.25 MB
---------------------------	------------------------	------------------------	------------------------	------------------------	--------------------------	---------------------------

Slot starts: 0x01740000, 0x04740000, 0x07740000, 0x0A740000

Full 48 MB Bitstream Partitions

Keep the original 23.25 MB system region.
Give each bitstream a separate partition.
Access partitions through MTD.

Independent Record Erasure

Record region: 0x0D740000–0x0D7C0000.
Each record has its own 128 KB erase block.
Updating one record preserves the others.

Records are separate. Bitstreams start at partition offset 0. Both layouts use the following update and load rules.

Multiple-Bitstream Flash Loading



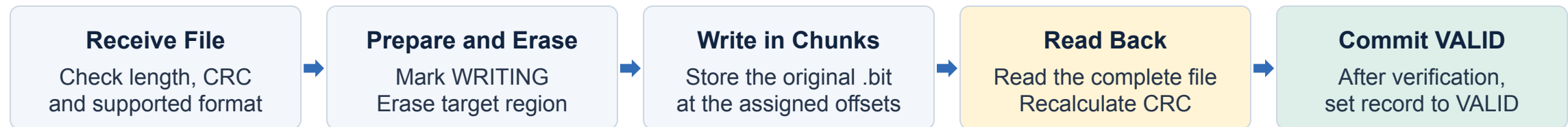
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Update and Load

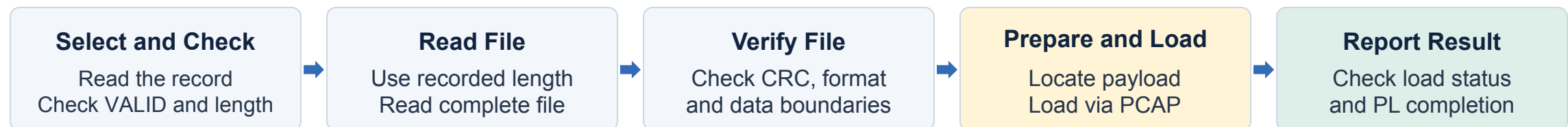
Bitstream Slot Updates and the Common Configuration Entry

Use the storage layout to access the selected bitstream slot. Store the complete .bit file, then load the saved bitstream for full PL configuration.

File update: store a complete file whose integrity can be checked



Load from a slot: use its file record to determine the data range, then reuse the common configuration mechanism



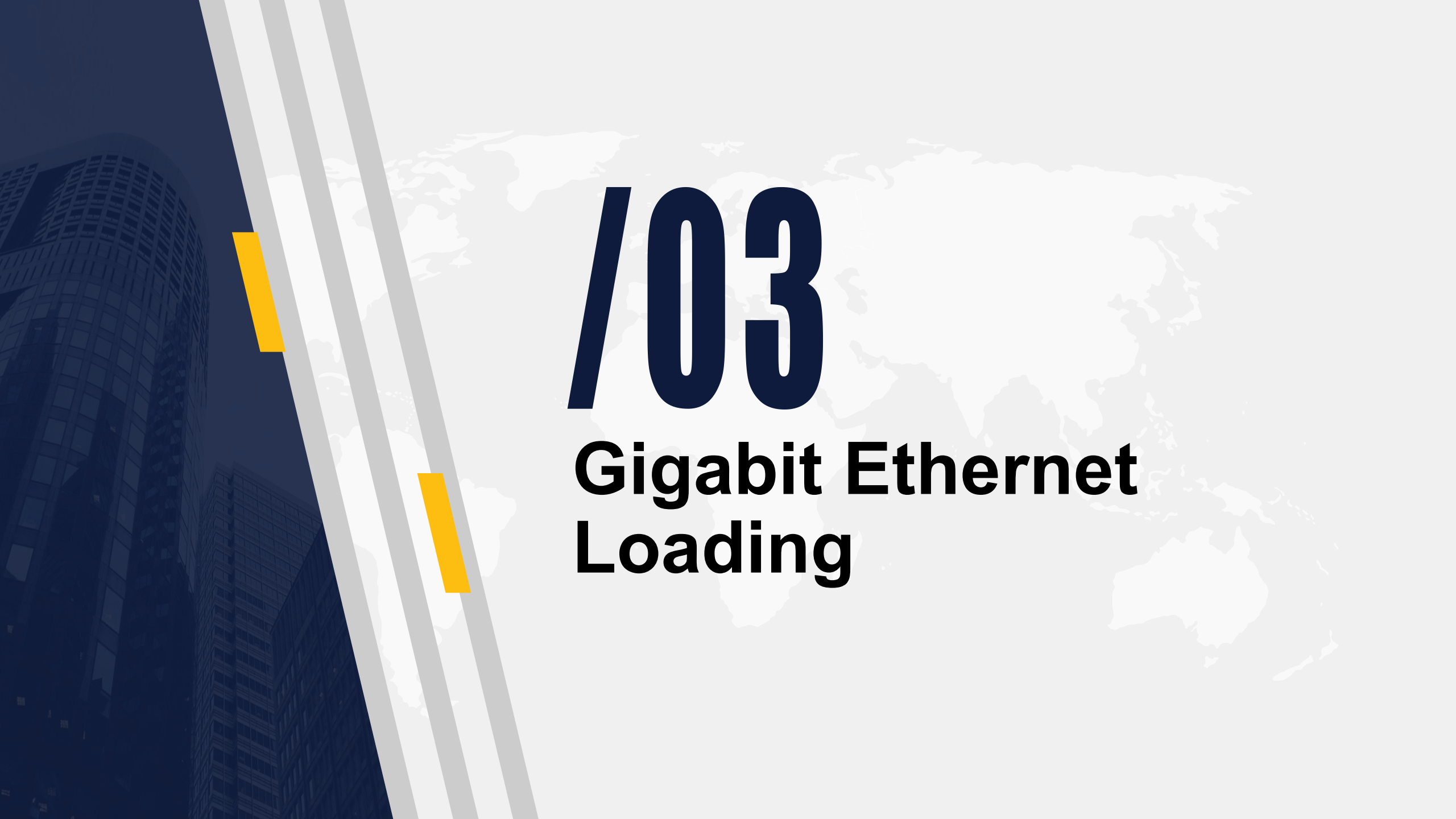
Standalone: Flash Access and PL Configuration

XQspiPsu: QSPI driver for Flash commands and data.
XFpga: XilFPGA library interface to submit configuration and return status.

Linux: fpgautil and FPGA Manager

fpgautil: user-space tool to submit a load request.
FPGA Manager: kernel framework using the device driver and firmware to configure PL and track state.

Interrupted updates leave the slot invalid. No automatic rollback. Loading uses the common PL configuration mechanism.



/03

**Gigabit Ethernet
Loading**

Gigabit Ethernet Loading



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Receive and Verify

TCP File Reassembly and PL Loading

After receiving the complete file, the Ethernet path invokes the common configuration entry.

File Reassembly

TCP supplies an ordered byte stream. One receive may contain both protocol metadata and file data. Parse the declared length and CRC, then accumulate file bytes.

Offset = file bytes received
Remaining = declared – received
Accumulate file CRC

Checks Before Configuration

- 1 Received size = declared size
- 2 No early disconnection
- 3 File CRC matches declared CRC
- 4 Valid .bit format and data bounds

Configure PL After Verification

The standalone application assembles the file in DDR. Linux uses a temporary file. After verification, full PL configuration follows the common programming-data and word-processing mechanism.

**Reception or CRC failure:
return an error and retain the current
PL design**

Receive and verify the complete file before starting configuration.

Gigabit Ethernet Loading



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Load Results

Common Configuration Calls and Completion Checks

Software submits the complete received file to the same underlying PL configuration hardware.

Stage	Standalone	Linux	Common Requirement
Prepare File	Complete .bit in DDR	Complete .bit in a temporary file	Valid length, CRC and supported format
Submit Load	Flush cache and call XFpga	Convert data and call fpgautil	Correct data bounds and byte order
Hardware Path	XFpga controls CSU DMA / PCAP	FPGA Manager uses device firmware	PL logic parses packets and writes frames
Confirm Success	XFpga return status and PL_DONE	Tool return value and operating state	Confirm PL configuration completion

Load Failure

Report an explicit error if configuration fails. Reception or DMA completion alone does not establish PL configuration success.

Configuration status confirms PL loading after file verification. Check application behavior separately.



/04

PCIe Loading

Partitions

Persistent Download Path and Reconfigurable Partition

PCIe Endpoint (device interface) and XDMA reside in PL. Partial configuration updates only the target partition, while the static region retains the download and control paths.

Static Region: Remains Active

PCIe Endpoint, XDMA and DDR access

Control registers and clock-domain handoff

Target isolation, reset and status control

Reconfigurable Partition: Target Function

Fixed Boundary Interface

Matching port names, directions and widths

Fixed Partition and Controls

Fixed physical region. Static logic supplies clock and reset

Bitstream / Static Design Match

Generate and verify against the current static checkpoint

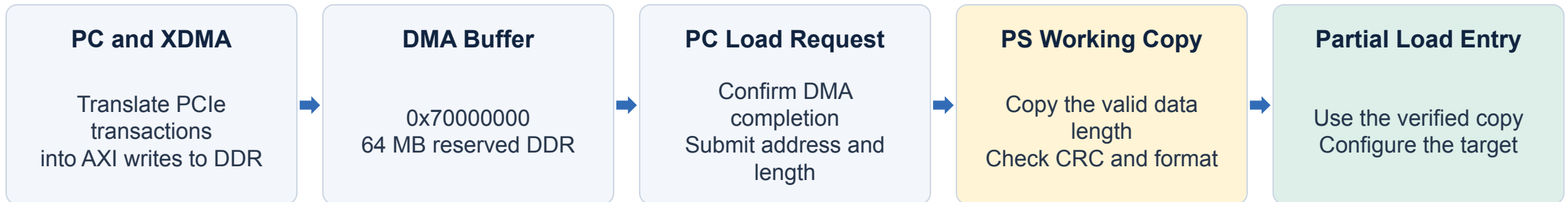
Keep the target isolated and in reset during loading. On success, release reset first, then remove isolation and restore outputs.

Partial bitstreams use PCAP and the same packet / frame-write mechanism. Writes remain within the target partition.

Data Handoff

XDMA Transfer and the PS Configuration Working Copy

The PC finishes DMA transfer before handing the request to the PS through control registers. DDR transfer and PCAP configuration are separate stages.



Stable Working Copy

A stable copy prevents receive-region DMA writes from changing data during configuration. Standalone: use a fixed 64 MB working region at 0x60000000. Linux: allocate a separate copy based on the requested length. Reserved DDR holds the DMA receive region.

Validate the address range, length ≤ 64 MB, 4-byte alignment and base-design identifier.

DMA completion confirms arrival in DDR. The PS must still validate the request and working copy, then invoke partial configuration.

PCIe Loading



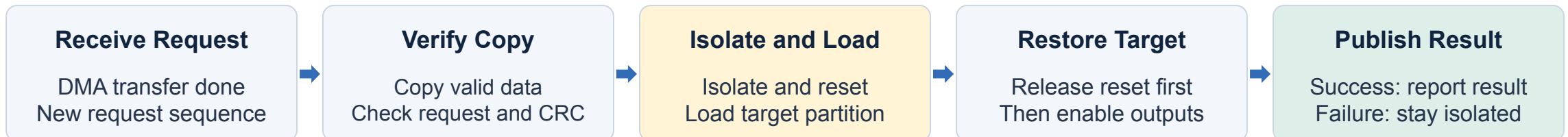
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Control / Results

Configuration Handoff and Target-Partition State

Control registers identify the data range and request sequence. After verification, the PS manages isolation, configuration and the response.

Information	PC Request	PS Check / Response	Purpose
Data Range	Source address and valid length	Address, length and alignment	Bound the configuration data
Integrity / Identity	CRC and base-design ID	Copy CRC and base-design ID	Reject corrupt or incorrect requests
Task / Result	Mailbox START and request sequence	Result code, state and response sequence	Avoid duplicates and match the response



The standalone application uses XFpga. Linux uses FPGA Manager. Precheck failure preserves the target. Load failure after isolation retains isolation and reset.

The base-design ID does not replace bitstream compatibility checks. All approaches reuse the PL configuration mechanism.



/05

Demonstration

Demonstration



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Multiple-Bitstream Flash Loading Demo

47DR PL 位流管理工具

板卡连接

☒ 千兆网 ☐ PCIe IP地址 192.168.1.10 端口 7404

选择 BIT/BIN 文件

文件 选择 .bit 或 .bin 文件

多文件启动配置

目标槽位

槽位	文件长度	文件名
0	-	-
1	-	-
2	-	-
3	-	-

空闲

通信和操作日志

Demonstration



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Ethernet Loading Demo

47DR PL 位流管理工具

板卡连接

千兆网 PCIe IP地址 192.168.1.10 端口 7404 连接 断开 未连接

选择 BIT/BIN 文件

文件 选择 .bit 或 .bin 文件 浏览... 配置

多文件启动配置

目标槽位 Slot 0 上传到槽位 从槽位配置 PL 清空槽位 刷新槽位信息

槽位	文件长度	文件名
0	-	-
1	-	-
2	-	-
3	-	-

空闲 0%

[16:44:46] CFG1/CFG2 上位机已启动

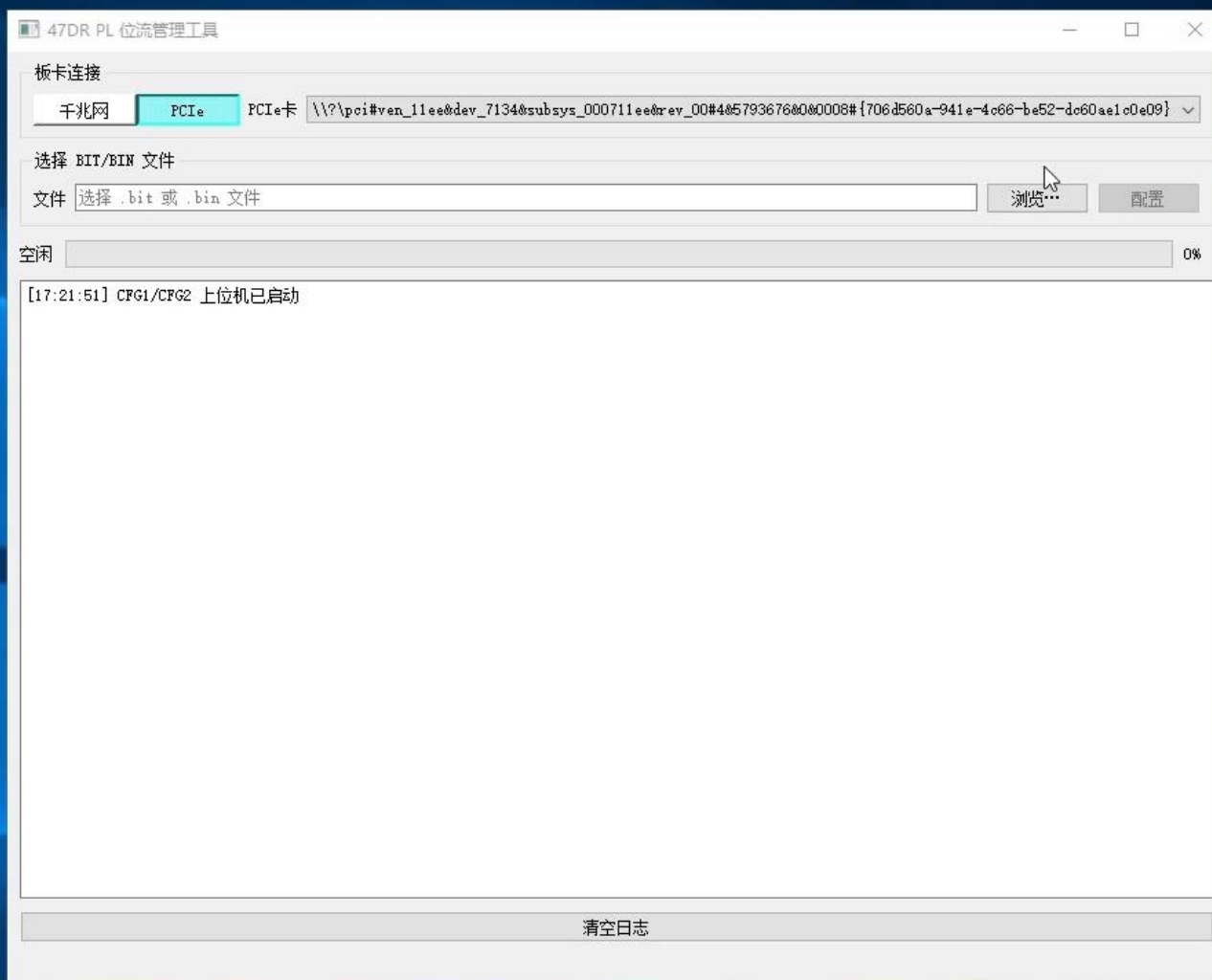
清空日志

Demonstration



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PCIe Loading Demo



RFSoc 47DR board card performance test



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10MHz@0dBm ADC通道隔离度测试记录表

ADC通道无杂散动态范围测试记录表1

通道 编号	采样率	1MHz @0dBm	10MHz @0dBm	68MHz @0dBm	300MHz @0dBm	314MHz @0dBm
1	5GHz	69.5	79.0	76.0	73.5	77.3
2		71.2	77.2	78.2	76.0	76.3
3		73.9	77.0	79.2	76.3	78.4
4		69.9	74.8	77.8	75.1	79.1
5		71.3	76.3	79.6	73.3	76.5
6		70.2	78.0	75.4	74.8	76.9
7		69.8	76.3	78.3	72.8	76.8
8		74.6	79.9	76.5	77.4	76.2

采样率	信号输入通道	幅度 dB	相邻通道	幅度 dB	隔离度 dB
5GHz	1	-0.87	2	-89.50	88.63
	2	-0.95	1	-90.56	89.61
	2	-0.95	3	-84.90	83.95
	3	-1.03	2	-85.49	84.46
	3	-1.03	4	-92.89	91.86
	4	-1.08	3	-93.33	92.25
	4	-1.08	5	-83.52	82.44
	5	-1.03	4	-86.30	85.27
	5	-1.03	6	-94.75	93.72
	6	-1.02	5	-89.12	88.10
	6	-1.02	7	-92.18	91.16
	7	-0.86	6	-95.80	94.94
	7	-0.86	8	-88.58	87.72
	8	-0.90	7	-91.27	90.37

RFSoc 47DR board card performance test



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ADC通道信噪比测试记录表2(dBc)

通道 编号	采样率	650MHz @0dBm	1300MHz @0dBm	2856MHz @0dBm	2998MHz @0dBm
1	5GHz	68.92	67.11	61.67	63.46
2		68.67	66.73	61.21	62.75
3		68.33	66.57	61.51	63.13
4		68.60	66.93	61.48	62.85
5		68.42	66.65	61.55	63.18
6		68.61	66.69	61.12	62.23
7		68.63	66.70	61.05	62.86
8		68.56	66.69	61.75	63.29

1300MHz@0dBm ADC噪声谱密度记录表

采样率	信号输入通道	NSD (dBFS/Hz)
5GHz	1	-141.09
	2	-141.12
	3	-141.03
	4	-141.52
	5	-140.96
	6	-141.09
	7	-141.09
	8	-141.26

A low-angle, upward-looking photograph of several modern skyscrapers with glass facades, creating a sense of height and architectural scale. The image is in a dark blue monochrome palette. The word "THANKS" is centered in a bold, white, sans-serif font.

THANKS