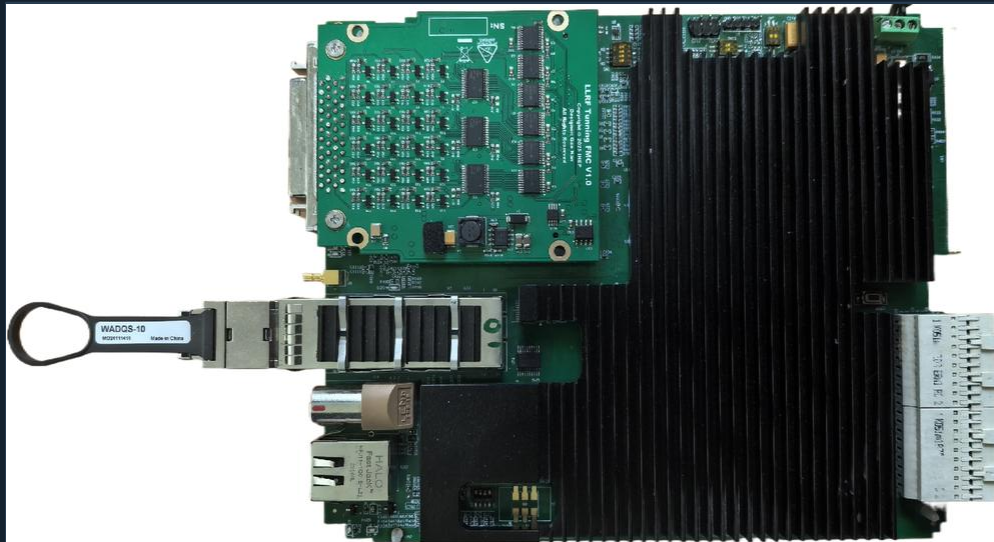
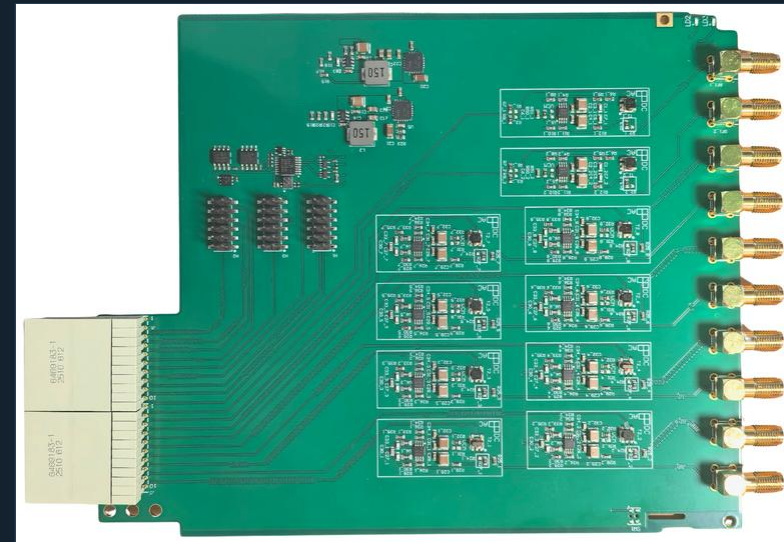


Development of Superconducting Cavity Simulator Based on MicroTCA Platform

An FPGA-based hardware-in-the-loop emulator that lets superconducting-cavity LLRF controllers be commissioned before the machine exists



AMC-7Z045 carrier — Zynq XC7Z045 SoC



Interface RTM on μ TCA.4 Zone 3 rear I/O

Outline

- 01** **Background & motivation**
CEPC LLRF development and the missing cavity plant

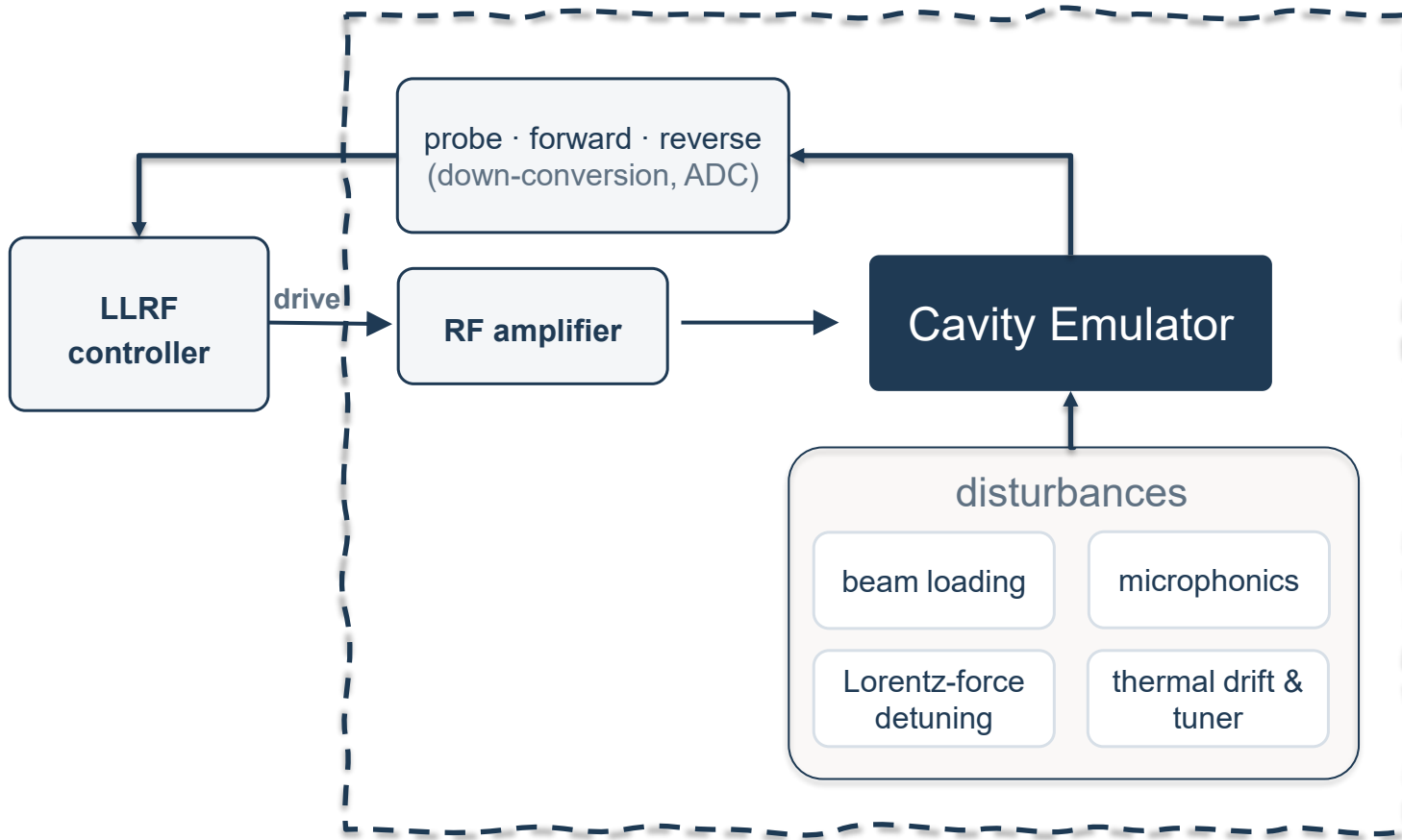
- 02** **MicroTCA platform**
AMC-7Z045 carrier and the drop-in interface RTM

- 03** **Implementation & principle**
plant chain, model derivations, fixed point, timing, operation

- 04** **Summary & outlook**
status and the next steps toward closed-loop operation

BACKGROUND

The plant: a narrow-band, high-Q resonator



Narrow-band, high stored energy

650 MHz · 2-cell collider (Higgs, CW):

$Q_L = 1.6 \times 10^6 \rightarrow$ half-bandwidth ≈ 203 Hz

1.3 GHz · 9-cell booster (Higgs):

$Q_L = 1.0 \times 10^7 \rightarrow$ half-bandwidth ≈ 65 Hz

Multi-source disturbances

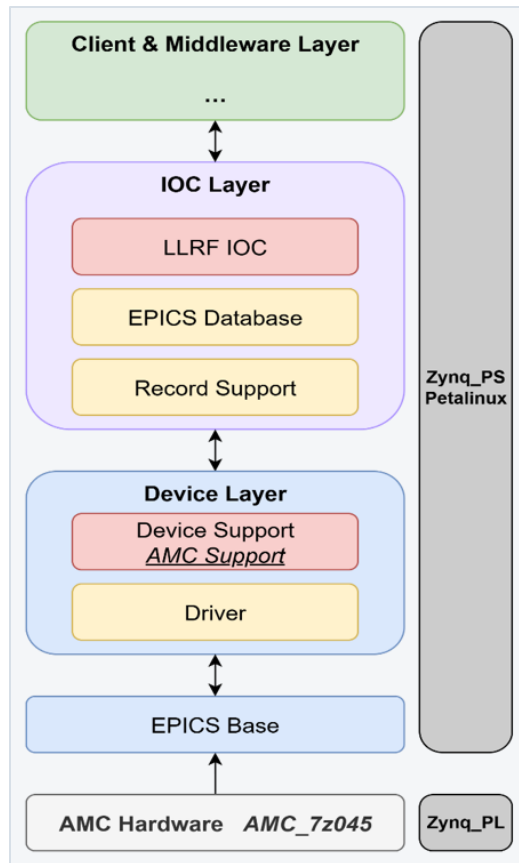
beam loading, microphonics, Lorentz force and helium pressure act on the field at once

Delay bounds the loop

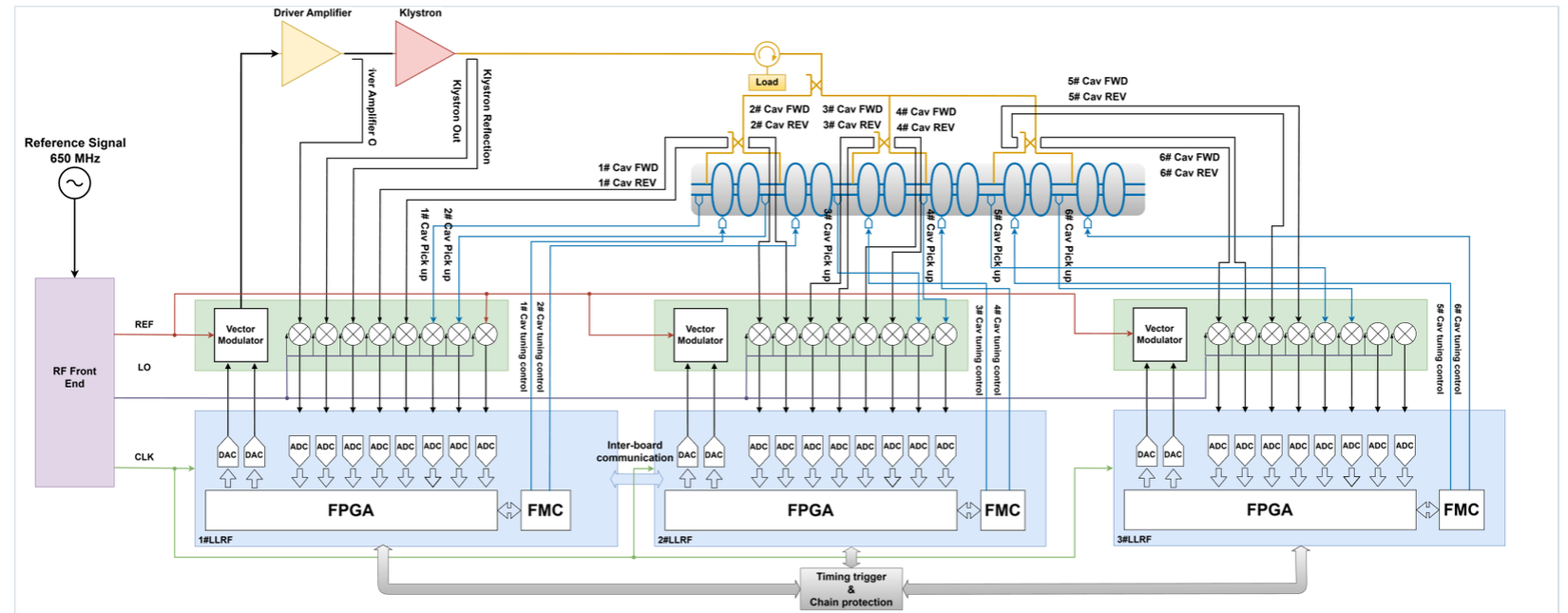
converter, cable and filter delays eat phase margin before control starts

BACKGROUND

The project: CEPC LLRF system under development



Software stack: EPICS layers on the Zynq PS, AMC hardware below



LLRF design for the 650 MHz main ring: 3 FPGA boards, 6 cavities, shared reference — one controller station per two cavities

3 × LLRF boards

8 ADC + 2 DAC channels each,
FMC expansion

Superheterodyne front end

vector modulator IF → I/Q baseband

Common REF / LO / CLK

timing, trigger and
machine-protection chain

The gap: no cavity available for commissioning

- Neither cavity class is in operation yet, and cryogenic operation plus high-power RF are not always on tap
- Machine-protection rules restrict what may be attempted on a live cavity
- Quench-like events are rare and hard to reproduce — yet protection logic must be proven against them
- A controller checked only against offline models misses cables, converters, delays — and the unexpected

650 MHz · 2-cell

collider (Higgs, CW):

$$Q_L = 1.6 \times 10^6 \rightarrow \text{half-bandwidth} \approx 203 \text{ Hz}$$

1.3 GHz · 9-cell

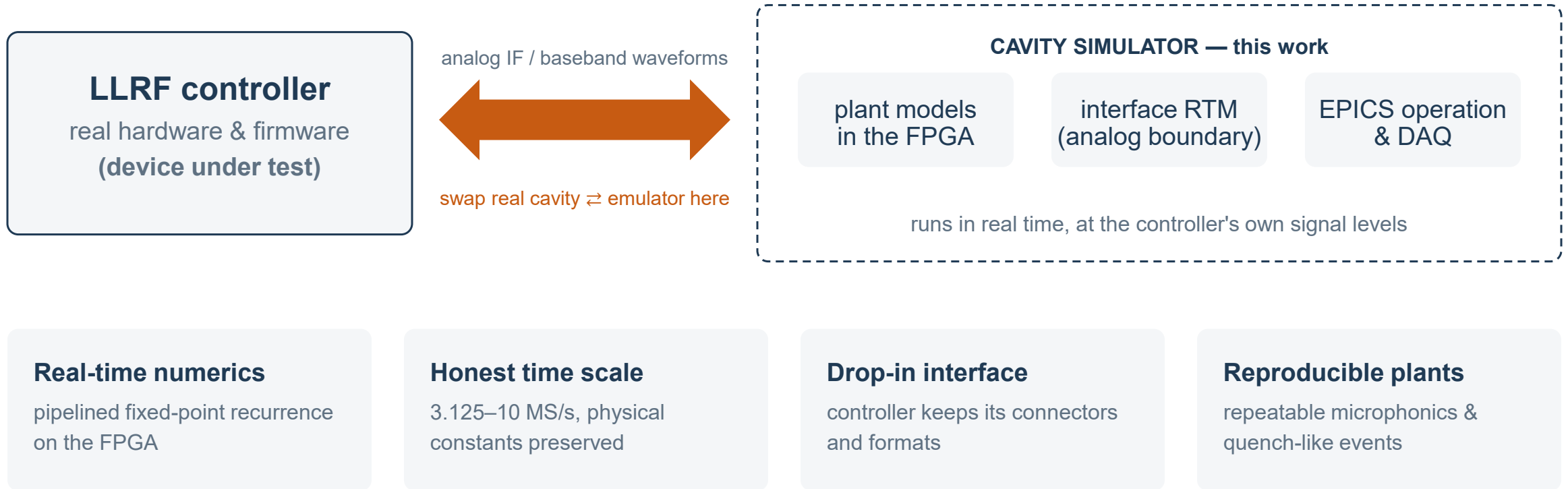
booster (Higgs):

$$Q_L = 1.0 \times 10^7 \rightarrow \text{half-bandwidth} \approx 65 \text{ Hz}$$

Commissioning needs a realistic, real-time stand-in for the cavity — one the controller cannot tell from the real plant.

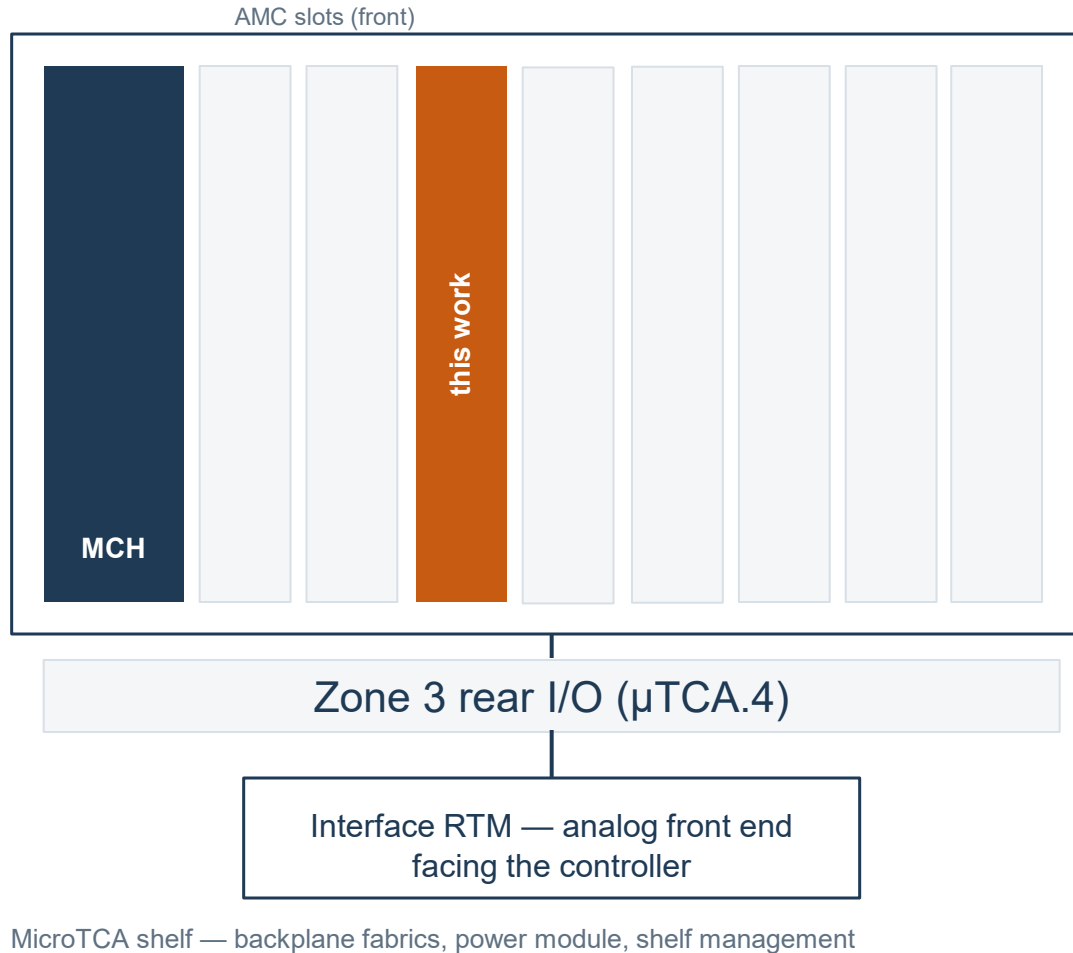
BACKGROUND

The approach: hardware-in-the-loop cavity emulator



BACKGROUND

The platform: MicroTCA and μ TCA.4 rear I/O



Compact & modular

AMC card $\approx 74 \times 180$ mm, hot-pluggable;
standard PICMG fabric and connectors

Managed hardware

IPMI shelf management plus on-card
MMC: health, temperature, status

μ TCA.4 — physics variant

rear I/O designed for experiment front
ends; RTM carries the analog boundary

Room to grow

spare slots and QSFP optics for future
multi-cavity stations

IMPLEMENTATION

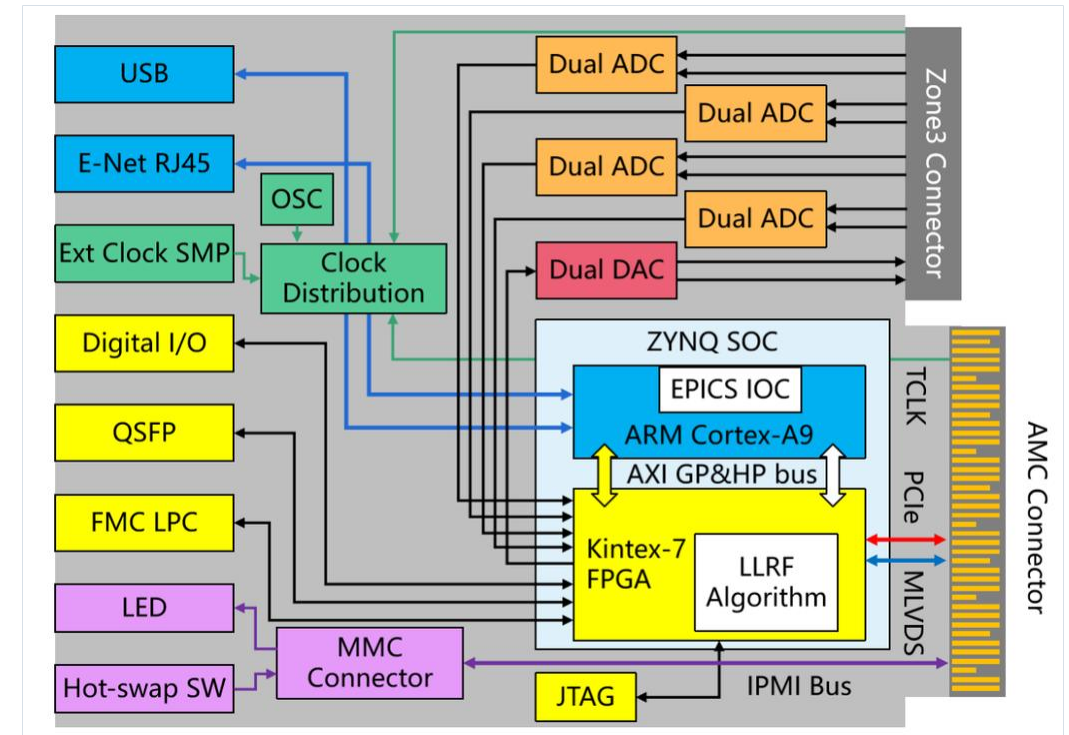
Platform & implementation

Hardware platform, the FPGA plant chain with its models, and the EPICS-based operating interface.

AMC-7Z045 carrier: Zynq SoC + converters



The carrier card: converters and clocking feed the FPGA; AMC connector at the rear edge



Board architecture — Zone 3 connector exits to the RTM

Zynq XC7Z045

dual ARM Cortex-A9 + Kintex-7 FPGA

8 × 16-bit ADC

4× AD9268, up to 125 MS/s each

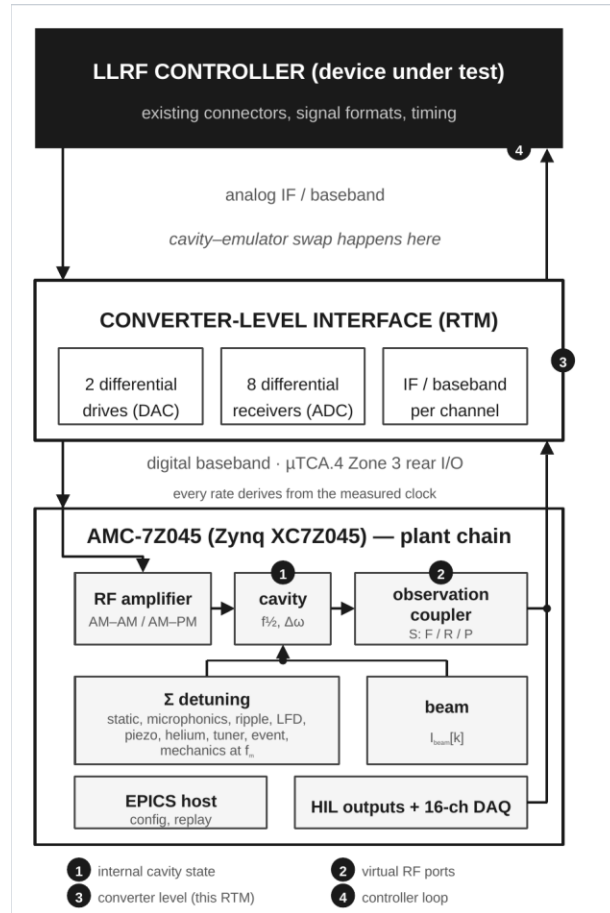
2 × 16-bit DAC

AD9783, up to 500 MS/s

EPICS IOC on board

Linux on the ARM; QSFP for expansion

System architecture: controller ↔ RTM ↔ emulator



Three tiers, one clean boundary between them:

LLRF controller — unchanged

keeps its connectors, signal formats, and timing

Interface RTM — the analog boundary

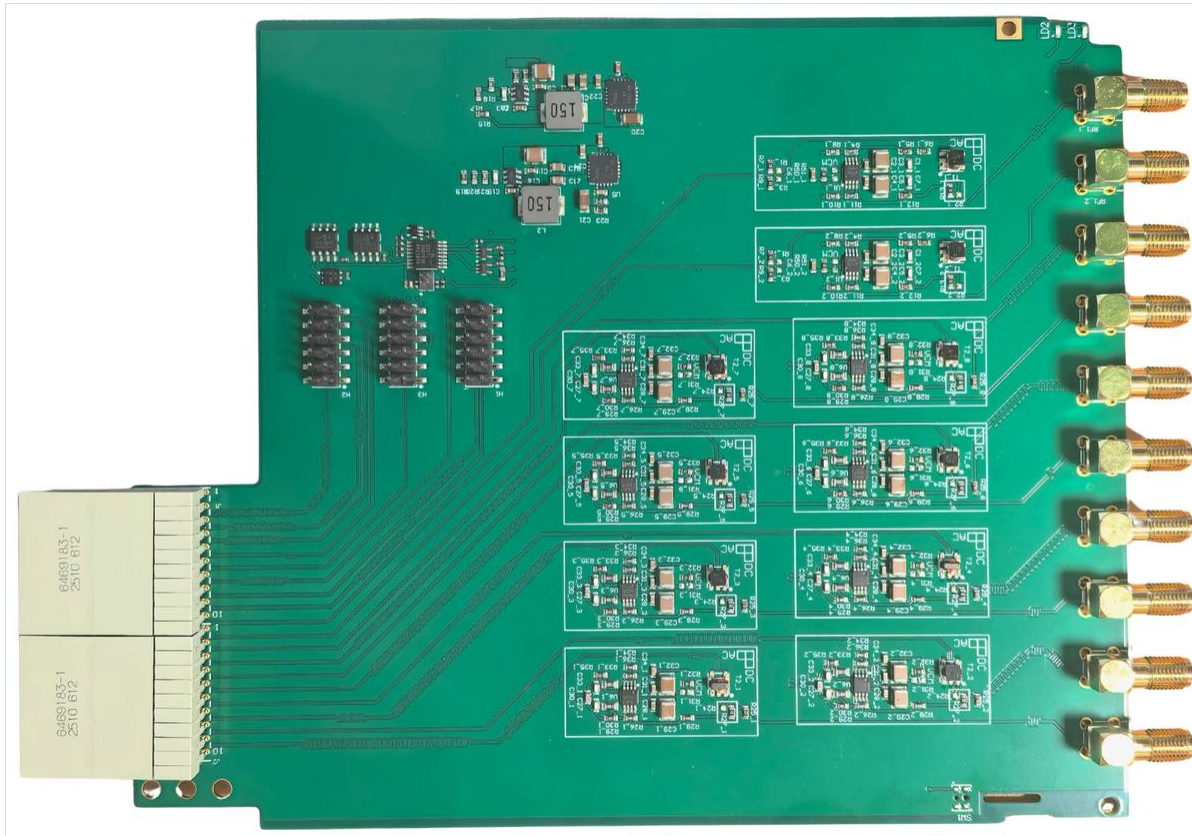
2 differential drives, 8 receivers, IF or baseband per channel

AMC-7Z045 — cavity model & Software

FPGA plant chain, 16-channel DAQ, EPICS on the ARM

Real cavity $\rightleftharpoons$ emulator swap happens at the RTM boundary — nothing on the controller side changes.

Interface RTM: the drop-in analog boundary



The fabricated RTM: 10 differential channels leave through the SMA field; Zone 3 connector at the left edge

2 differential drive paths

emulator DAC → IF or baseband, native controller levels

8 differential receiver channels

transformer-coupled IF or direct baseband, per channel

Reference-clock routing

shares the emulator clock domain with the controller interface

I2C management plane

board identity, temperature readout, status

Drop-in: the controller keeps its existing connectors, signal formats, and timing — no modification, no external conversion.

IMPLEMENTATION

FPGA plant chain: amplifier → cavity → coupler

RF-amplifier model

static AM–AM / AM–PM map plus
envelope bandwidth

Cavity recurrence

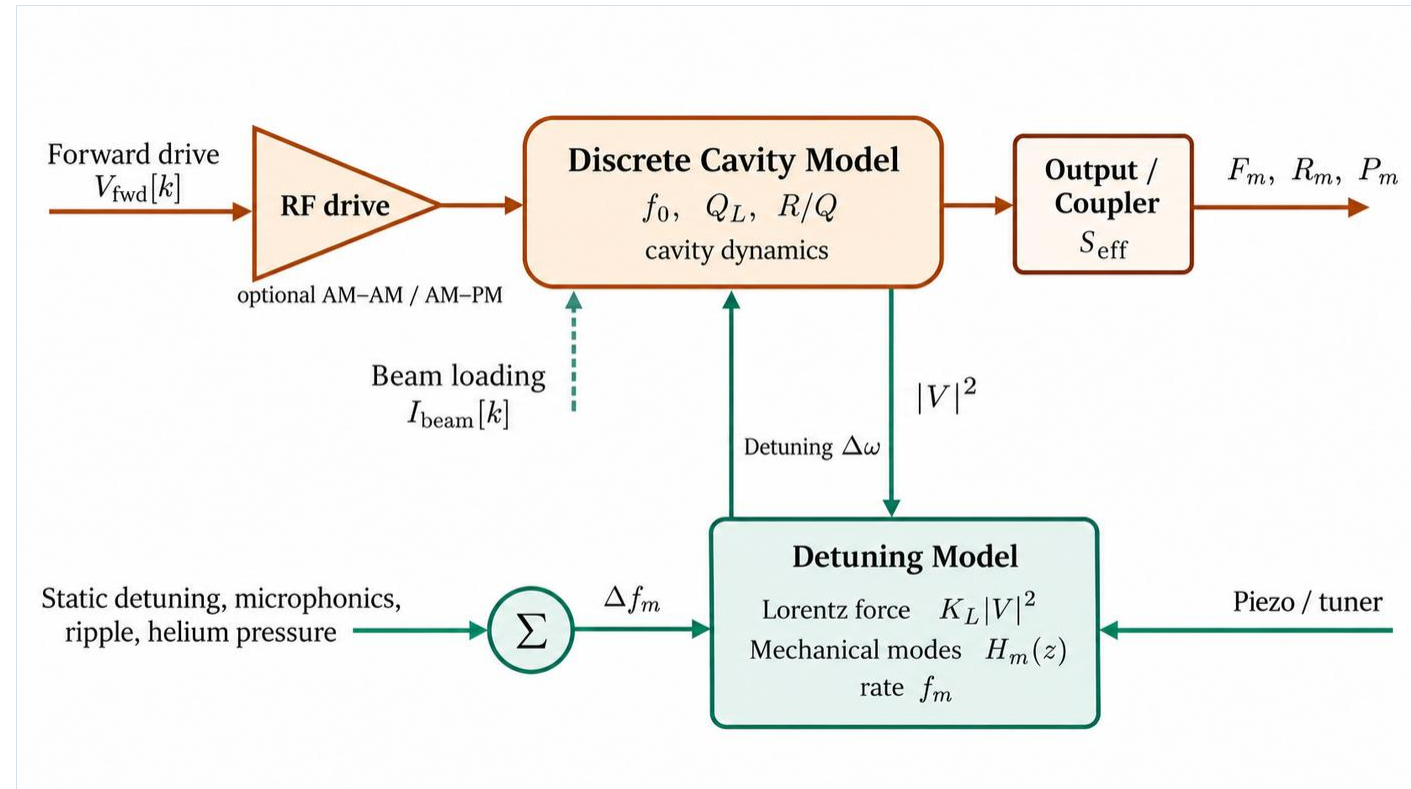
exact zero-order-hold: real decay ×
complex rotation; beam current injected
directly

Detuning model

Lorentz force, microphonics, ripple,
helium, piezo — via the mechanical
transfer model

Observation coupler

narrow-band matrix maps cavity state
onto forward / probe / reverse ports



Plant chain implemented on the XC7Z045 — every block runs as a pipelined fixed-point recurrence

Cavity model: exact discrete recurrence

1 Envelope equation

rotating wave at the carrier; V is the complex envelope, u the forward drive plus beam current

$$dV/dt + (\omega_{1/2} - j\Delta\omega(t)) \cdot V(t) = \omega_{1/2} \cdot u(t), \quad \omega_{1/2} = \omega_0 / 2Q_L$$

2 Exact zero-order-hold step

u and $\Delta\omega$ constant over one model interval $T_s \rightarrow$ the exact solution, not an approximation

$$V[k+1] = \Phi[k] \cdot V[k] + \Gamma[k] \cdot u[k]$$

$$\Phi[k] = \exp[(-\omega_{1/2} + j\Delta\omega[k]) \cdot T_s], \quad \Gamma[k] = \omega_{1/2} \cdot (1 - \Phi[k]) / (\omega_{1/2} - j\Delta\omega[k])$$

3 Implemented recurrence

pole split into a real decay and a unit complex rotation

$$A = \exp(-\omega_{1/2} \cdot T_s) \text{ (real)}, \quad R(\theta[k]) = e^{j\theta[k]}, \quad \theta[k] = \Delta\omega[k] \cdot T_s$$

$$V[k+1] = A \cdot R(\theta[k]) \cdot V[k] + B_f \cdot V_{fwd}[k] + B_b \cdot I_b[k]$$

Why this factorization: for a high-Q cavity $\omega_{1/2} \cdot T_s \ll 1$ — keeping the real decay and the unit rotation separate preserves the pole accuracy of the 32-bit fixed-point state (S1.30 coefficients, Q3.28 state).

IMPLEMENTATION

Coupled models: beam, amplifier, mechanics, coupler

Beam excitation

$$I_b[k] = g_b \cdot p[k] \cdot (I_{bl} + jI_{bQ}) \cdot e^{i\varphi_b}$$

gated complex profile with programmable amplitude, phase, delay and width — an edge lands within one model step

RF amplifier

$$V_a[k] = (1 - \alpha_a) \cdot V_a[k-1] + \alpha_a \cdot N(V_{in}[k]), \alpha_a = 1 - \exp(-2\pi f_a T_s)$$

exact step of a first-order lag at bandwidth f_a , followed by the static AM–AM / AM–PM map N ; pure transport delay kept separate

Mechanical response

$$\Delta f_m[k] = K_{mf} \cdot H_m(z) \cdot [K_{fm} \cdot p_e[k] + K_{pm} \cdot u_p[k]]$$

field energy and piezo command drive a bank of second-order sections or FIR filters; runs at a slower rate f_m

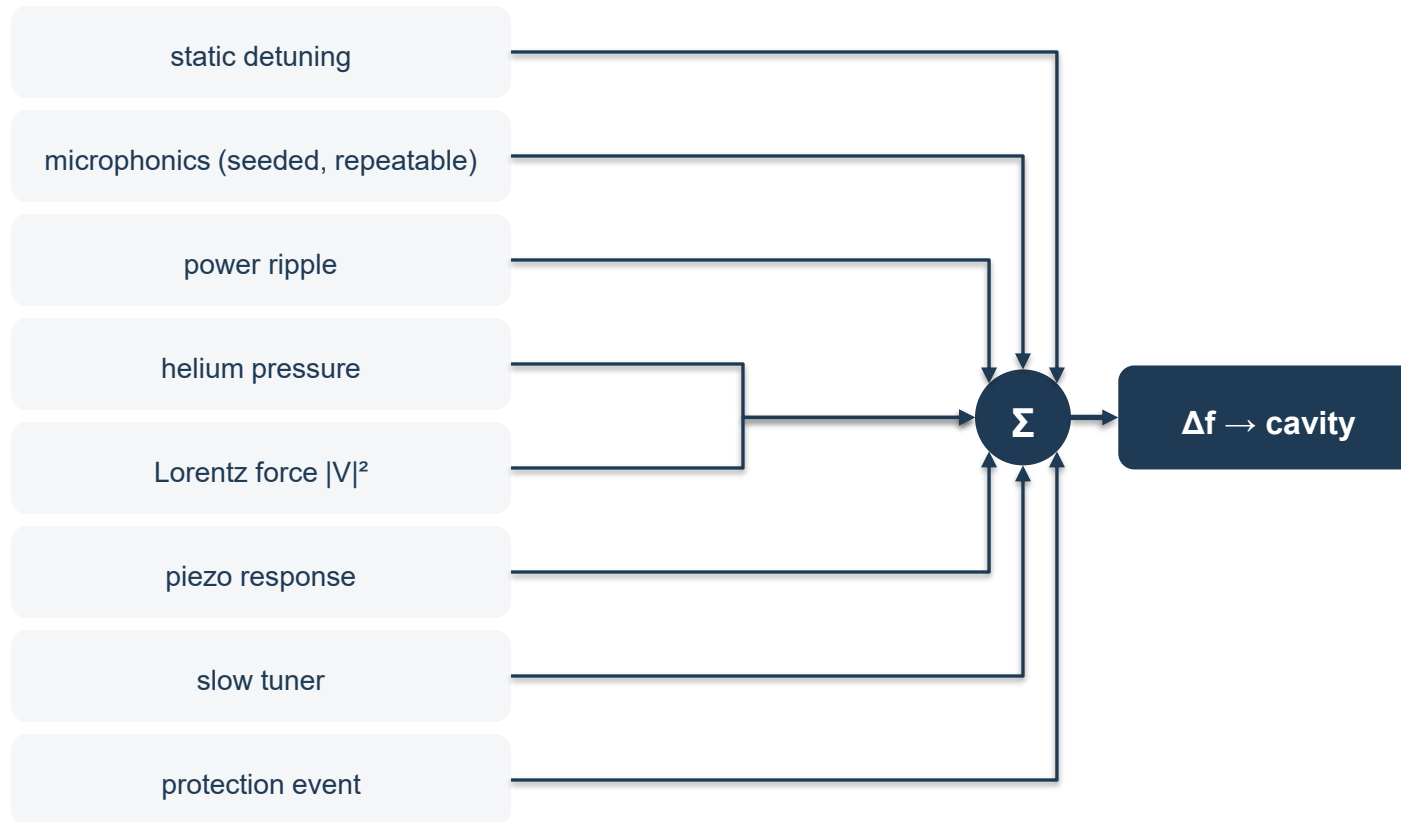
Observation coupler

$$\begin{bmatrix} F_m & R_m & P_m \end{bmatrix} = S \cdot \begin{bmatrix} F & R & P \end{bmatrix}$$

3×3 complex matrix set per reference plane — absorbs per-channel gain, phase and leakage

IMPLEMENTATION

Disturbances: detuning budget & quench events



Quench-like events

A two-state electrothermal model — fast RF loss, slow thermal detuning — drives the field build-up and collapse that protection logic must survive.

Abnormal operation becomes a scripted, repeatable scenario.

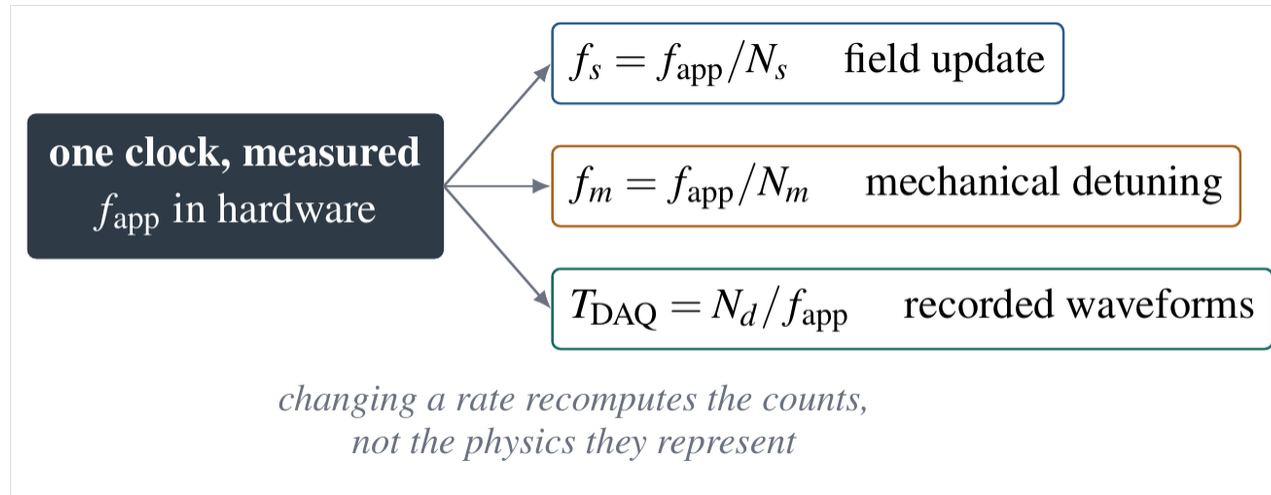
Why it matters

scenarios that are impossible on a live machine become routine

$$\Delta f = \Delta f_{static} + \Delta f_{micro} + \Delta f_{ripple} + \Delta f_{LFD} + \Delta f_{piezo} + \Delta f_{he} + \Delta f_{tuner} + \Delta f_{event} \text{ — each source separately configurable}$$

IMPLEMENTATION

Timing: one measured clock, all rates derived



Every rate is an integer division of the measured clock:

FIELD UPDATE

$$N_s = \text{round}(f_{\text{app}} / f_{s,\text{req}}), f_s = f_{\text{app}} / N_s$$

MECHANICAL & DAQ

$$f_m = f_{\text{app}} / N_m, T_{\text{DAQ}} = N_d / f_{\text{app}}$$

≈ 100 MHz

application clock, measured in hardware

3.125–10 MS/s

model rate, physical constants preserved

LATENCY, CYCLE-TAGGED

$$T_{\text{int}} = N_{\text{int}} / f_{\text{app}}$$

50 clk period / 510 ns

internal delay, cycle-tagged end to end

16-ch DAQ

full observability of the emulated plant

PIPELINE LIMIT

$$N_s \geq 9 \rightarrow f_s \leq f_{\text{app}} / 9 \approx 11.1 \text{ MS/s}$$

IMPLEMENTATION

Operation: EPICS interface in physical units

- EPICS IOC runs on the card's ARM/Linux — standard accelerator control interface
- Requests in physical units (Hz, μ s); the IOC derives counts and fixed-point coefficients
- Requested vs applied values both reported — a mistyped rate is exposed, not silently applied
- Live signal-flow monitor: every model block observable while running
- 16-channel DAQ for full observability of the emulated plant



EPICS signal-flow monitor (top) and DAQ scope (bottom)

SUMMARY

A reconfigurable cavity stand-in on one MicroTCA card

1 AMC card

complete plant chain, DAQ and EPICS on one Zynq XC7Z045

μ TCA.4 RTM

drop-in analog boundary at the controller's native signals

3.125–10 MS/s

physical time scale preserved at any model rate

8 + detuning model

detuning sources and event models synthesized in real time

Next steps

- Characterize the RTM analog path (gain, flatness, pure delay) → close the converter-level delay budget
- Controller-in-the-loop: closed-loop commissioning experiments through the RTM interface
- Re-parameterize for the 650 MHz main-ring class; multi-cavity stations on the μ TCA fabric

Thank you — questions welcome