Introduction of SOI Pixel Development

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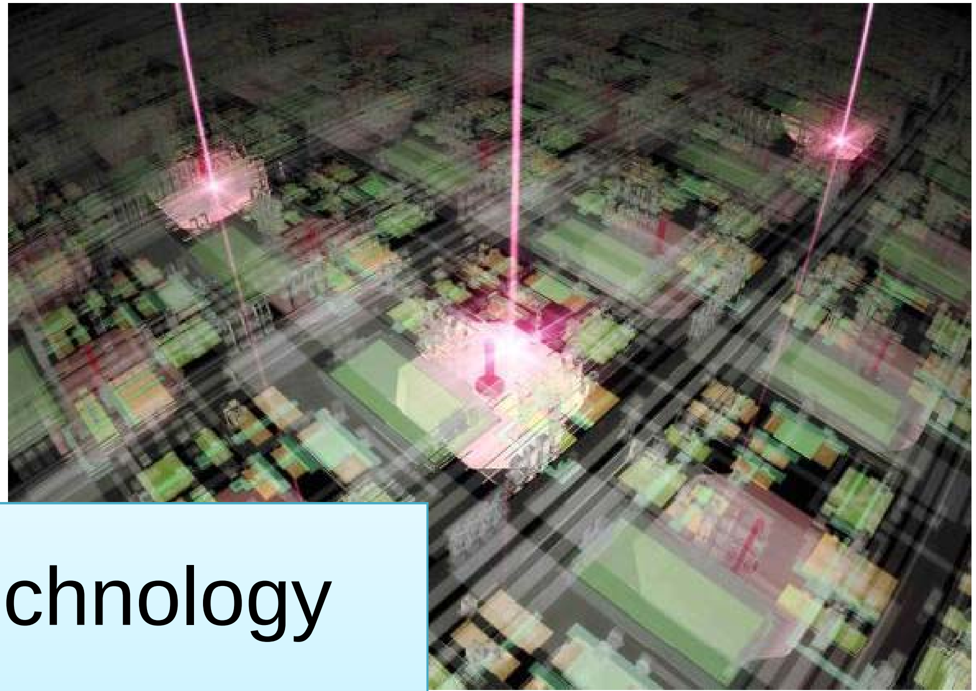
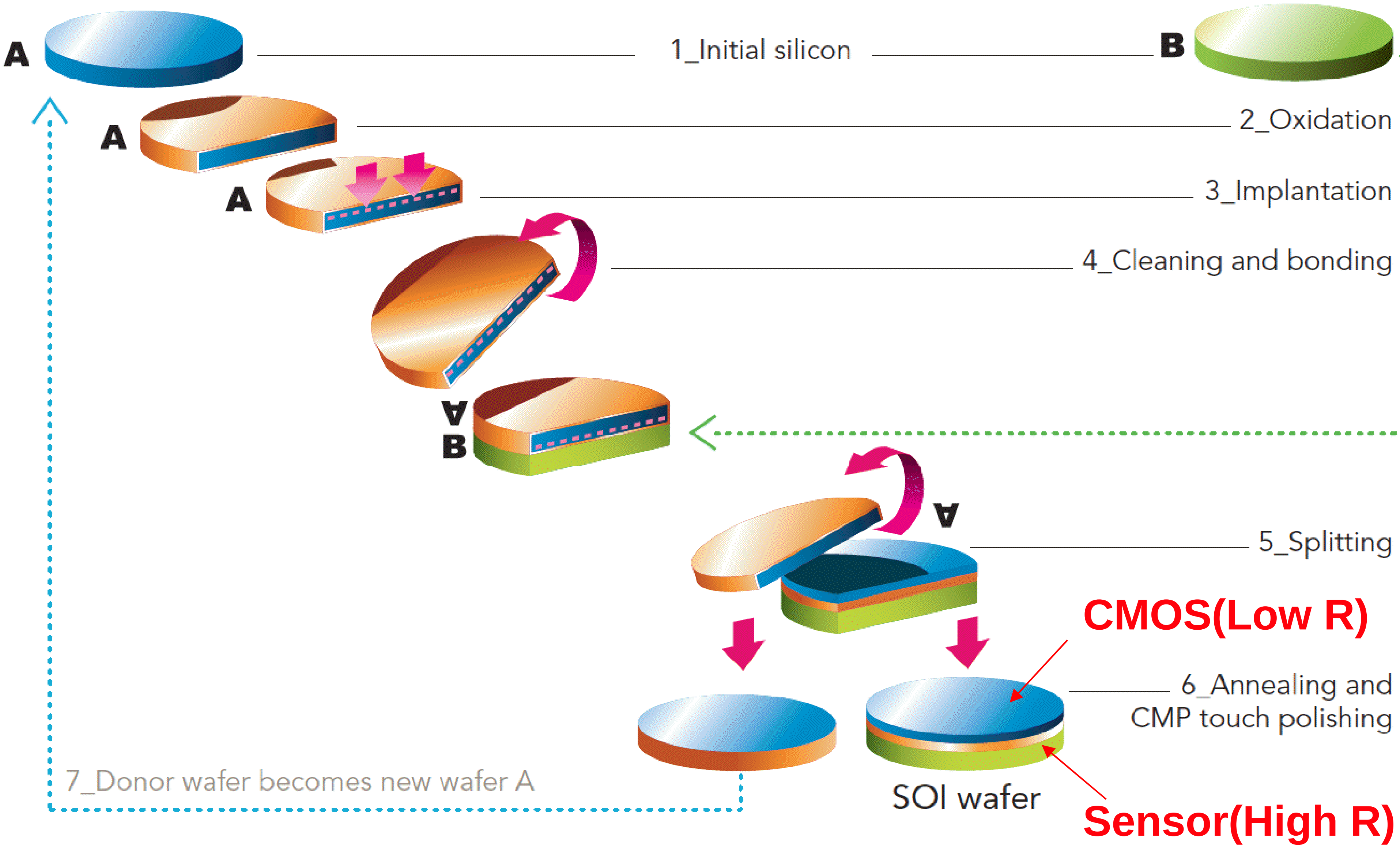
http://rd.kek.jp/project/soi/

OUTLINE

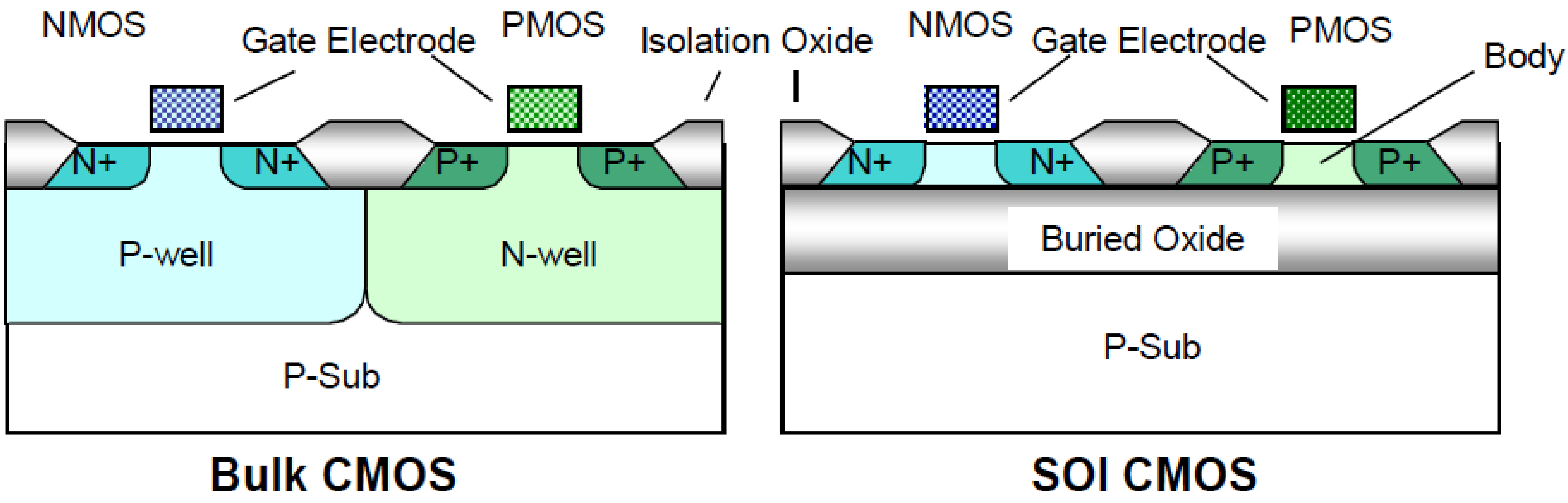


- Introduction of SOI Technology
- SOI Pixel Detector Development
- On-Going R&D’s
- Summary

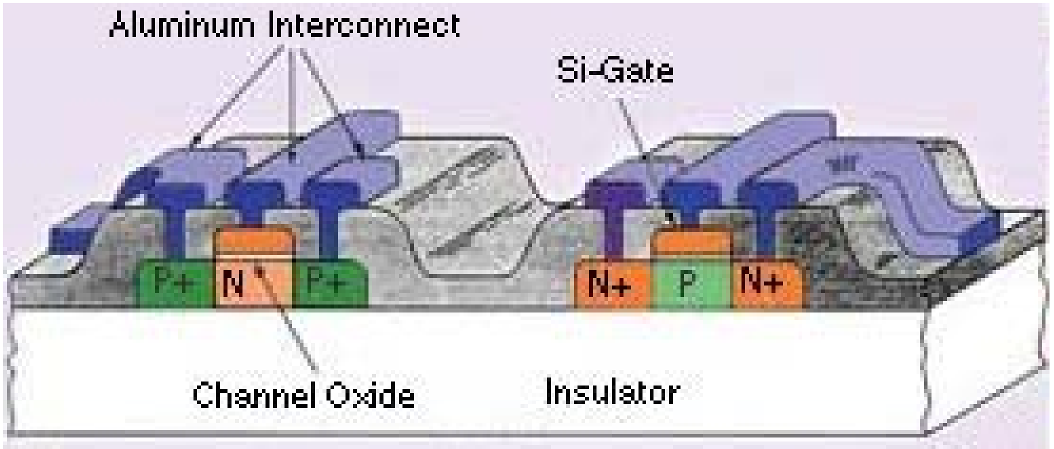
SOI Wafer Production (Smart Cut by SOITEC)



Bulk CMOS vs. SOI CMOS

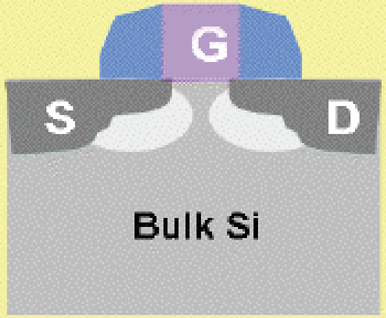


In SOI, Each Device is completely isolated by Oxide.



Industry move : Bulk CMOS to PD-/FD- SOI CMOS

Bulk Transistor

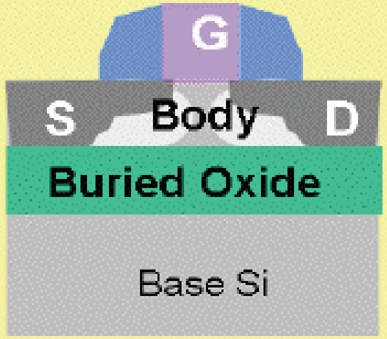


Channel
Forms in
Bulk Silicon

Faces many barriers to further miniaturization

Partially-Depleted

PD-SOI Transistor



Body
is Partially Depleted
and 'floats' independent
from Bulk substrate

Floating Body
boosts performance
but introduces
some peculiarities
(History Effect, kink)

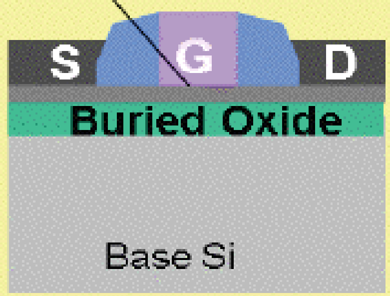
Tsi ~ 70nm . Tbox ~ 145nm

Our SOI

Fully-Depleted

FD-SOI Transistor

Ultra-Thin Body (undoped)



Ultra-Thin Body
is Fully Depleted

Box can optionally be
ultra-thin, too

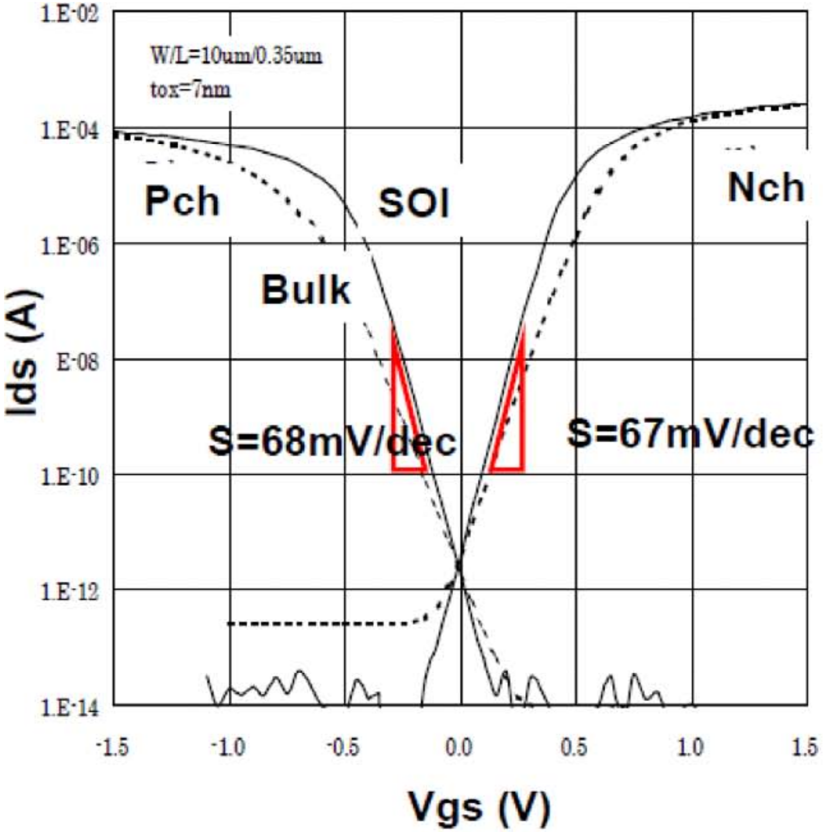
Addresses scalability issues

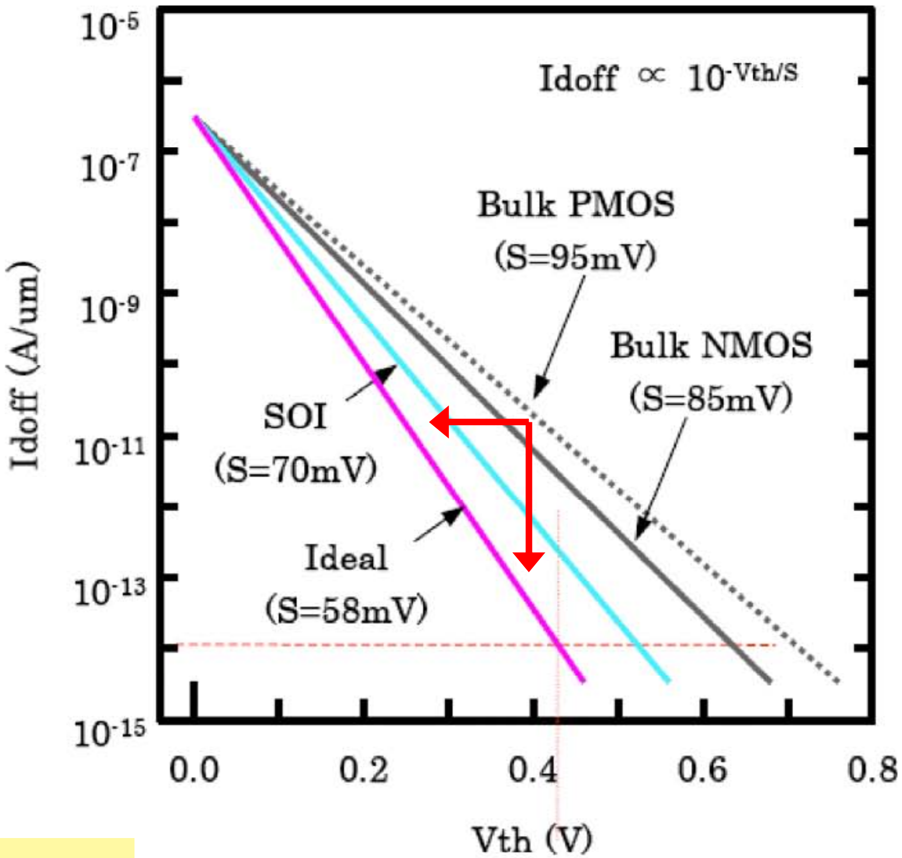
No History Effect
No kink effect

Tsi ~5-10nm (e/o process)
Tbox ~ 145nm / Tutbox ~ 10-30nm

(from "Fully DepletedSOI", Xavior Cauchy, SOI Industry Consortium)

Steep Sub Threshold Slope



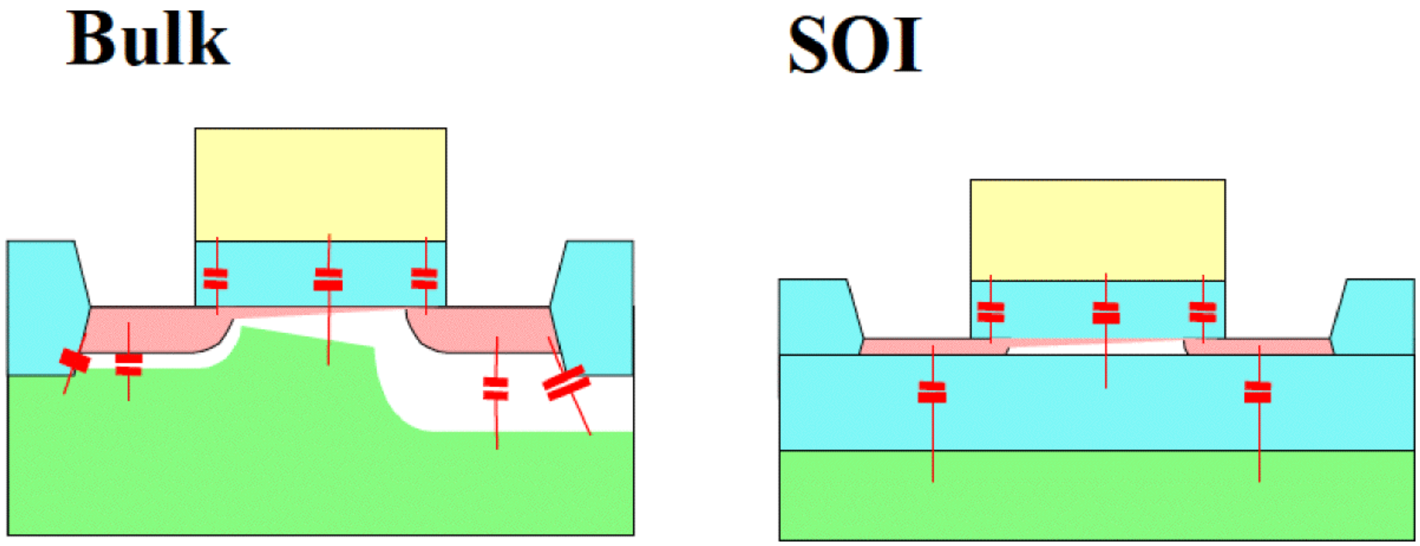


F.Ichikawa et al., SSDM, 2004

Gate voltage is not wasted to deplete the bulk.

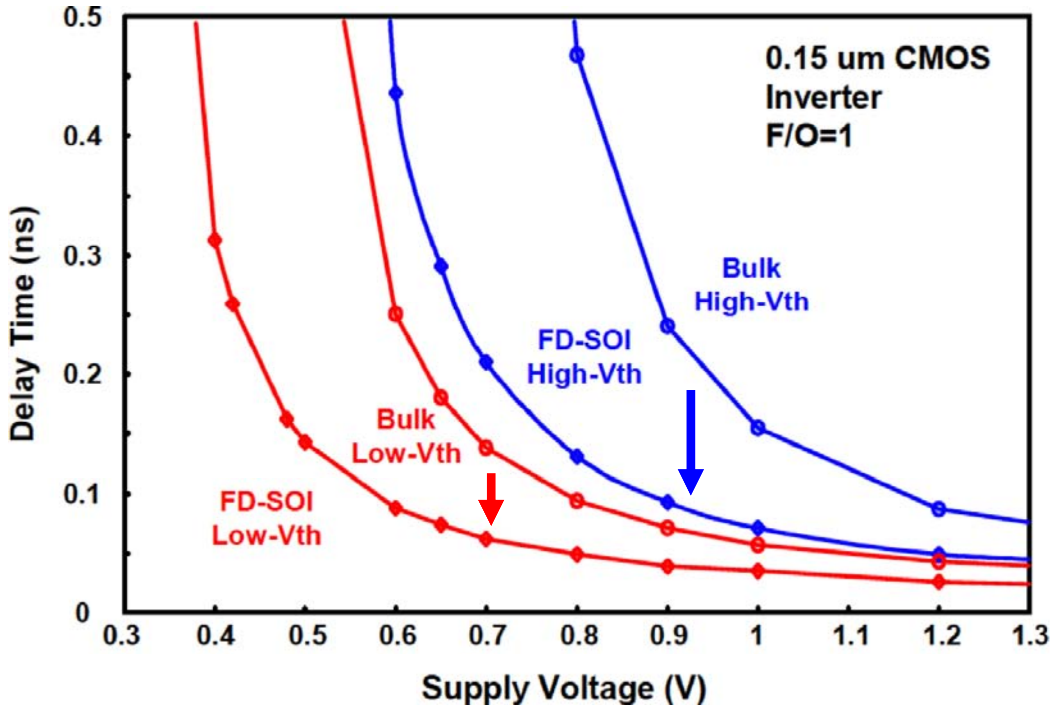
Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).

SOI Performance : Smaller Junction Capacitance



Cj is 1/10 of Bulk technology.

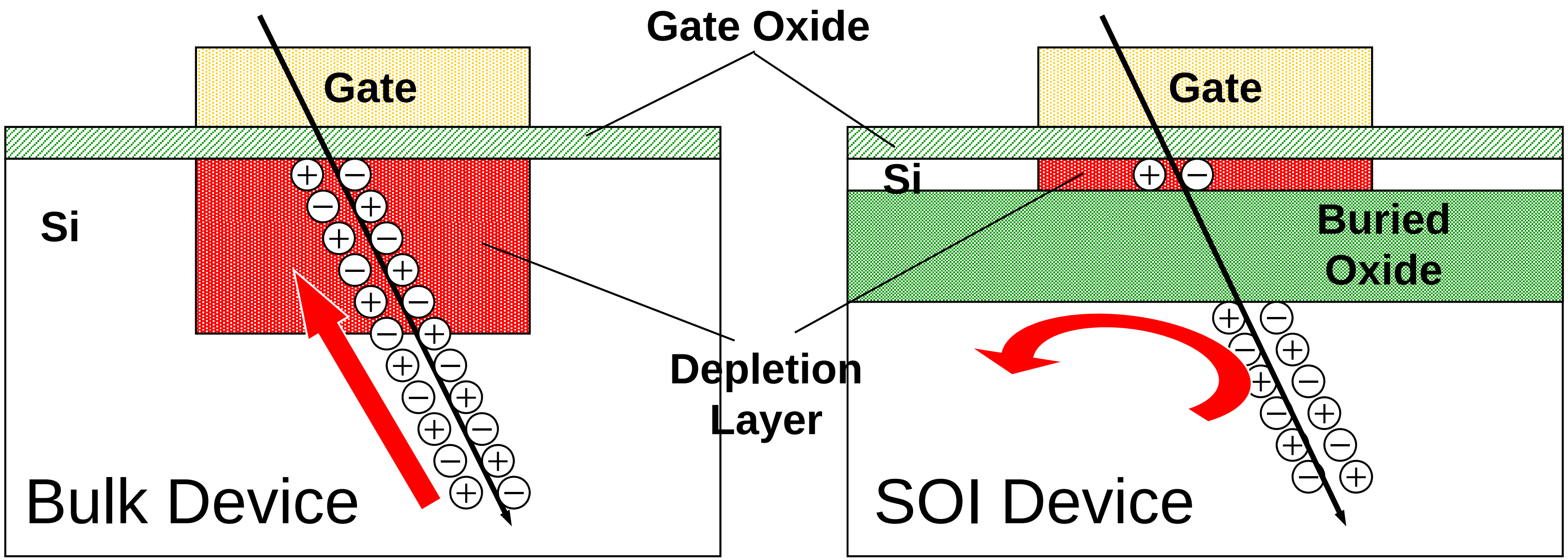
Gate Capacitance is 30-40% Lower.



High Speed / Low Power

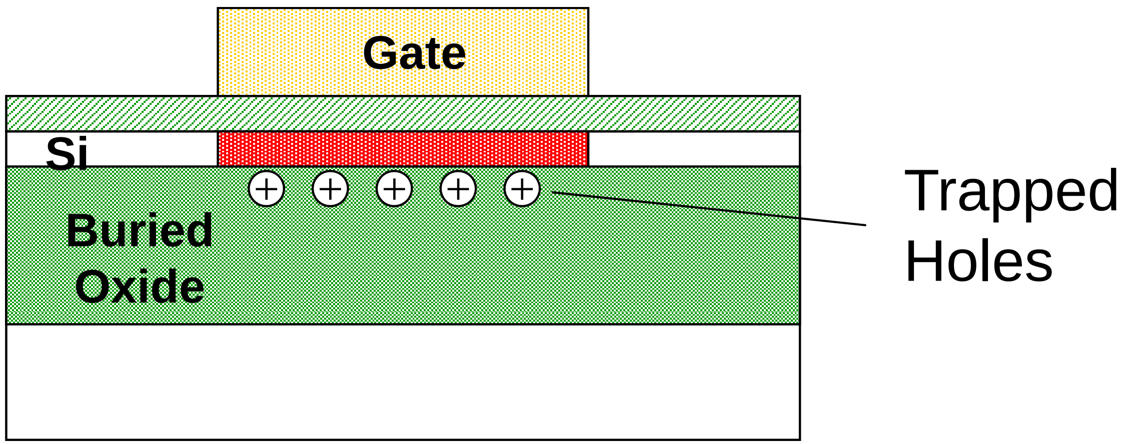
Radiation Tolerance

SOI is Immune to Single Event Effect

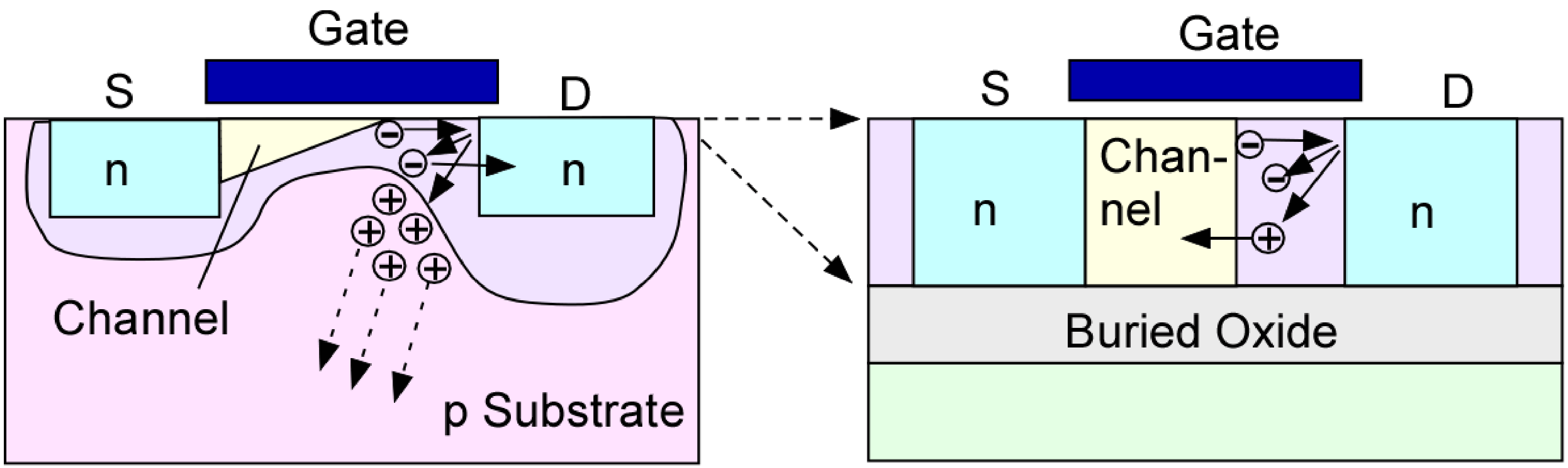


But not necessary strong to Total Ionization Dose due to thick BOX layer

This must be remedy for the application under high radiation environment.



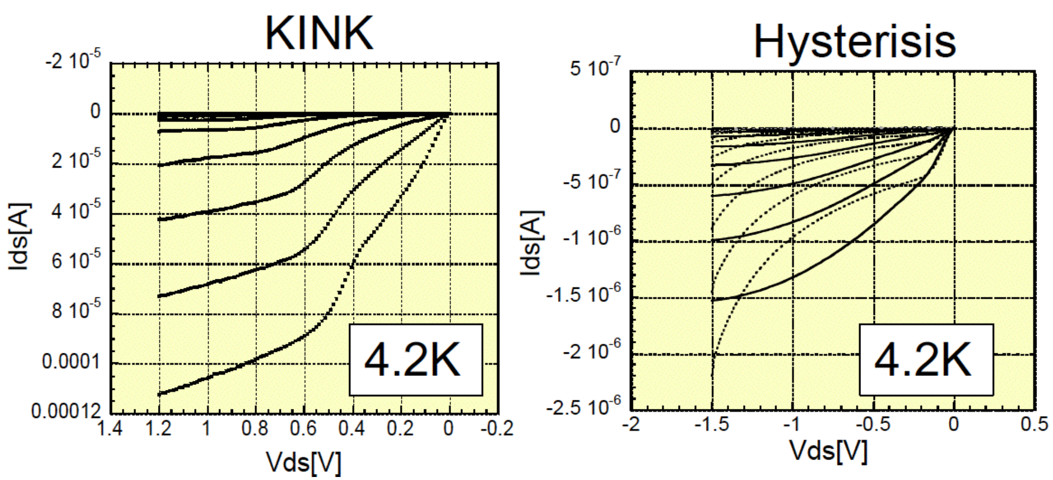
Operation at Cryogenic Temperature

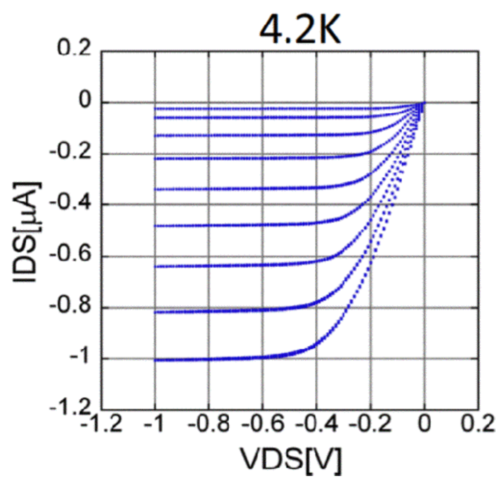


Bulk MOS

4.2K

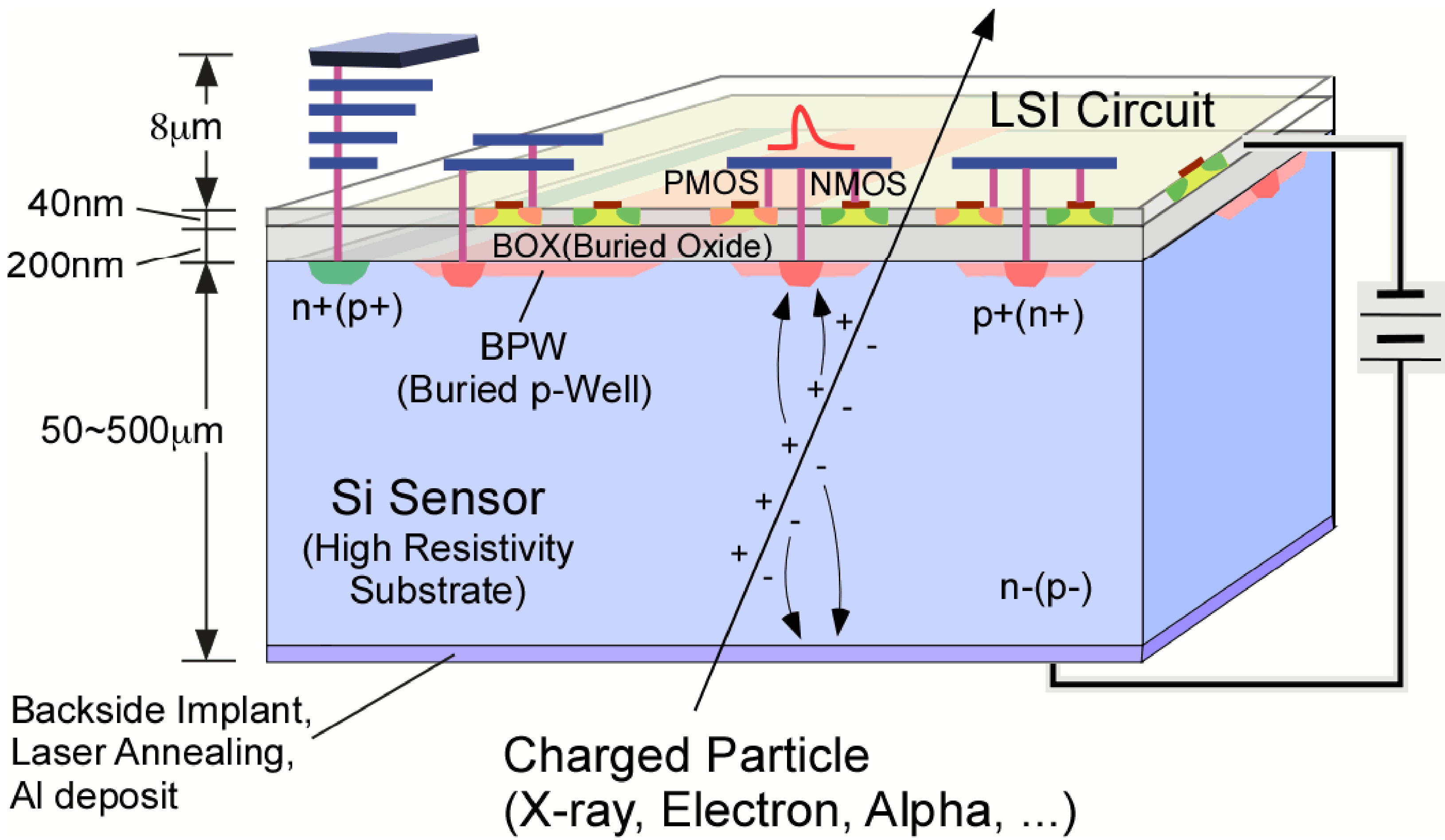
SOI MOS
(worked in 1.4K)





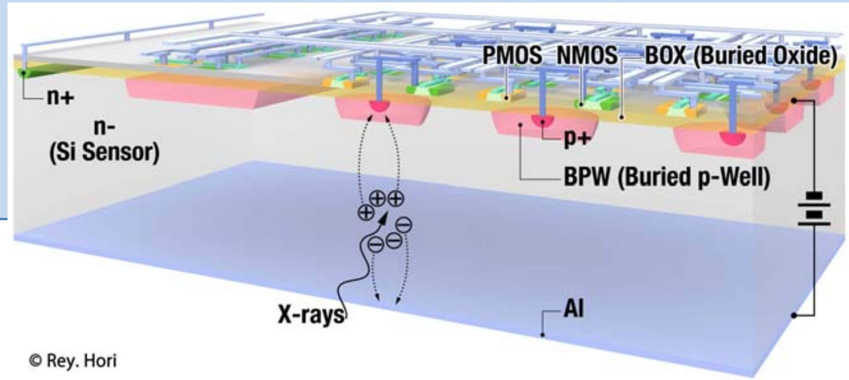
SOI Pixel Detector (SOIPIX)

Monolithic Detector having fine resolution of silicon and data processing power of CMOS LSI by using Silicon-On-Insulator (SOI) Technology.



Feature of SOI Pixel Detector

- No mechanical bonding. Fabricated with semiconductor process only, so high reliability, low cost are expected.
- Fully depleted thick sensing region with Low sense node capacitance.
- On Pixel processing with CMOS transistors.
- Can be operated in wide temperature (4K-570K) range, and has low single event cross section.
- Based on Industry Standard Technology.

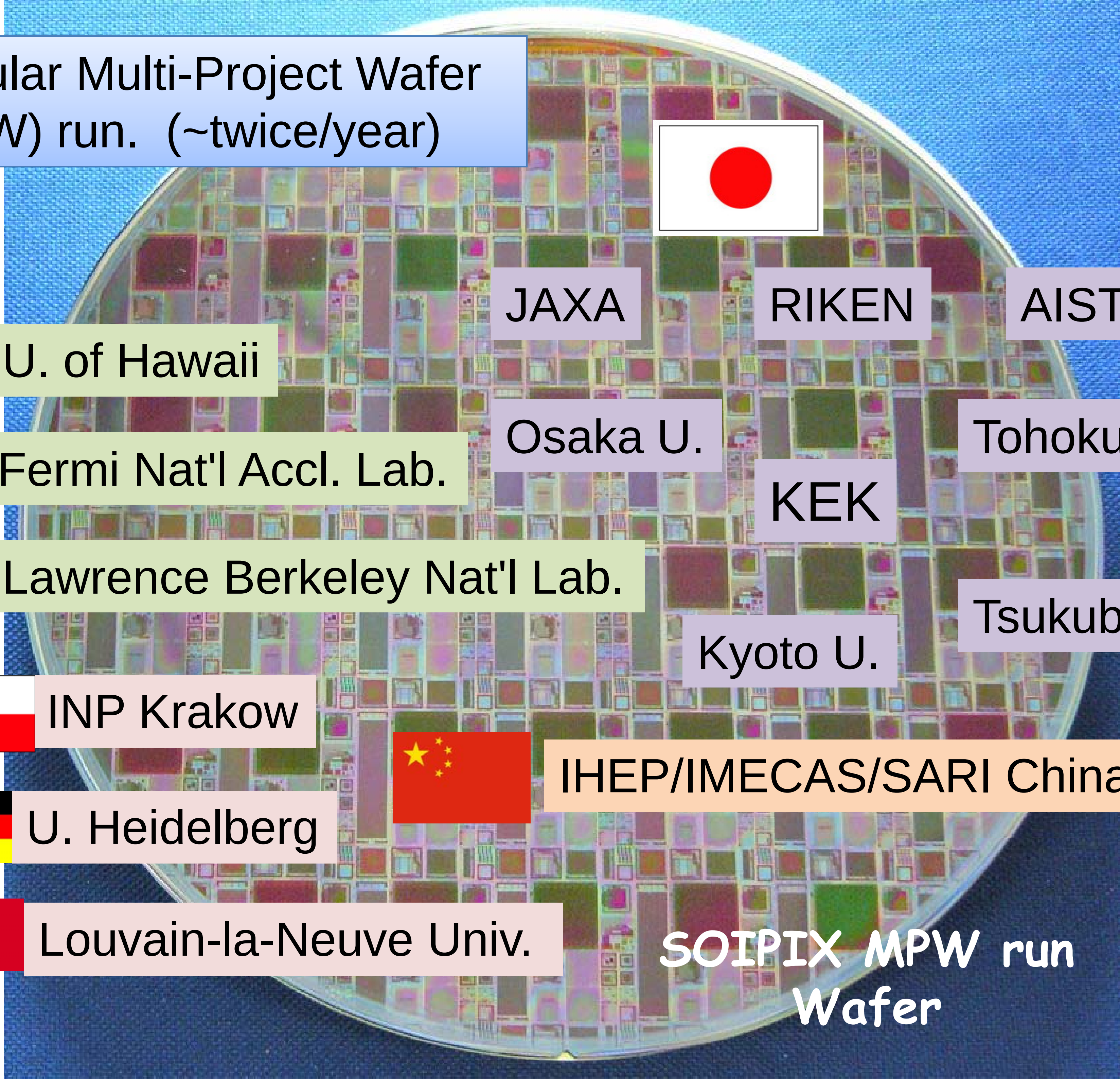


Lapis (*) Semiconductor 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) >1 k Ω-cm, FZ(p) >1 k Ω-cm
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

(*) Former OKI Semiconductor Co. Ltd.

Regular Multi-Project Wafer (MPW) run. (~twice/year)

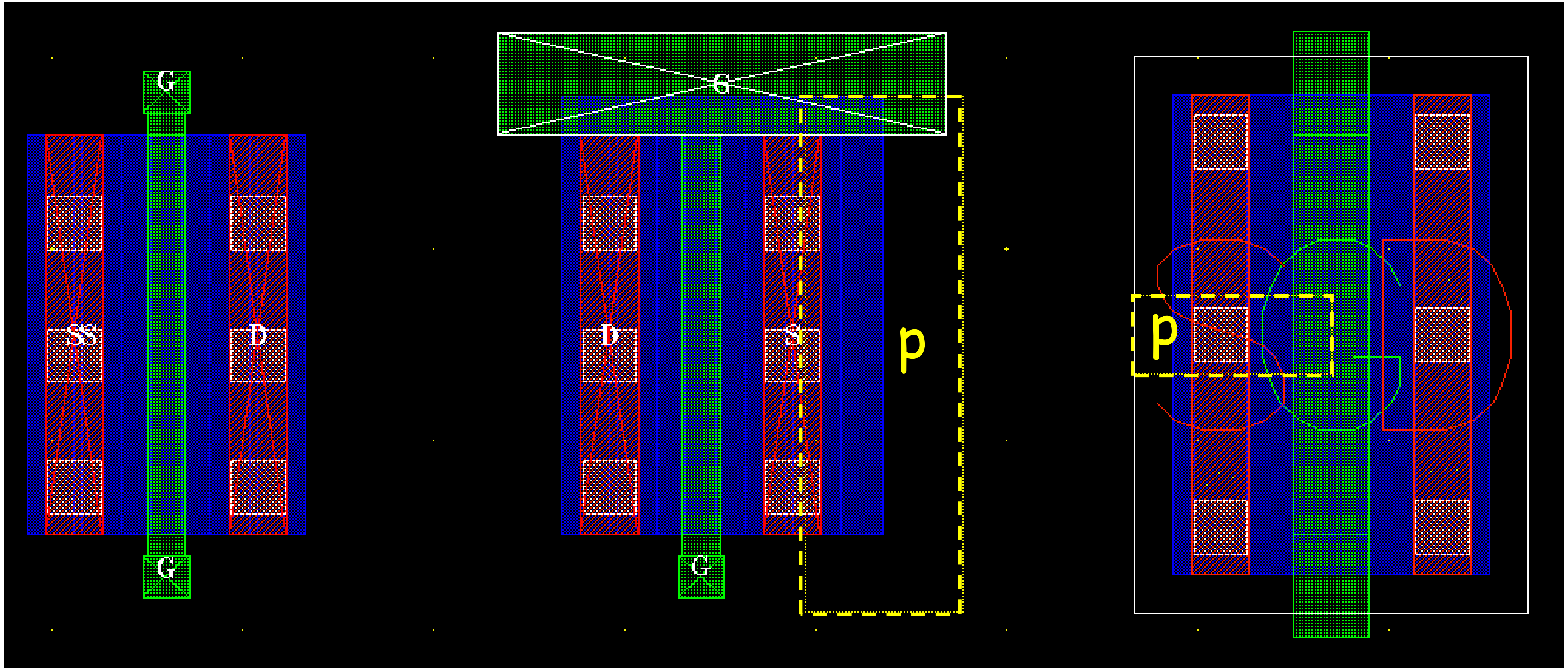


Submission from Chinese Coleague

- 2013.1 MX1594
  IHEP (Lu Yunpeng) 6x6 mm^2 + 2.9x2.9 mm^2
  SARI (Ning, Wang, Li Tian) 2.9x2.9 mm^2
- 2012.7 MX1542
  IMECAS(Zhao Kai) 12.2x12.2 mm^2 + 2.9x2.9mm2
- 2011.10 MX1501
  IHEP (Liu Gang, Lei Fan) 2.9x2.9 mm^2
  IHEP (Lu Yunpeng) 2.9x2.9mm^2
- 2011.1 MX1442
  IHEP(Liu Gang) 2.4x2.4mm^2
- 2010.8 MX1413
  IHEP(Zheng Wang, Lei Fan) 2.4x2.4 mm^2 x2

Transistor Type

Core Transistor (1.8V) : Normal Vth & Low Vth
I/O Transistor (3.3V) : Normal Vth & High Vth



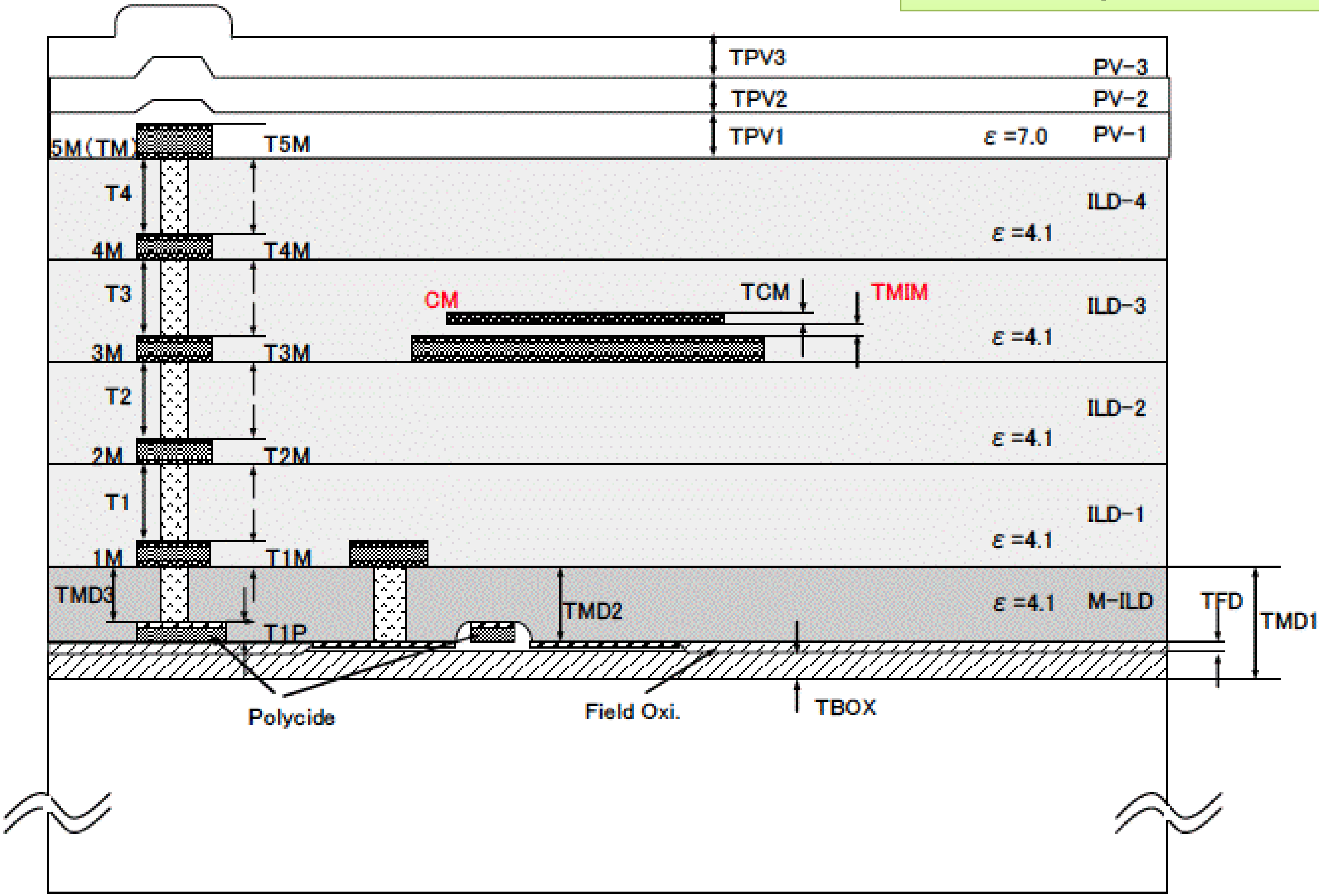
Body Floating

Source-Tie (Type 1)

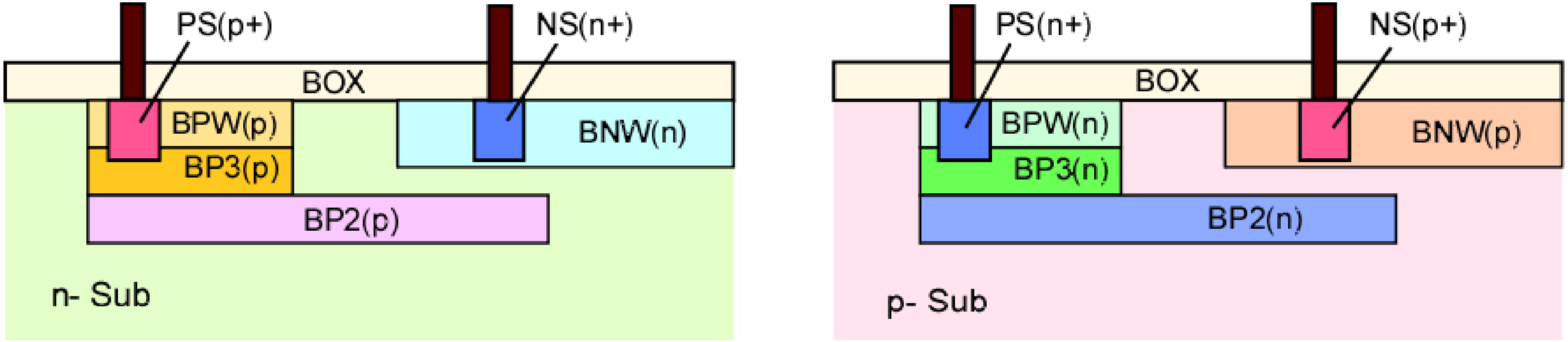
Source-Tie (Type 2)

Structure of Top Si

1 Poly + 5 Metal
MIM Capacitor on 3M



Sensor Structure



Normal Process for n- substrate

Reverse Process for p- substrate

- PS & NS --- High Doping Density Layer (Top Si is removed)
- BPW, BP2, BP3 & BNW --- Low Doping Density Layer (Top Si is not removed)

Trace Fuse (option)

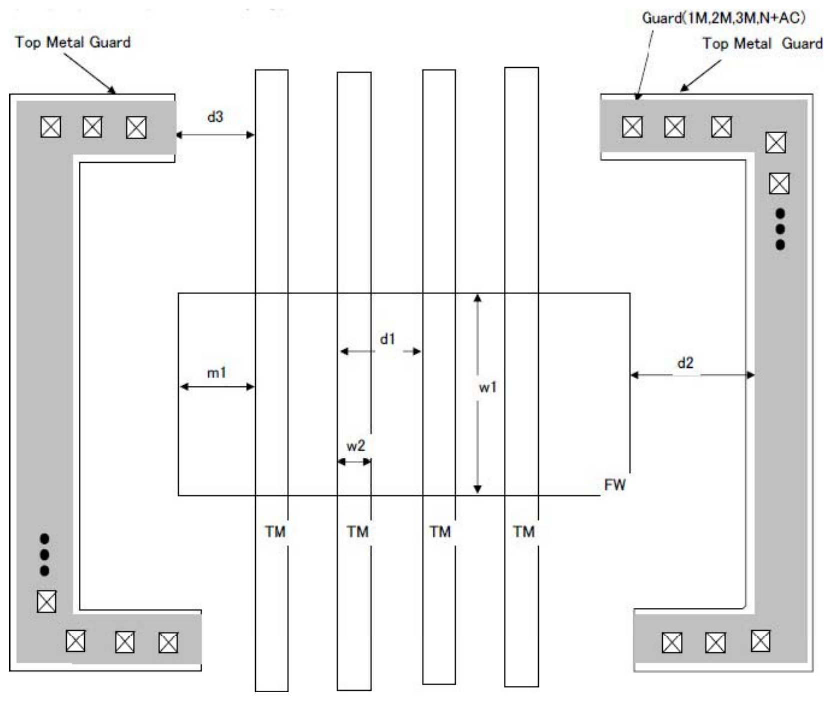
You can chase the chip location where it come from if you include this fuse in your design.

Number of Fuse (total 16 lines)

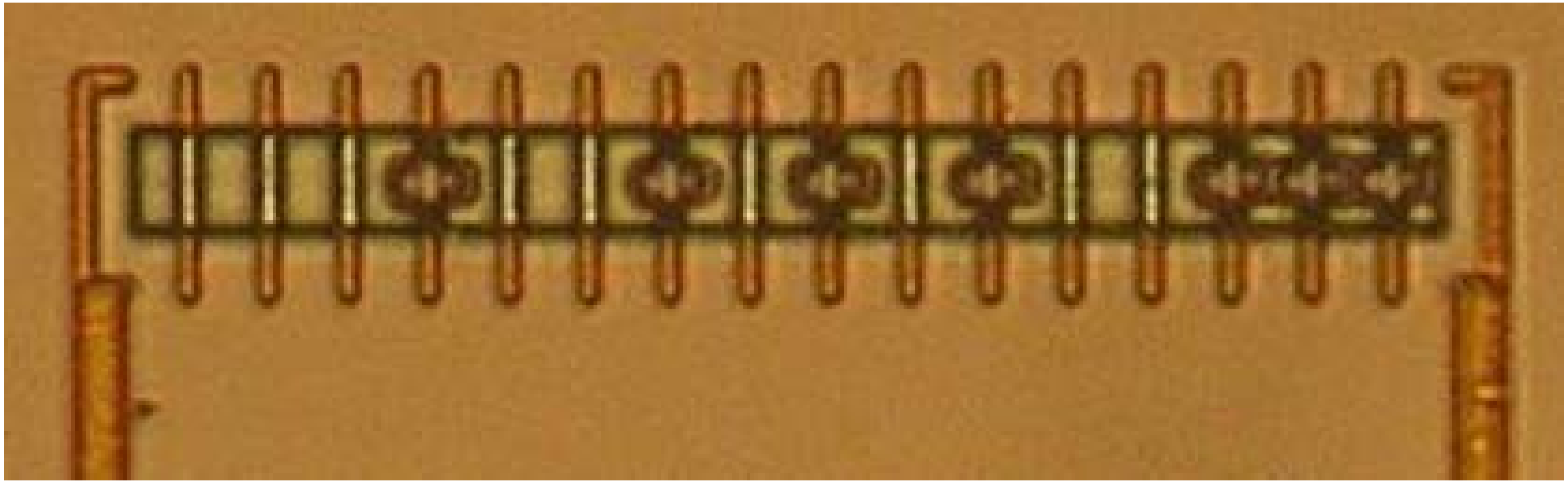
* Lot No. : 4 lines (1~15)

* Wafer No. : 5 lines (1~31)

* Chip Location in wafer : 7 lines (1~127)



Laser Cut

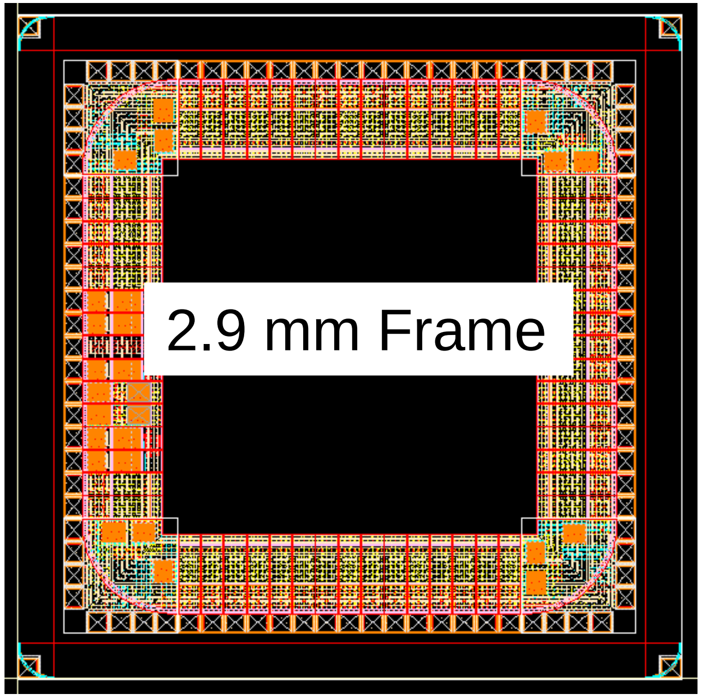


I/O Cell Libraries

We prepared several I/O frames for your convenience.

Chip Frame for Pixel

I/O Buffers
+ Vdet ring
+ Vbias ring
+ BPW



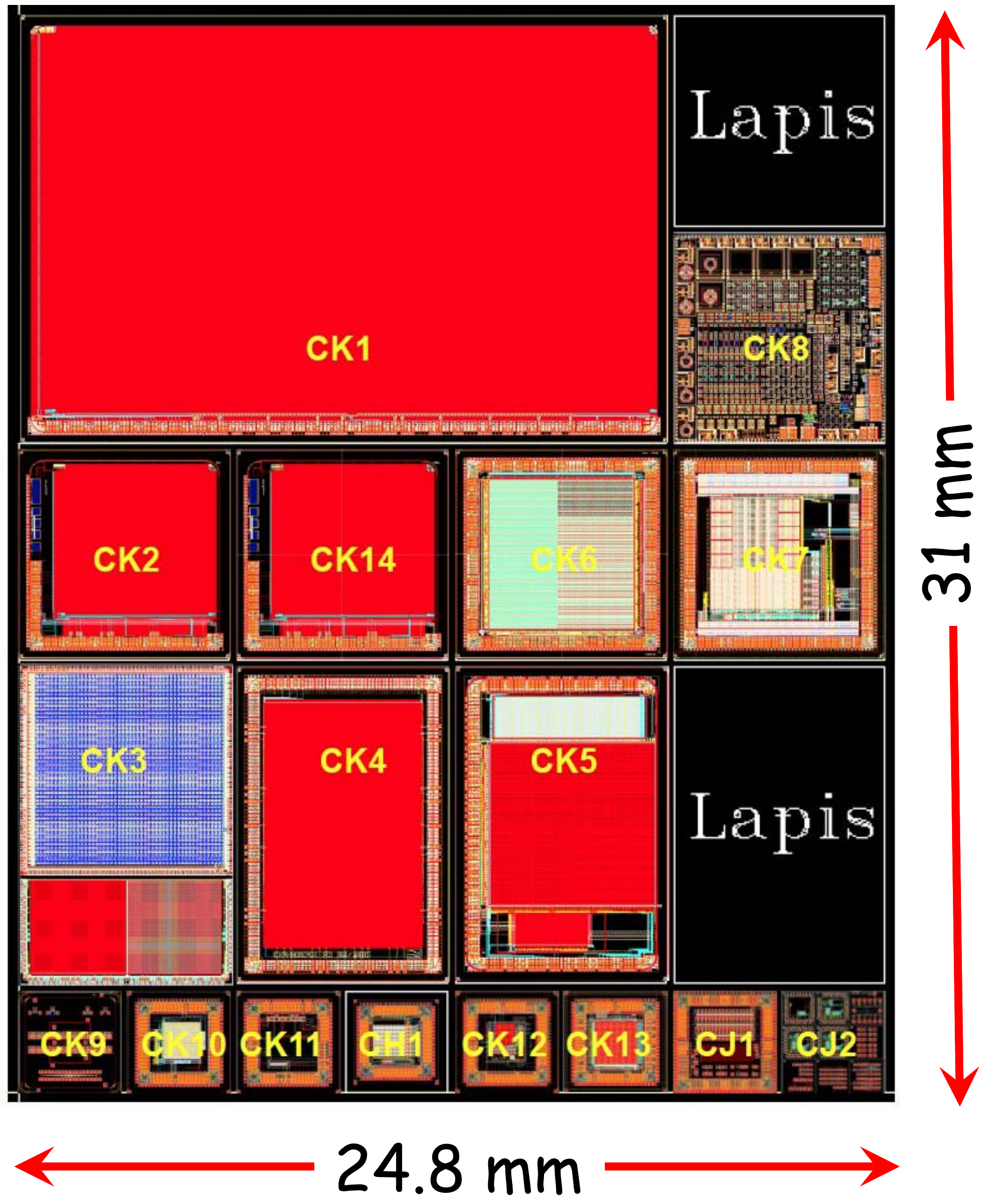
Lapis Library	KEK IOLIB5M3	Comment
S02_IT4N_2_5M	ioIT4N_5M2	Digital Input Buffer
S02_OT4A_2_5M	ioOT4A_5M2	Digital Output Buffer
S02_VDD33_5M	ioVDD33_5M3	3.3 V Power
S02_VDD18_5M	ioVDD18_5M3	1.8V Power
S02_VSS_5M	ioVSS_5M3	Ground
S02_CORNER_VER2_5M	ioCORNER_5M2	Corner Cell
	iodr_5M2	Analog pad with protection diodes and resistor
	iod_5M2, iod_5M3	Analog pad with protection diodes
	iothr_5M2	Direct analog pad
	iobuf_5M2	Digital bidirectional Input/Output Buffer
	ioring29_5M3	IO ring for 2.9mm chip
	ioring29L2_5M3	IO ring for 2.9mm chip with 200um bias spacing for pixel (new)
	ioring60_5M3	IO ring for 6.0 mm chip
	ioring60L2_5M3	IO ring for 6.0 mm chip with 200um bias spacing for pixel
	LVDSDRV_00	LVDS Driver
	LVDSRCV_00R	LVDS Receiver with 100 Ohm terminator
	LVDSRCV_01	LVDS Receiver without terminator
	LVDSBIAS_oo	LVDS Bias Circuit
	io_lvds	LVDS cells layout example
	io_AOBUF33EN_5M3	Analog output buffer
	ioBIAS33_5M3	Analog buffer bias circuit
	io_aobuf	Analog buffer layout example

We get minimum number of I/O cells from Lapis.
Then we have created many more for users.

Please provide us your I/O cells if you develop new one.

Mask

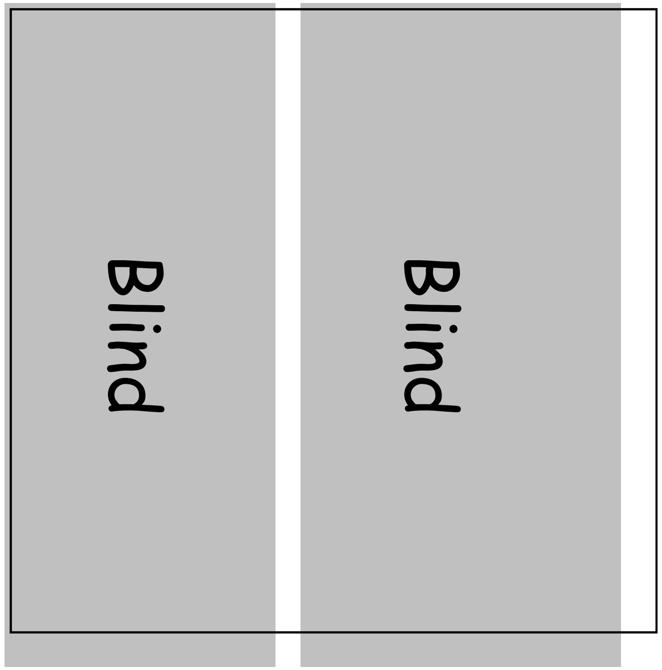
- We are using relatively large mask to enable many designs and large sensors
- Low cost per area.
- Smallest chip area : 2.9 x 2.9 mm^2

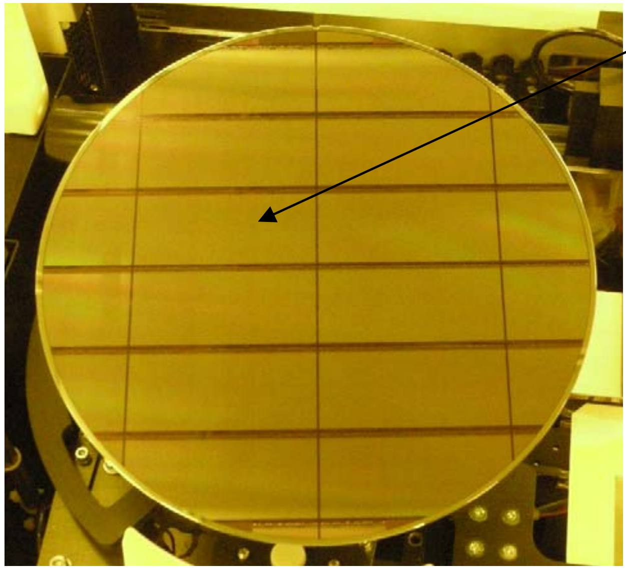


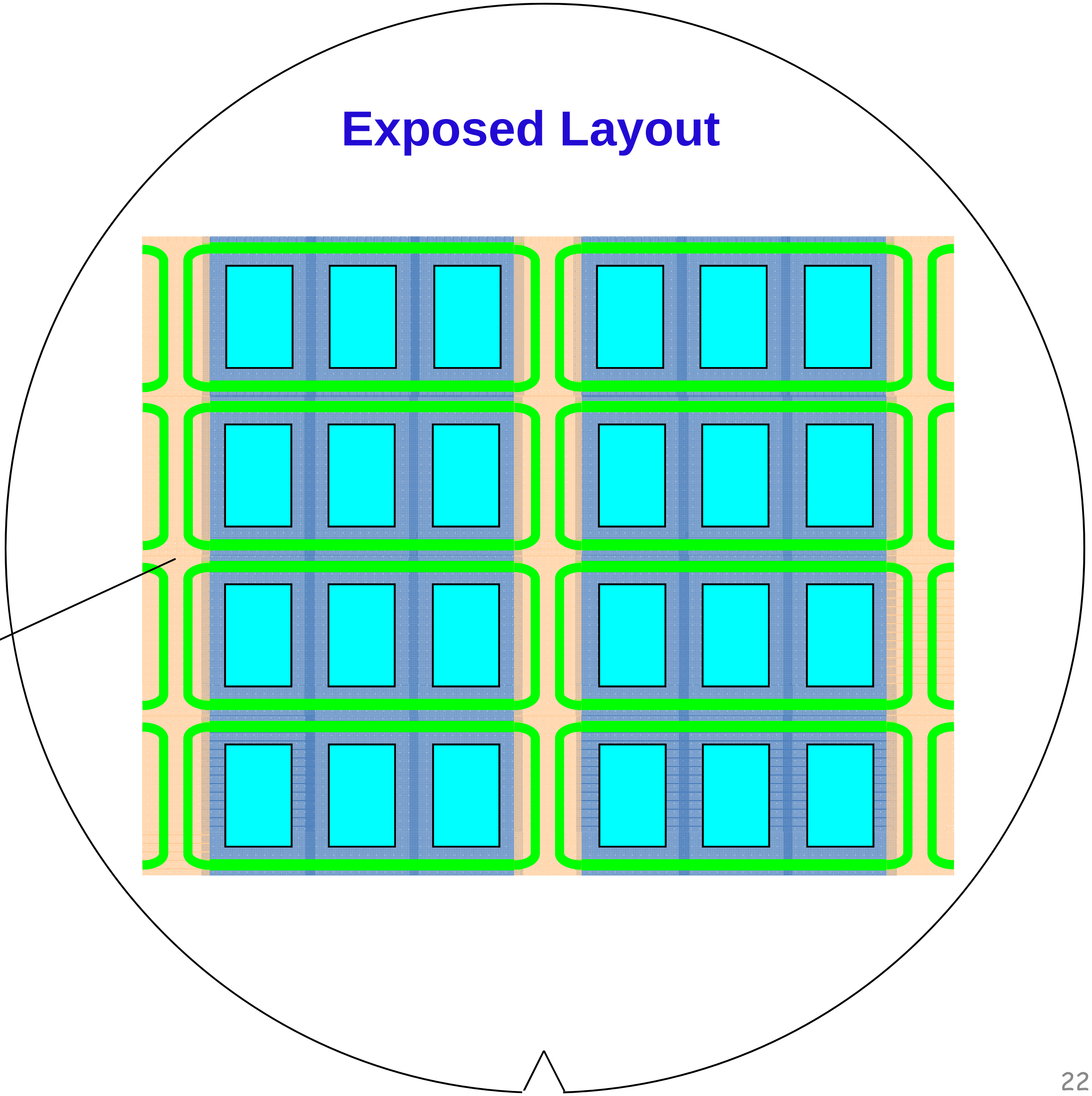
Stitching Exposure

If you want much larger detector …

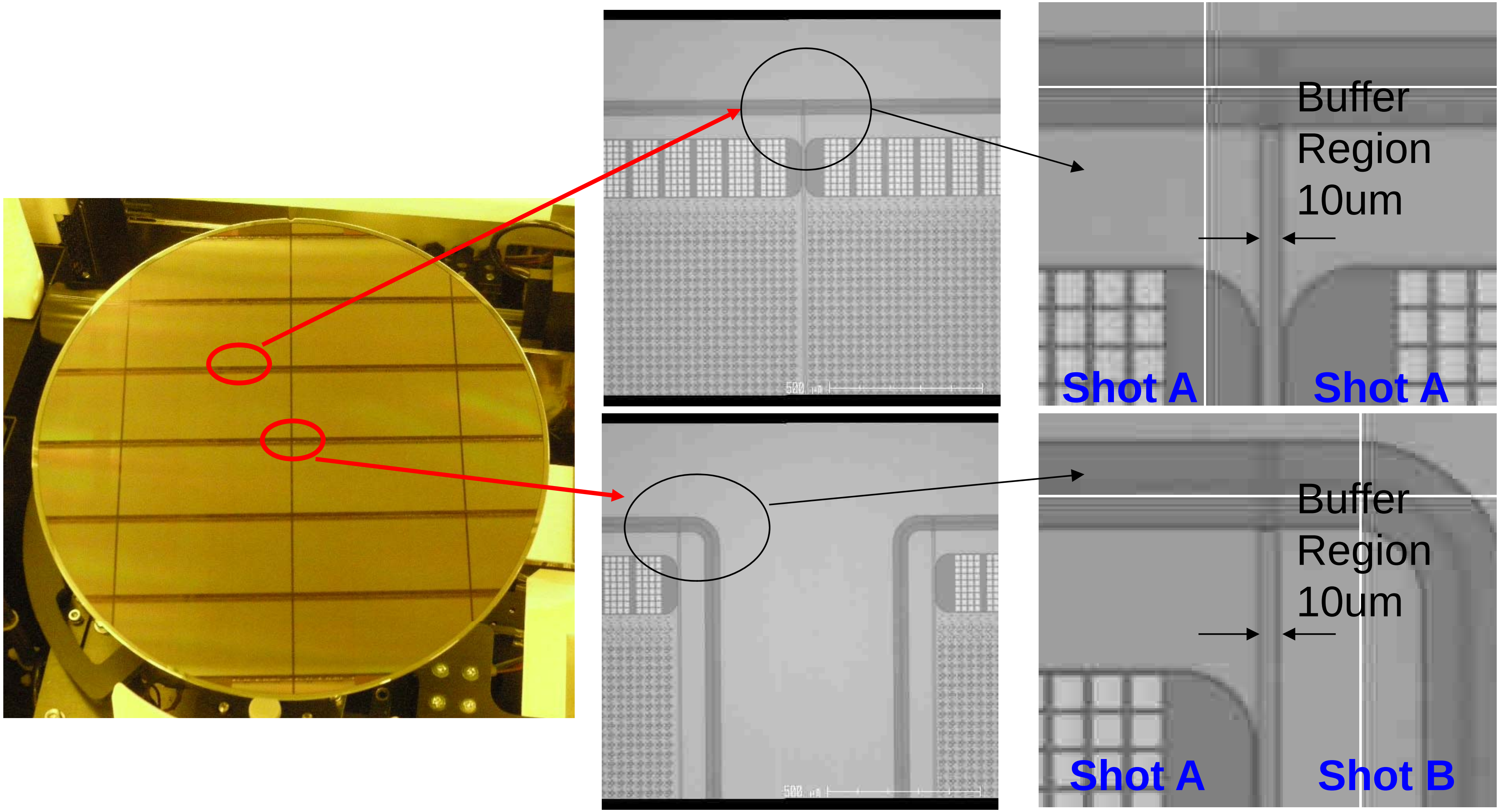
Mask Layout







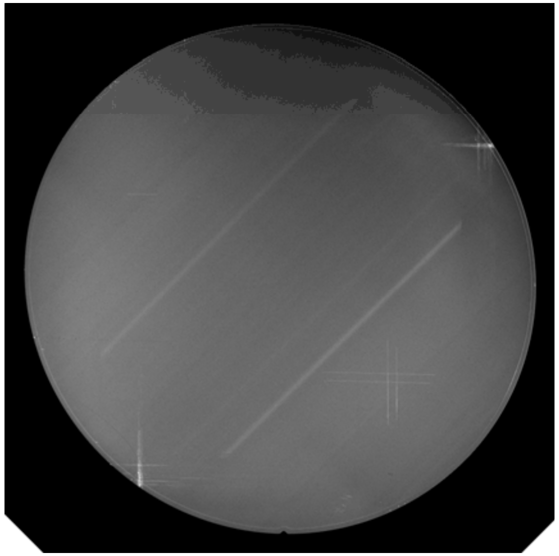
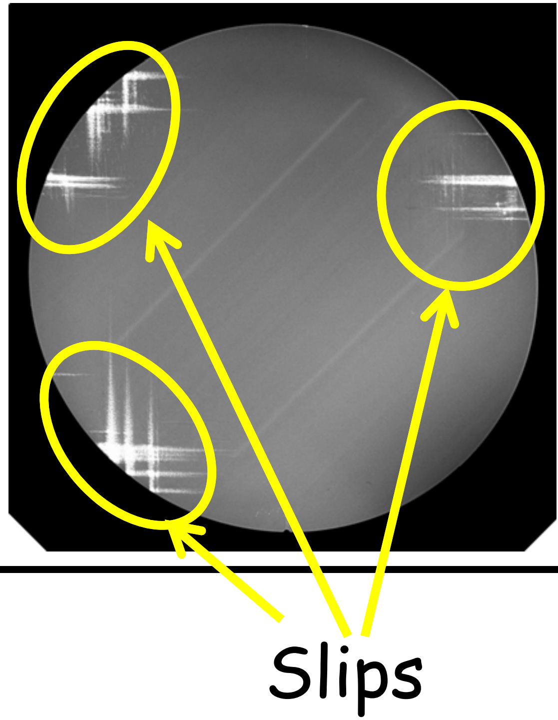
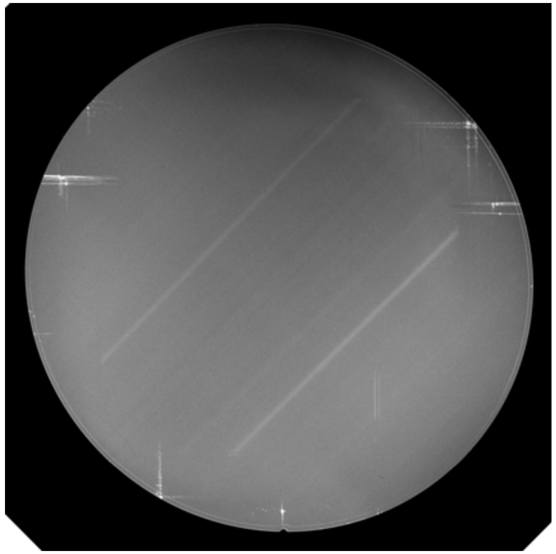
Riken SOPHIAS detector



- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.

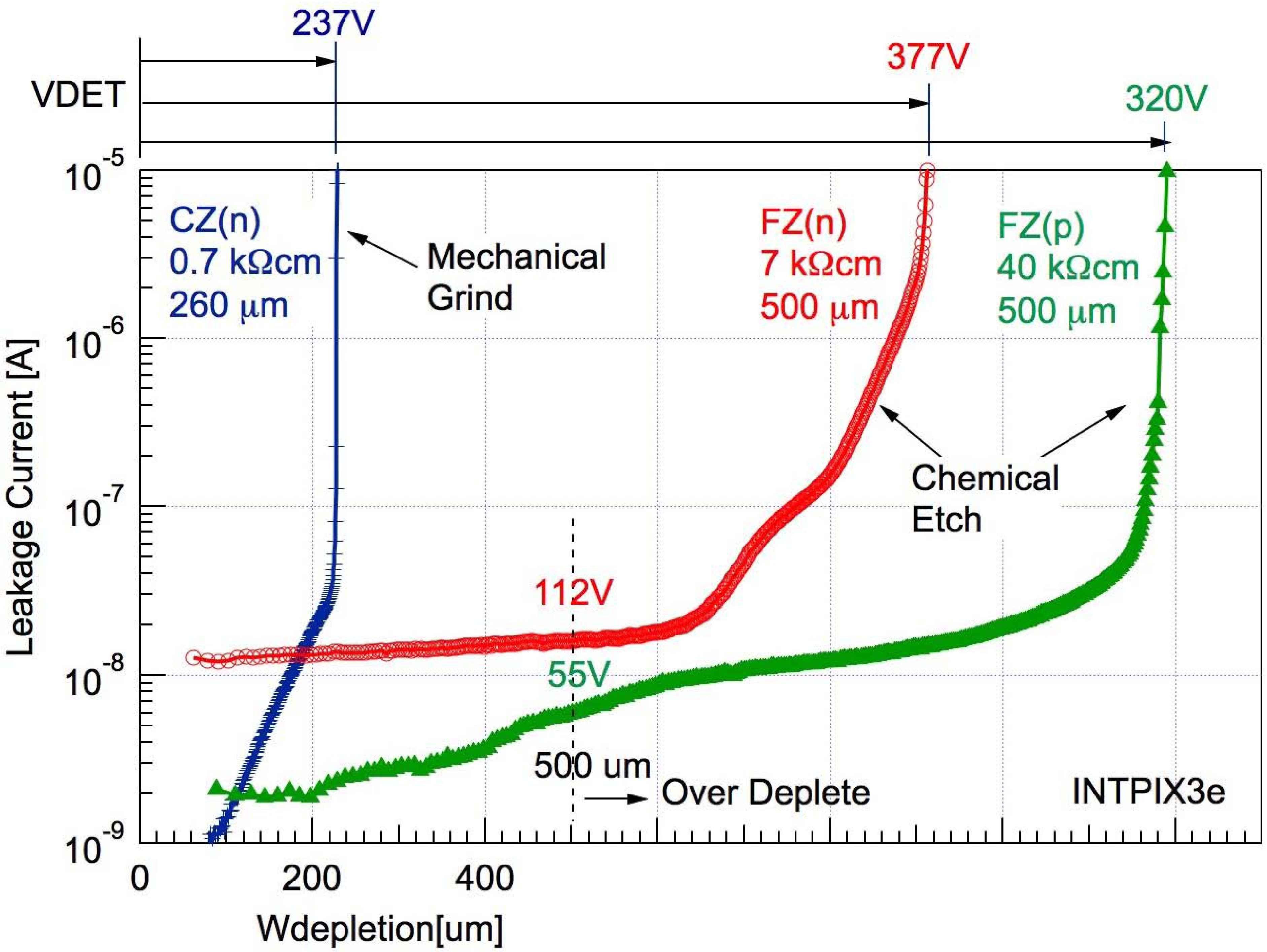
FZ(p and n) SOI Wafer

It was difficult to process 8” FZ-SOI wafer in CMOS process.

Before Oxidation	Conventional SOI Process	Improved SOI Process
		

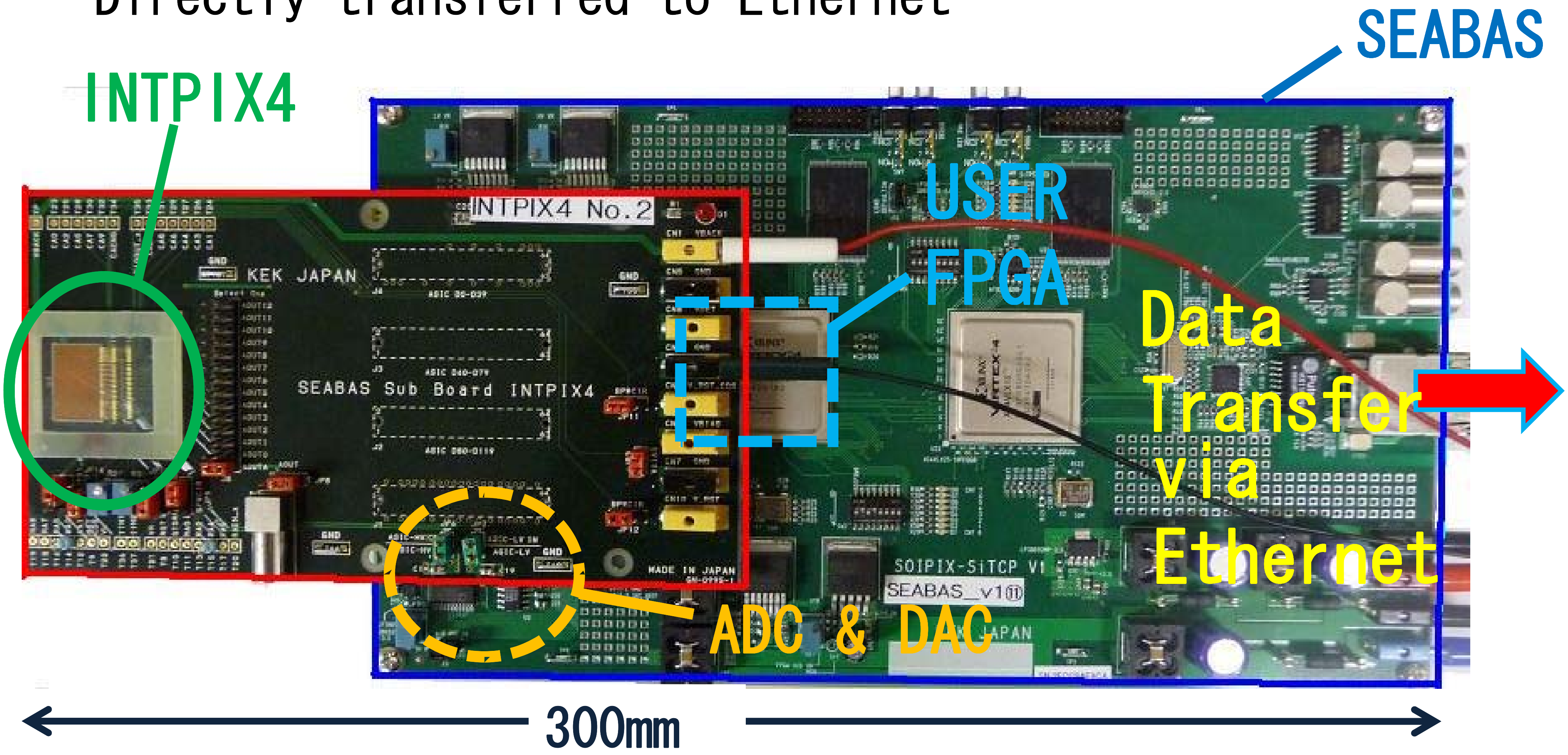
We optimized the process parameters, and succeeded to perform the process without creating many slips.

High Resistive wafers



Data Acquisition Board

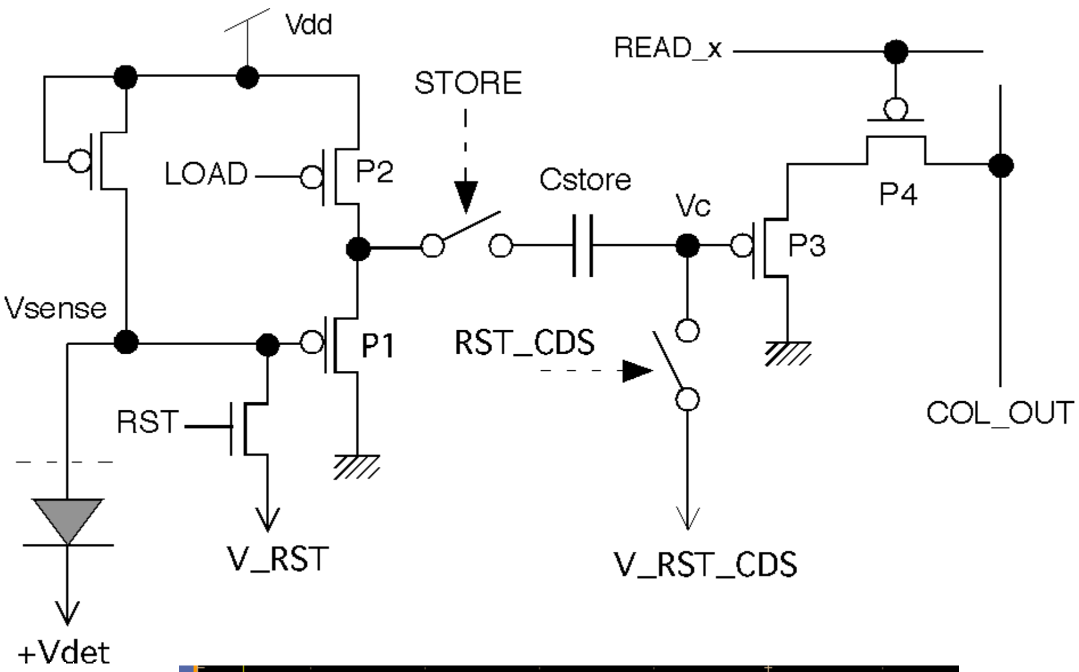
- Soi EvAluation BoArd with Sitcp(SEABAS)
- A FPGA controls the SOI Pixel chip
- Directly transferred to Ethernet

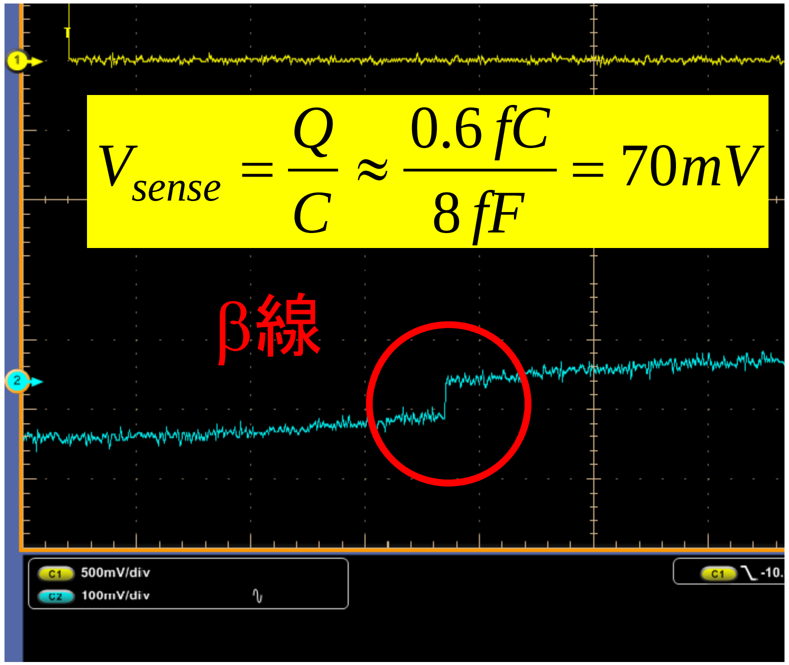


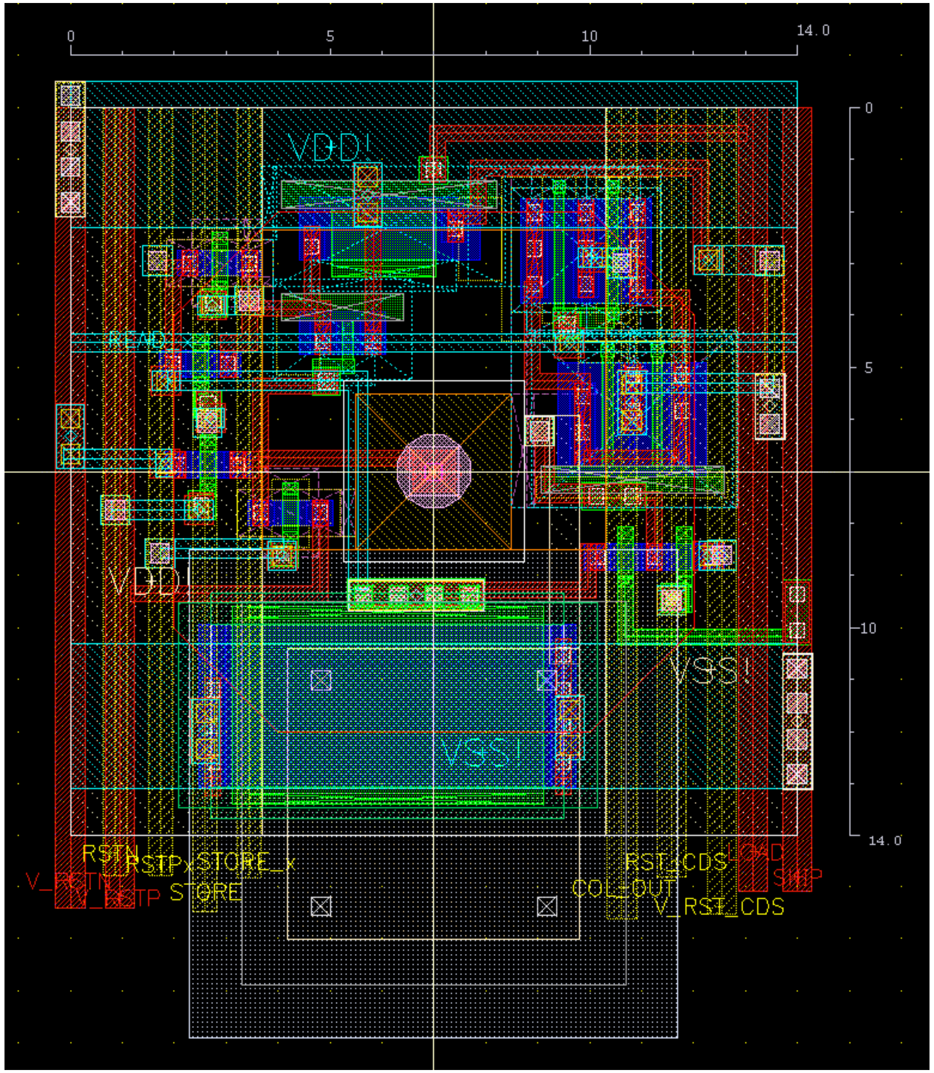
On-Going SOI Projects in Japan

- INTPIX : Genera Purpose Integration Type
- CNTPIX : General Purpose Counting Type
- SOPHIAS : Large Dynamic Range for XFEL
- PIXOR : Belle II Vertex Detector
- XRPIX : X-ray Astronomy in Satellite
- MALPIX : TOF Imaging Mass Spectrometer
- TDIPIX : Contamination Inspection
- LHDPIX : Nuclear Fusion Plasma X-ray
- ...

Integration Type Pixel (INTPIX)

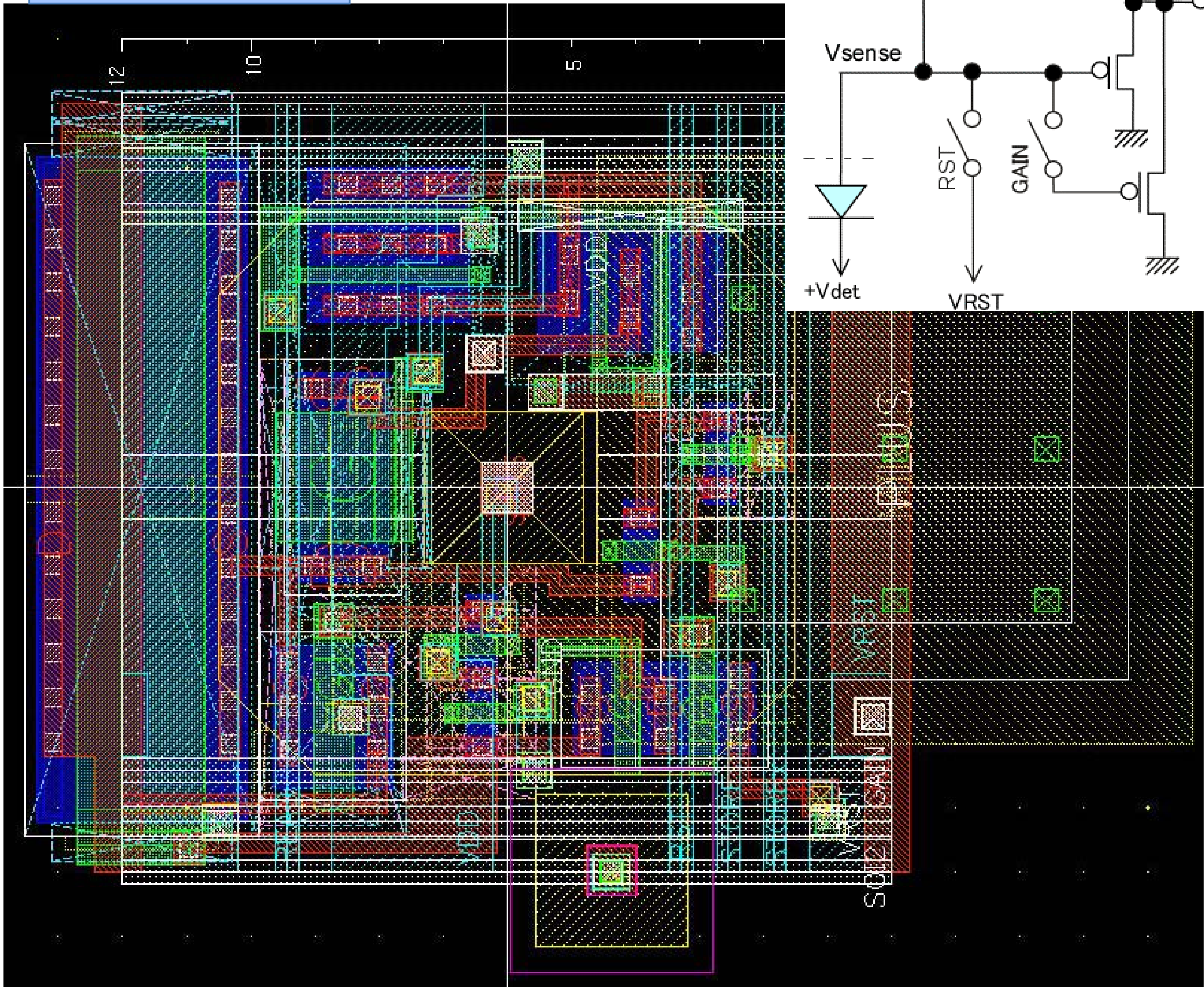


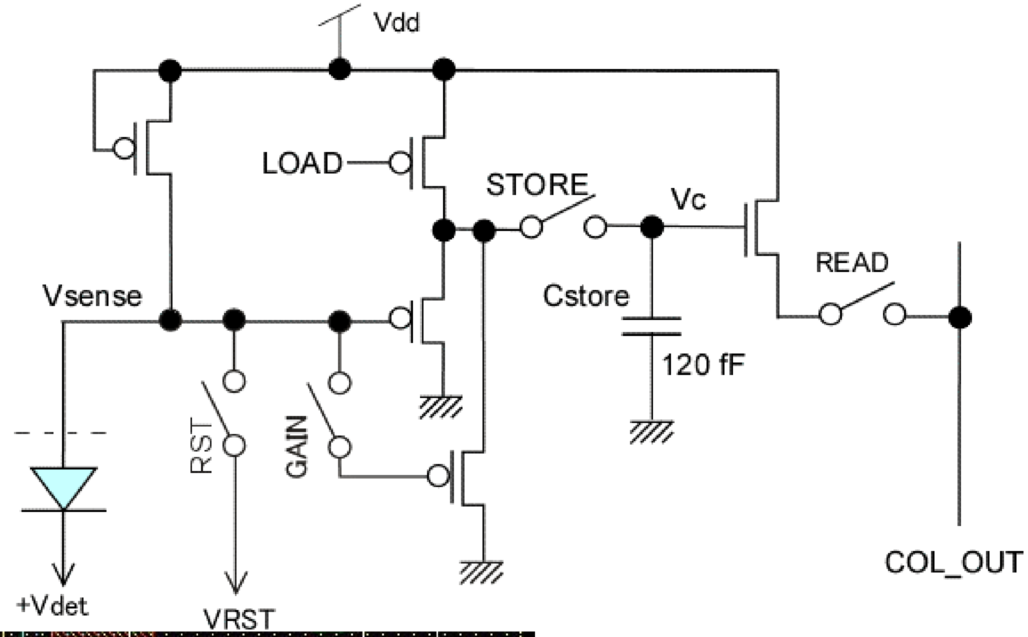


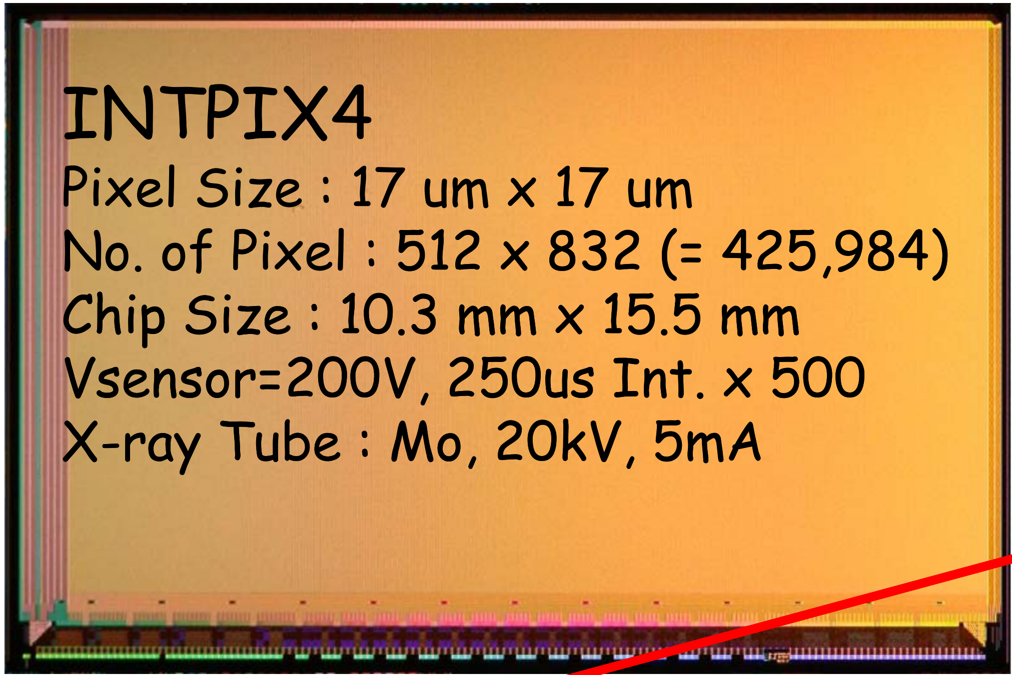


Size : 14 μm x 14 μm
with CDS circuit

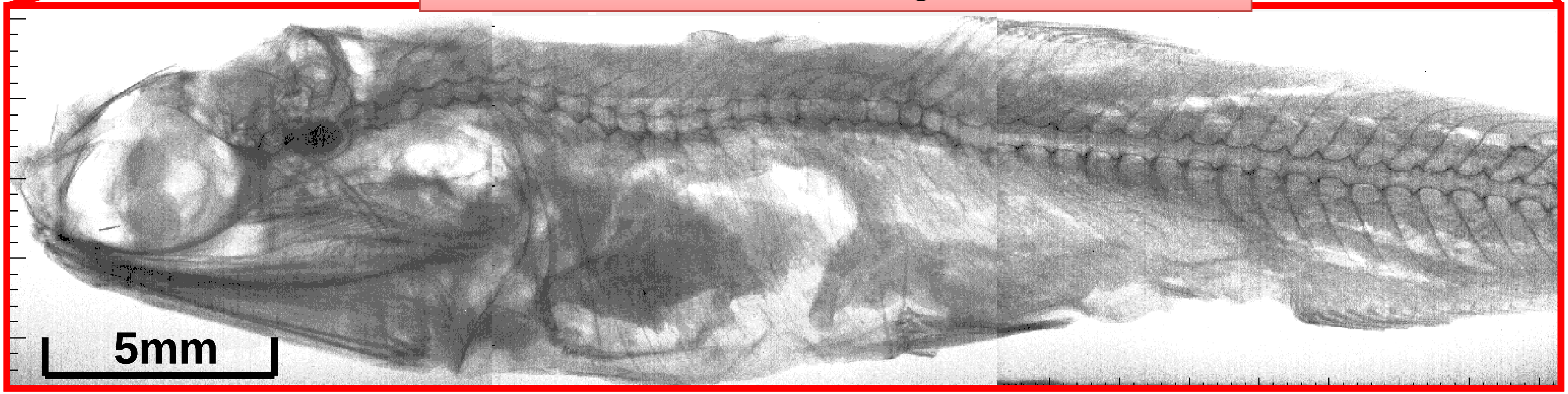
INTPIX6 Pixel
2 Gain
12 x 12 um^2







Fine resolution & High Contrast



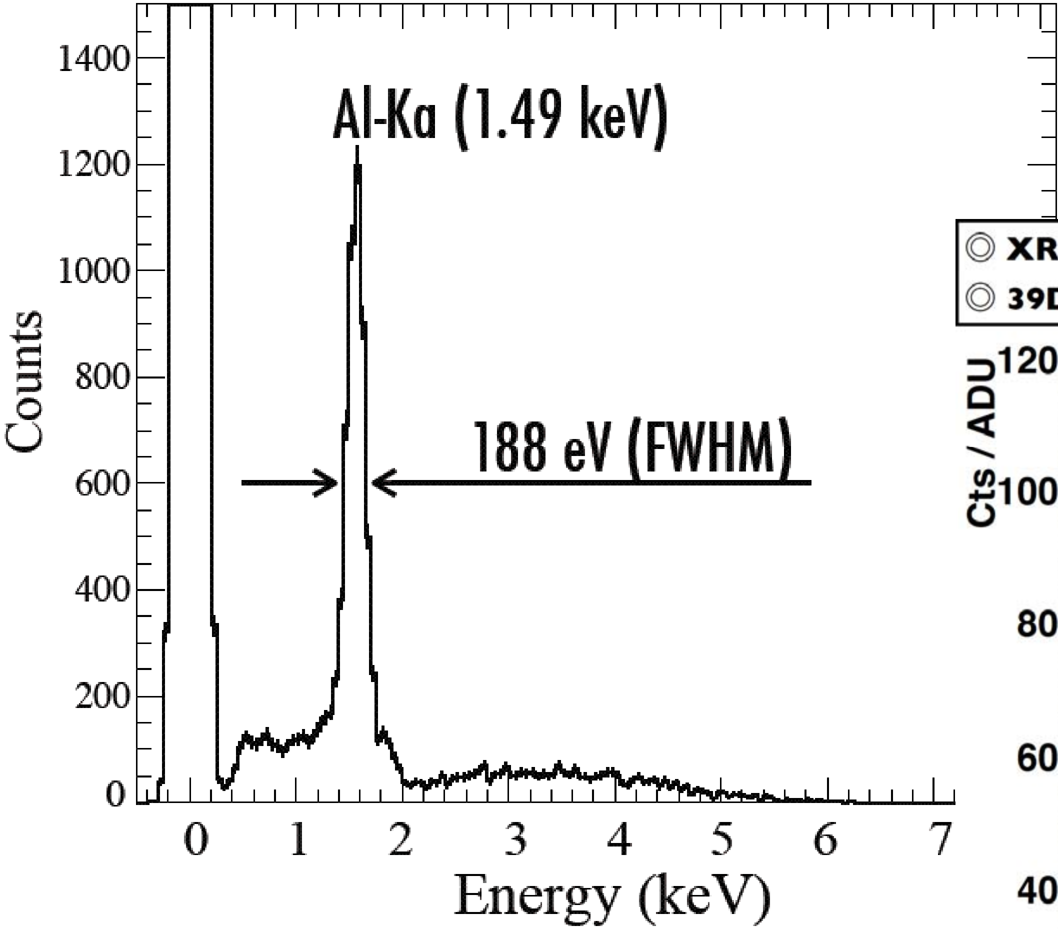
X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined).

(A. Takeda)

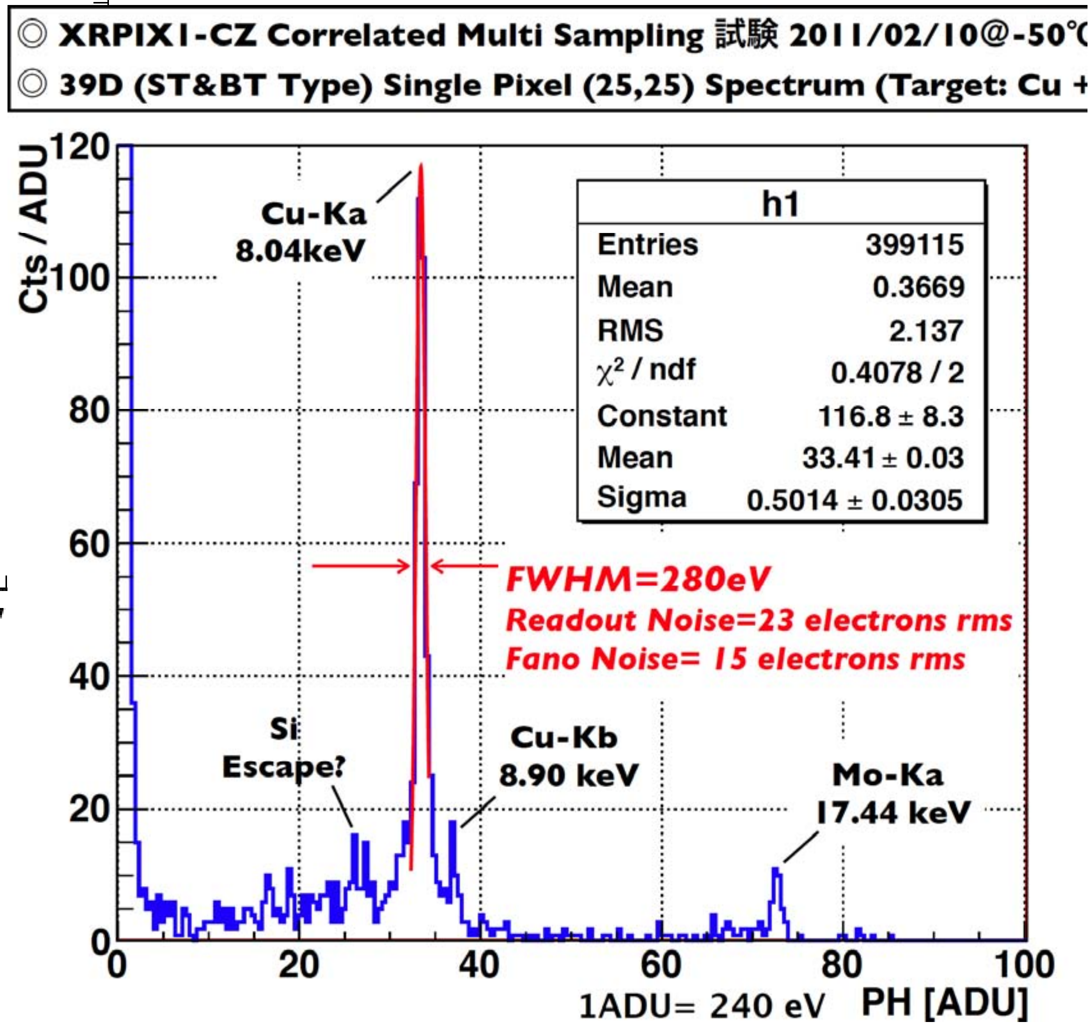
XRPIX1

X-ray Energy Spectrum

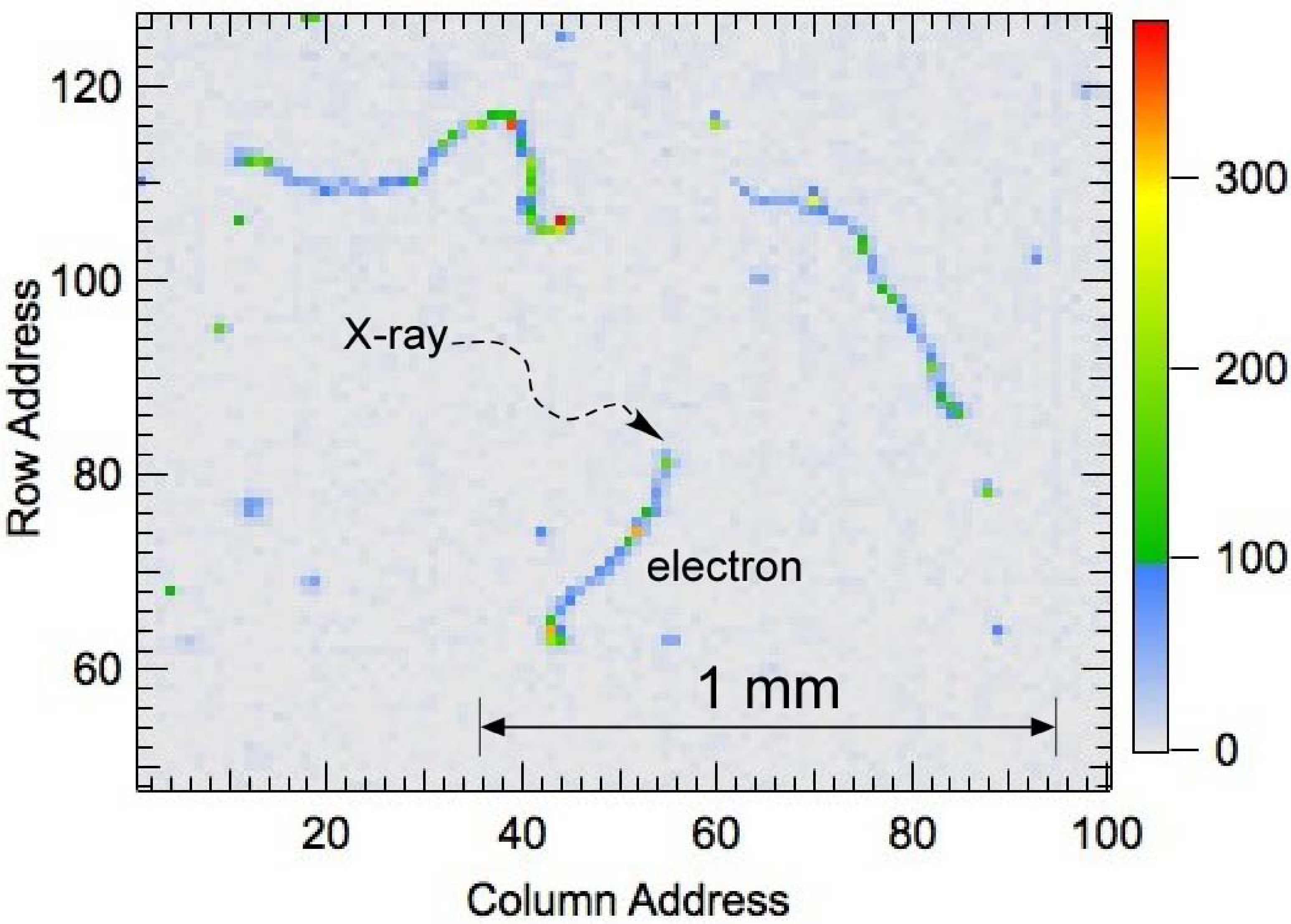
Cu Kα and Kβ is separated
Noise ~ 23e⁻ @-50˚C



(Kyoto Univ.)

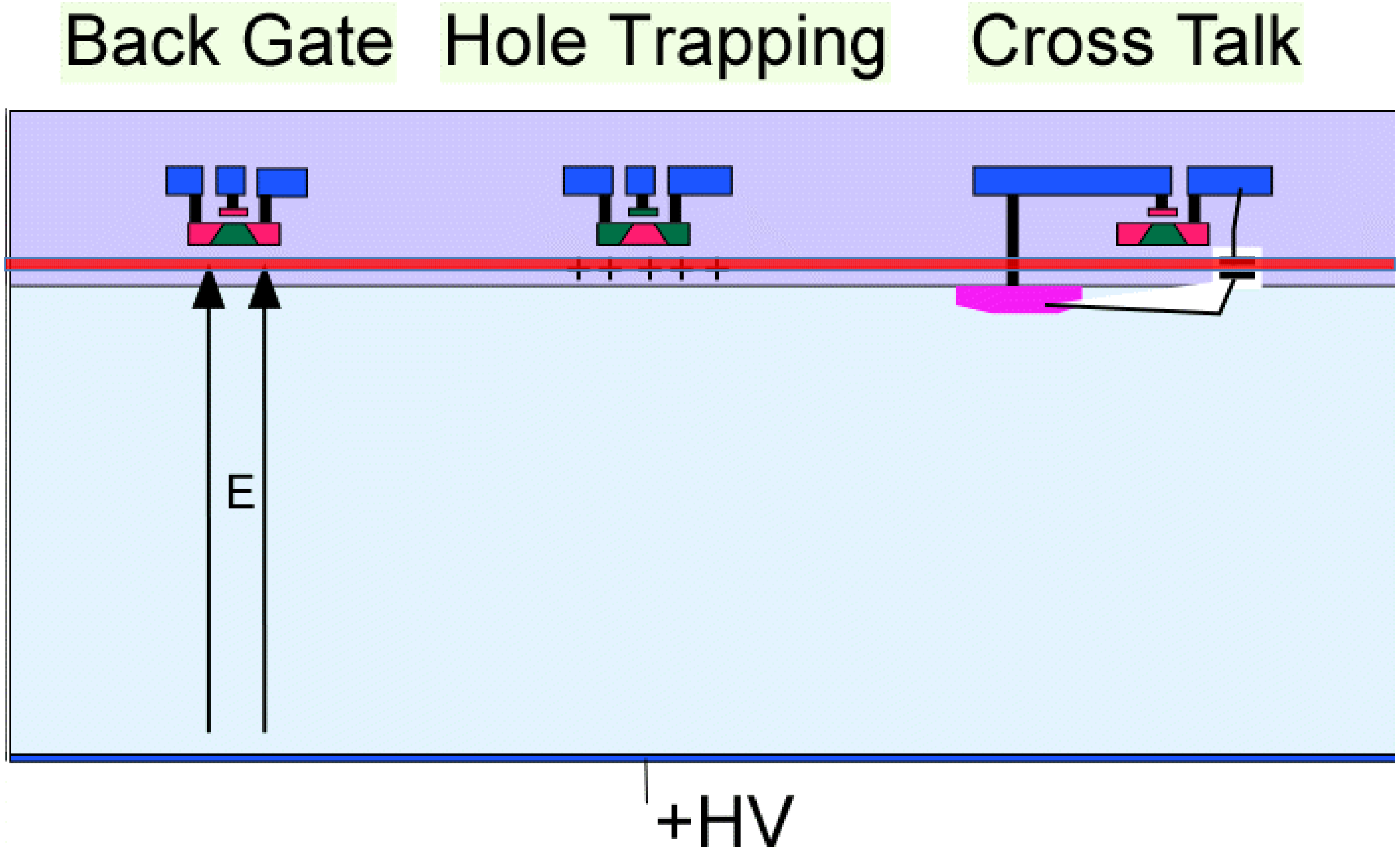


Compton Electrons from High-Energy X-rays



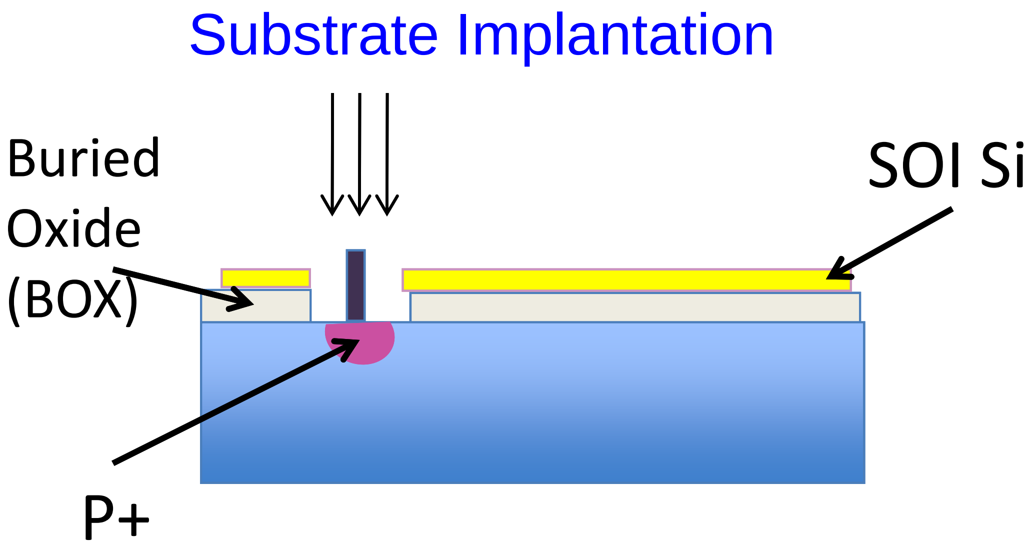
Isuues in SOI Pixel

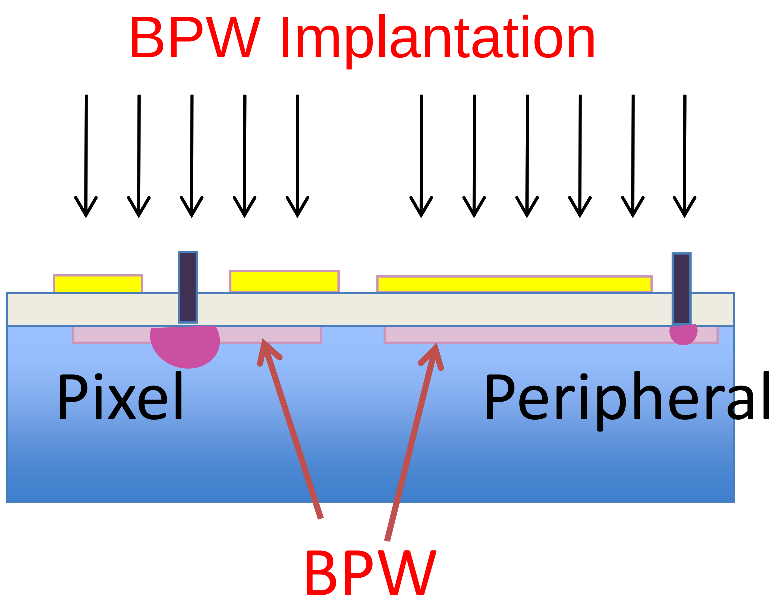
Sensor and Electronics are located very near. This cause ..



We need additional back-plane to suppress these effects.

Buried p-Well (BPW)



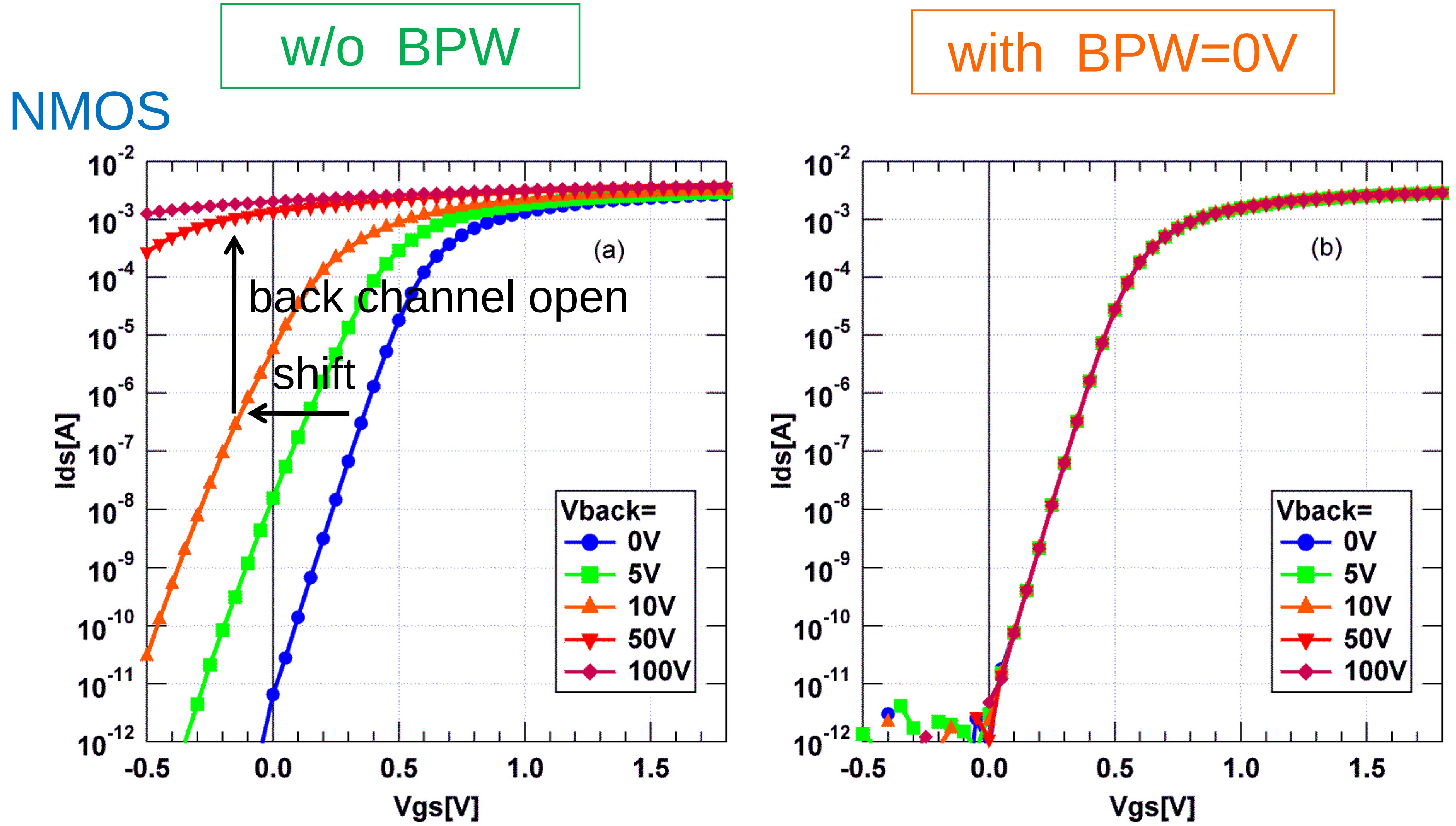


- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

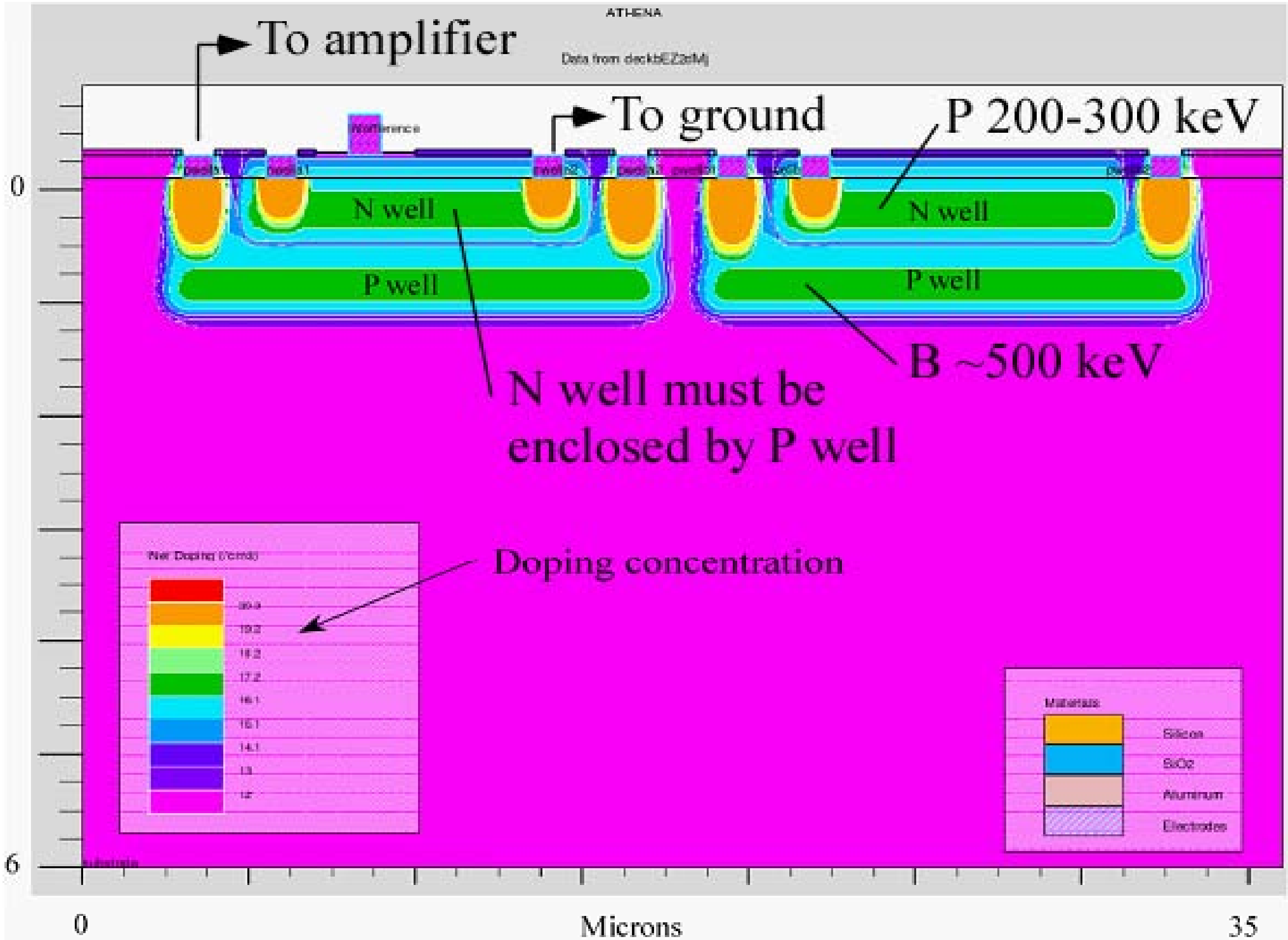
- Suppress the **Back Gate Effect**.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which improve radiation hardness.

I_d-V_g and BPW



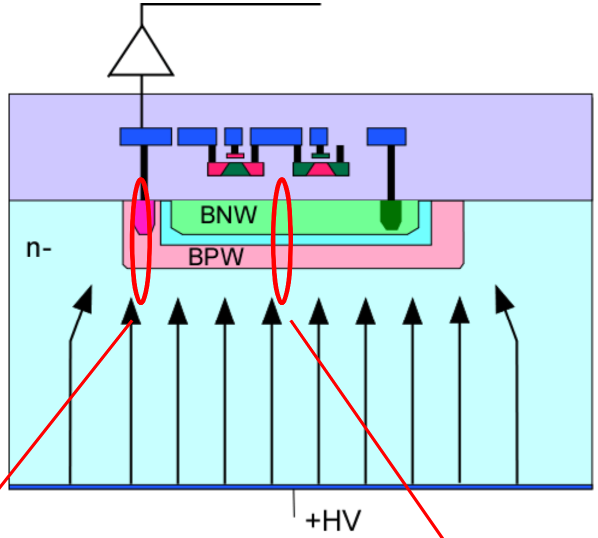
Back gate effect is suppressed by the BPW.

Nested Well Structure

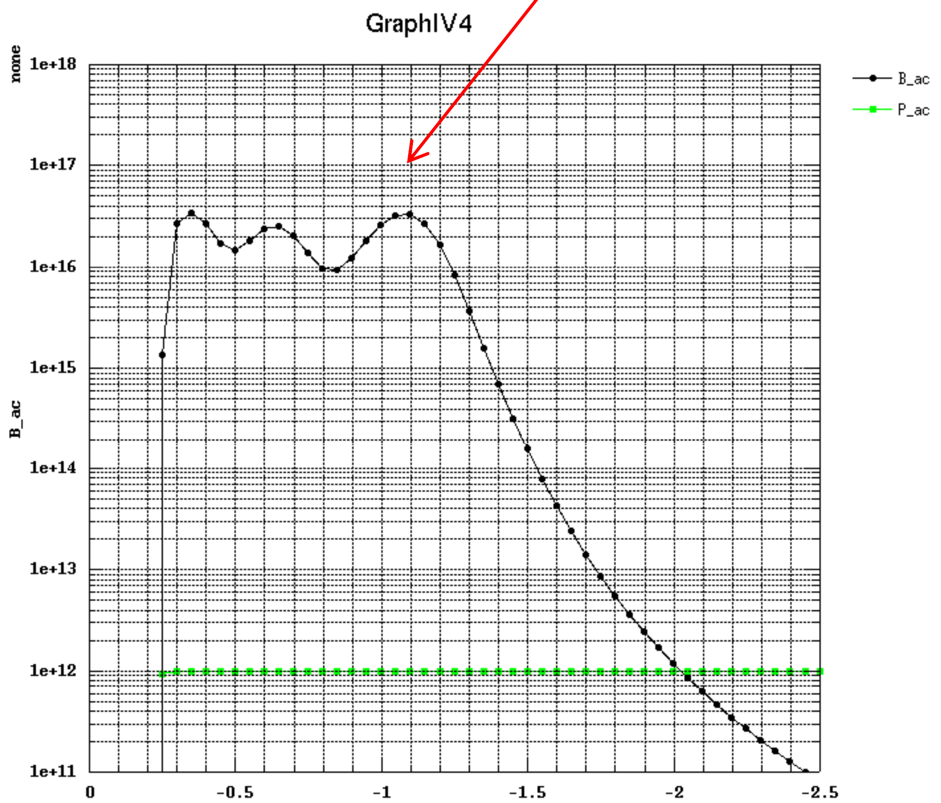


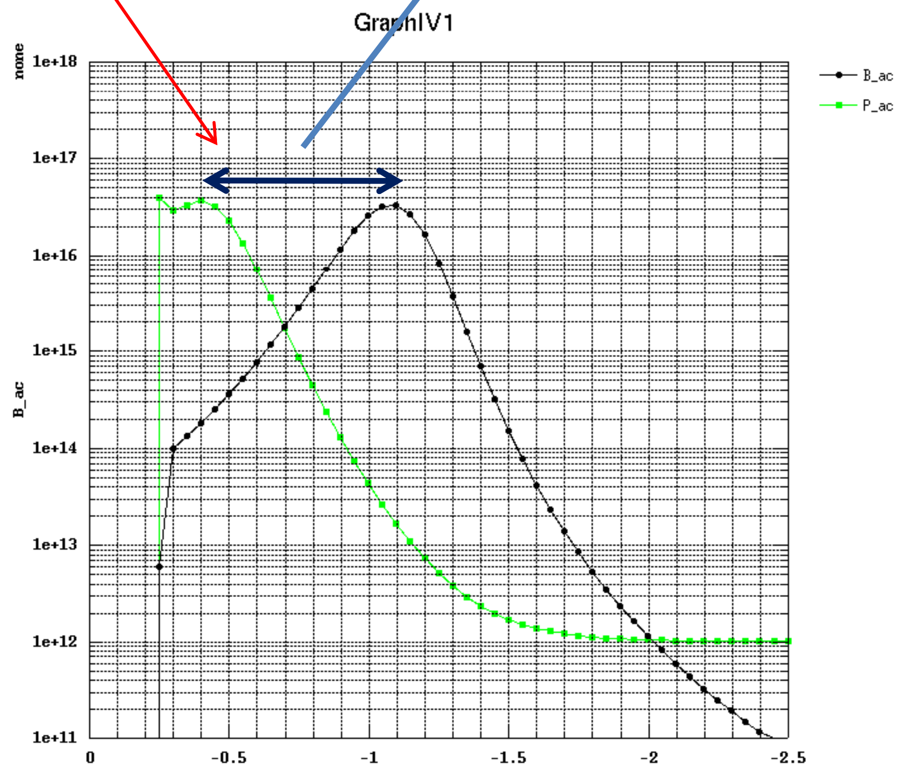
- Signal is collected with the deep Buried P-well.
- Back gate and Cross Talk are shielded with the Buried N-well.

Impurity Concentration



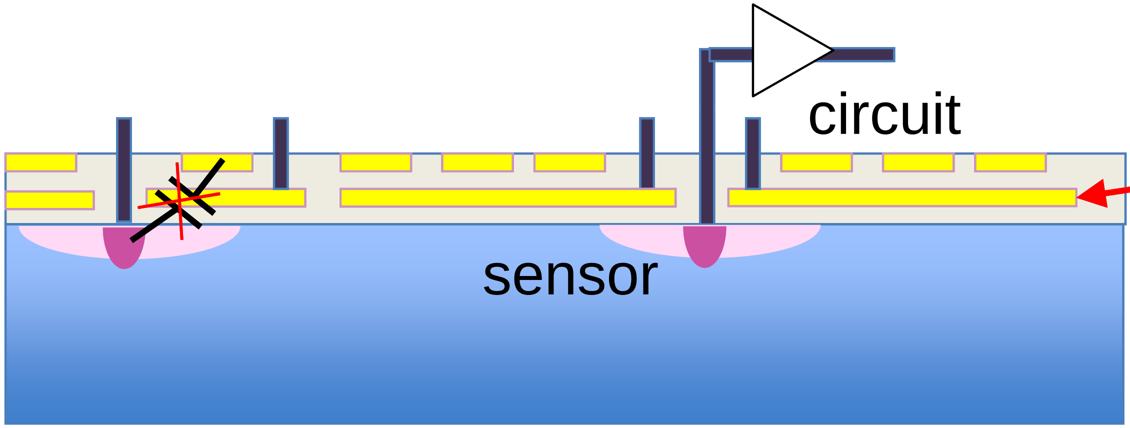
Peaks of BNW and BPW are separated ~0.7 μm to reduce capacitance





Double SOI Wafer

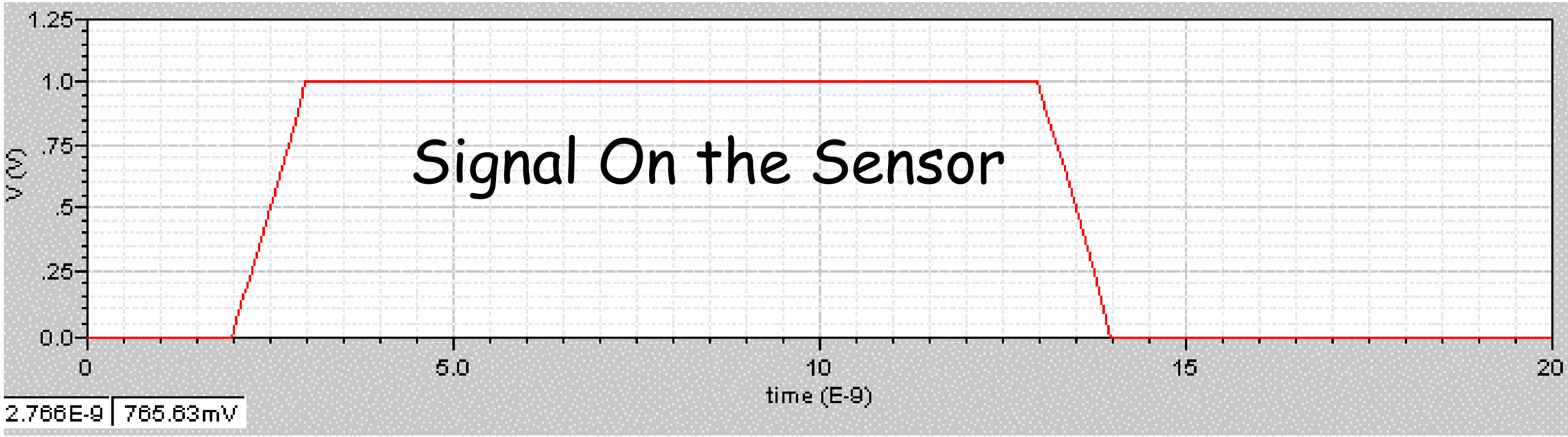
LAPIS SEMICONDUCTOR

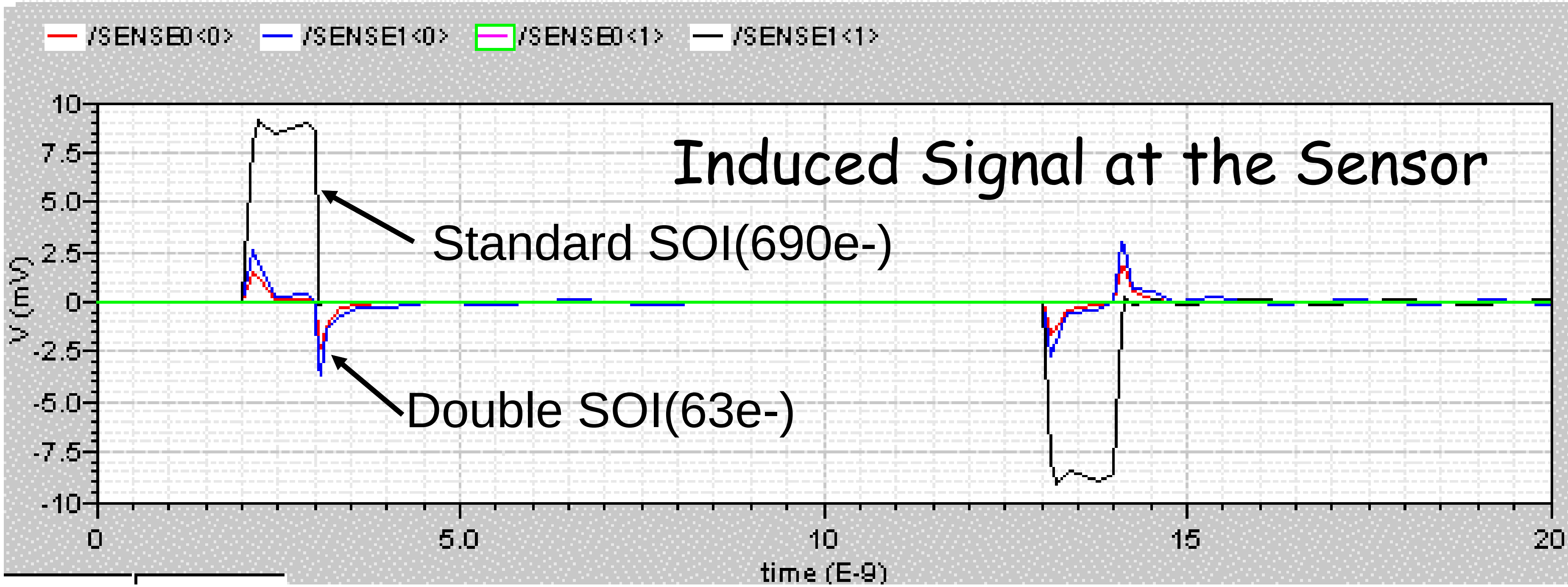


additional conduction layer

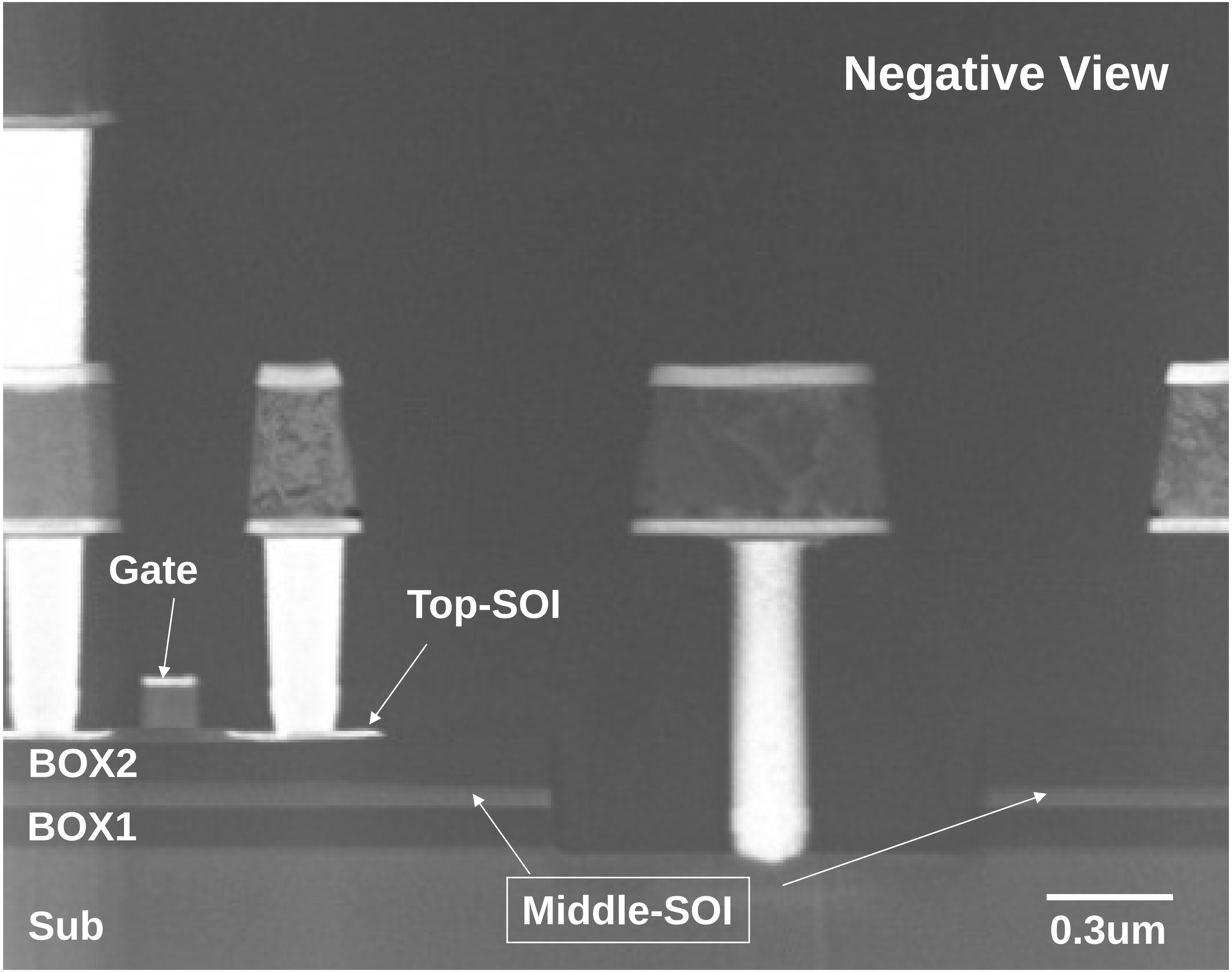
- Shield transistors from bottom electric field
- Compensate electric field generated by the trapped hole in the BOX.
- Reduce crosstalk between sensors and circuits.

Cross Talk Simulation



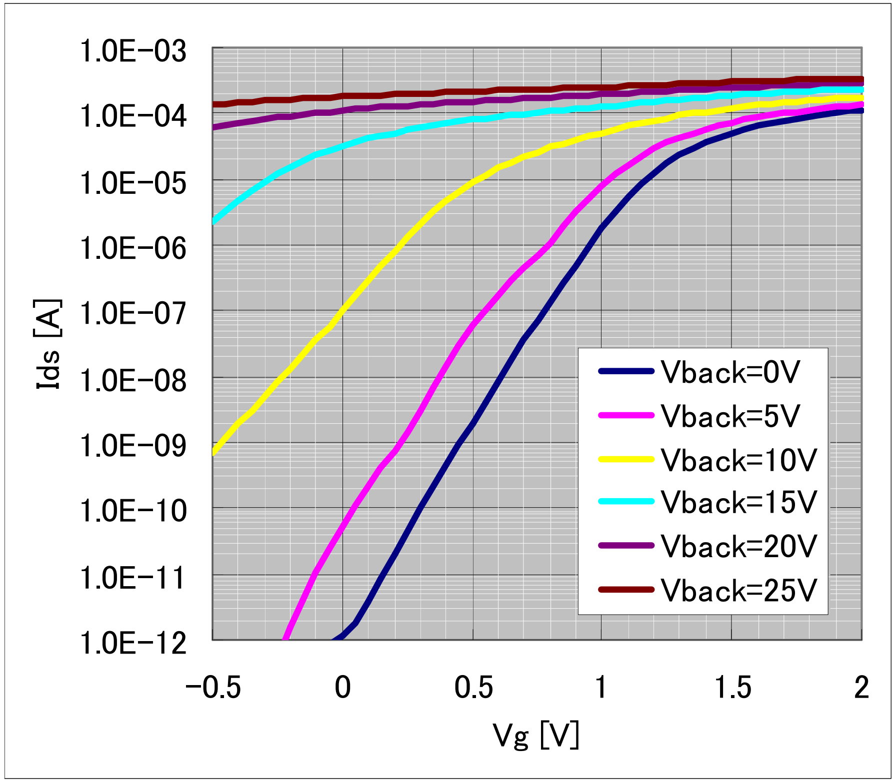


Cross Talk from the circuit to the sensor can be reduced 1/10, and signal shape will be bipolar. → disappear in charge amp.

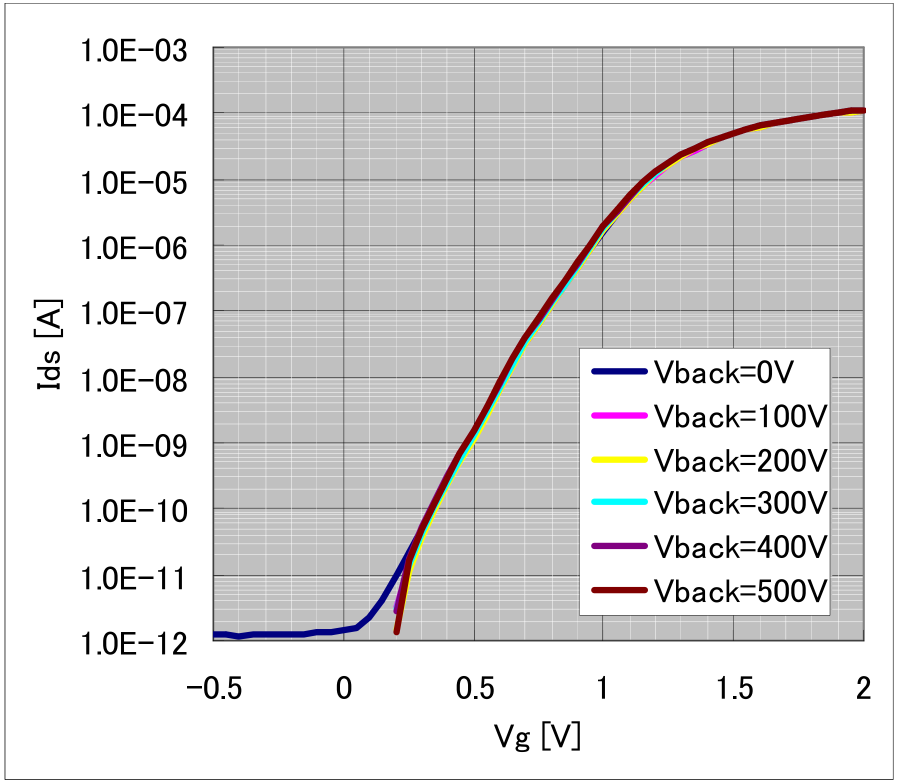

Negative View
Gate
Top-SOI
BOX2
BOX1
Middle-SOI
Sub
0.3um

Suppression of Back-Gate Effect with Middle-Si layer

a) Middls-Si Floating



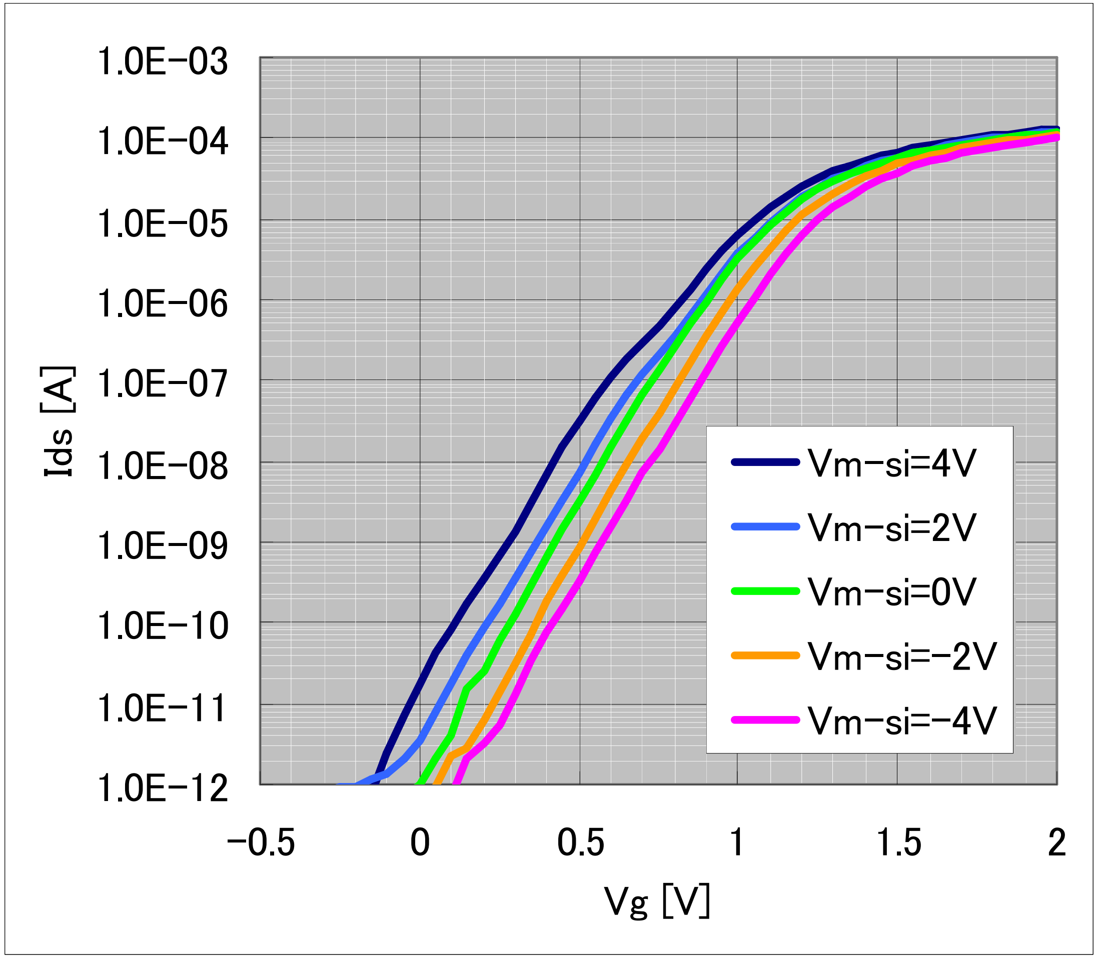
b) Middle-Si = GND



Nch Core Normal-Vt
L / W = 0.2 / 5.0um
Vd=0.1V

Back-Gate Effect is fully suppressed with the Middle Si Layer of fixed voltage.

Trapped Charge Compensation (Threshold Control)with Middle-Si Layer

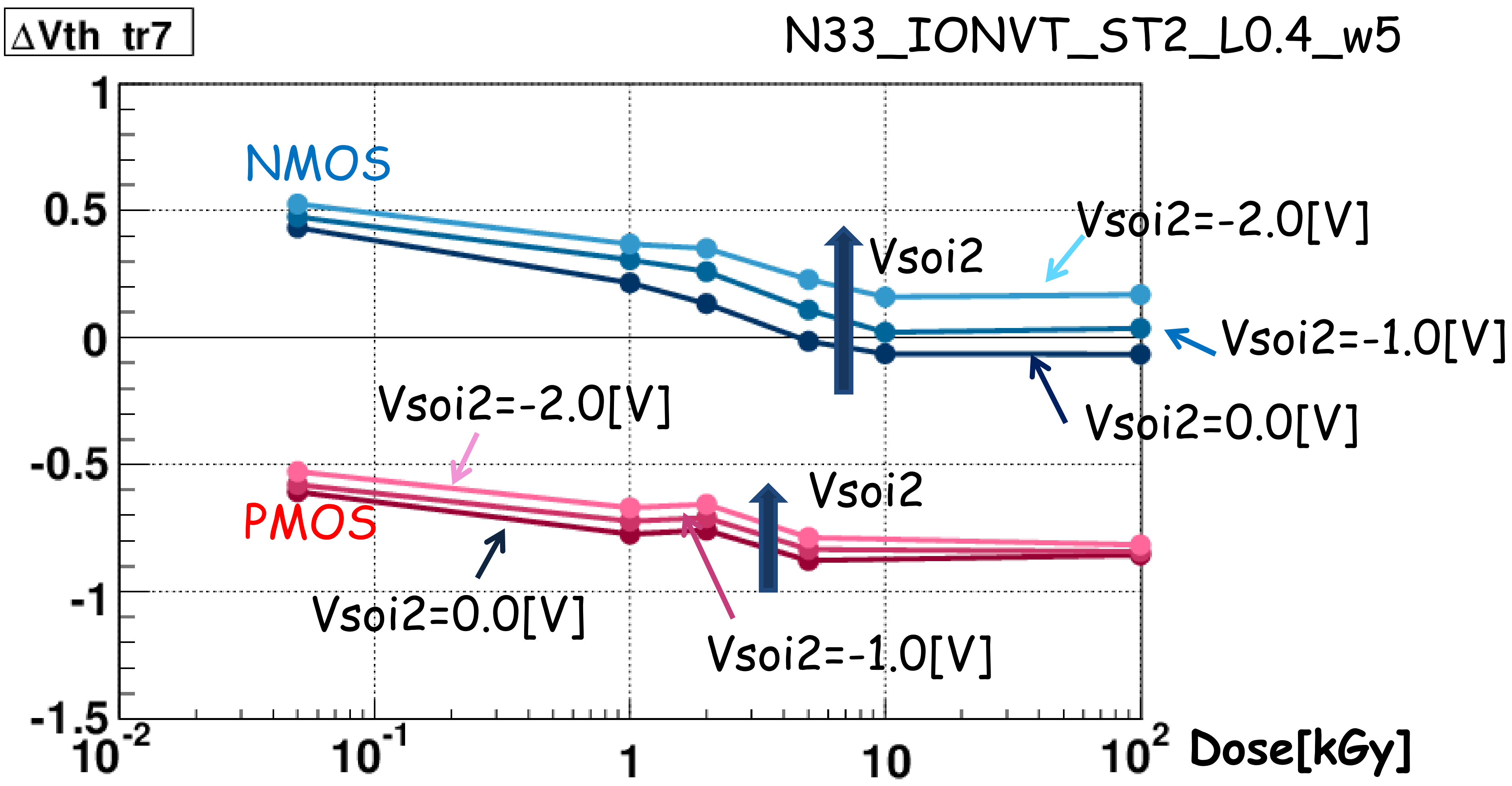


Threshold voltage of a transistor is controlled with the bias voltege of the Middle-Si layer.
This indicate effects of the trapped charge in the BOX can be compensated with the bias voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0 um
Vd=0.1V, Vback:floating

Double SOI Irradiation Test

Preliminary!



We could observe restoration of the threshold shift with applying negative voltage to the SOI2 layer.

Summary

- SOI technology has many good features; low power, low variability, large operating temperature range, no latch up..., and Industries are moving to extremely thin SOI.
- SOIPIX is monolithic detector, and many kinds of detectors are already working.
- We have ~twice/year regular MPW runs with increasing no. of users.
- The process technology is still progressing; Higher resistivity wafer, Nested well structure, Larger mask size, Stitching, and Double SOI, etc. …
- We welcome new collaborators to the SOI pixel development!