# SOI Activities at IHEP

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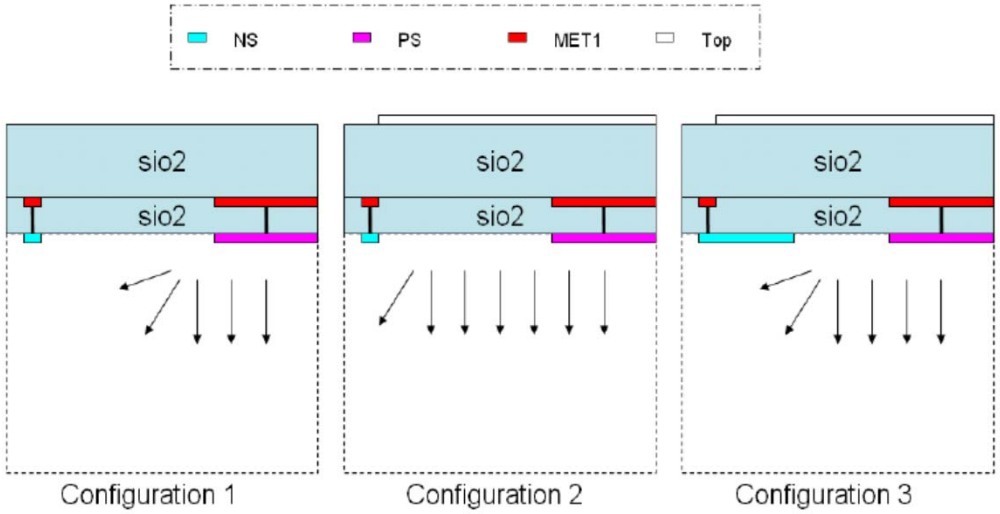
- 2 chips with full function submitted to SOI MPW
  - FY11-1, Integrating pixel
  - FY12-2, Counting pixel

# Integrating pixel

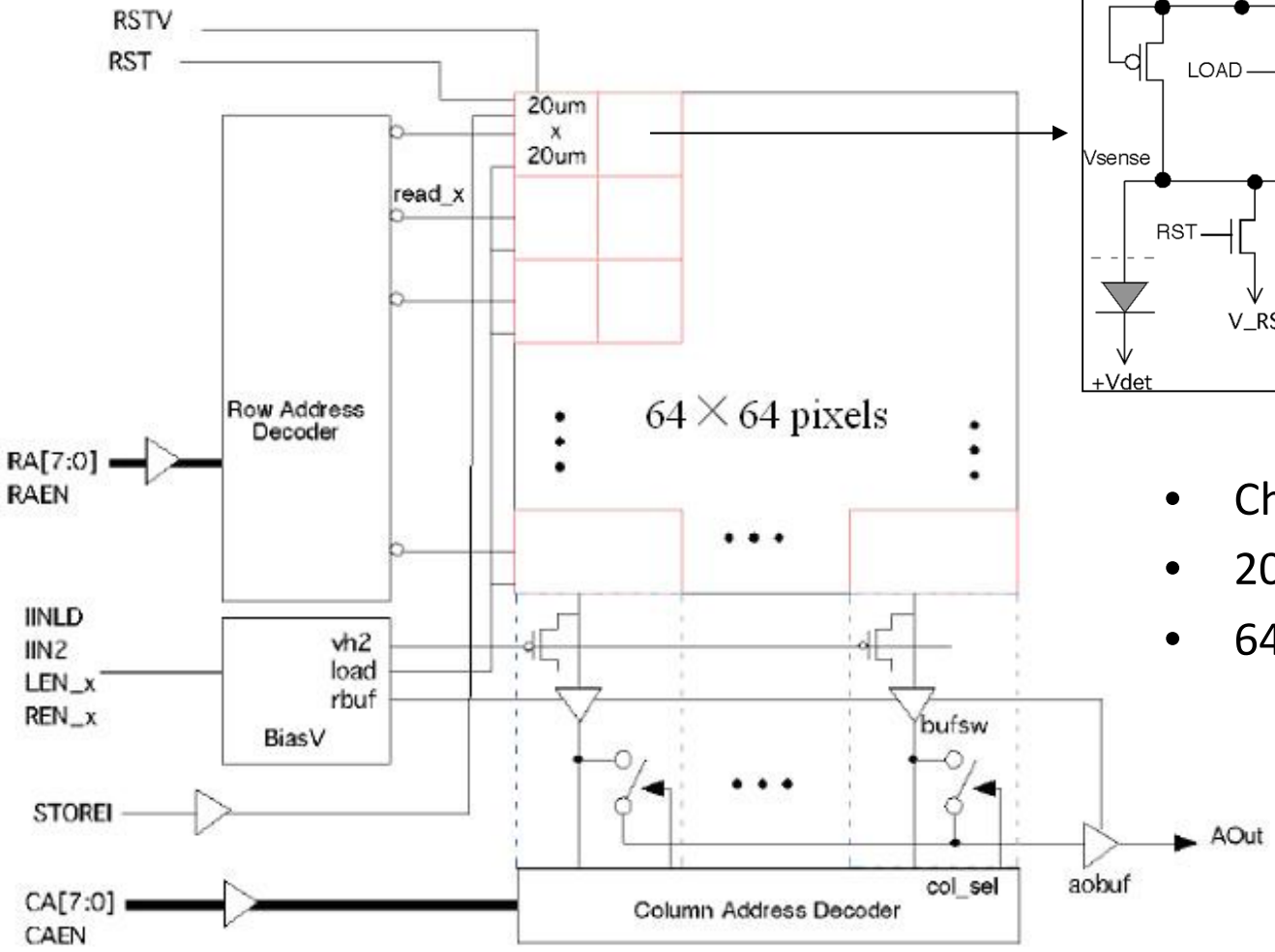
- My first try on SOI detector, aimed at going through the design process
  - TCAD simulation
  - Circuit design
  - Layout
  - Test setup
  - Chip test

# TCAD Simulation

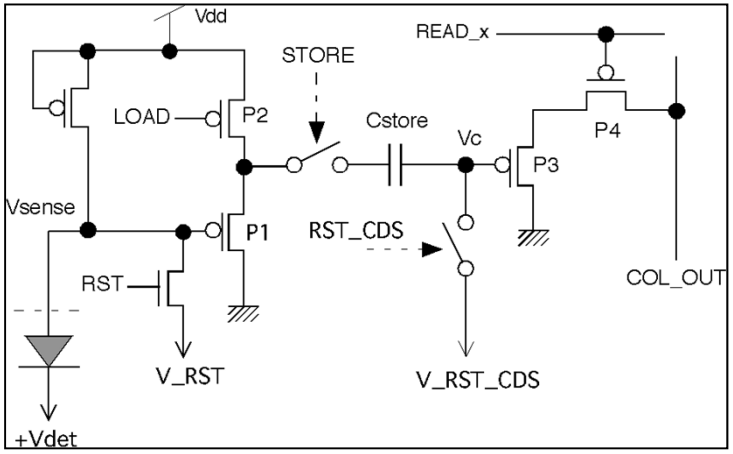
- Simulated 3 different scenarios regarding the edge structure of a chip.
- Concluded that a wider NS implant would improve the leakage.



# Circuit block of the chip



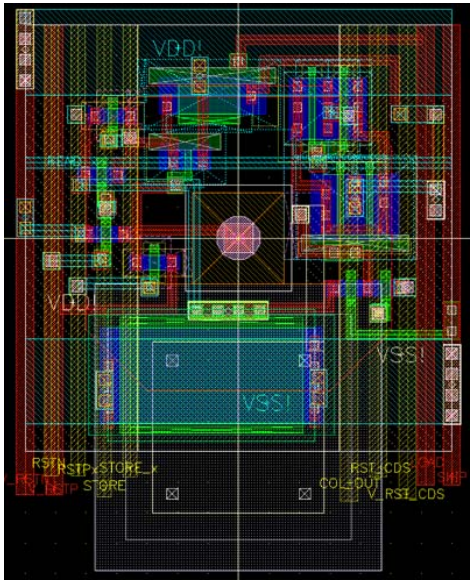

Pixel Circuit



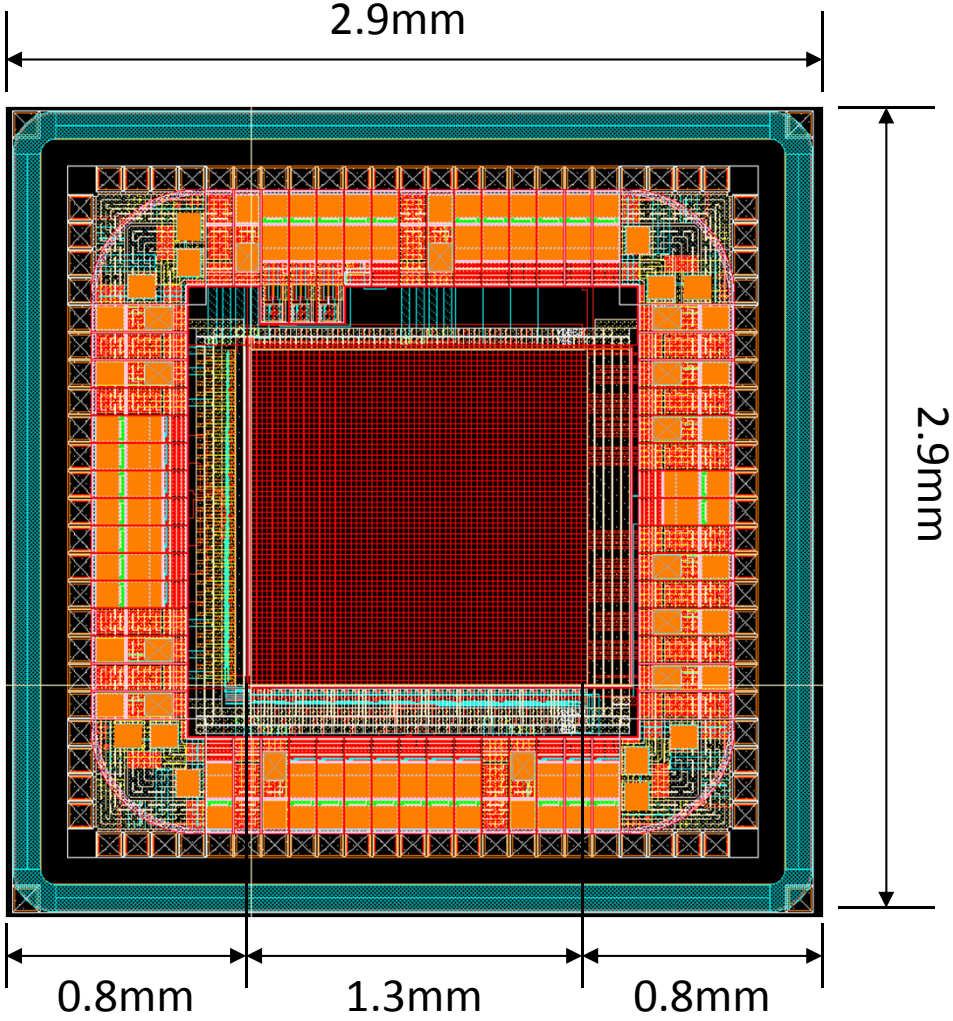

- Charge integrating， CDS
- 20um*20um pixel
- 64*64 array

# Layout

- 2.9mm*2.9mm
- 72 Pads surrounding
- 20% of total area sensitive



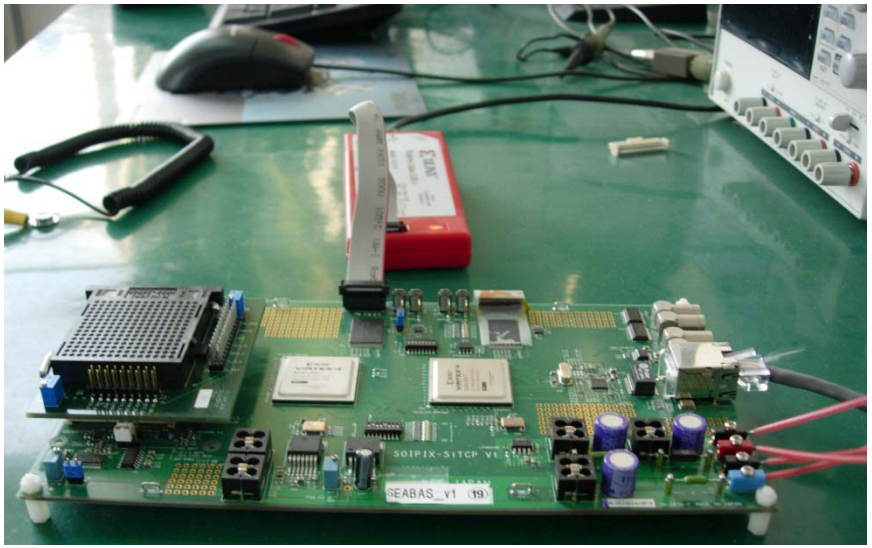

**Single Pixel layout**




**The chip layout**

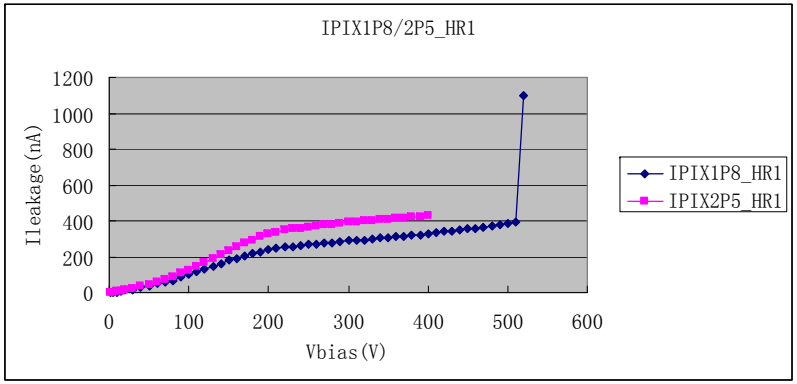
# Test Setup

- Keithley source meter: HV bias and I-V test.
- Major component: SEABAS (Soi EvAluation BoArd with Sitcp) from KEK. Encrypted TCP/IP firmware.
- Sub-board, FPGA coding.
- Software .



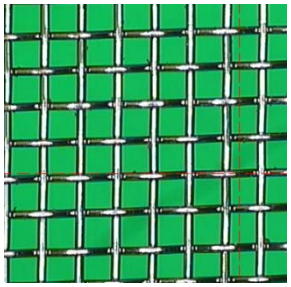
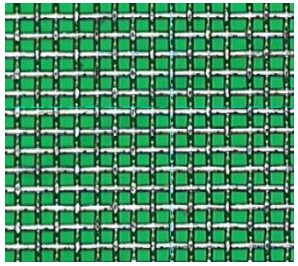
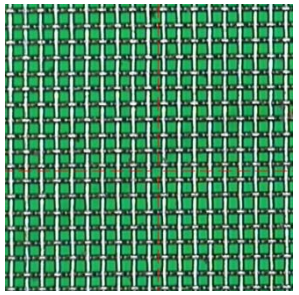
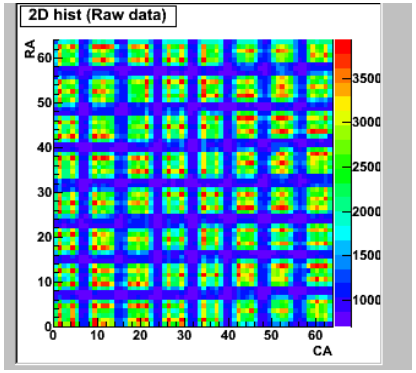
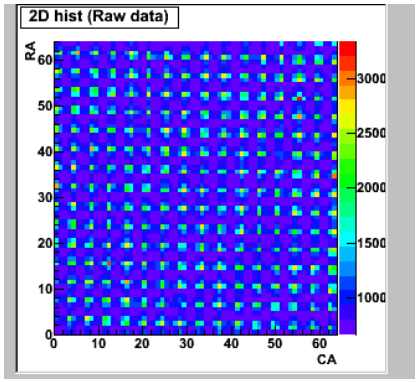
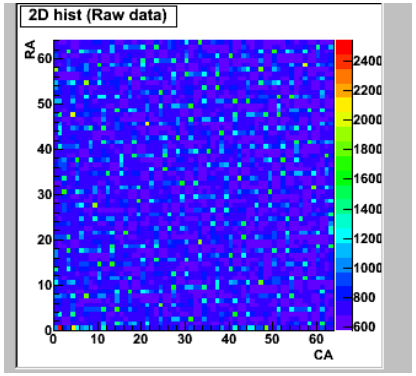
# Play with the chip

- Got the chip back in March 2012.
- Power up
  - Voltage on with reasonable current, a good start.
- Check the response of digital circuit
  - Responds as expected, a piece of silicon communicating with outside world!
- Full control of the chip
  - Seems in good order.
- Bias the sensor, make a I-V curve
  - HV up to 500V can be applied, while 300V should deplete the 260um substrate completely.



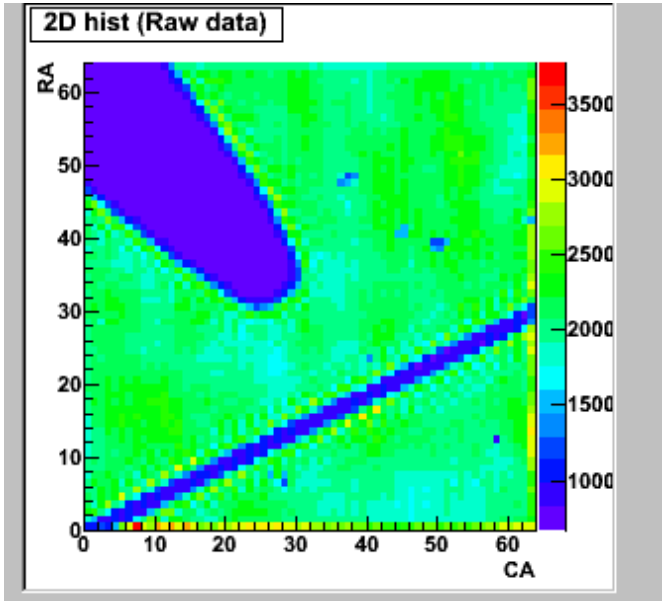

- Took images with red pointer as source
  - 4um*4um window for light illumination in each pixel.

# Red Light Imaging of Metallic Mesh

| | 159um pitch | 79um pitch | 64um pitch |
|---|---|---|---|
| Microscope pictures |  |  |  |
| Images taken by the chip |   |   |   |

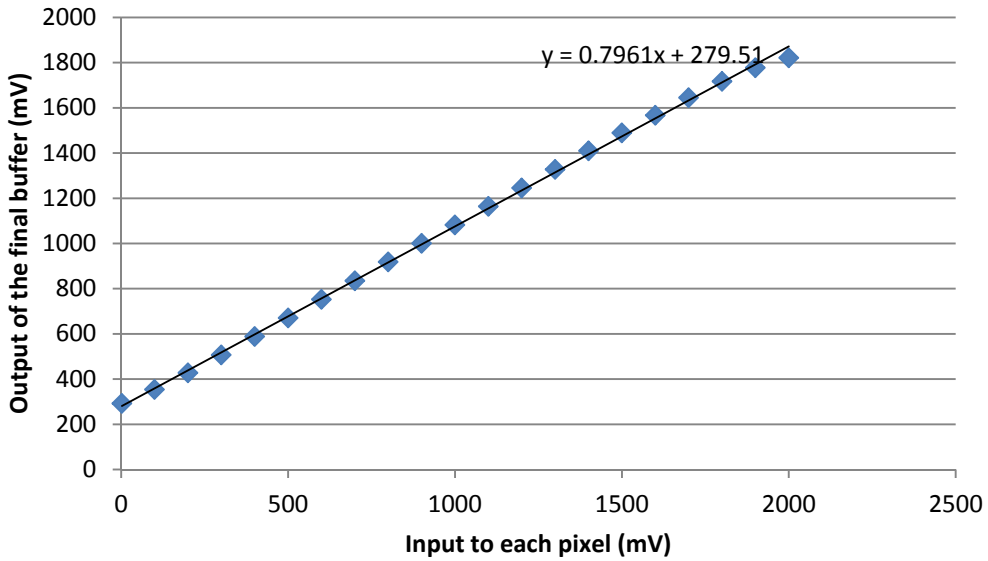
# Red Light Imaging of small objects

- The tip of a pin and 30um golden wire.
- The saw-teeth is a proof of good response to light.
  - 20um*20um pixel.



# Characterize the chip quantitatively

- Calibrate the circuit
  - Gain=0.7961
  - Dynamic range > 1.8V



# Measure the Capacitance in pixel

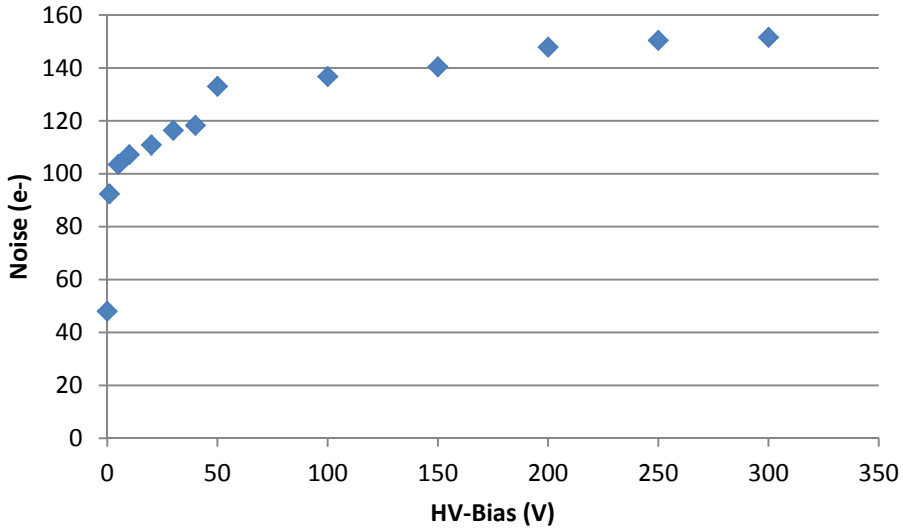
- Integrating leakage current for a period of 250us results in 340mV.
- Leakage current 70nA in total for 4096 pixels.

$$Cd = \frac{\Delta Q}{\Delta V} = \frac{\frac{70nA}{4096\ pixels} \times 250us}{340mV}$$ = 12.6fF

- Conversion Coefficient = 1/Cd = 12mV/1000e-

# Noise as a function of HV Bias

- Measure the integration of leakage current for 100 times, take the standard deviation as noise.
- Noise increases with HV bias, around 150e- when fully depleted.



# Outlook on this work

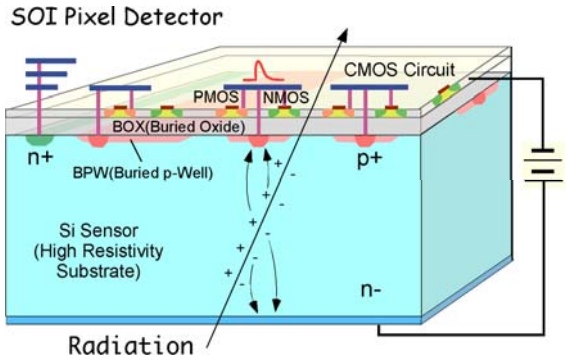
- Leakage current needs to be understood.
- X-ray imaging test had a problem.
- X-ray imager should be able to achieve:
  - Up to 700um thickness full depleted
  - Frame rates: 1K frame/s
  - Full well depth: 150K e- @ 20um□pixel
  - Noise: 100e-

# Counting pixel

- Counting pixel is suitable for synchrotron radiation light source, which is a major application for detector R&D at IHEP.
  - SR facility in campus.
  - 3rd generation SR facility in planning.
  - New beamlines to be built in Shanghai SR light source.

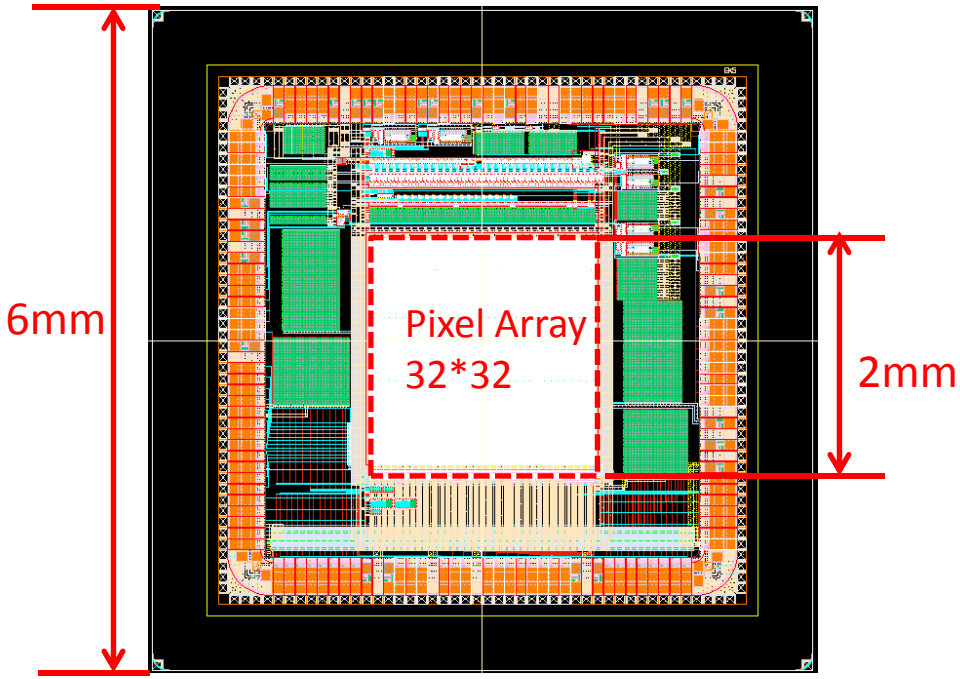
# SOI pixel for X-ray imaging

- Advantages:
  - Monolithic, no bump bonding.
  - Full depletion, direct detection of X-ray.
- Problems to be solved:
  - Radiation hardness, can't meet the requirements for a collider, but OK for synchrotron light source, dental imaging and mammography.
  - Cross talk between circuit and sensor, digital circuit injected charge to sensor by capacitive coupling, but integrating circuit works well by far.



# Counting pixel chip

- Much more complex than integrating pixel.
- Based on KEK previous design:
  - Corrected design flaw;
  - Enlarged pixel electrode.
- To check the S/N degradation due to increasing Cd.



# Summary

- Have got valuable experience from the design and test a integrating pixel chip.
- Got started with counting pixel chip as it is suitable for SR application.
- Collaboration with KEK is important for us. We would like to enhance the connection and contribute to the development of SOI detector technology.