中国科学院微电子研究所

INSTITUTE OF MICROELECTRONICS OF CHINESE ACADEMY OF SCIENCES

Development of SOI Electronics

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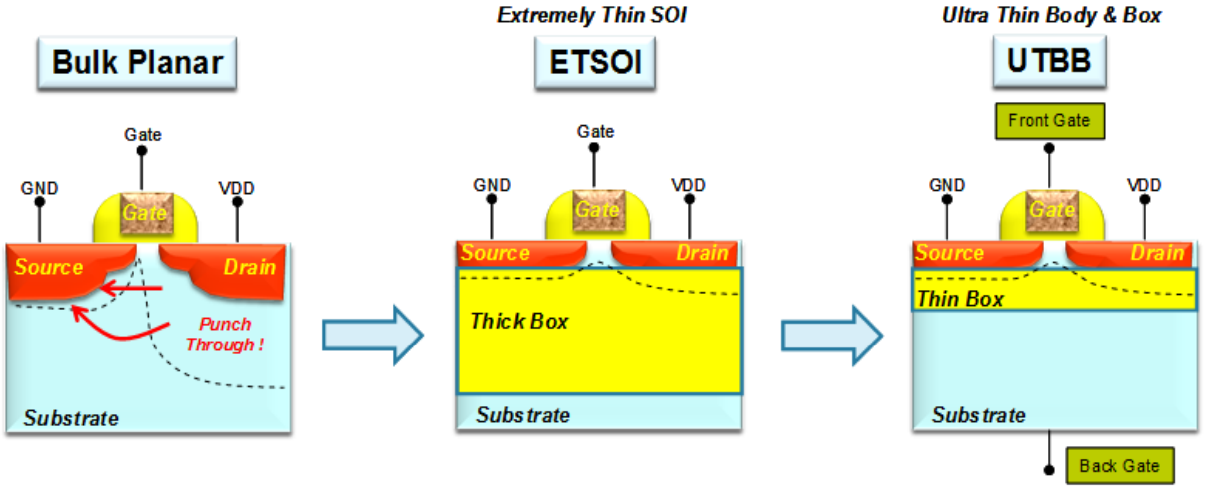
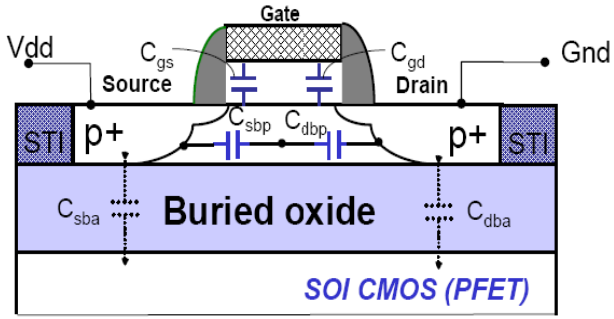
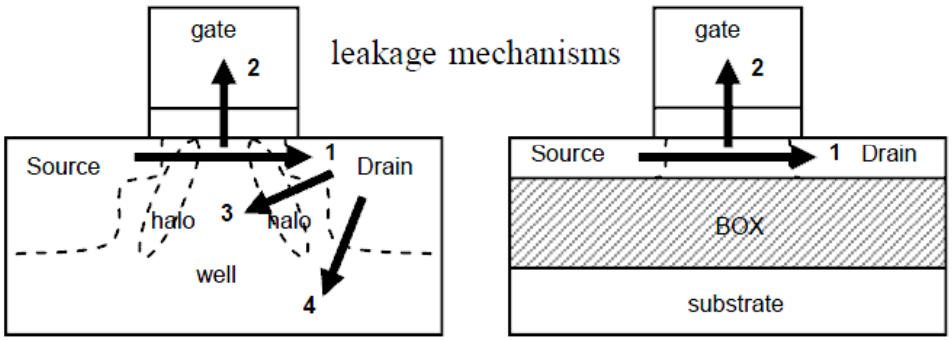
Outline

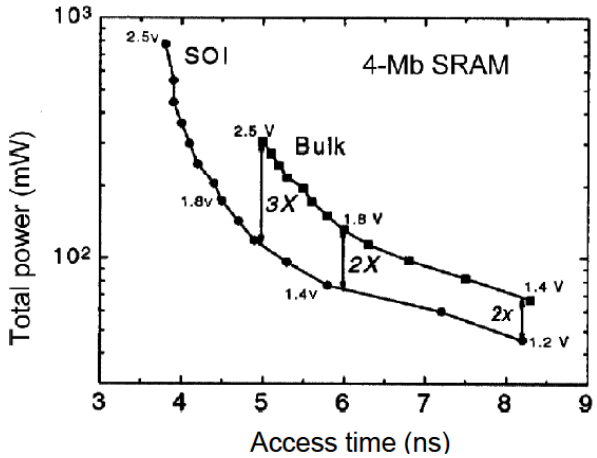
1. SOI Technology in Microelectronics
2. SOI in System Integrated Chip
3. SOI in Harsh-Environment Application
4. Relative Works of our Research Group
5. Summary

SOI Technology in Microelectronics





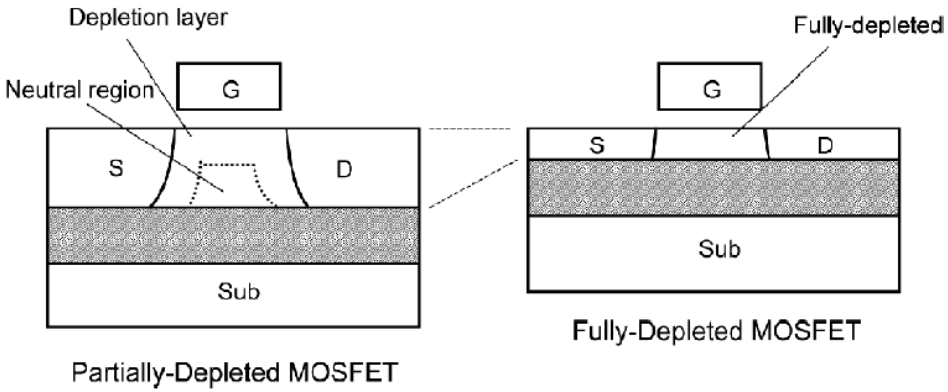


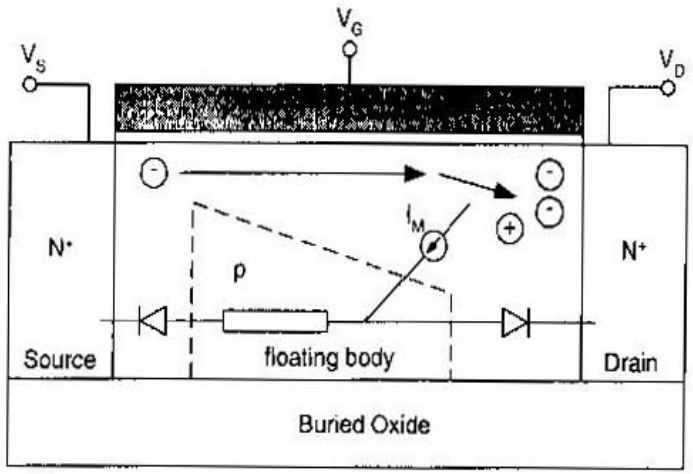


High-Speed (Low Capacitor), Low-Power (Low Leakgage), No Latch-up, Better SER etc.

CMOS: SOI vs. Bulk

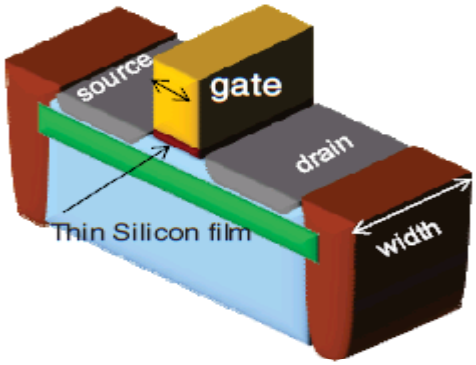
SOI Technology in Microelectronics





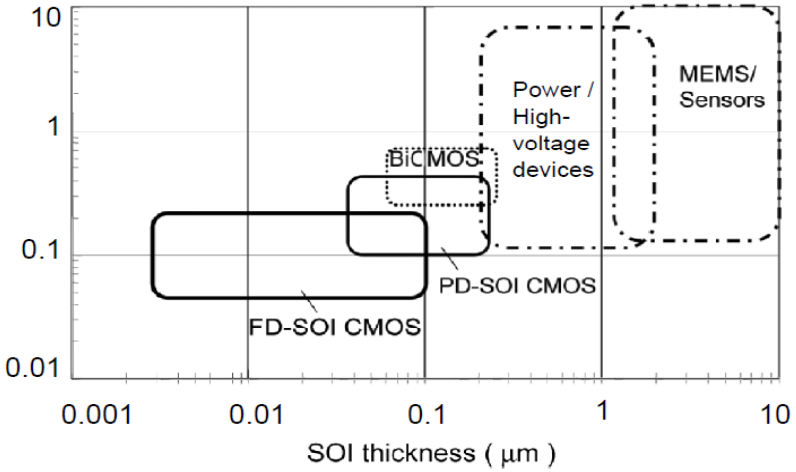
Advantages of FDSOI CMOS technology:

- **No Kink effects, No body-contact area;**
- **More speed, Less RC, Lower Power;**
- **Easy design transfer from Bulk;**
- **First choice for Sub-10nm node.**

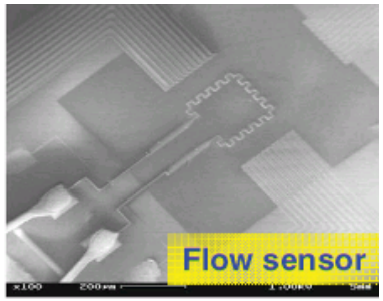


PD-SOI, FD-SOI and UTB-SOI

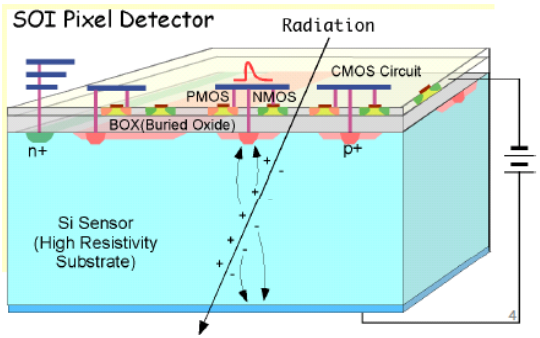
SOI in System Integrated Chip

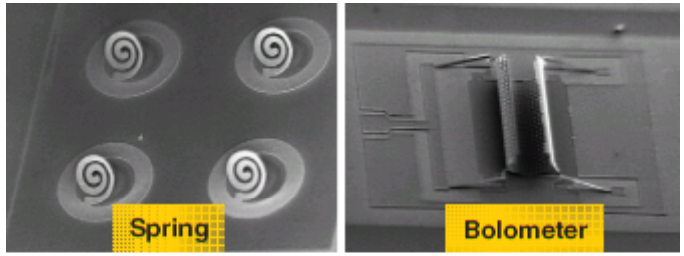


- **High Performance CMOS Circuits**
- **Excellent Analog/RF Circuits**
- **Complex MEMS/Sensor/Actuator**
- **Dedicated Optical-devices**
- SOI, to fabricate complex SOC.

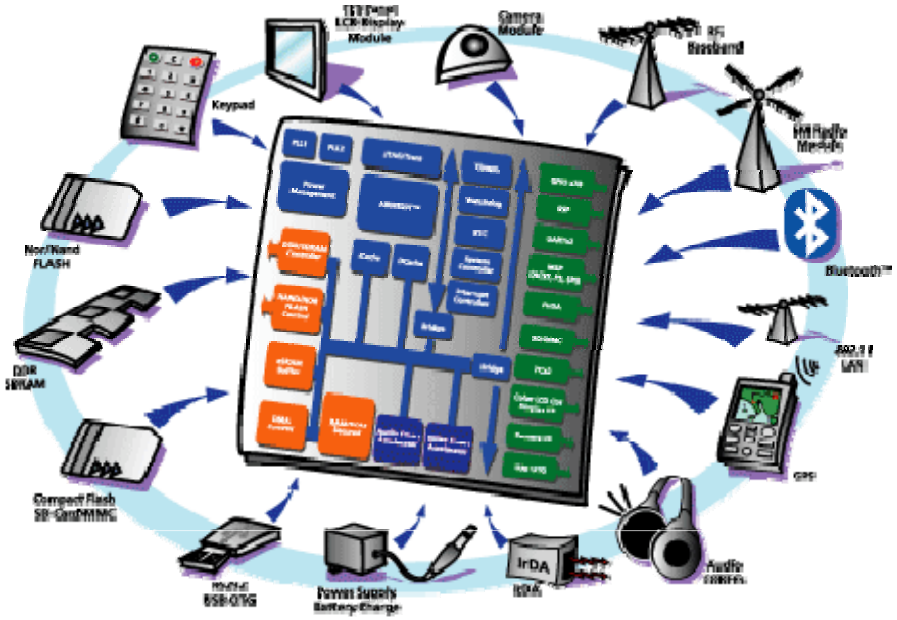


[J. Laconte *et al.*, *IEEE Sensors 2004*]





[M. El Ghorba *et al.*, *Transducers 2007*]
[S. Sobieski *et al.*, *Sensors Letters*, 2009]

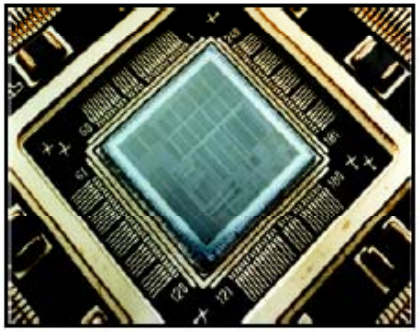


SOI in Harsh-Environment Application

IMECAS

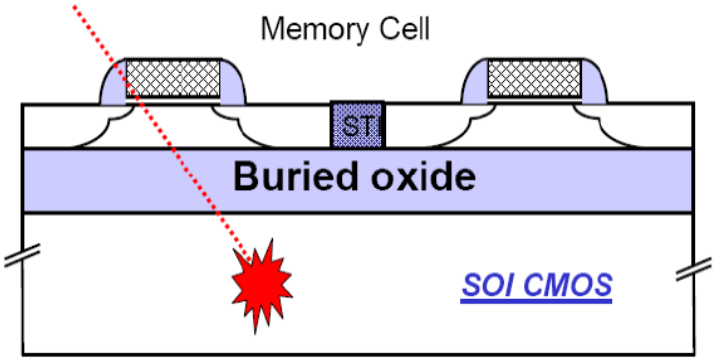
Aerospace

Commercial



High Temp

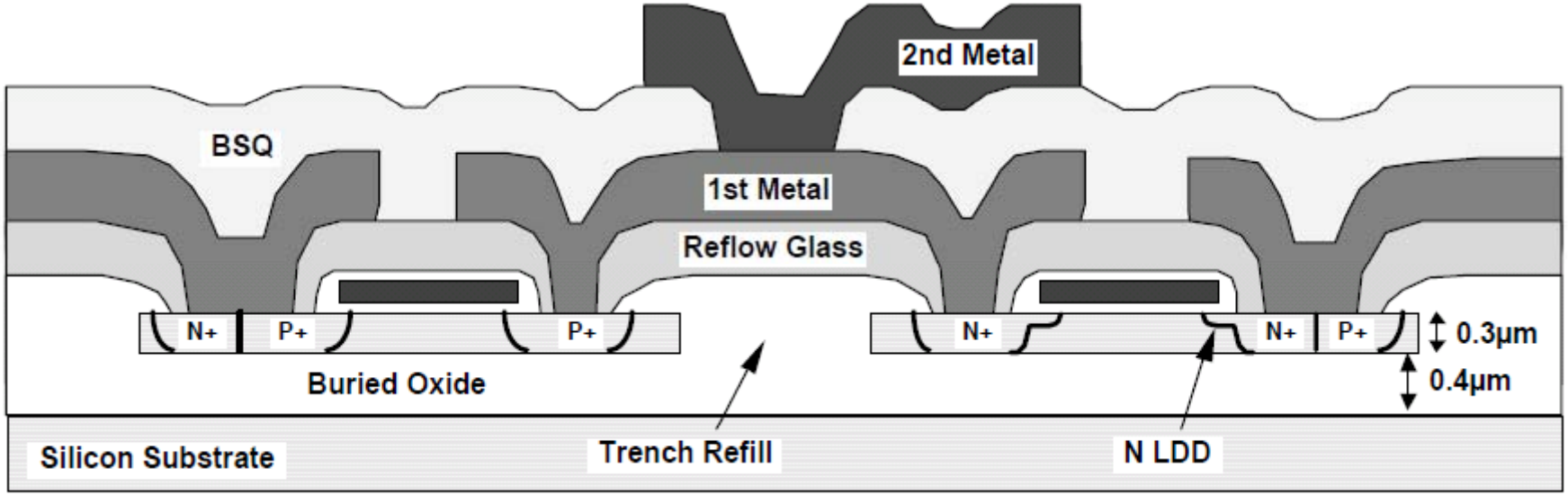
Sensors



- Less susceptibility to soft errors
  - **SER reduced by 5~7X**
  - **Low power high reliability**
  - **No single-event latch-up**
  - **FDSOI has better SER than PDSOI**

High-Temp: Guaranteed Operation To 225℃ For Five Years Pressure!

SOI in Harsh-Environment Application



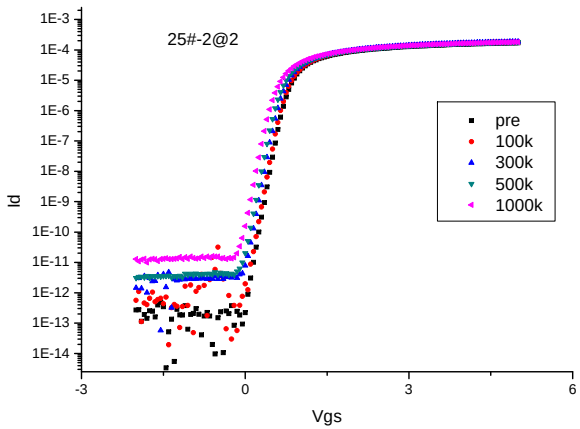
Total Dose radiation — cumulative radiation from trapped protons, electrons, solar energetic particles. These can cause permanent damage to most unhardened electronics. Especially for SOI Circuits!

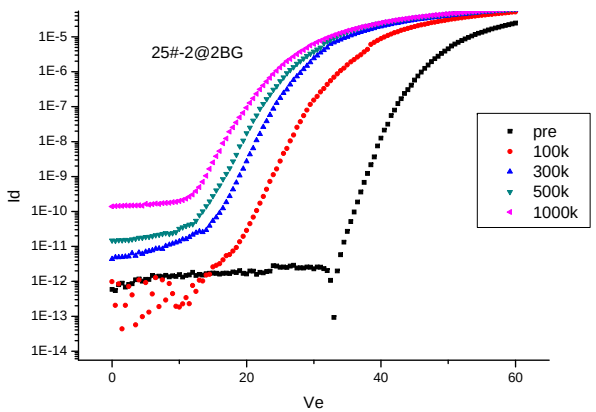
Gate-Oxide, Buried-Oxide, Field-Oxide , Island-Edge and Substrate Engineering。

Research on TID Hardening offers more chances for harsh environments application!

Relative Works of our Research Group

- SOI CMOS Device Physics





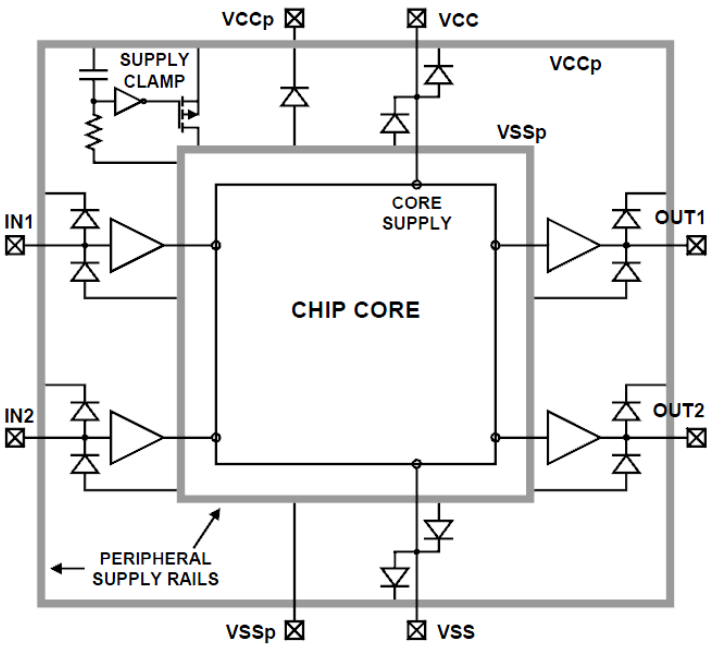
27#-1@2	vt	pre	100k	300k	500k	1000k
		0.902056	0.888492	0.847343	0.80956	0.786874
	shift		-0.01356	-0.05471	-0.0925	-0.11518

27#-5@2	vt	pre	100k	300k	500k	1000k
		0.877937	0.867269	0.814606	0.770182	0.685316
	shift		-0.01067	-0.06333	-0.10775	-0.19262

Physical Theories； SOI CMOS Device Models。

Relative Works of our Research Group

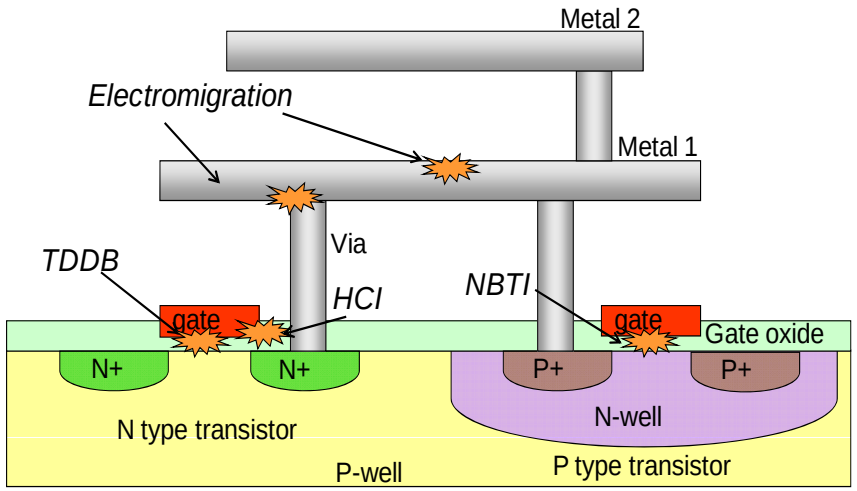
- Large Scale SOI CMOS Circuits



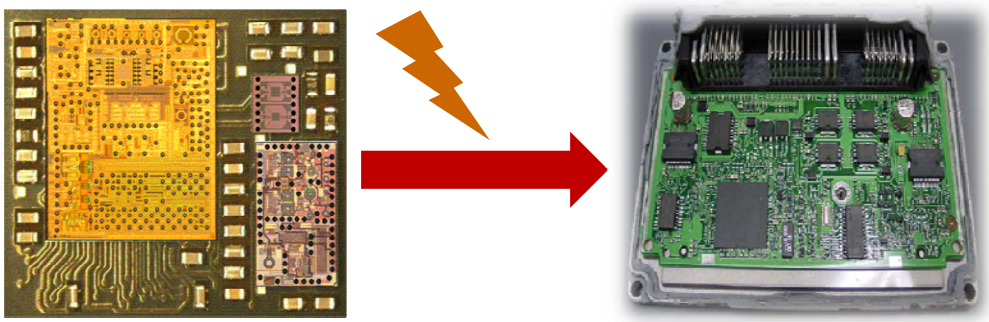
SRAM & Structured ASIC Circuits

Relative Works of our Research Group

- SOI CMOS Reliability and Electro-Magnetic Compatibility



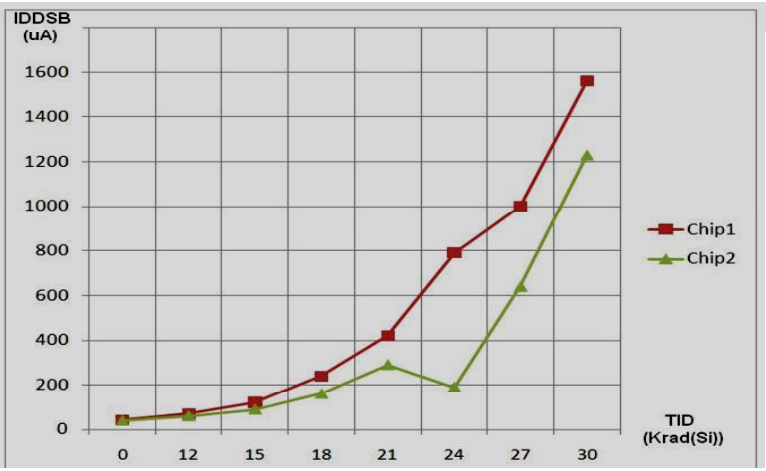
Temperature, voltage and radiation.

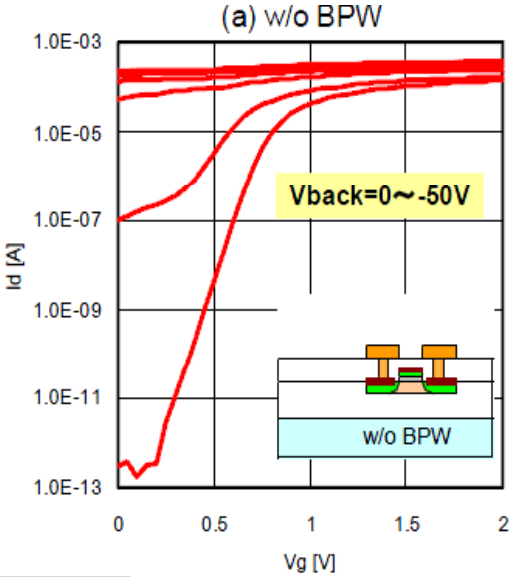


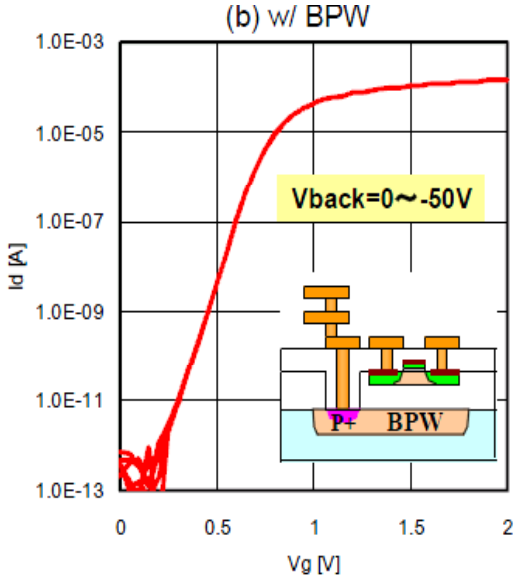
Reliability；Electro-Magnetic Compatibility；Radiation Hardening。

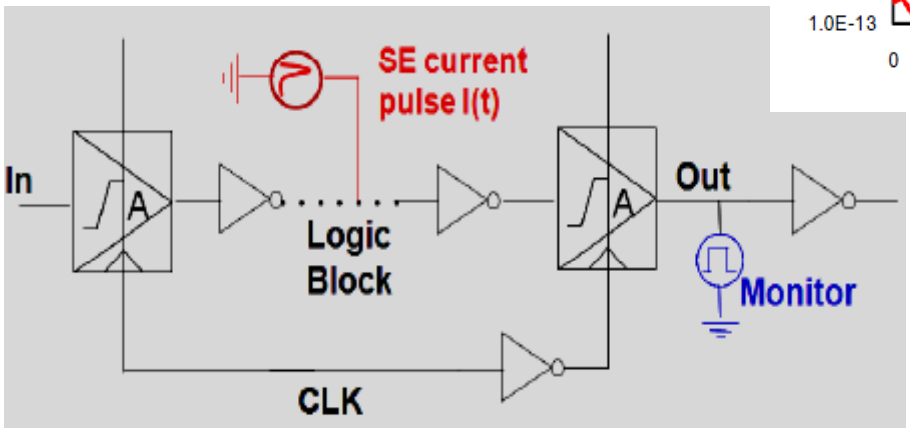
Relative Works of our Research Group

- Radiation Hardening by Technology and Circuit Design









$$I(t) = f(LET) \cdot \left(e^{-\alpha t} - e^{-\beta t}\right)$$

Reliability； Electro-Magnetic Compatibility； Radiation Hardening。

Summary

➢ Advanced SOI Electronics

- ◆ First choice beyond 10nm node CMOS Tech.
- ◆ Possibility to fabricate complex SOC.
- ◆ Ability for harsh environment application.

➢ Relative Works of our group

- ◆ SOI CMOS Device Physics.
- ◆ Large Scale SOI CMOS Circuits.
- ◆ SOI CMOS Reliability and EMC.
- ◆ Radiation Hardening by Tech. and Design.

➢ Farther efforts to improve chip ability

- ◆ Find and solve related scientific problems.
- ◆ To get better chips with excellent performance.

THANKS!