中国科学院高能物理研究所
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Weekly Meeting

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Vertex Specification

- CEPC Reference Detector(AGORA)
  - Spatial resolution < 5 um
  - Time stamp precision < 100 ns
  - Power Consumption in sensitive area < 40 mW/cm^2
  - Higgs & low-luminosity Z operation
  - Maximum hit rate expected ~ 39 MHz/cm^2@r_{min}=11 mm

Table 4.2: Vertex Detector Design Parameters

Parameter	Design
Spatial Resolution	~ 5 μm
Detector material budget	~ 0.8% X_0
First layer radius	11.1 mm
Power Consumption	< 40 mW/cm^2 (air cooling requirement)
Time stamp precision	100 ns
Fluence	~ 2×10^{14} Neq/cm^2
Operation temperature	~ 5 °C to 30 °C
Readout electronics	Fast, low-noise, low-power
Mechanical Support	Ultralight structures
Angular Coverage	$\lvert\cos\theta\rvert < 0.99$

Synergy with FCC-ee

- FCC-ee Vertex detector
  - **High-luminosity Z operation**
  - Maximum hit rate > 200 MHz/cm^2 @ r_{min}=11.7 mm
  - Maximum hit rate > 100 MHz/cm^2 @ r_{min}=13.7 mm
- CEPC-stitching design maximum readout speed up to 43.3 MHz per RSU
  - constrained by the RSU power 38 mW/cm^2

Projects for FCC-ee vertex detector, Dominik Dannheim
Detector background in vertex detector, Armin Ilg
@ FCC week 2026, Helsinki

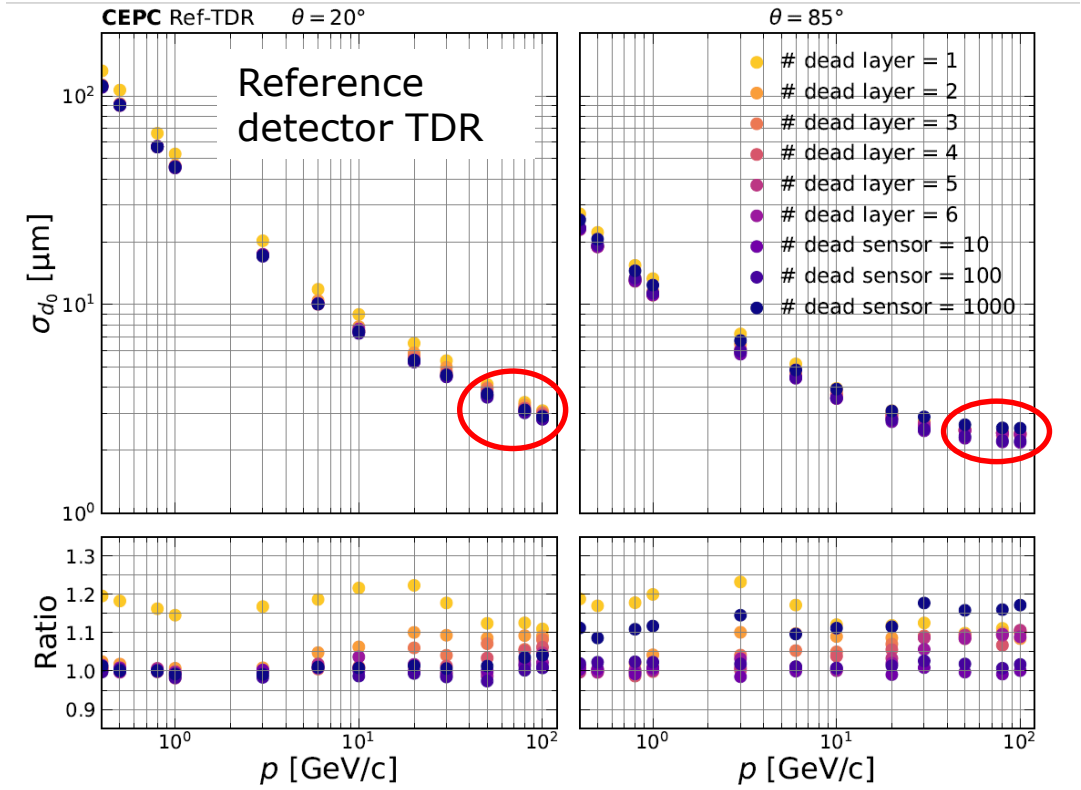
Table 4.9: Estimates of power consumption of one RSU. All values are for 27 °C temperature and 1.2 V power supply voltage.

Components	Pixel Analog	Pixel Digital	Biasing Block	Matrix Readout	Data Interface	RSU Total
Power [mW]	36	30	8	40	17	131

Mitigation to the high hit rate

- Keep CEPC-stitching design not changed
  - Increase r_{min} and optimize layer geometry for FCC-ee
  - Rectangular pixel to improve single point resolution at rφ direction < 3 um → compensate the loss for high momentum tracks (and FCC-ee also assumes 3 um)

Performance under sensor failure scenarios



$$\sigma_{r\phi} = a \oplus \frac{b}{p(\,\mathrm{GeV})\sin^{3/2}\theta}$$

Bread down the specification

- Pixel pitch：16 x 30 um
  - Analog front-end 16 x 16 um，pixel logic and readout 14 x 16 um
- Time precision：100 ns (σ_t)
  - Time walk 300 ns (peak-peak) + clock sampling 50 ns (peak-peak)
- Average power：<**100 mW/cm²** （total power 160 mW）for the first submission
  - Analog Front-end 80 mW，digital logic 10 mW，data readout 60 mW
  - DAC 2 mW，LVDS 3 mW, analog buffer 3 mW
  - Other 2 mW

Pixel sensor process

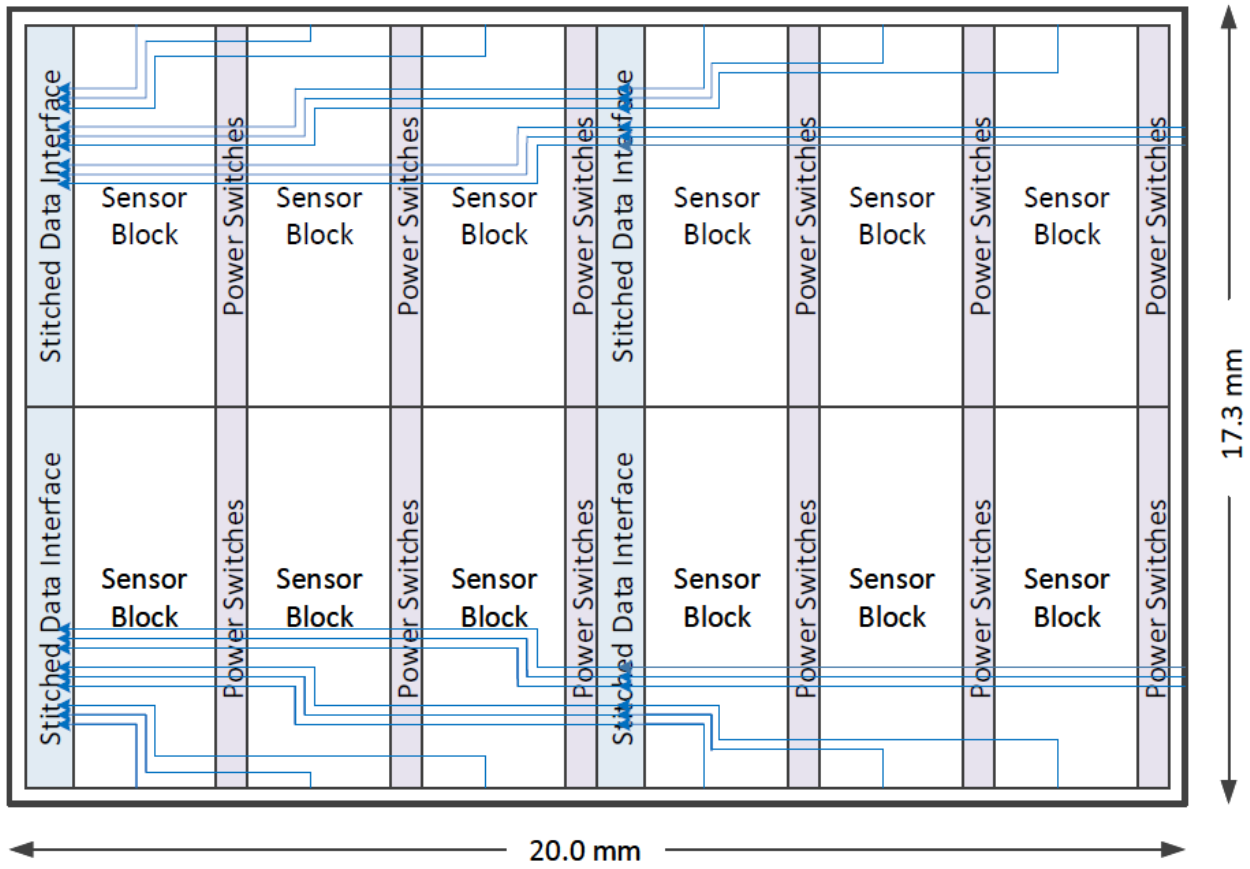
Ying Zhang, Zhijun Liang

- 90 nm CIS process, domestic foundry
  - **Mature production line**
  - **Quadruple-well**
  - **Support High-resistivity epitaxial layer**
  - Custom implant not allowed yet, needed for radiation hardness
- Contacting the foundry via an agent
  - PDK provided, 5 metal layers
  - Qualified HR wafers are under investigation
  - Engineering run only
  - Quotation will be provided based on the device choice

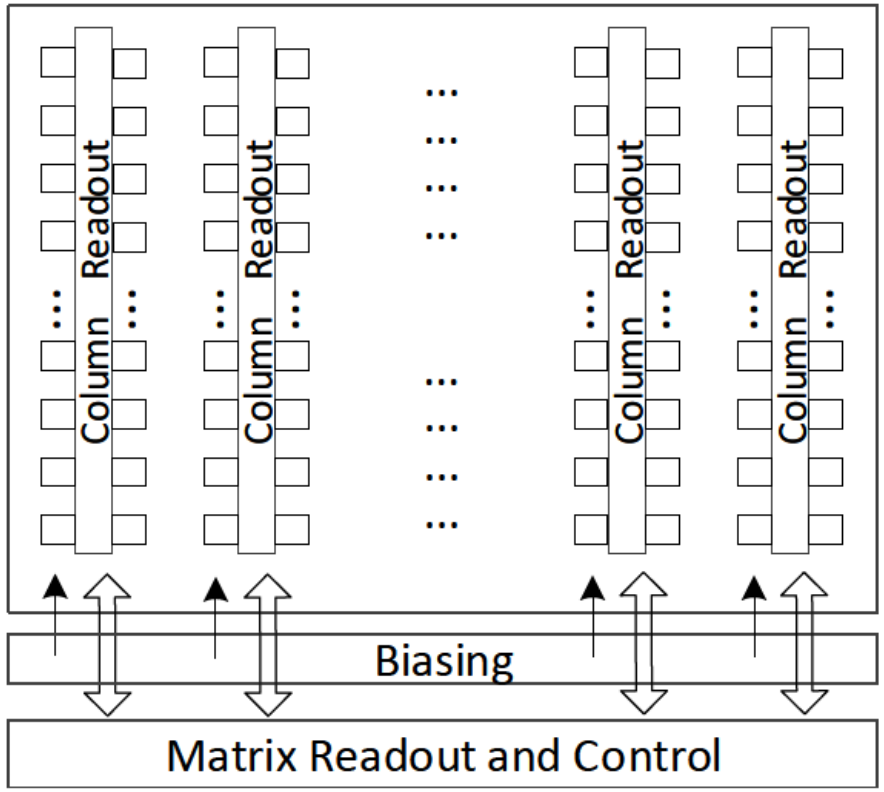
Validation of process

- Only Sensor Block for this submission
  - Compatible with the **Stitched sensor prototype design** (Reference Detector TDR)

top-level floor plan of a RSU (Repeated Sensor Unit)

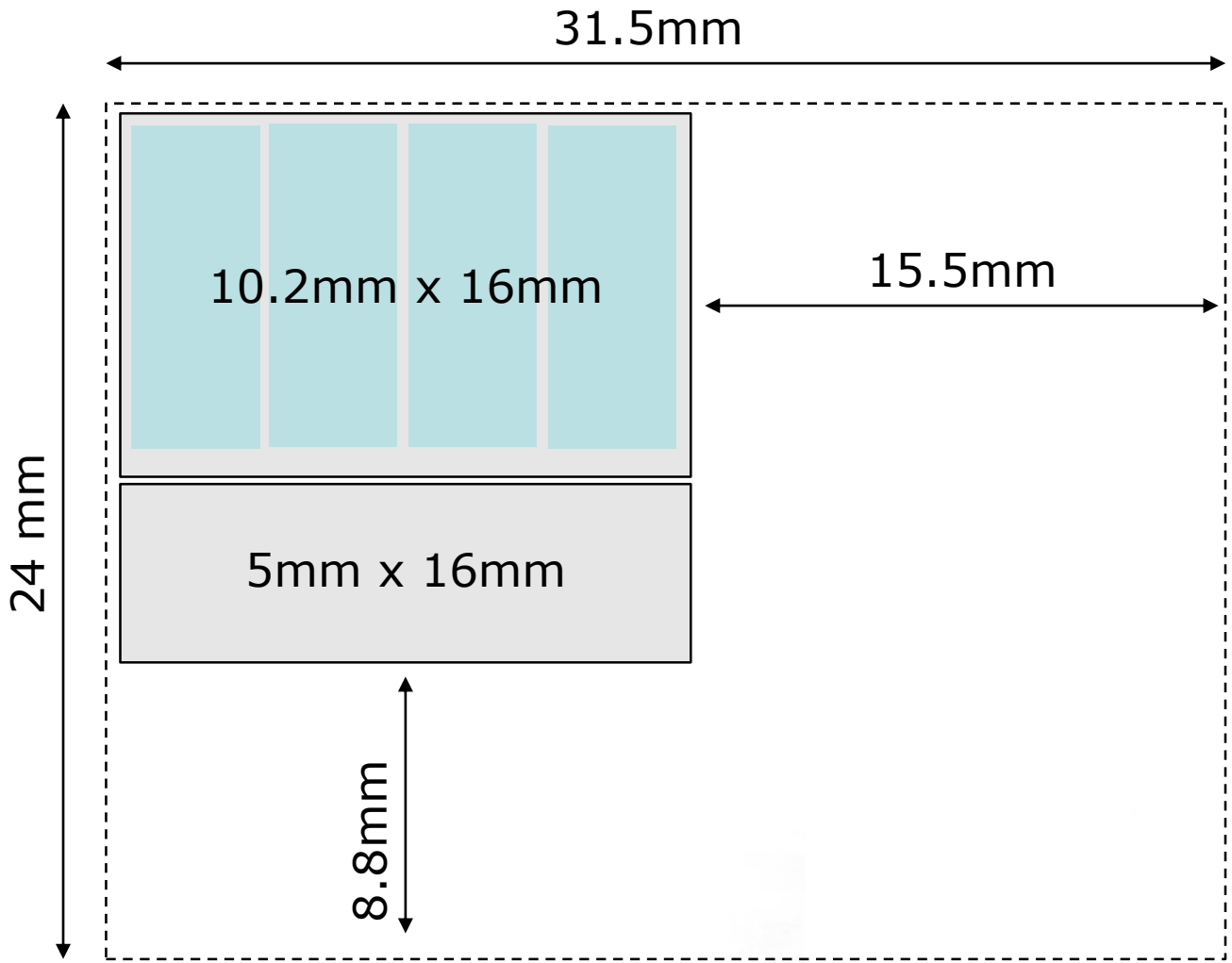


Architecture of the Sensor Block



Preliminary floor plan

- Maximum Mask Area：24mm x 31.5mm
- Estimated design Area: 10.2mm x 16mm
  - Pixel pitch 16um x 30um
  - Matrix height 16um x 512行 = 8.192 mm
  - Matrix width 30um x 512列 = 15.36 mm
  - 4 sensor blocks
  - Peripheral + Pad height 2mm
- Independent test circuit module
  - 5mm x 16mm



Pixel Sensor Task Assignment

- Team members from the past TaichuPix and JadePix team

Task	Responsible person	Affiliation
Integration and verification	Yunepng Lu & Han Yu	IHEP
Process and analog front-end	Ying Zhang	IHEP
Matrix readout logic	Tianya Wu & Tong Li	NCU
Peripheral data readout	Xiaoming Wei & Student	NWPU
LVDS	Ping Yang & Student	CCNU
DAC	Ping Yang & Baoshu Hao	CCNU
Negative biased PAD	Ping Yang & Student	CCNU
Analog buffer	Hao Xiong	IHEP
PLL & Serializer & CML	Ping Yang & Quanwei Hu	CCNU
ASIC consultant	Wei Wei	IHEP
TCAD	Bo Liu, Ziying Liu, Ying Zhang, Zhijun Liang	NKU & IHEP

Key points of design

- Analog front-end: TN，FPN，Time walk，power (ongoing)
- Logic analysis on FastOR signal and desertion
  - FastOR assertion and Freeze function（见郁晗报告）
  - FastOR desertion and readout debug（见邓思琪的分析）
- Understanding and definition of time stamp precision
  - Key contributor identified（见郁晗报告）
- Timing, power and area optimization on peripheral readout (to start)
- Static power analysis on full chip (in plan)
- Testability (in plan)
  - Single module verification
  - Avoid single-point failure in the signal chain

Schedule

- Tape-out in March 2027 (Preliminary plan, 9 months)
  - Scheme Design – 8 weeks, mid-July
  - Scheme Review – 1 week, late July
  - Module Design – 4 weeks, late August
  - Schematic Review – 1 week, mid-September
  - Layout Design – 8 weeks, mid-November
  - System Integration – 8 weeks, mid-January
  - Design Verification – 4 weeks, mid-February
  - Design Review – 1 week, late February
  - Submission – 1 week, early March
  - Tape-out in March 2027

Relevant task in MOST3

- 课题2：硅像素探测器和无线数据传输技术
  - **Vertex detector prototype:** position resolution 3 um, time stamp precesion100 ns, power consumption 100 mW/cm^2
  - HVCMOS tracker prototype: position resolution 10 um, time stamp precesion10 ns, power consumption 200 mW/cm^2
  - Wireless data transmission: total data rate > 30 Gbps

Proposal of the design name

- Pixelated Resolution-Enhanced CMOS Imaging Sensor （PRECIS）
- 含义解析：
  - PRECIS：取自英语单词 “Precision” （精确）和 “Precise” ，体现了粒子物理实验对高精度的极致追求。
  - Pixelated：强调像素化成像能力。
  - Resolution-Enhanced：突出了高空间分辨率的优势。
  - 优势： 简洁明了，直接用名字为探测器的质量背书。