PRECISE / CHIP ARCHITECTURE STUDY

芯片架构与功耗评估

基于 Hit rate=150 MHz/cm² 评估，考虑 200 MHz/cm² 设计

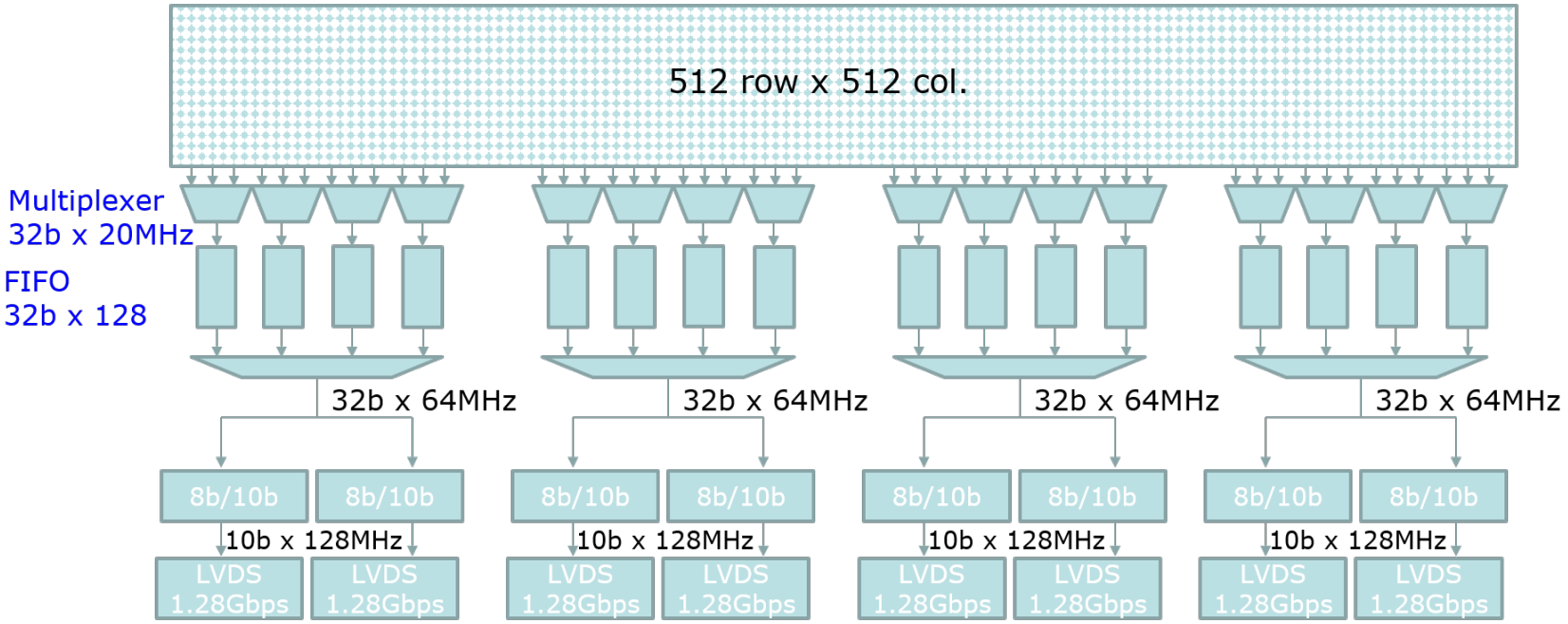
结论：

- 150 MHz/cm^2 在现有 4 组×64 MHz 架构下满足；200 MHz/cm^2 需要增加并行读出。
- 最内层考虑束流散热，可提高功耗预算；第二层可通过降频、关闭LVDS满足功耗预算。

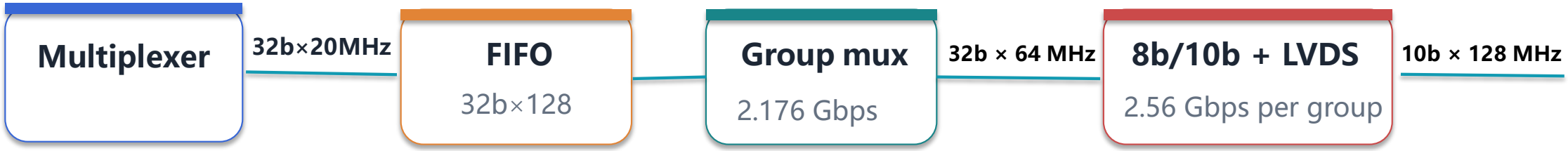
2026-08-27

Peripheral Readout

- Hit rate决定了data transmission的端口数量和功耗（最内层 Maximum pixel hit rate =150MHz·cm^{-2}）
  - 252 MHz pixel hit rate x 40 bit = 10.08 Gbps

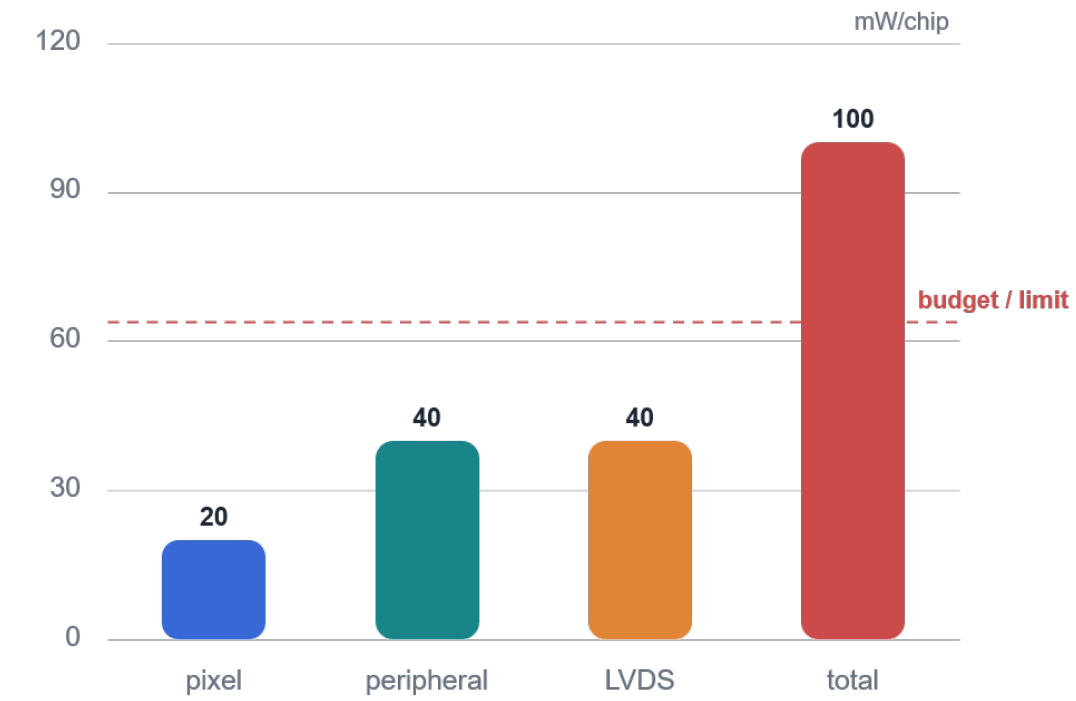


- 512 × 512 pixel
- 16 regions: 16 × (16 double columns + 1 Multiplexer + 1 FIFO)
- 4 groups: 4 × (4 regions + 2 8b/10b + 2 LVDS)



功耗评估

最内层 Pixel hit rate =150MHz·cm-2



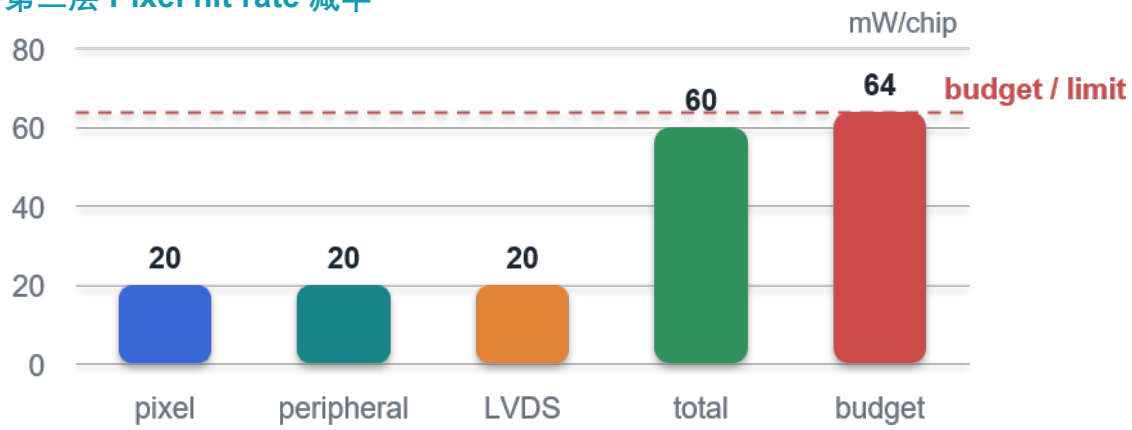
P_density = 100 / 1.6 = 62.5 mW/cm^2

P_budget= 40 mW/cm^2（CEPC气冷散热限制）

最内层功耗说明

- 束流辅助散热允许 **Power> 40mW/cm^2**；但仍需实际热路径和结构验证。

第二层 Pixel hit rate 减半

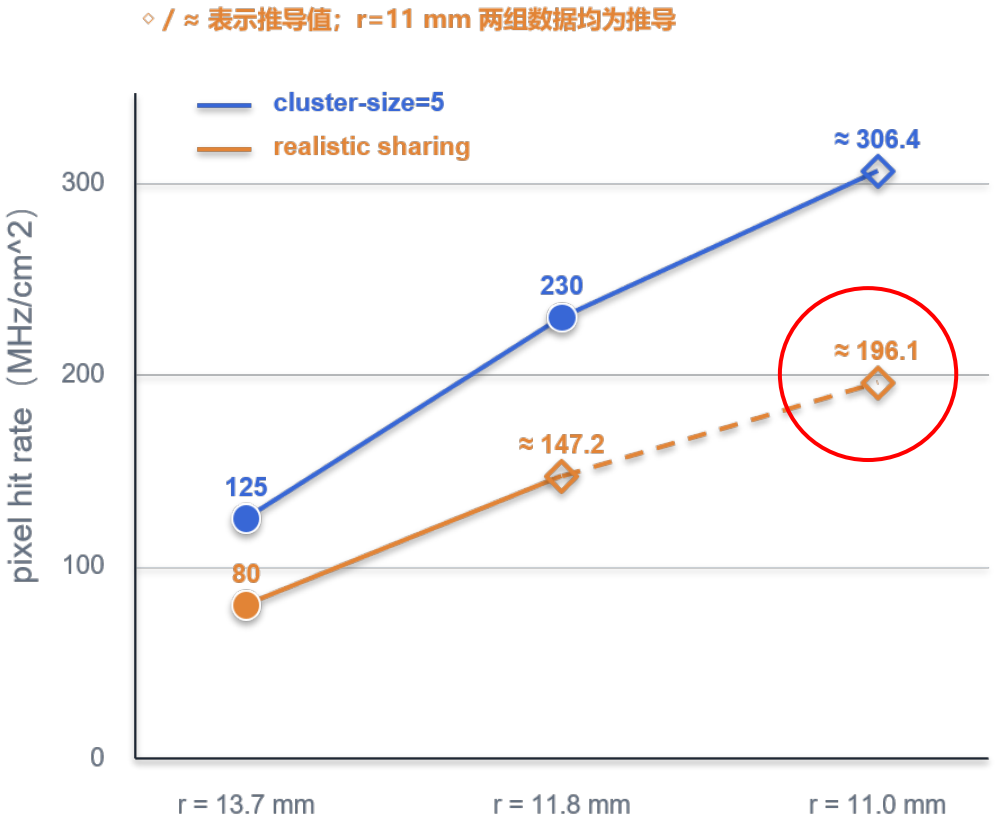


P_L2,density = 60 / 1.6 = 37.5 mW/cm^2

第二层功耗说明

- **peripheral** 时钟减半
- 关掉一半**LVDS**
- 功耗满足预算

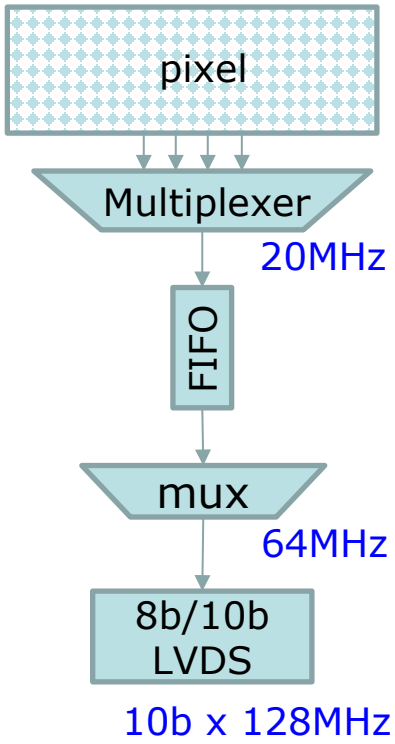
Pixel hit rate =200MHz·cm^{-2}评估



- AGORA vertex inner radius 11mm
  - Pixel hit rate =200MHz·cm^{-2} 来设计架构

- 320 MHz pixel hit rate x 40 bit = 12.8 Gbps
- 16 FIFO 分成 8 个 groups，输入320/8=40 Mhit/s
- group mux 读出保持 64MHz（考虑减小>40Mhz）
- LVDS 数量翻倍16个（10个正好，不方便通道映射）

➢ 待考虑 timestamp integration 受 hit rate 影响



总结

- Hit rate=150MHz·cm^{-2} 对应的设计架构如下图
  - 具体实现方案（如Multipexer, SRAM）待讨论
- Hit rate=200MHz·cm^{-2}的设计架构有待完善（使用 200 or 150 ???）
- Timestamp Integration/precision 待考虑