

芯片架构与功耗评估

基于 Hit rate= 200 MHz/cm² 设计

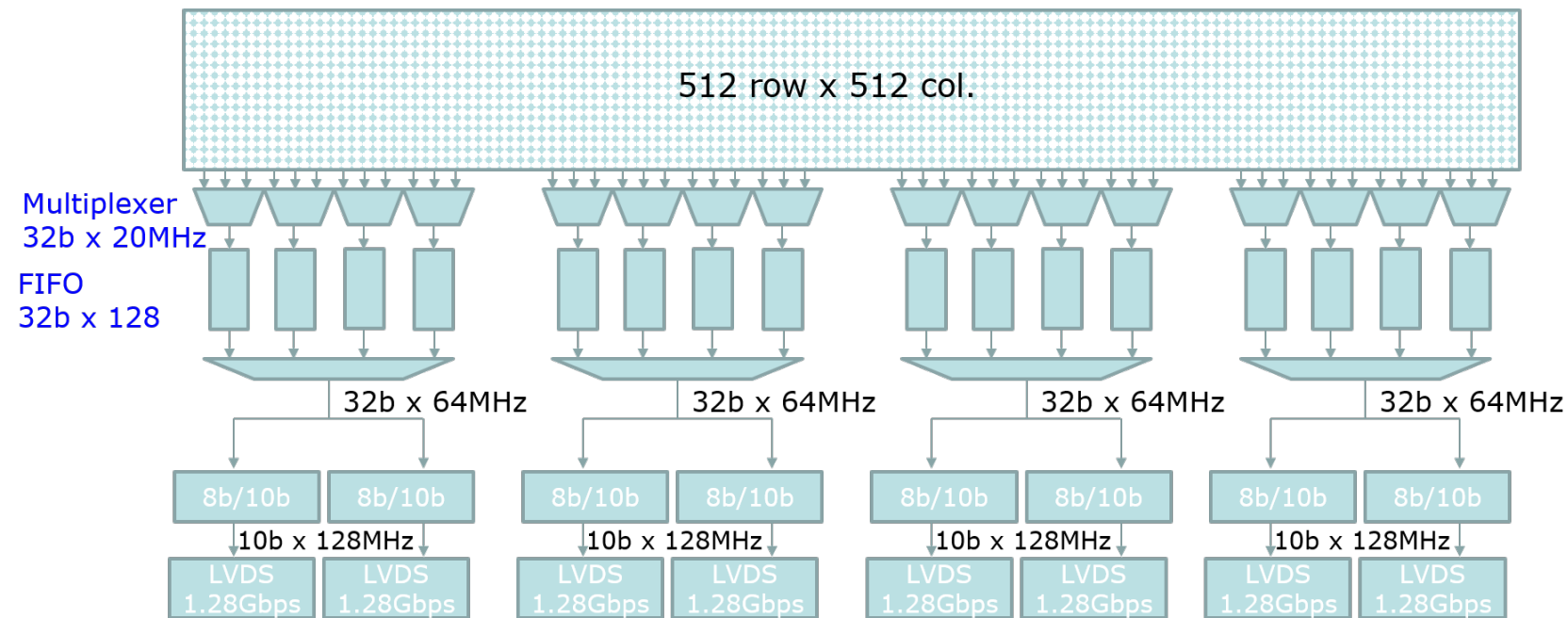
结论:

- 200 MHz/cm² 在现有 4 组×64 MHz 架构下满足。
- 最内层考虑束流散热，可提高功耗预算；第二层可通过降频、关闭LVDS满足功耗预算。

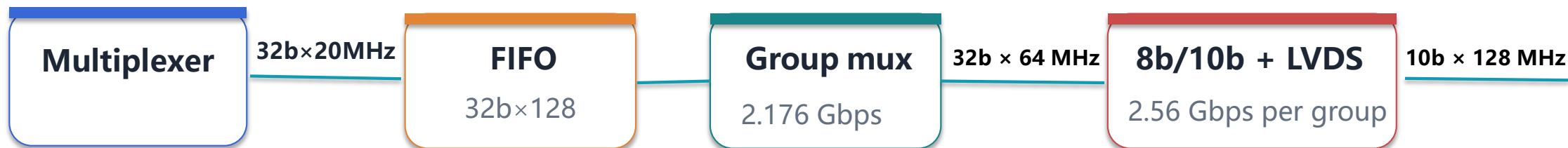
Peripheral Readout



- Hit rate决定了data transmission的端口数量和功耗 (最内层 Maximum pixel hit rate = $200\text{MHz}\cdot\text{cm}^{-2}$)
 - 252 MHz pixel hit rate x 40 bit = 10.08 Gbps



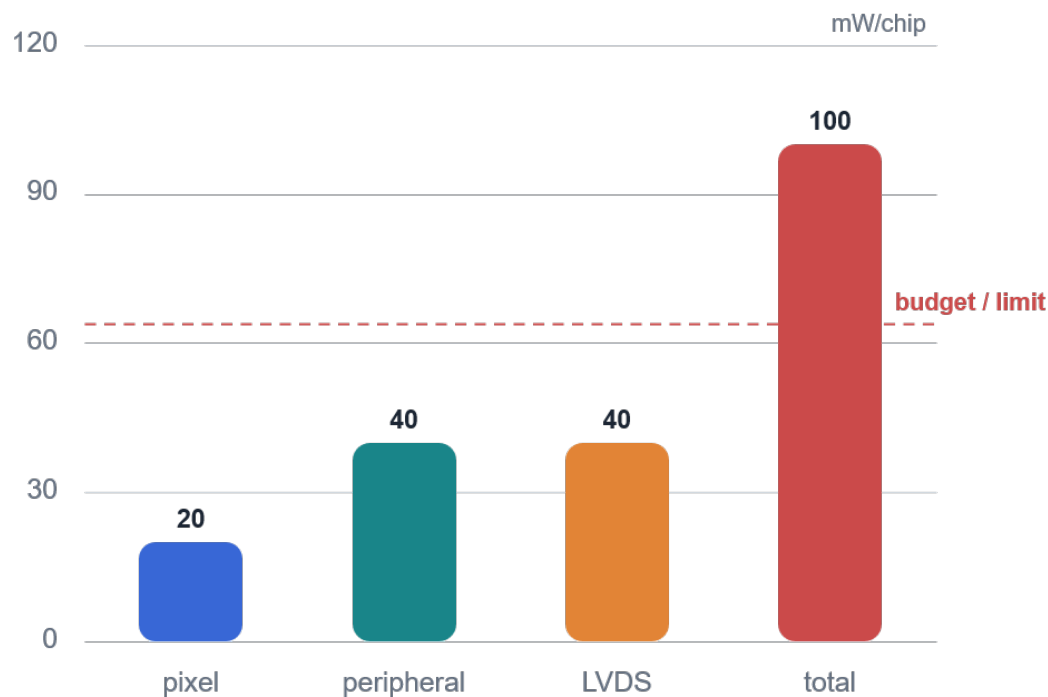
- 512 × 512 pixel
- 16 regions: 16 × (16 double columns + 1 Multiplexer + 1 FIFO)
- 4 groups: 4 × (4 regions + 2 8b/10b + 2 LVDS)



功耗评估



最内层 Pixel hit rate =150MHz-cm-2



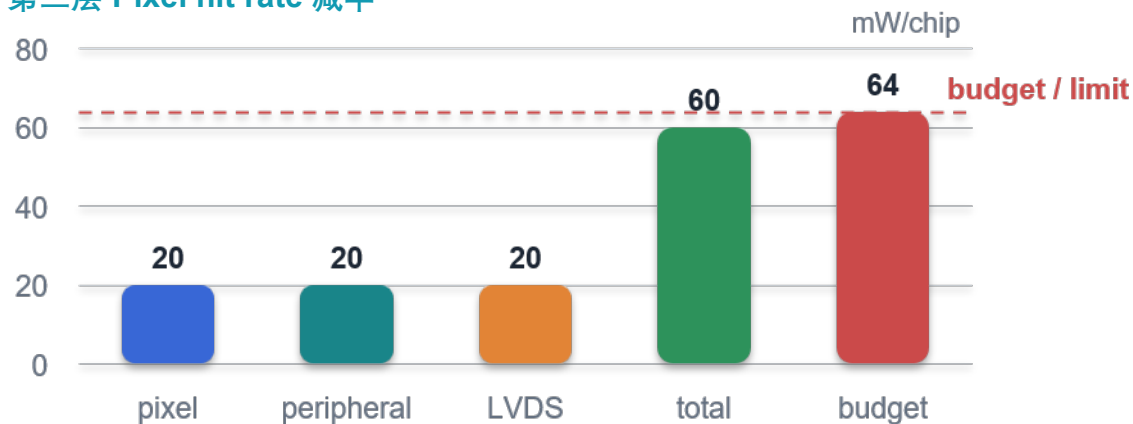
$$P_{\text{density}} = 100 / 1.6 = 62.5 \text{ mW/cm}^2$$

$P_{\text{budget}} = 40 \text{ mW/cm}^2$ (CEPC气冷散热限制)

最内层功耗说明

- 束流辅助散热允许 $\text{Power} > 40 \text{ mW/cm}^2$ ；但仍需实际热路径和结构验证。

第二层 Pixel hit rate 减半

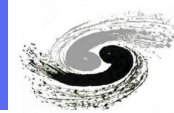


$$P_{\text{L2,density}} = 60 / 1.6 = 37.5 \text{ mW/cm}^2$$

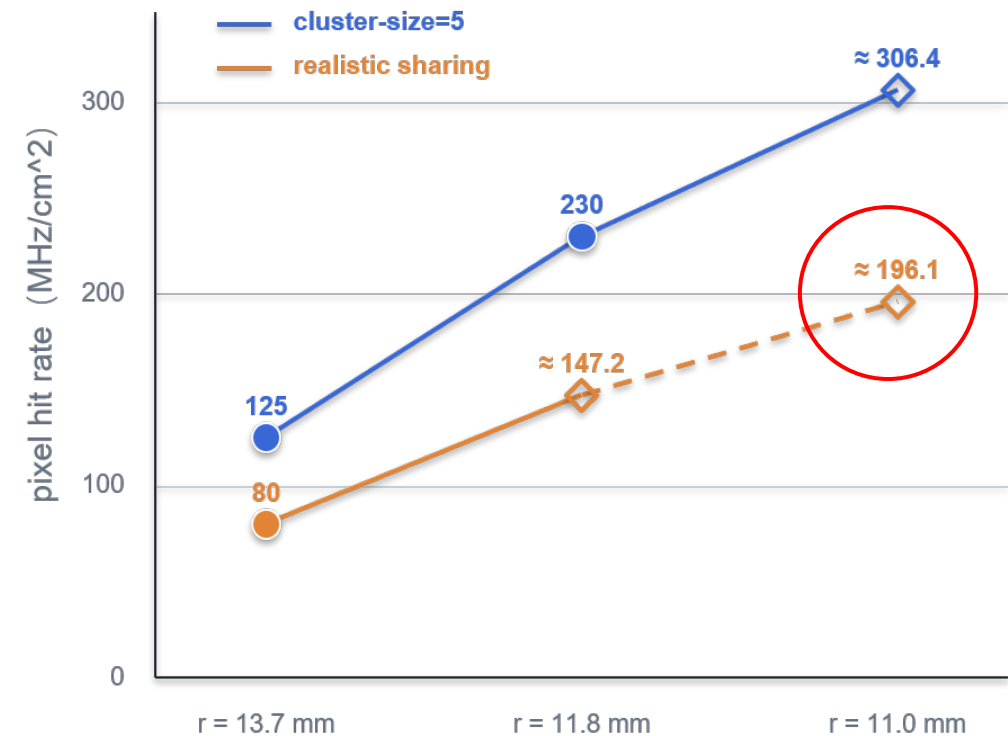
第二层功耗说明

- peripheral 时钟减半
- 关掉一半LVDS
- 功耗满足预算

Pixel hit rate = $200\text{MHz}\cdot\text{cm}^{-2}$ 评估



◇ / $\approx$ 表示推导值; $r=11\text{ mm}$ 两组数据均为推导



● AGORA vertex inner radius 11mm

■ Pixel hit rate = $200\text{MHz}\cdot\text{cm}^{-2}$ 来设计架构

总结



- Hit rate= $200 \text{ MHz} \cdot \text{cm}^{-2}$ 对应的设计架构如下图
 - 具体实施方案 (如Multiplexer, SRAM) 待讨论
- Timestamp Integration/precision 待考虑

