



華中師範大學
CENTRAL CHINA NORMAL UNIVERSITY



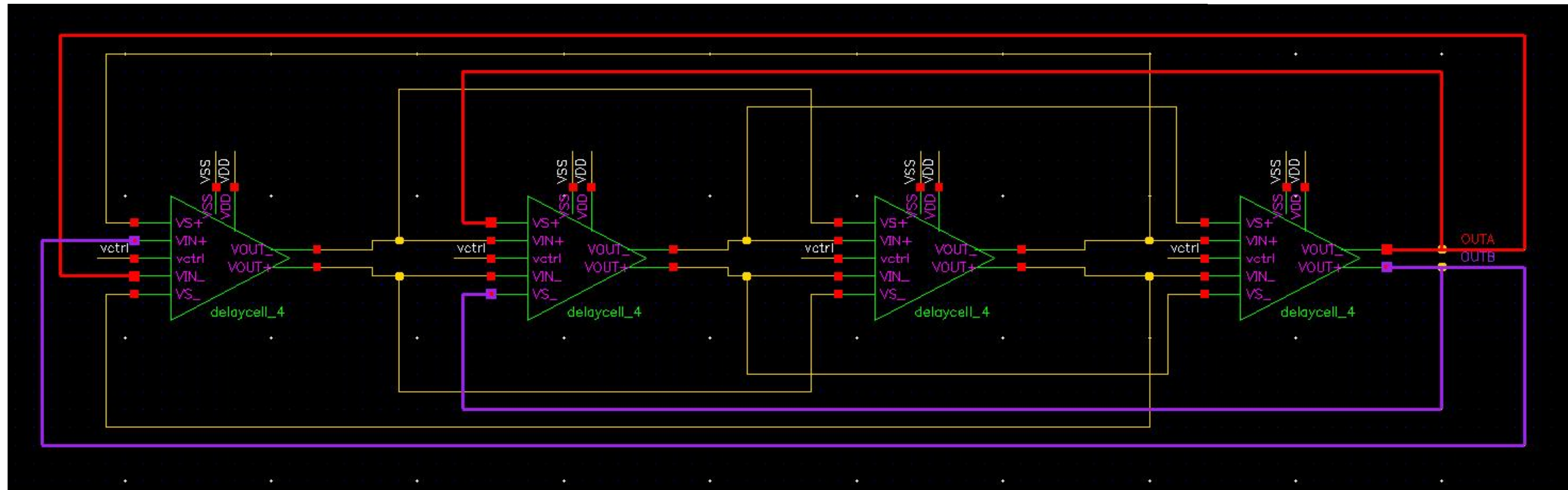
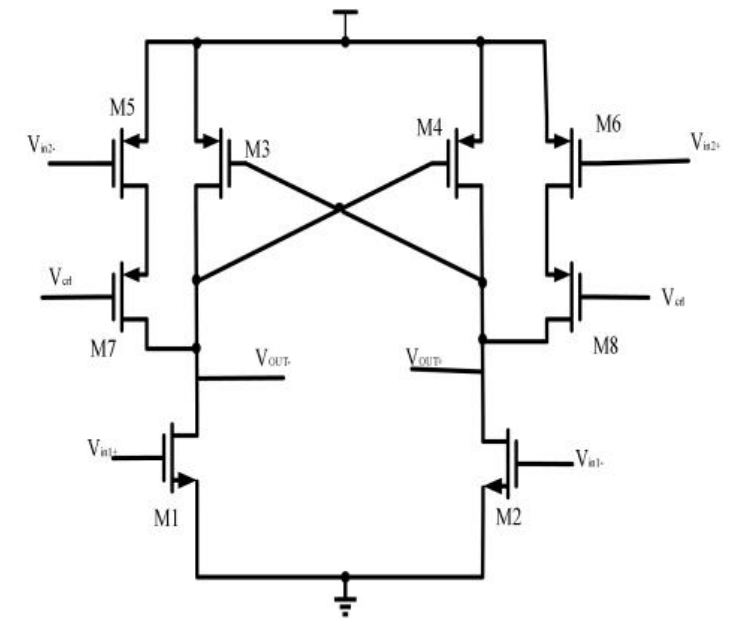
组会汇报

汇报人：胡权威

日期：2026.9.24

VCO结构选择

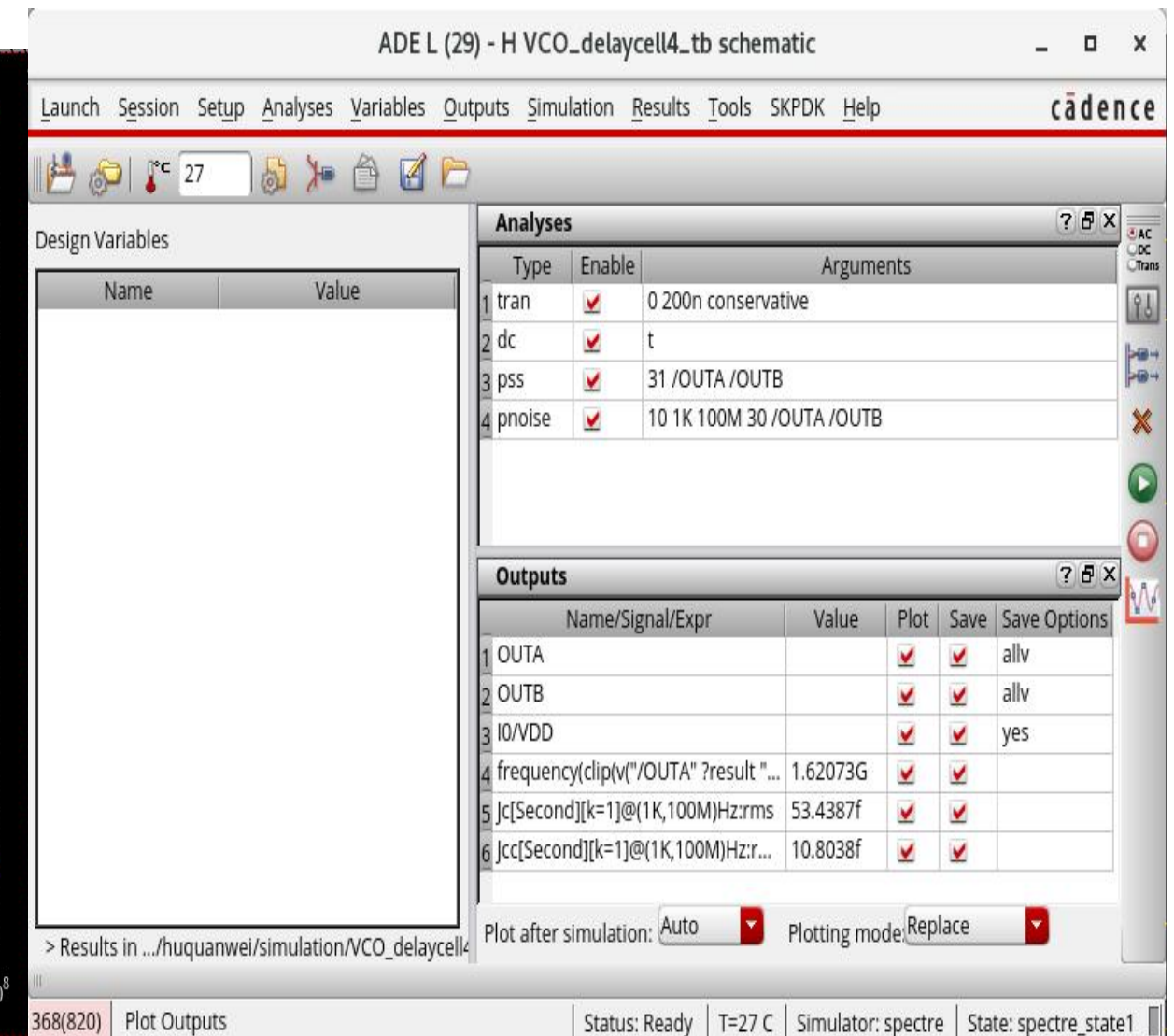
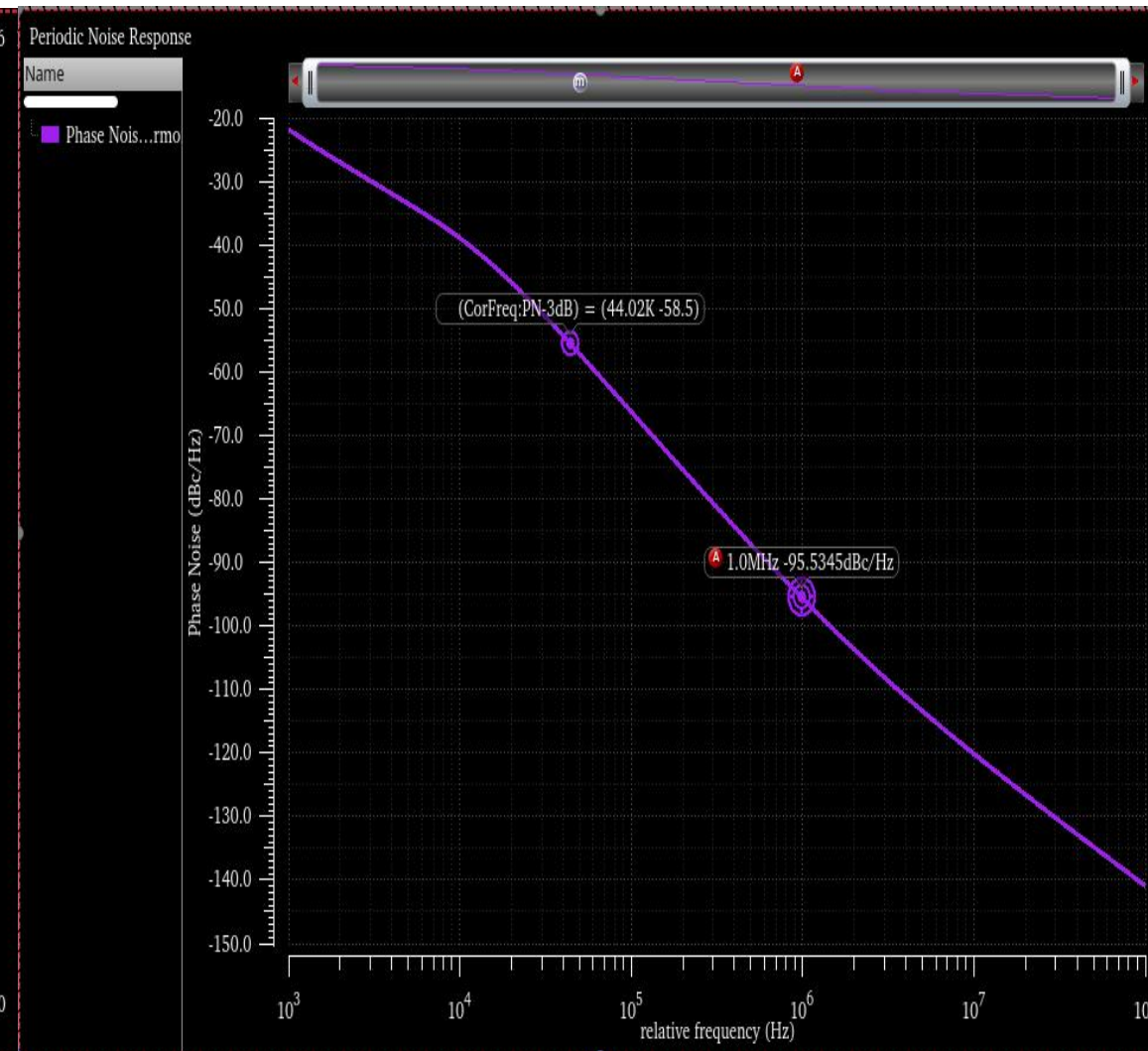
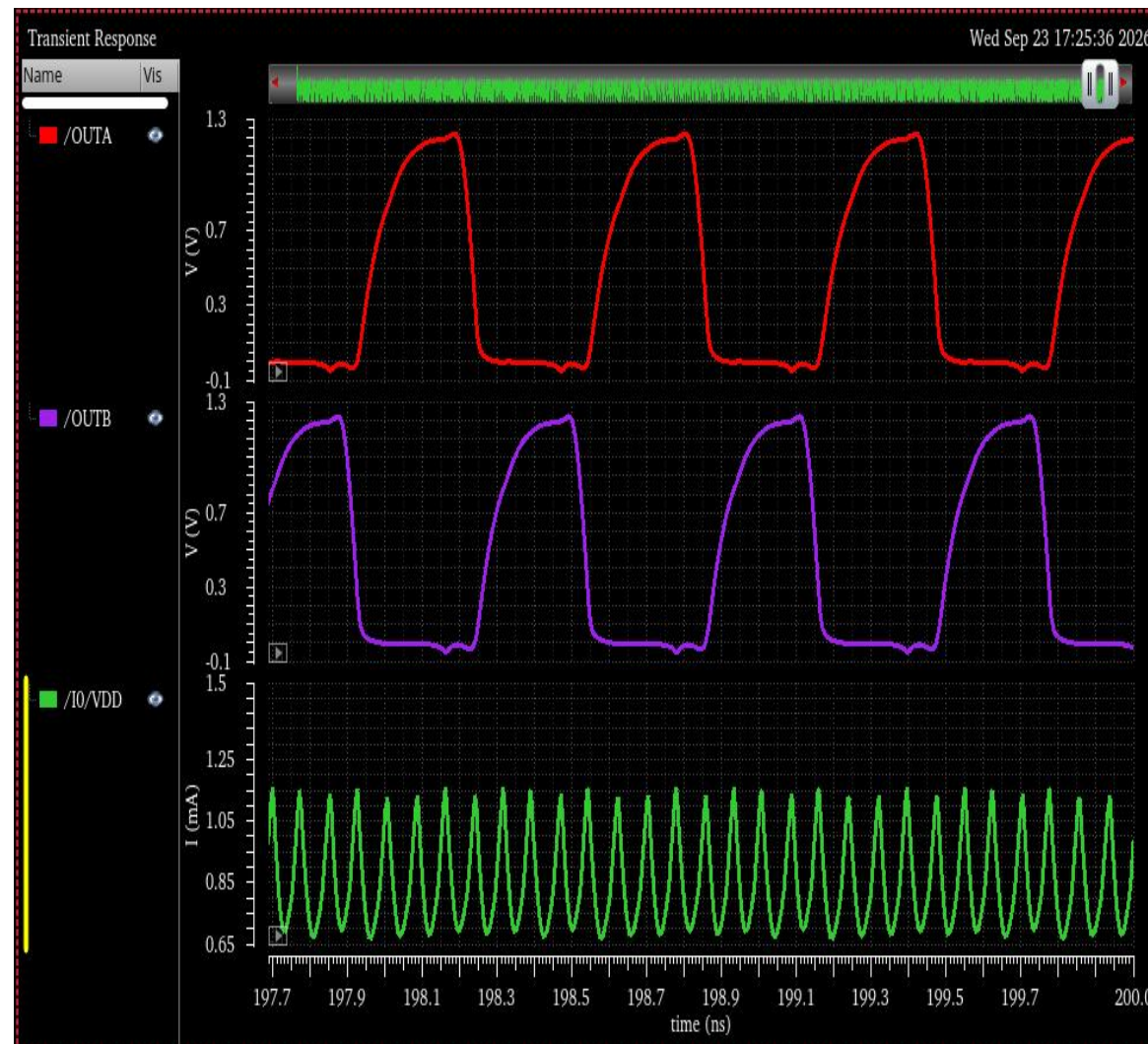
前馈型环形压控振荡器（Feedforward Ring VCO）通过在传统多级环形结构中引入跨级传输的“前馈路径”来突破最高频率上限。它的核心原理是让每个延迟单元同时接收相邻上一级的主路径信号和跨级传递的超前信号。通过调节控制电压（**vctrl**），电路能够动态改变这两路信号的叠加权重。当增大前馈信号的权重时，整体的单级等效延迟会显著缩短，这使得该结构不仅能获得极宽的频率调谐范围，还能达到远超传统环形VCO的超高振荡频率。





VCO架构

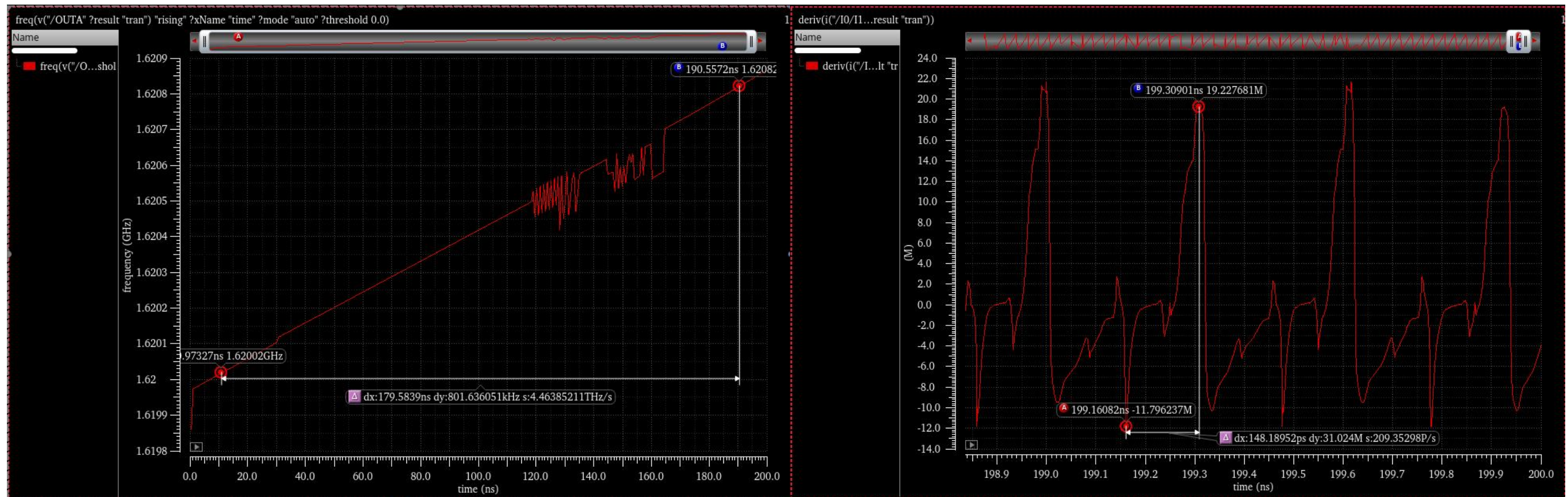
- 前馈型
- 振荡频率1.6G
- 平均电流862.3u
- 1M相噪95.5dBC/HZ, JC11fs, JCC54fs





VCO架构

- 在控制电压 v_{ctrl} 保持理想恒定的情况下，VCO的输出瞬态频率并未立即稳定在一条水平直线上，而是随着时间推移呈现出持续、单调的缓慢向上漂移。在近180ns的时间内，频率从约1.6200GHz逐渐爬升至1.6208GHz，整体漂移量约为800kHz。相对于1.62GHz的中心频率，偏差不到0.05%，属于极微小的波动。
- 在内部稳态建立期间，前馈路径与主路径的相对驱动权重在发生极微弱的相对变化，导致每级的等效传播延迟随时间极其缓慢地缩短，宏观上就表现为输出频率一点点往上漂。
- delaycell电流变化率巨大，峰值19M



VCO架构

- 图示为伪差分电流饥饿型VCO。它通过上下偏置管（受VBN/VBP控制）调节充放电电流来改变振荡频率，级间的交叉耦合管用于维持差分对称性
- 在大信号波形翻转到末期时，开关管完全导通，导致偏置管两端的漏源压差（ V_{ds} ）被严重压缩，使其被迫从饱和区跌入线性区（三极管区）
- 调谐线性度变差，抗电源噪声能力下降（PSRR恶化），相位噪声变差

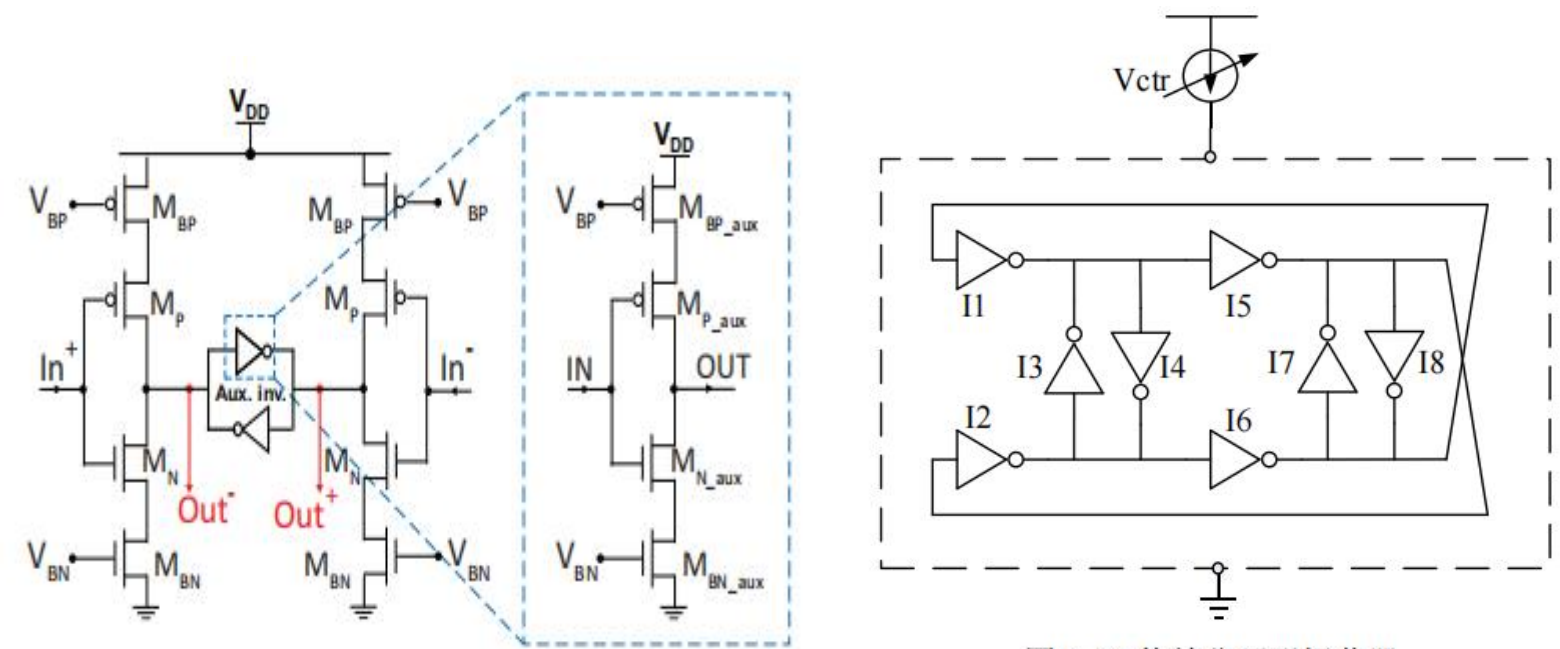
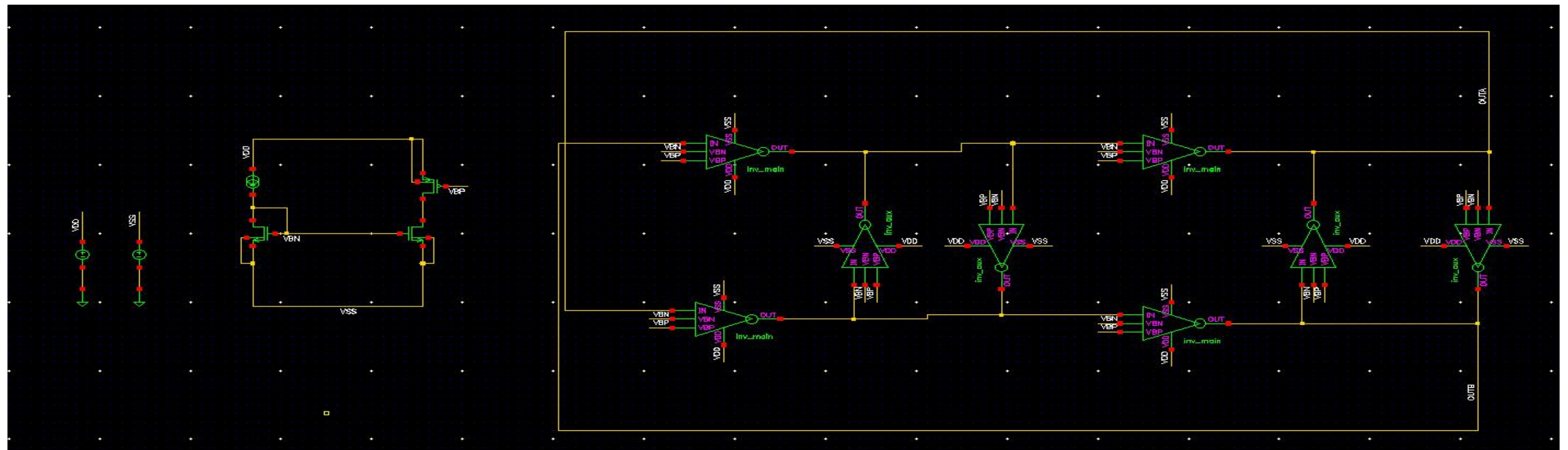


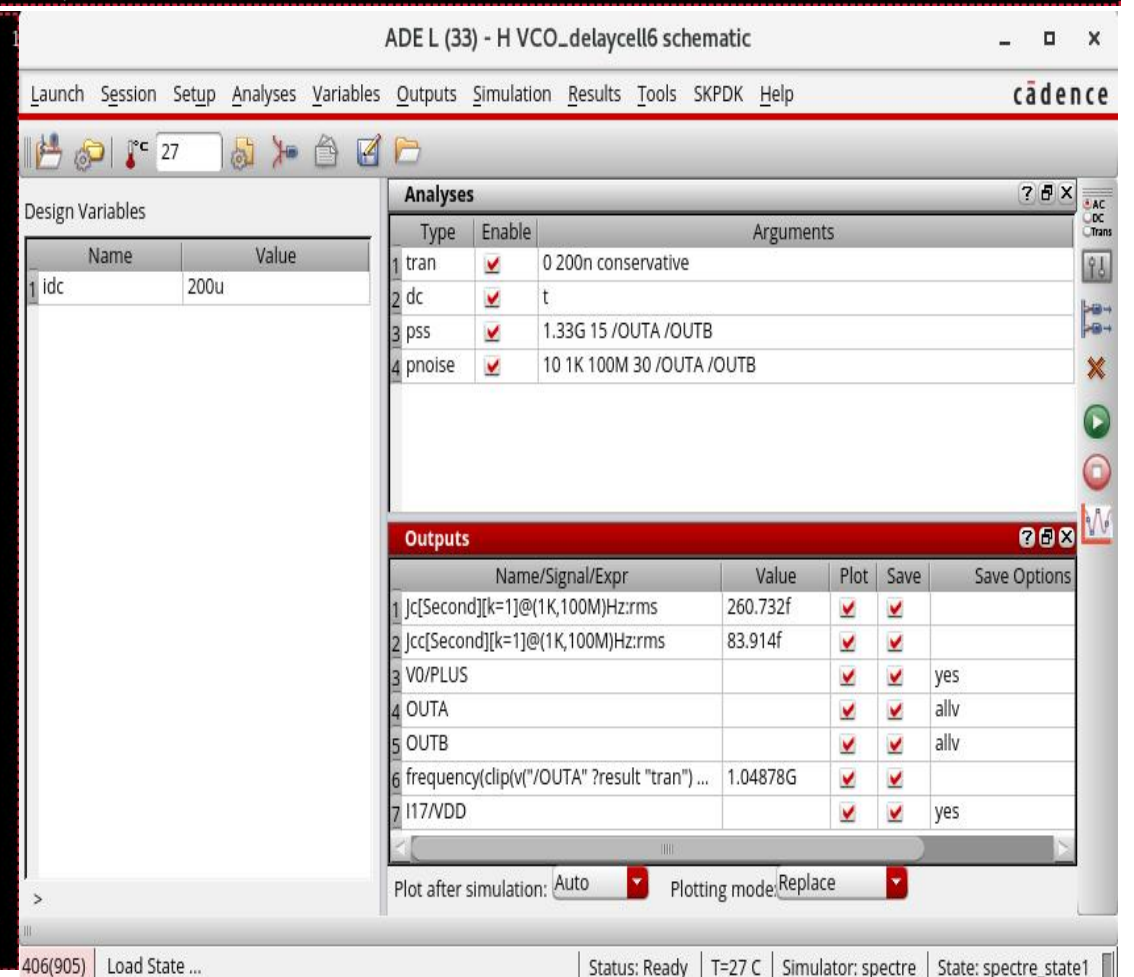
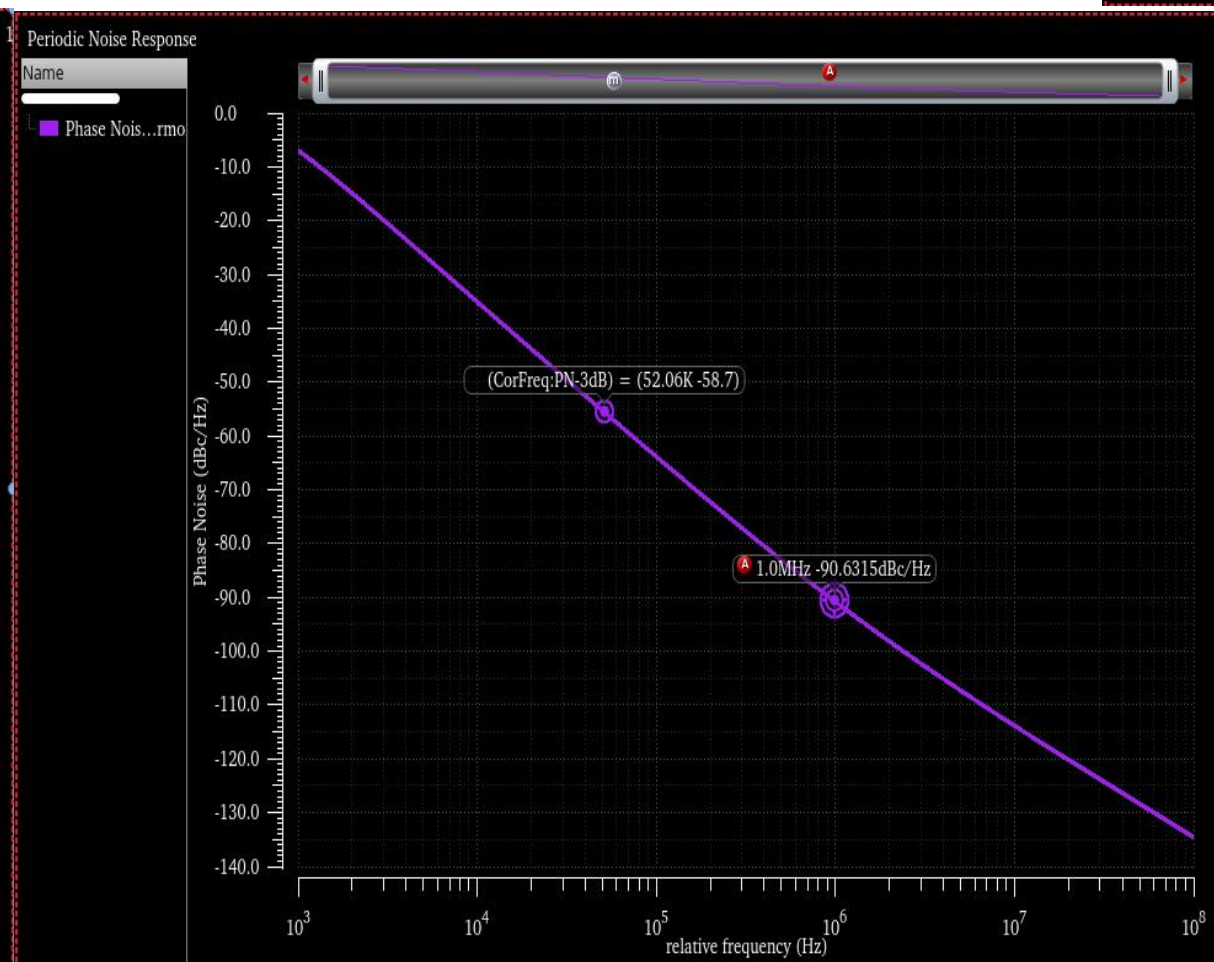
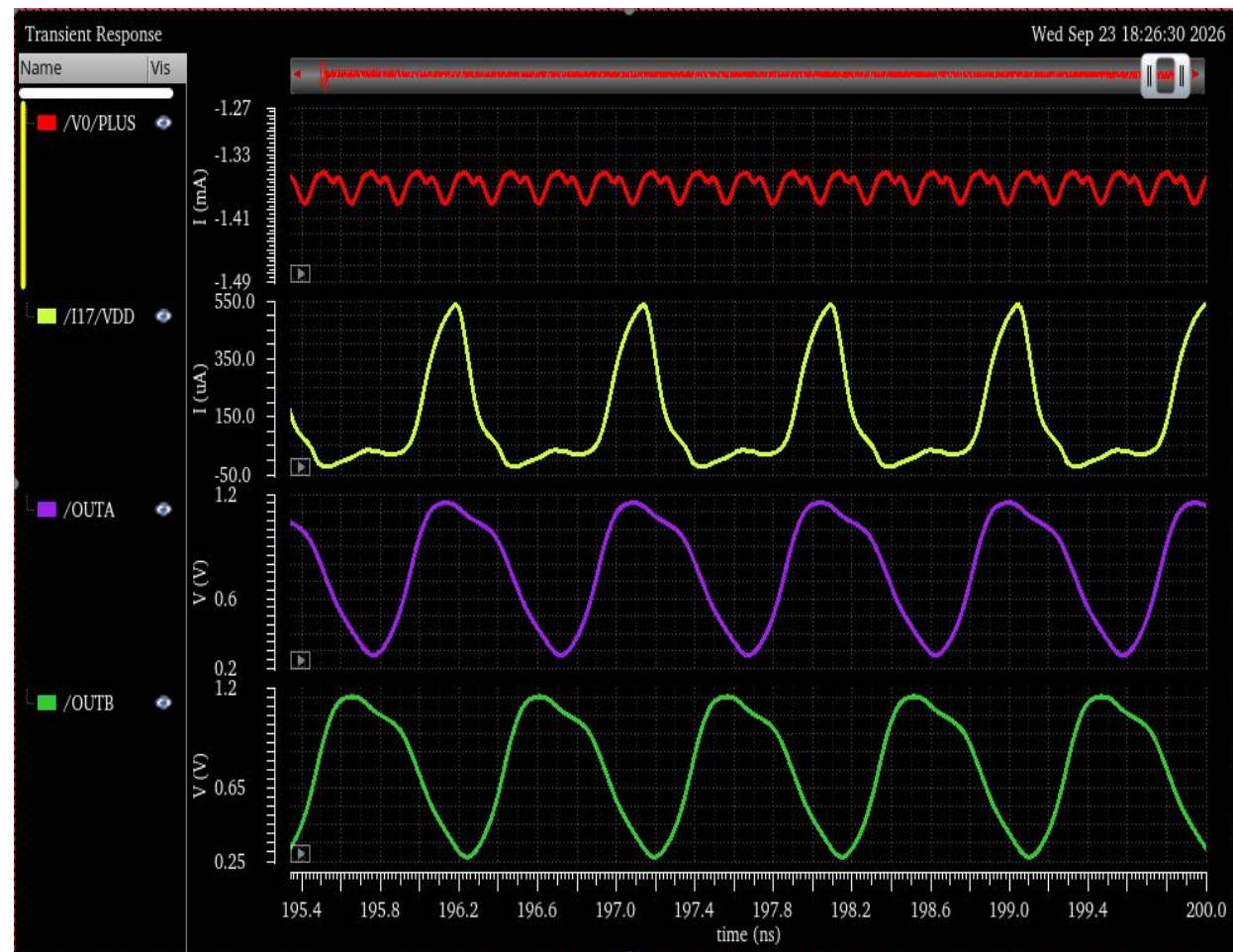
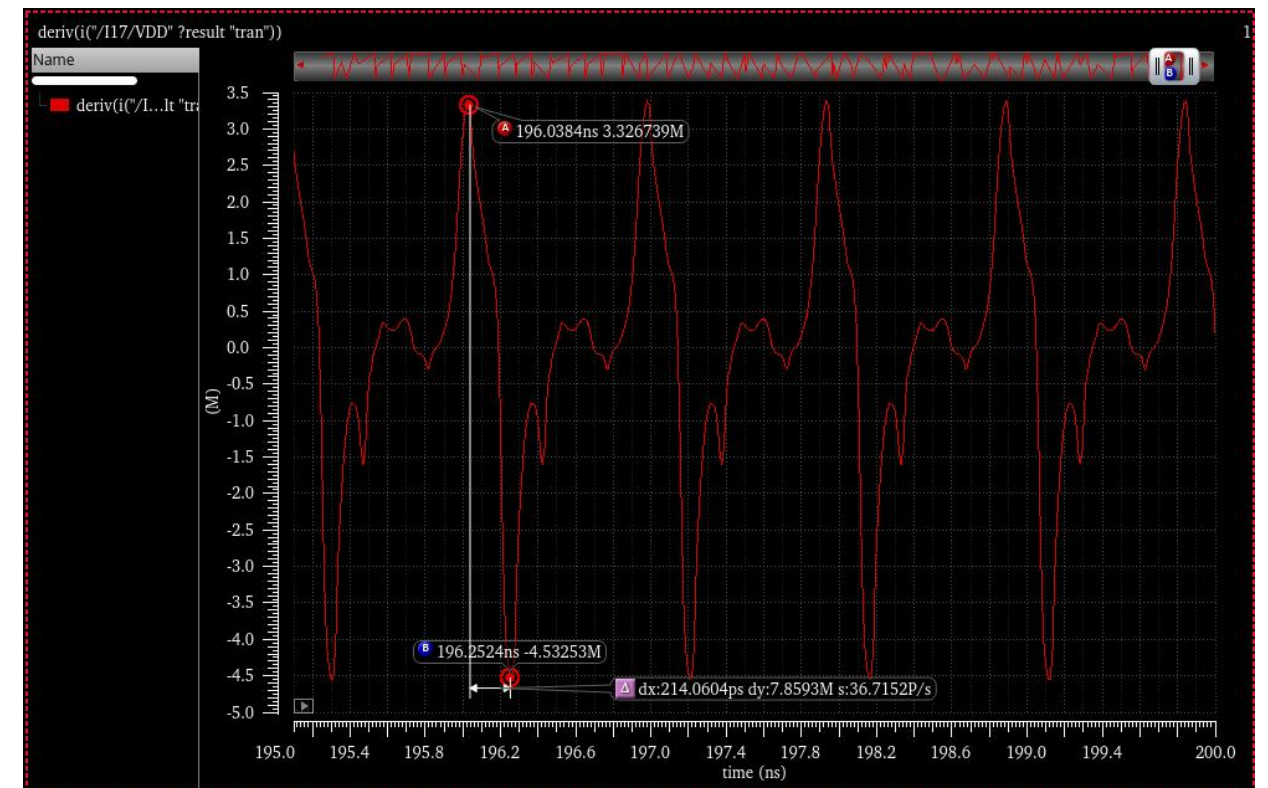
图 5-23 伪差分环形振荡器





VCO架构

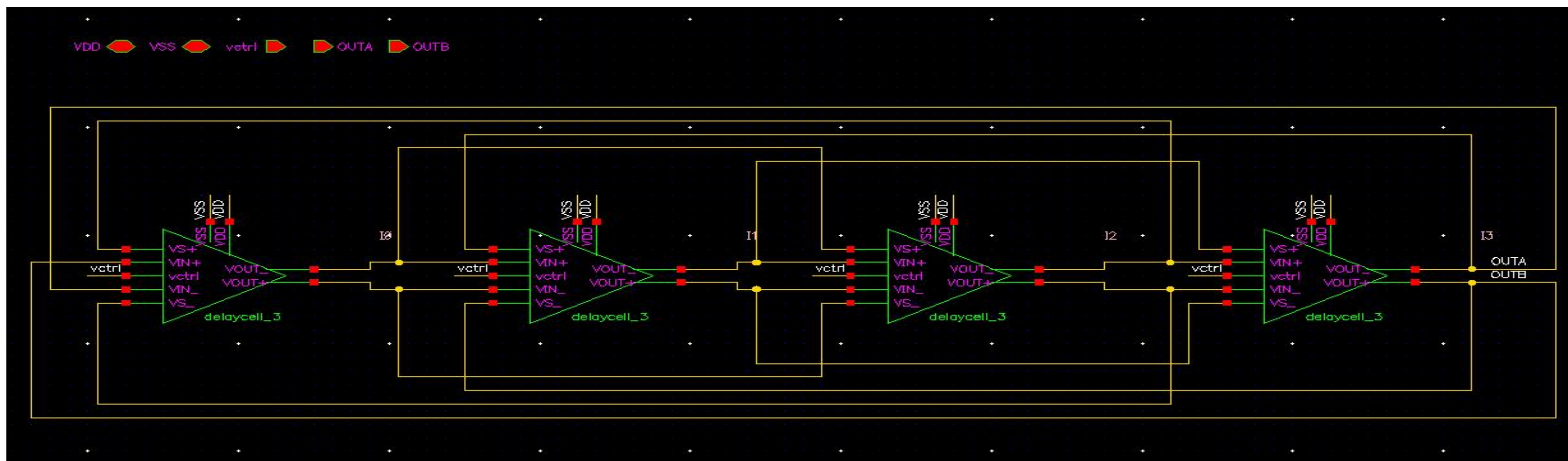
- 电流饥饿型
- 振荡频率1.046G
- 平均电流1.366m
- 1M相噪90.6dBC/HZ, JC84fs, JCC260fs
- delaycell电流变化率大, 峰值3M





VCO架构

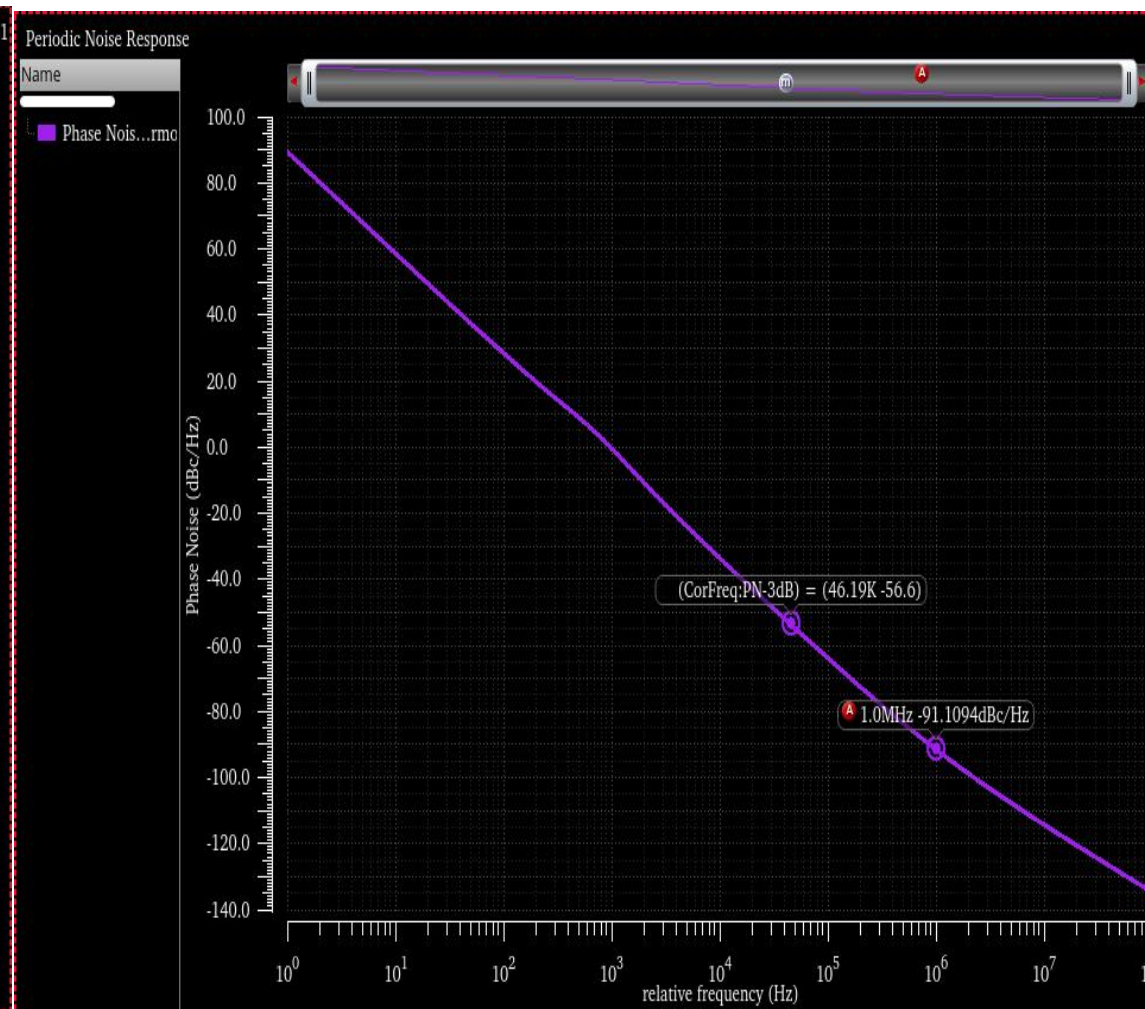
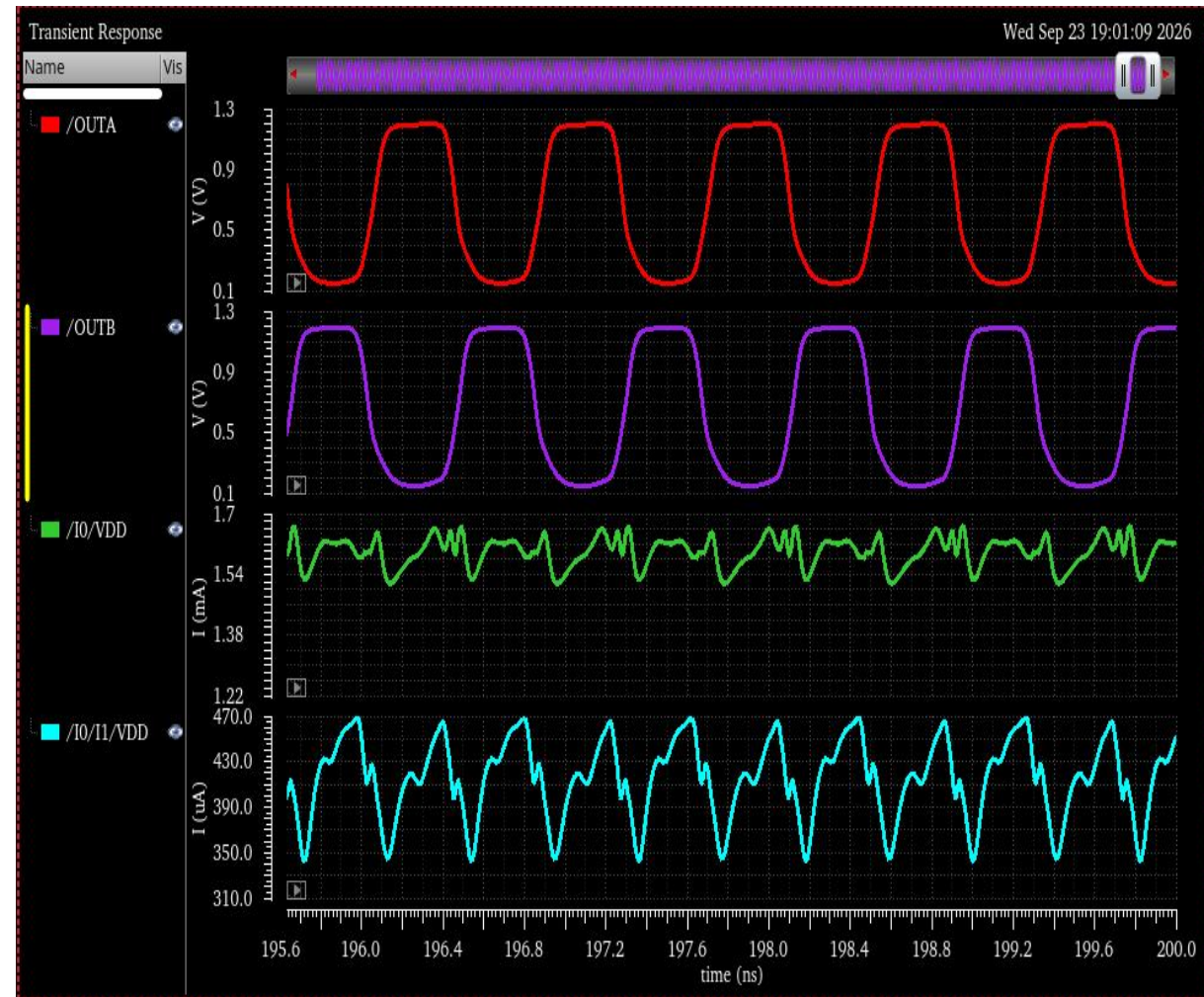
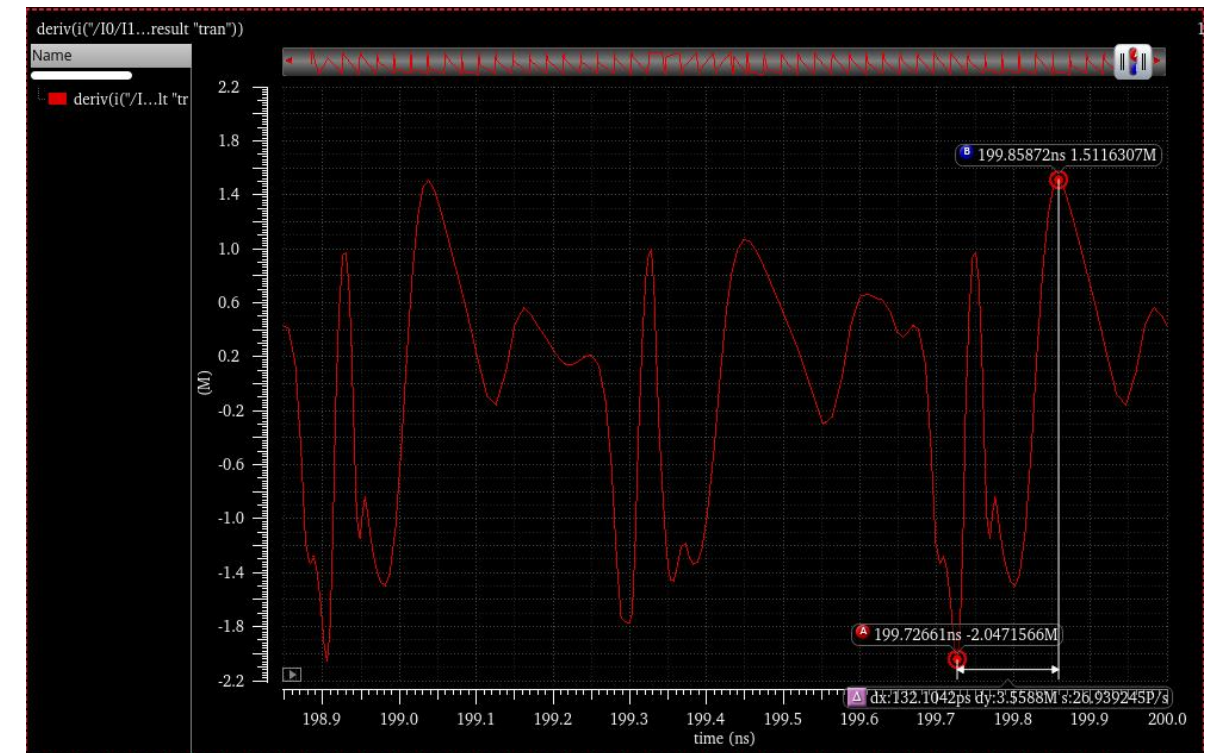
- 参考论文采用前馈环形架构来突破振荡频率极限，其原设计依赖变容二极管（Varactor）进行电容调谐。但受限于当前工艺库缺少变容二极管，无法直接沿用原文献的调谐方案
- 在各级延迟单元底部引入 NMOS 尾管（NM4），将调频机制改为电流饥饿控制。通过改变控制电压 v_{ctrl} 调节充放电电流的大小，实现连续的频率调节。
- 引入尾管后，在振荡器大信号摆动及高 v_{ctrl} 偏置下，尾管存在动态跌入线性区的风险。





VCO架构

- 结合型
- 振荡频率1.21G
- 平均电流1.6m
- 1M相噪91dBC/HZ, JC56fs, JCC211fs
- delaycell电流变化率大, 峰值2M



ADE L (30) - H VCO_delaycell3_tb schematic

Launch Session Setup Analyses Variables Outputs Simulation Results Tools SKPDK Help cadence

Design Variables

Name	Value

Analyses

Type	Enable	Arguments
1 tran	☒	0 200n conservative
2 dc	☒	t
3 pss	☒	1.218G 10 /OUTA /OUTB
4 pnoise	☒	10 1 100M 30 /OUTA /OUTB

Outputs

Name/Signal/Expr	Value	Plot	Save	Save Op
2 /OUTA		☒	☒	
3 IO/VDD		☒	☒	yes
4 IO/I0/net3		☒	☒	allv
5 Jc[Second][k=1]@(1,100M)...	210.601f	☒	☒	
6 Jcc[Second][k=1]@(1,100M)...	55.4285f	☒	☒	
7 IO/I1/VDD		☒	☒	yes

Plot after simulation: Auto Plotting mode: Replace

> Results in .../huquanwei/simulation/VCO_c

395(880) Main Form ... Status: Ready T=27 C Simulator: spectre State: spectre_state1

VCO架构

- 对称负载架构
- 振荡频率1.21G
- 平均电流592.1u
- 1M相噪83.6dBC/HZ, JC135f, JCC487f
- delaycell电流变化率小, 峰值677k

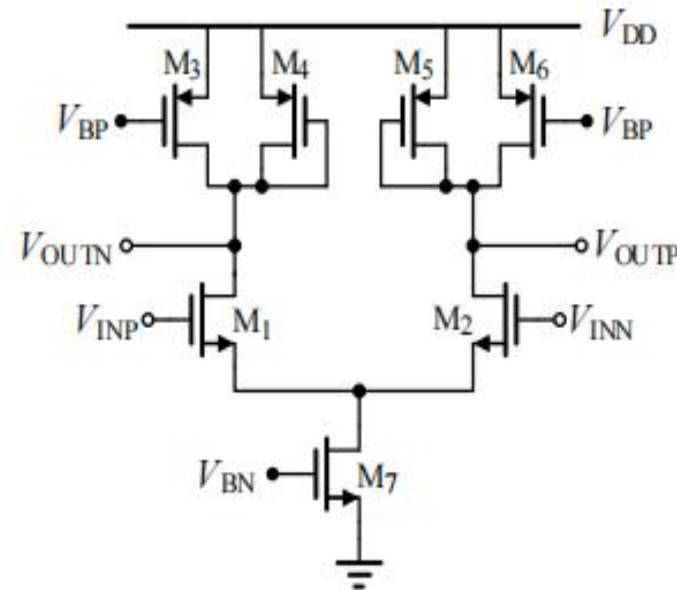
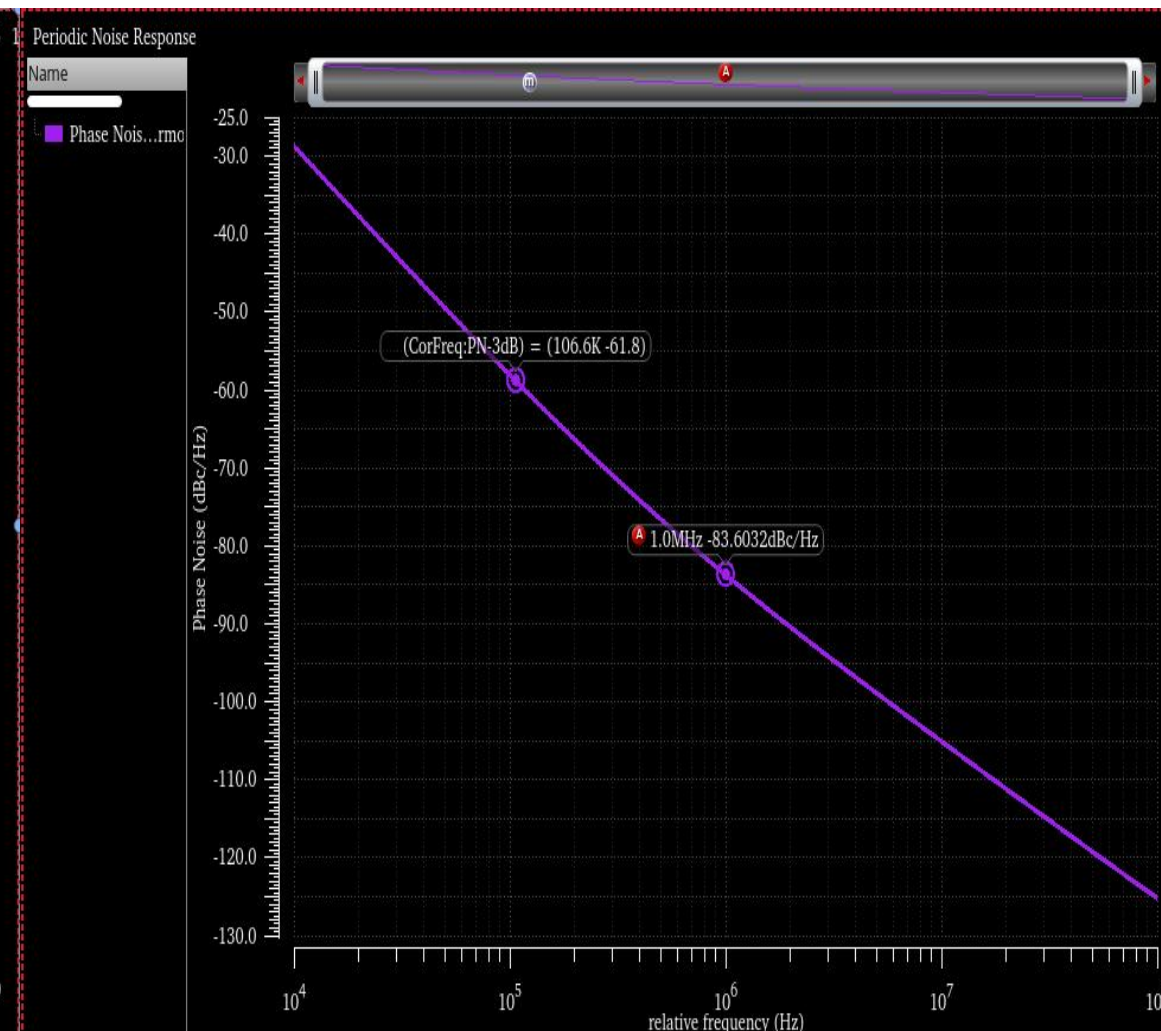
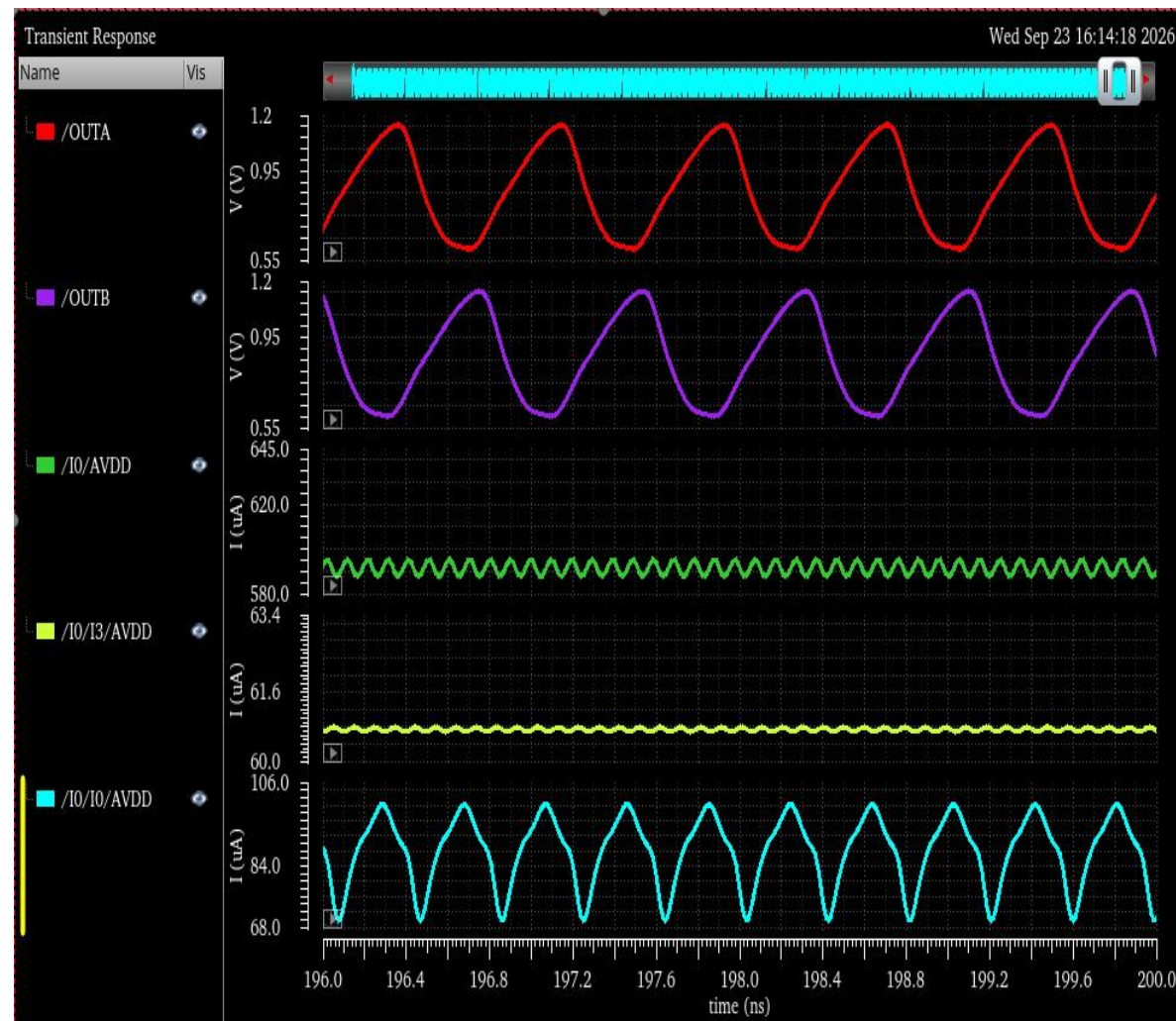
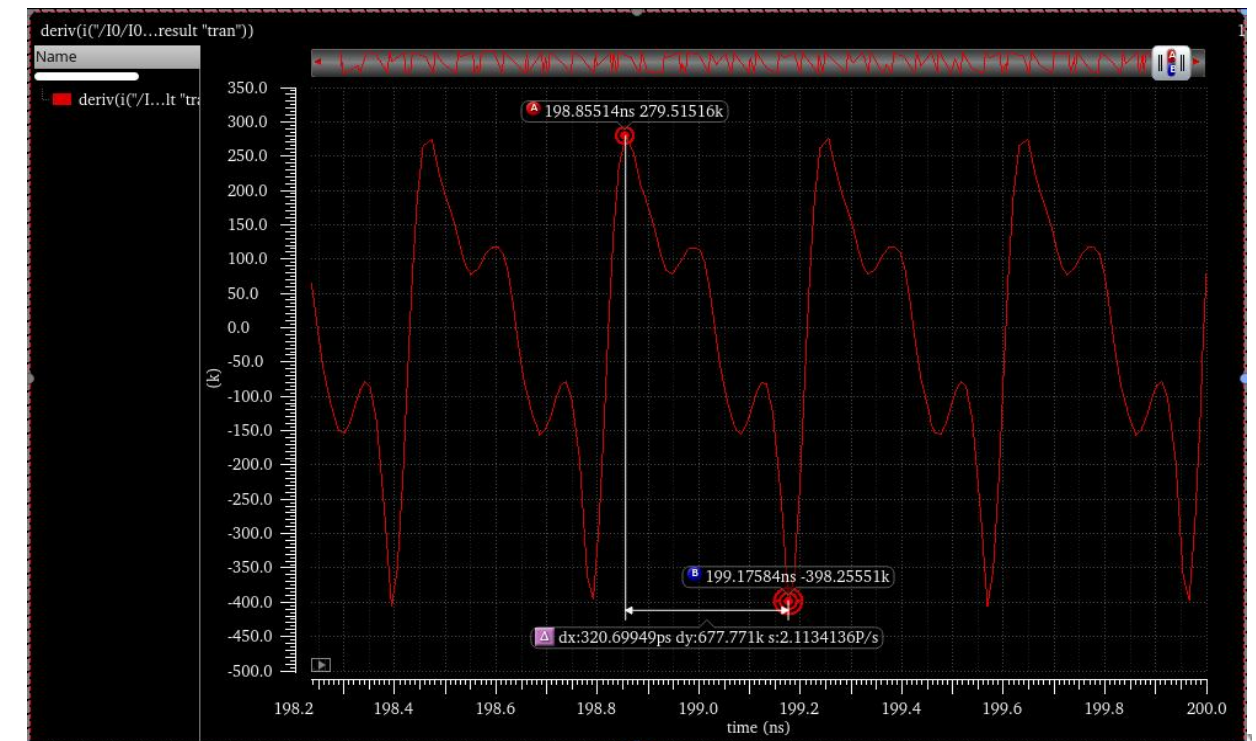


图 3.14 对称负载结构的延迟单元



ADE L (28) - H VCO2_1.tb schematic

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre » cadence

Design Variables

Name	Value
1 vctrl	550m

Analyses

Type	Enable	Arguments
1 tran	☒	0 200n conservative
2 dc	☒	t
3 pss	☒	1.279G 20 /OUTA /OUTB
4 pnoise	☒	20 10K 100M /OUTA /OUTB
5 pxf	☐	7 1K 500M 20 /OUTA /OUTB
6 pac	☐	7 1 200M 20

Outputs

Name/Signal/Expr	Value	Plot	Save	Save C
3 I0/I0/net6		☐	☒	allv
4 I0/VB		☐	☒	allv
5 Jc[Second][k=1]@(10K,100...	486.31f	☒	☒	
6 Jcc[Second][k=1]@(10K,10...	134.623f	☒	☒	
7 I0/AVDD		☒	☒	yes
8 I0/I2/AVDD		☒	☒	yes

Plot after simulation: Auto Plotting mode: Replace

> Results in /home/huquanwei/simulation/V

360(803) Main Form ... Status: Ready T=27.0 C Simulator: spectre State: spectre_state1



对比

架构类型	振荡频率	平均电流	1M相噪	JC	JCC	电流变化率峰值
对称负载架构	1.21G	592.1u	83.6dBc/Hz	135fs	487fs	小(峰值677k)
电流饥饿型	1.046G	1.366m	90.6dBc/Hz	84fs	260fs	大(峰值3M)
结合型	1.21G	1.6m	91dBc/Hz	56fs	211fs	大(峰值2M)
前馈型	1.6G	862.3u	95.5dBc/Hz	11fs	54fs	巨大（峰值19M）



谢谢