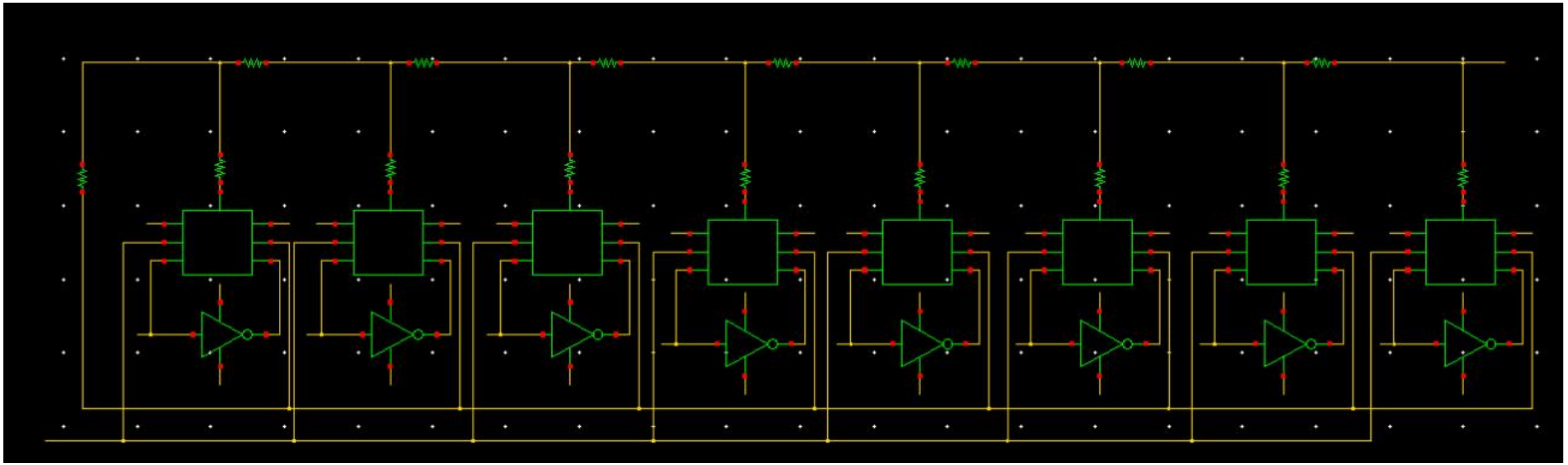
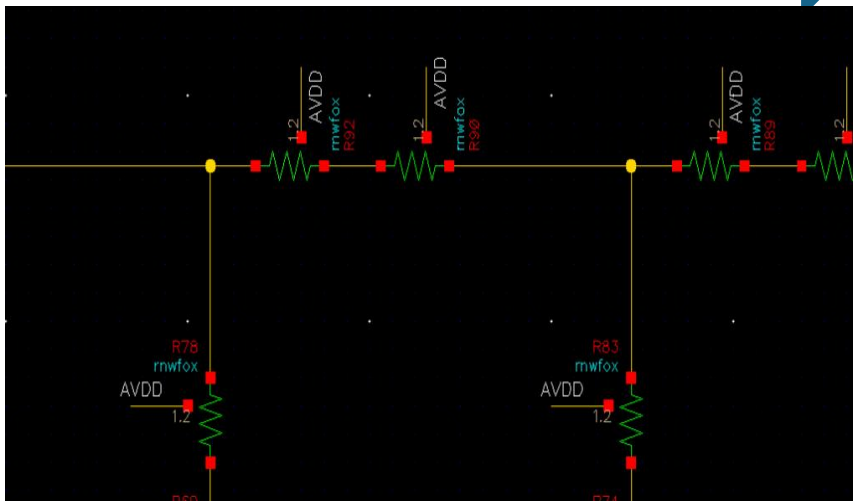
2026.9.24组会

郝宝书





- 电阻
  图1.rnwfox_633ohm_2个39K串联
  串联电阻电流不一致——漏电

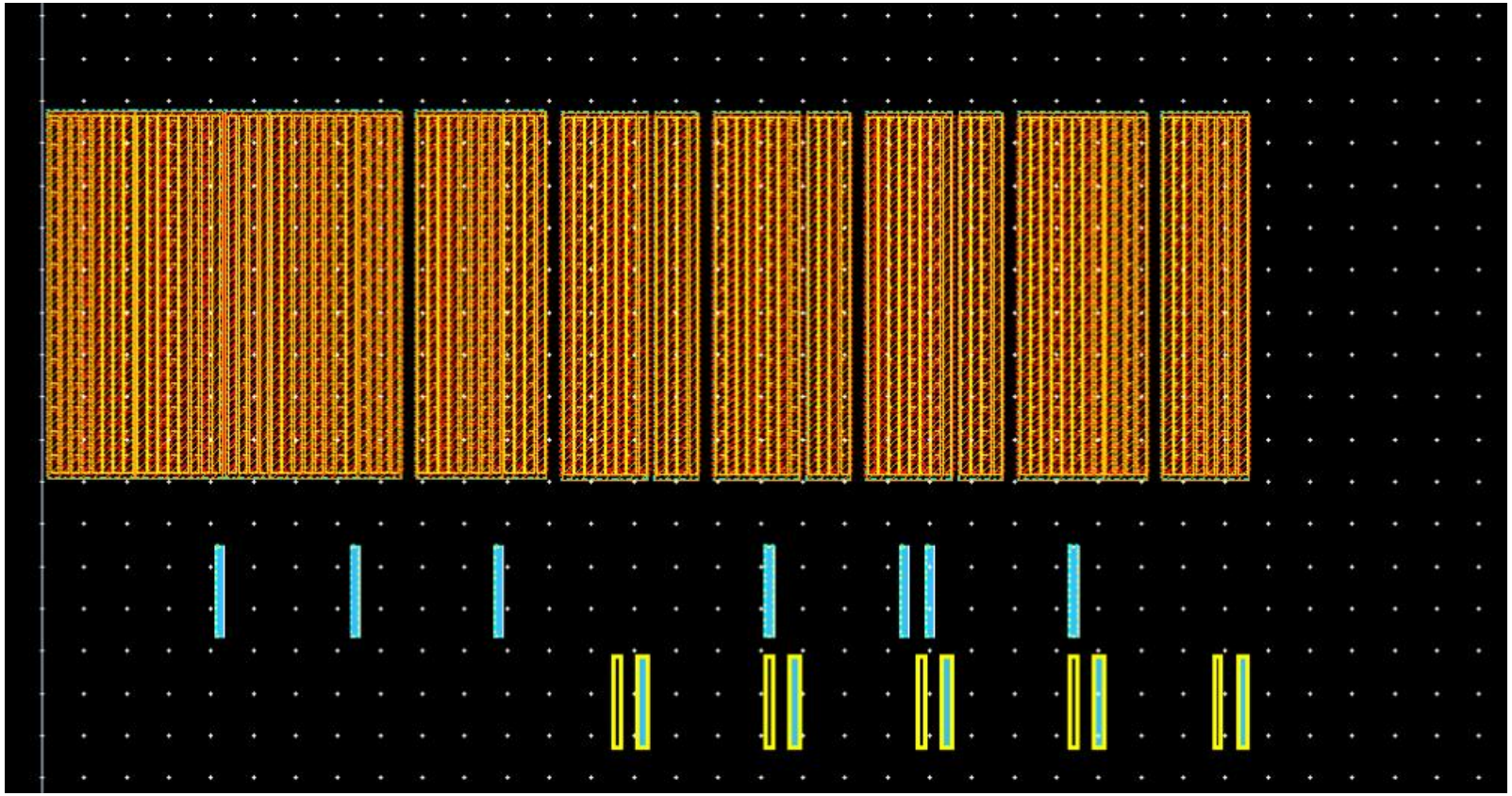
  图2.rppolywo_455ohm_80k

- layout_长150u_宽45u

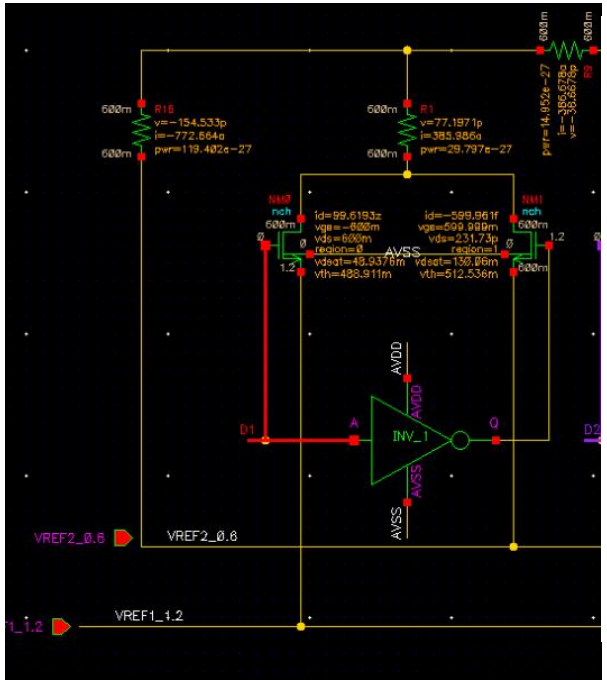
Cell Name	rppolywo	value
View Name	symbol	off
Instance Nam	R98	off

Add Delete Modify

CDF Parameter	Value	Display
Model name	rppolywo	off
Description	P+ POLY Resistor	off
Segments	4	off
Segment Connection	Series	off
Calculated Parameter	Length	off
Resistance	80.004K Ohms	off
Segment Width	1u M	off
Segment Length	42.228u M	off
Effective Width	1u M	off
Effective Length	819.876m M	off
Temp rise from ambien	0	off
Mismatch Flag	1	off
Sheet Resistivity	455.87 Ohms	off
End Resistance	124.56u Ohms	off
Delta Width	31.297n M	off



layout_长150u_宽45u



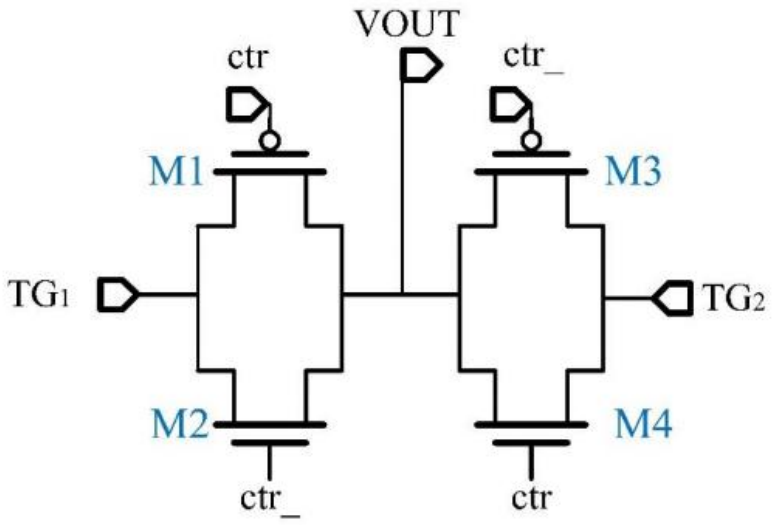
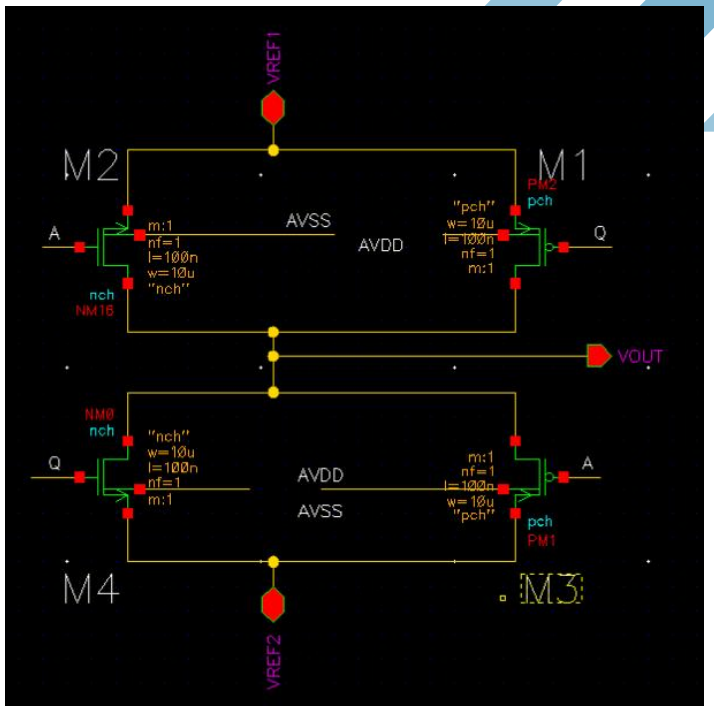


图 3-3 传输门结构



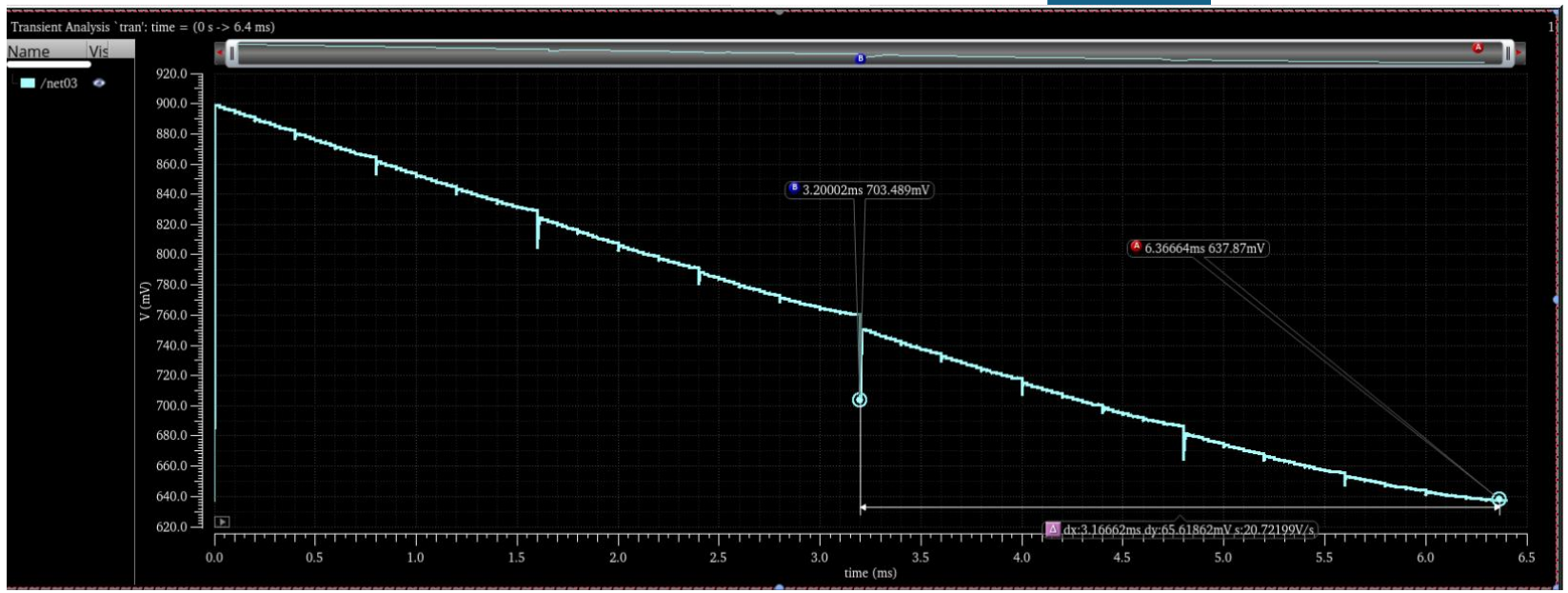
D1=1.2V

$$V_{gs} = 1.2\text{V} - 0.9\text{V} = 0.3\text{V}$$

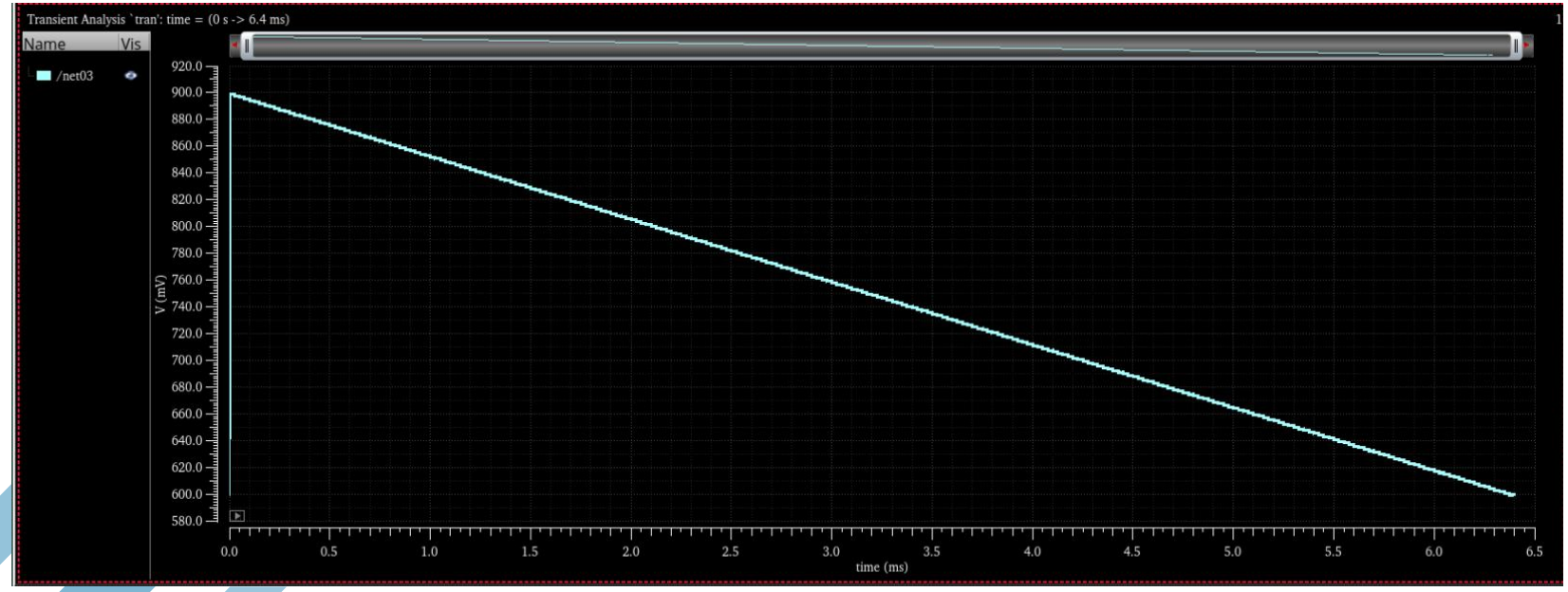
Vgs<Vth,截止，无法将900mv建立到电阻处

vref1=900mv；vref2=600mv

- 当D1=1时，PMOS栅极接0，Vgs=0.9V>Vth,线性导通，vout=900mv
- 当D1=0时,NMOS栅极接1.2v，Vgs=0.6V>Vth,线性导通，vout=600mv
- 开关电阻：线性电阻约为200~350欧，相对占比小

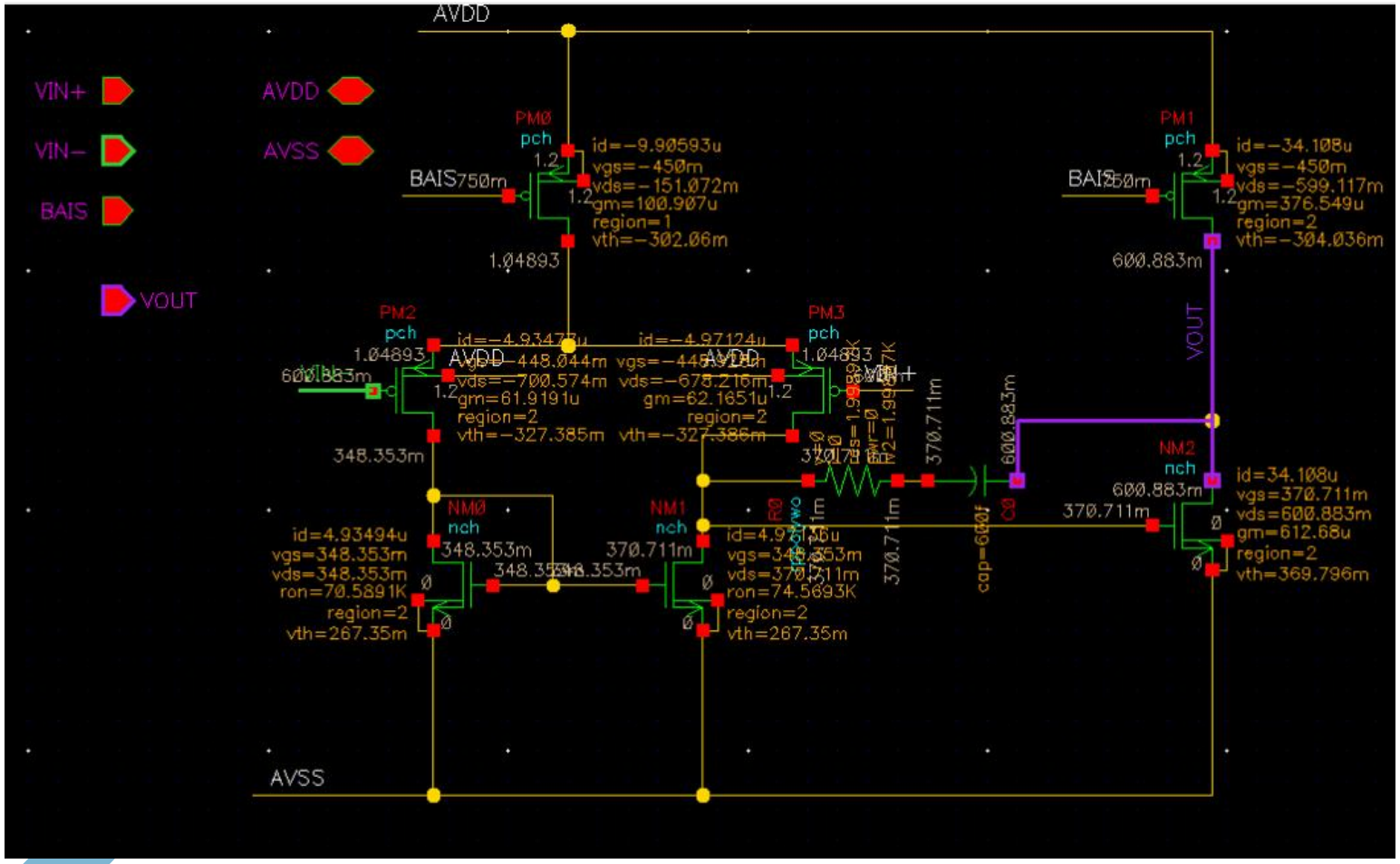

Transient Analysis `tran': time = (0 s -> 6.4 ms)
Name
Vis
/net03
3.20002ms 703.489mV
6.36664ms 637.87mV
dx:3.16662ms dy:65.61862mV s:20.72199V/s
V (mV)
time (ms)

调节前_

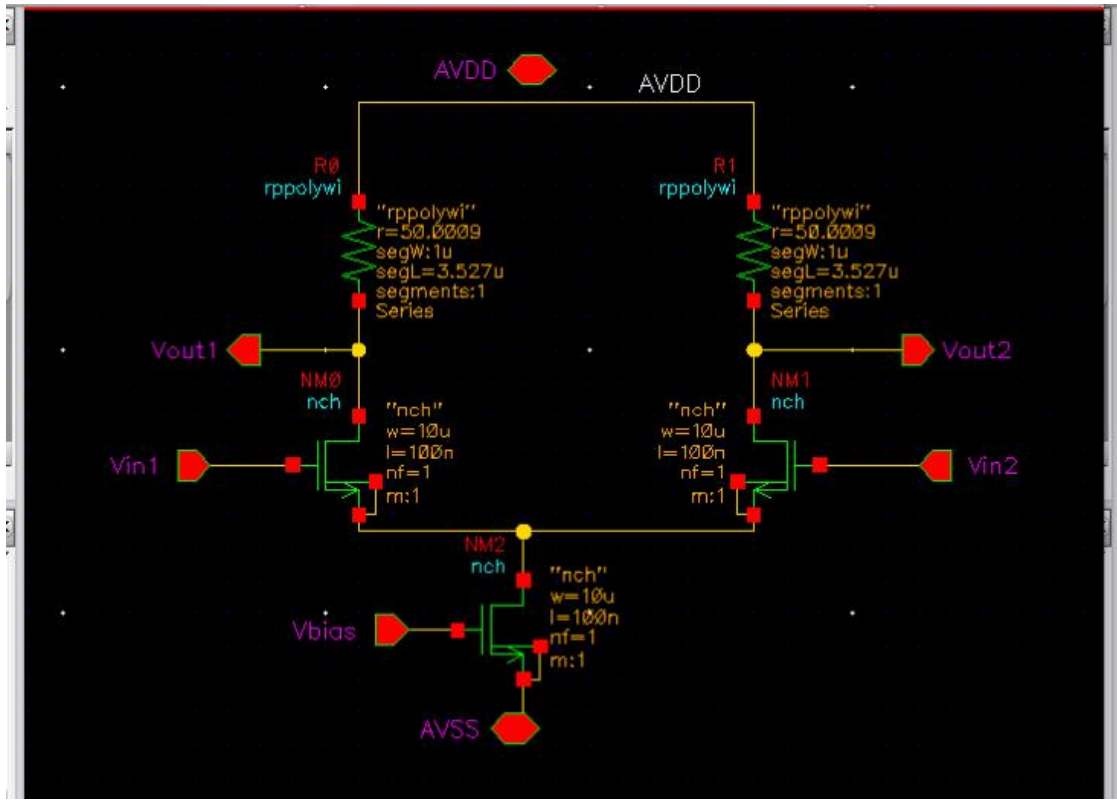

Transient Analysis `tran': time = (0 s -> 6.4 ms)
Name
Vis
/net03
V (mV)
time (ms)

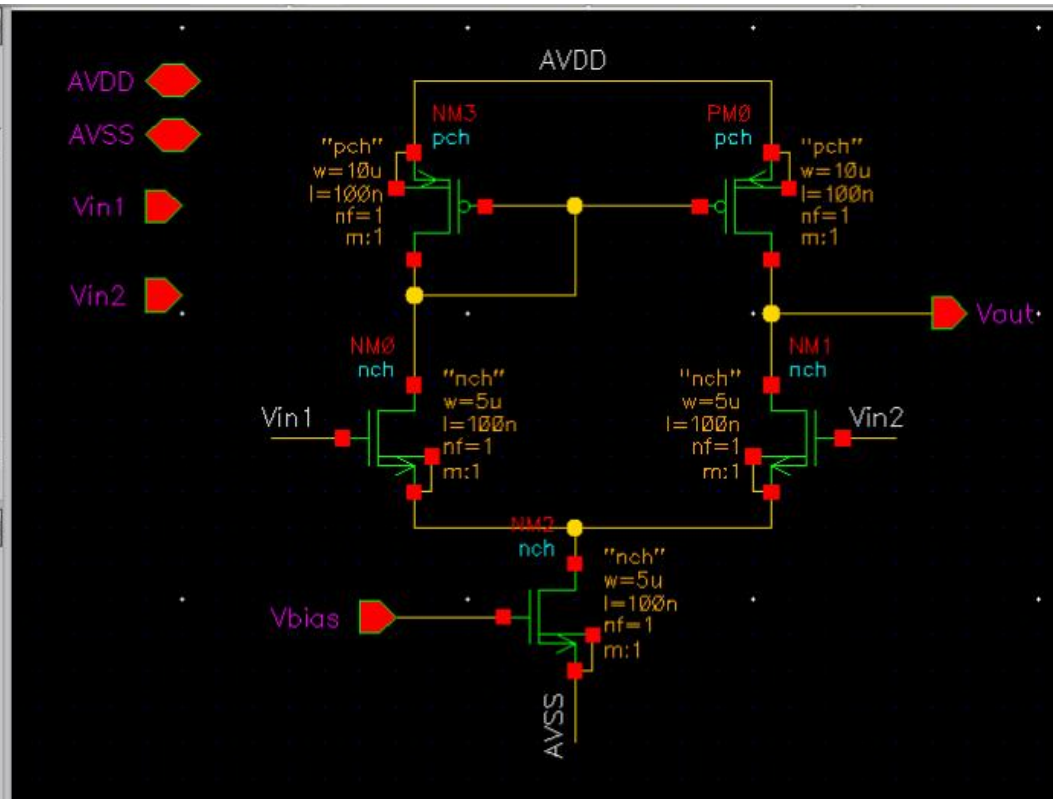
调节后_

DAC——buffer



1.负载大小_目前600f
2.驱动电流_目前34u
3.增益要求_目前57dB


AVDD
AVDD
R0
rppolywi
"rppolywi"
r=50.0009
segW:1u
segL=3.527u
segments:1
Series
R1
rppolywi
"rppolywi"
r=50.0009
segW:1u
segL=3.527u
segments:1
Series
Vout1
Vout2
NM0
nch
"nch"
w=10u
l=100n
nf=1
m:1
NM1
nch
"nch"
w=10u
l=100n
nf=1
m:1
Vin1
Vin2
NM2
nch
"nch"
w=10u
l=100n
nf=1
m:1
Vbias
AVSS


AVDD
AVDD
AVSS
Vin1
Vin2
NM3
pch
"pch"
w=10u
l=100n
nf=1
m:1
PM0
pch
"pch"
w=10u
l=100n
nf=1
m:1
Vout
NM0
nch
"nch"
w=5u
l=100n
nf=1
m:1
Vin1
NM1
nch
"nch"
w=5u
l=100n
nf=1
m:1
Vin2
NM2
nch
"nch"
w=5u
l=100n
nf=1
m:1
Vbias
AVSS

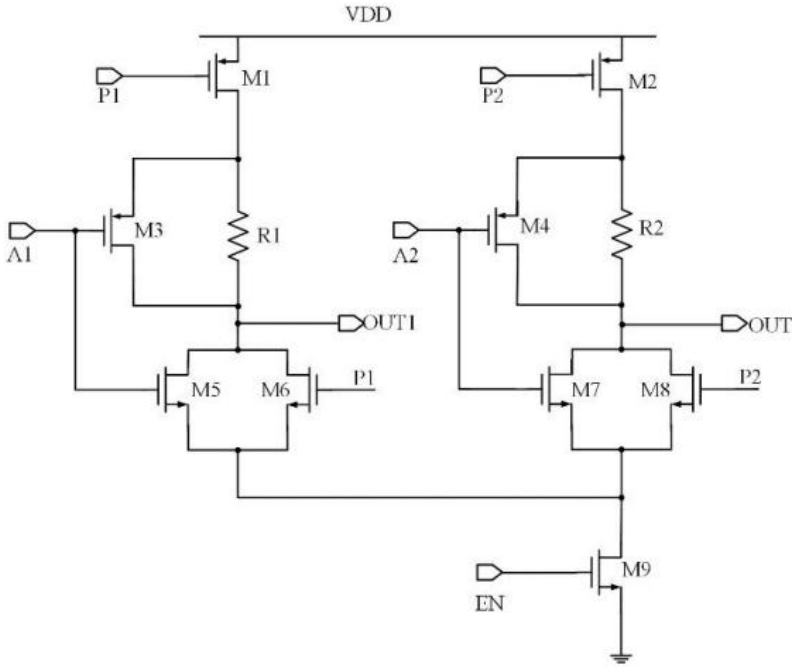


图 4-2 CML 预驱动结构图

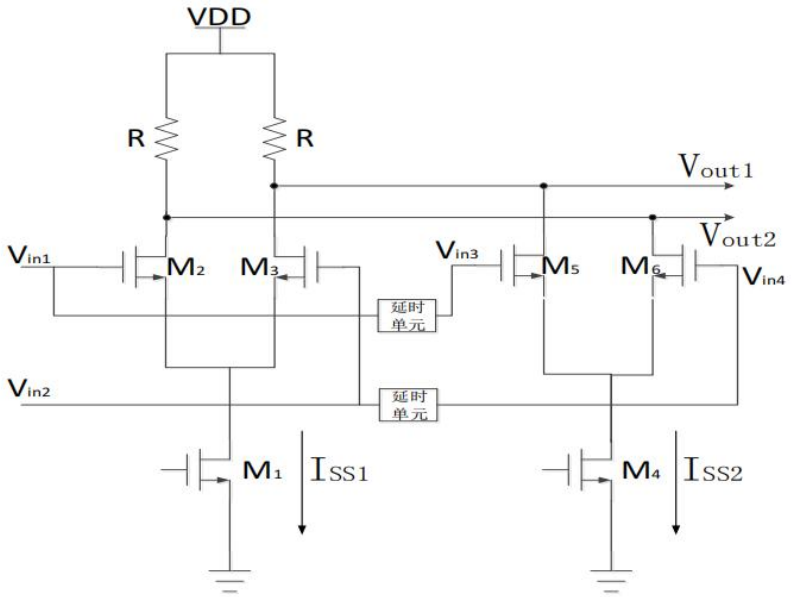


图 3.8　发送端预加重技术

接下来的工作

- 调节buffer/bias
- 给CML发送端结构加预驱动/预加重