

# 顶点探测器像素芯片设计

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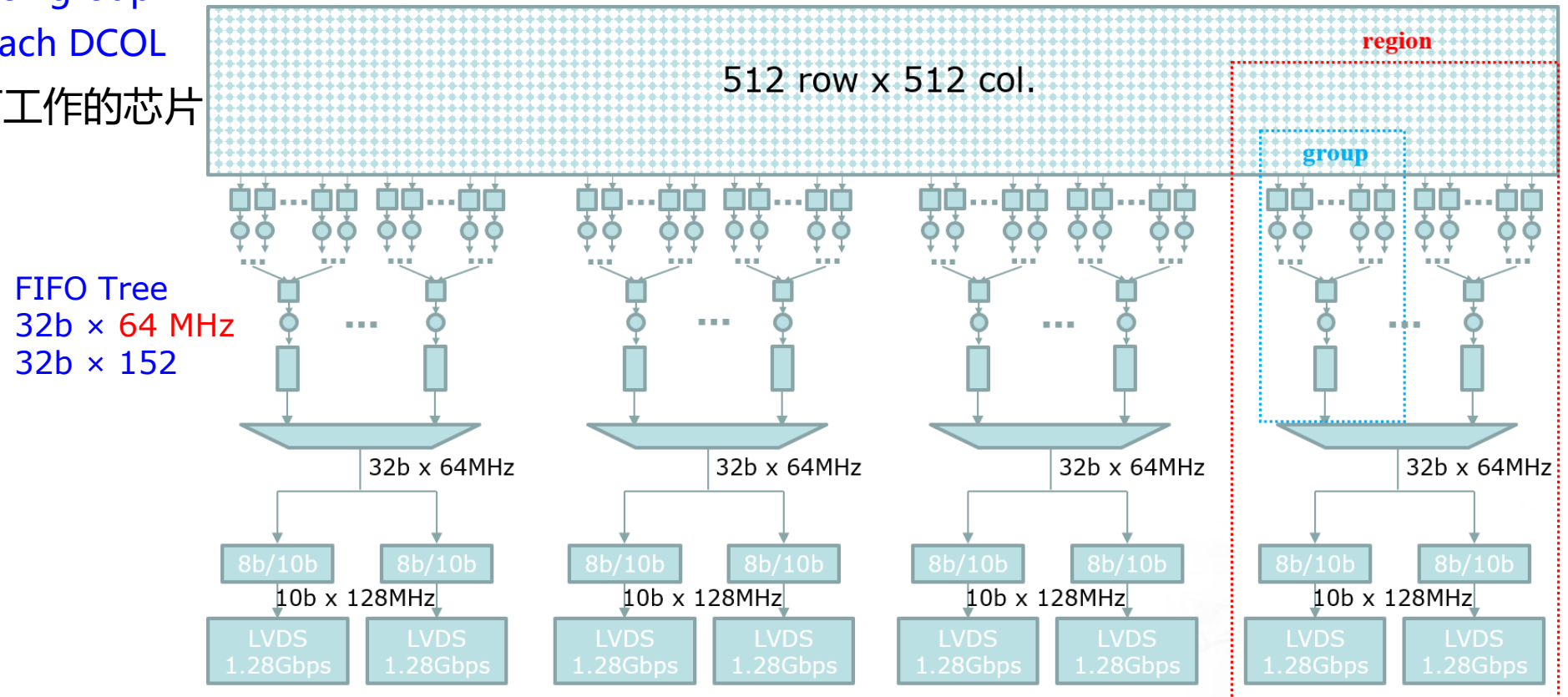


# 本周主要进展

- 像素逻辑电路对比了HVT和RVT的漏电流
  - 0.95nW vs 8.34 nW per pixel (不含地址ROM)
  - 作为对比, 模拟前端约60 nW per pixel (15 mW/chip)
  - HVT的门延迟基本可以满足时序要求
- 魏晓敏老师提出用64b/66b编码替换8b/10b编码
  - 如果线路速率保持1.28Gbps, 提高有效数据带宽
  - 或者保持有效数据带宽不变, 降低线路速率到1.056Gbps → 降低数据传输模块的带宽设计压力
  - 增加发送端的编码块缓存和拼接, 以及接收端的同步 (bit slip)
- 数据传输模块用CML还是LVDS?
  - 主要区别在偏置电流, 6 mA vs 3.5 mA
  - 功耗预算5 mW/通道, 含PLL和serializer
- PLL的VCO架构对比与电路参数调整

# 整体方案

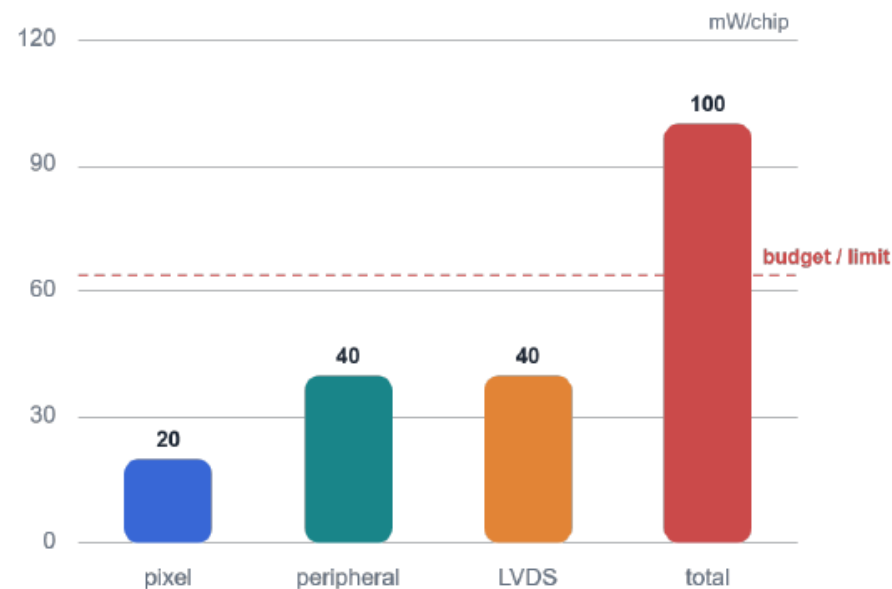
- 252 MHz pixel hit rate x 40 bit = 10.08 Gbps (Pixel hit rate = 200 MHz·cm<sup>-2</sup>)
  - 512 × 512 pixel
  - Regions = 4 groups + 2 x 8b/10b + 2 x LVDS transmitter
  - Groups = 16 double columns + 1 Shared FIFO tree
  - 152 words for each group
  - Time stamp on each DCOL
- 当前目标：简单，可工作的芯片



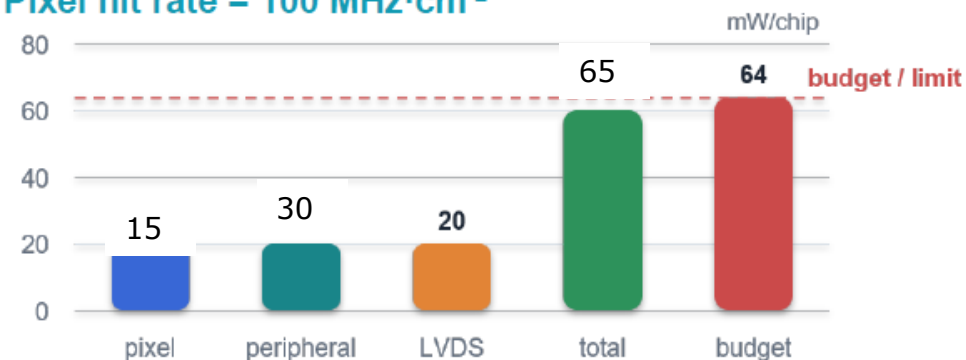
# Operating Condition

- 最内层 pixel hit rate = 200 MHz/cm<sup>2</sup>
  - 平均功耗 = 100 mW / 1.6 cm<sup>2</sup> = 62.5 mW/cm<sup>2</sup>
  - 利用 beam pipe 提高散热能力
- 次内层 pixel hit rate < 100 MHz/cm<sup>2</sup>
  - 系统时钟频率降低一半
  - 数据传输模块关闭一半
  - 平均功耗 = 65 mW / 1.6 cm<sup>2</sup> = 40.6 mW/cm<sup>2</sup>
  - 接近满足 < 40 mW/cm<sup>2</sup> 的散热要求

Pixel hit rate = 200 MHz·cm<sup>-2</sup>



Pixel hit rate = 100 MHz·cm<sup>-2</sup>



# CEPC workshop

- Shanghai from October 22 to 26, 2026
- Abstracts accepted as Oral presentation:
  - Modeling and Simulation of Column-Drain Readout for AGORA Vertex Detector Pixel Sensors
  - A Methodology for Determining Pixel Chip Parameters from Vertex Detector Design Requirements
  - Rehearsal next Thursday?