



CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

First beam test results of COFFEE3, an HV-CMOS Pixel Prototype for the CEPC Inner Tracker

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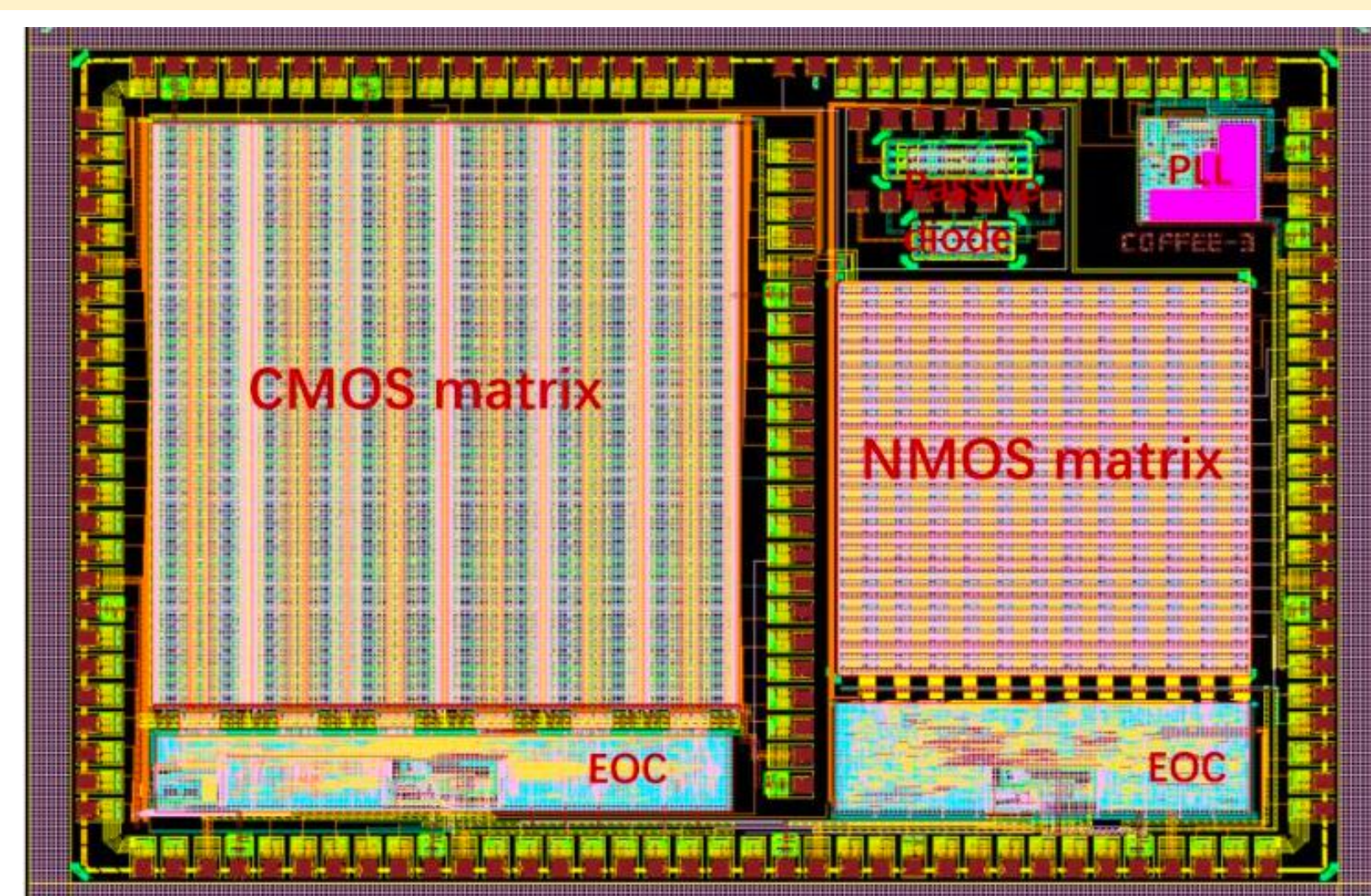
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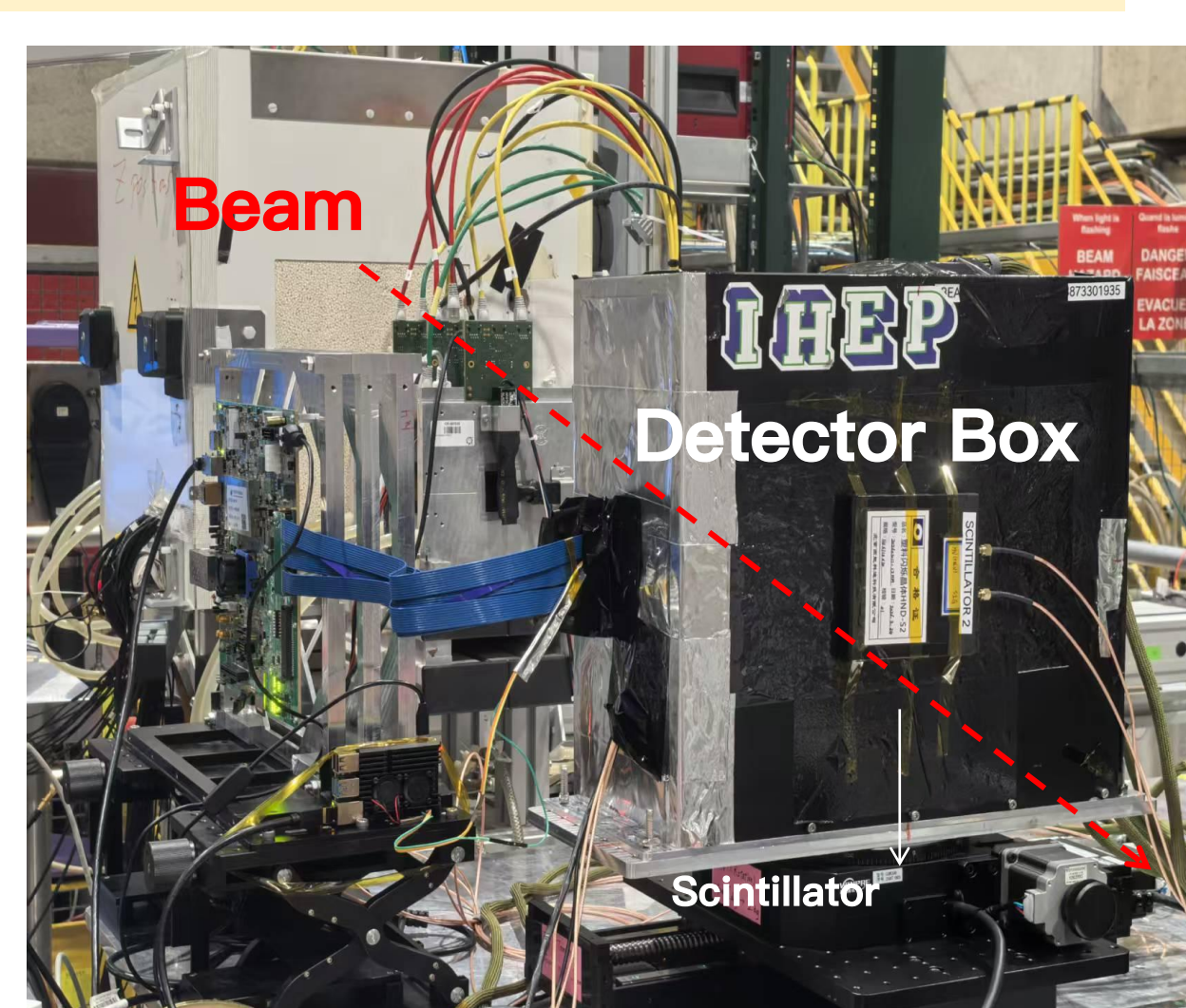


Introduction

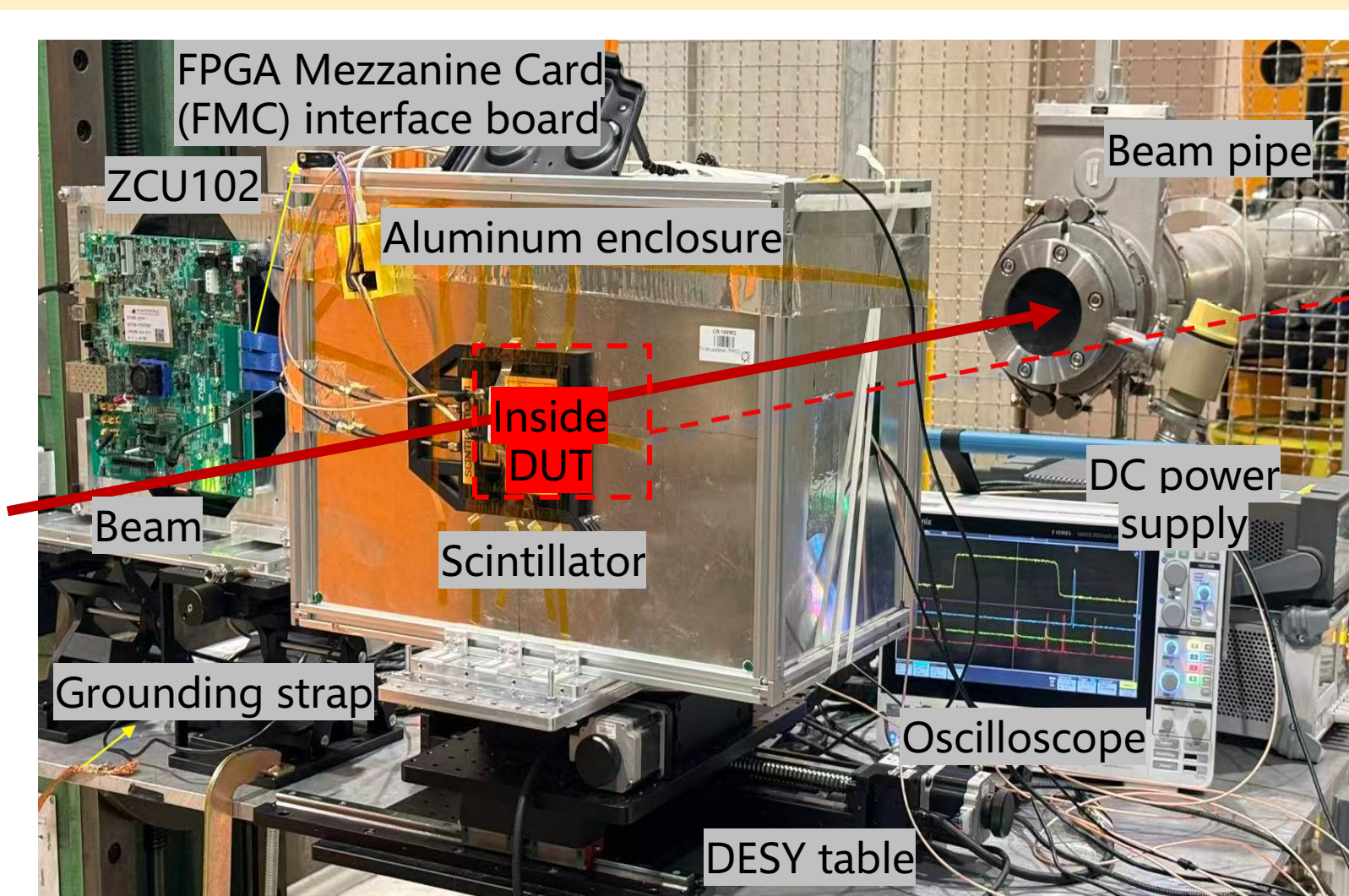
COFFEE3 is a 55 nm HV-CMOS pixel detector prototype developed for the CEPC inner tracker. Following previous bench tests with charge injection, laser illumination, and a ⁵⁵Fe source, two beam-test campaigns were carried out at the CERN SPS in May and July 2026. Clear responses to high-energy charged particles are observed, together with temporal correlation with scintillator reference signals. The measured single-pixel time-of-arrival (TOA) spread is studied and timewalk effect has been observed. Multi-pixel measurements demonstrated the full readout chain of the pixel array and validated the in-pixel threshold-tuning DAC (TDAC) capability. The beam tests also revealed pixel-to-pixel response non-uniformity and noise-induced hit bursts, providing important input for further optimization of COFFEE3 and the development of next-generation HV-CMOS pixel detectors.



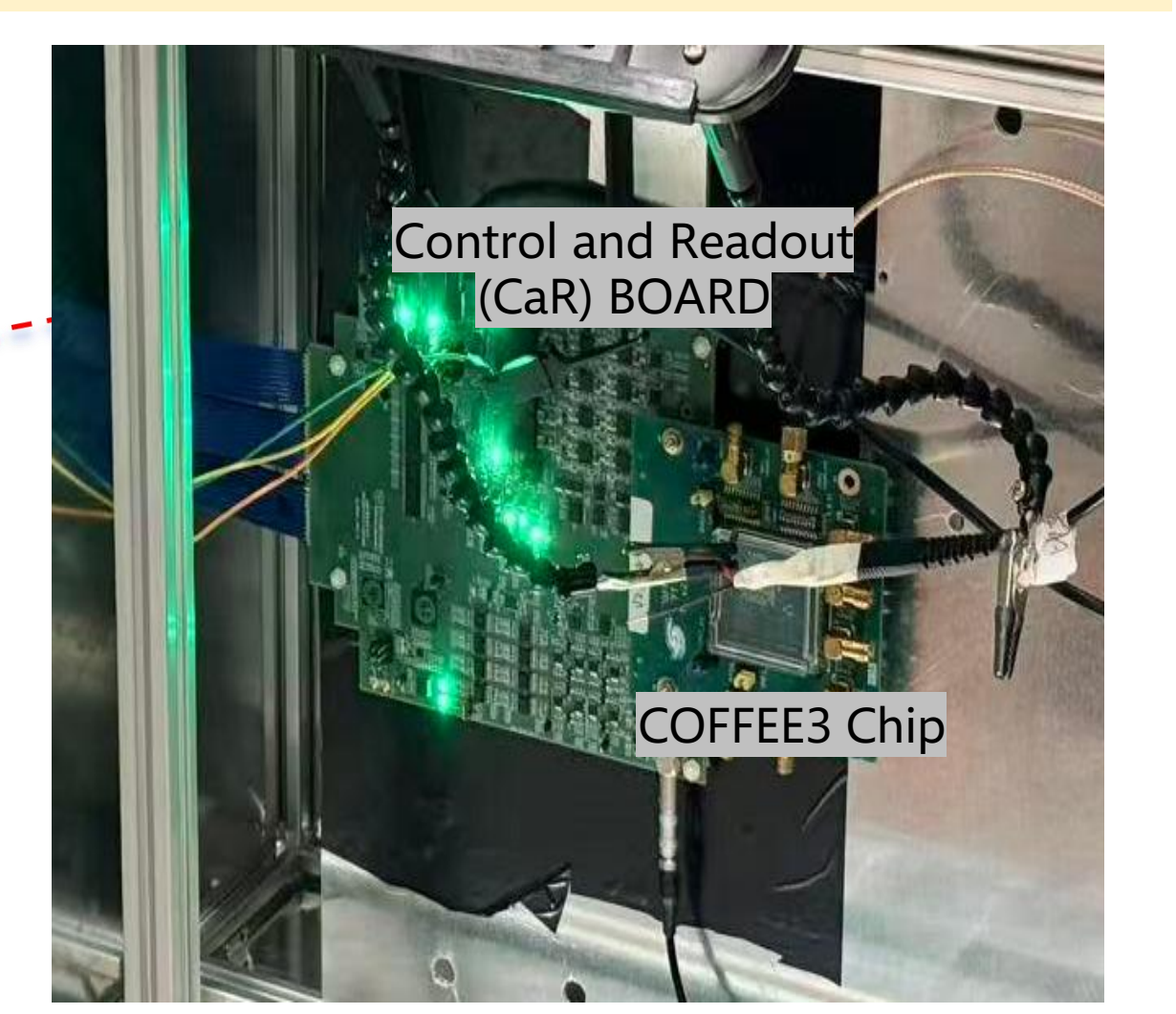
COFFEE3 chip layout



May: tracking setup



July: beam-test setup



DUT and CaR board

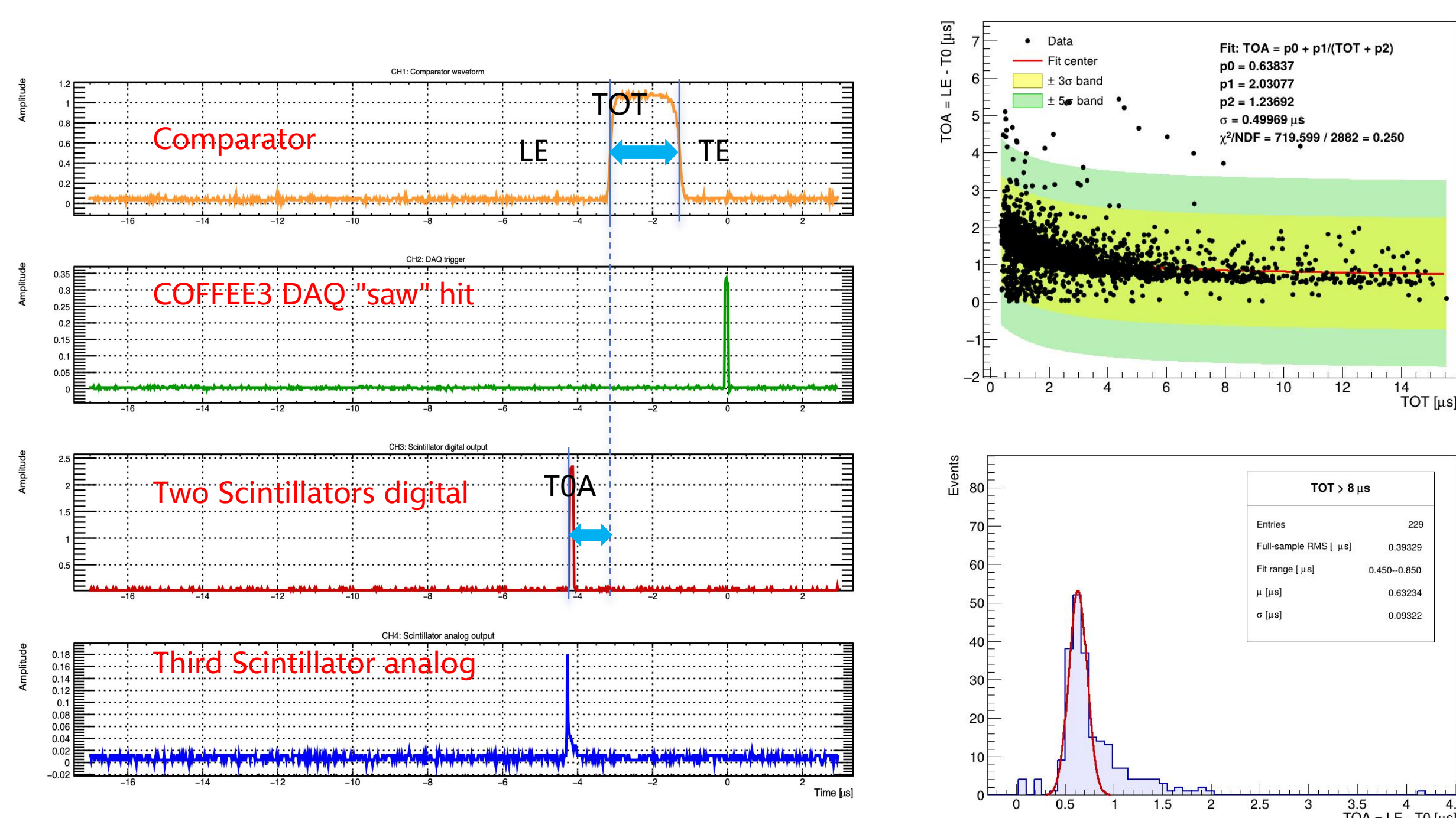
Array Design & Beam Test System

- Chip Size: 4000 μm (W) $\times$ 3000 μm (H)
 - Left Array Size: 1920 μm (H) $\times$ 1740 μm (W)
 - Pixel Pitch: 40 μm (Rows) $\times$ 145 μm (Columns)
 - Analog Front-End
 - 4 Types of Charge-Sensitive Amplifiers (CSA)
 - CMOS Discriminator with Threshold Adjustment TDAC
 - Peripheral read out circuit
- **CERN SPS H6, 200 GeV hadron beam in May**
- A 6-layer silicon strip detector beam monitor (BM) for tracking
 - Two scintillators with COFFEE provided trigger to BM
- **CERN SPS H8, 180 GeV hadron beam in July**
- COFFEE, and three scintillators provided time reference
 - Approximately 2×10^6 particles per spill

Test Results

1 Single-pixel timing and timewalk

Comparator timing: $\text{TOA} = \text{LE} - \text{T0}$ and $\text{TOT} = \text{TE} - \text{LE}$. The TOA depends strongly on pulse width. For $\text{TOT} > 8 \mu\text{s}$, the fitted TOA core has $\sigma \approx 93 \text{ ns}$.

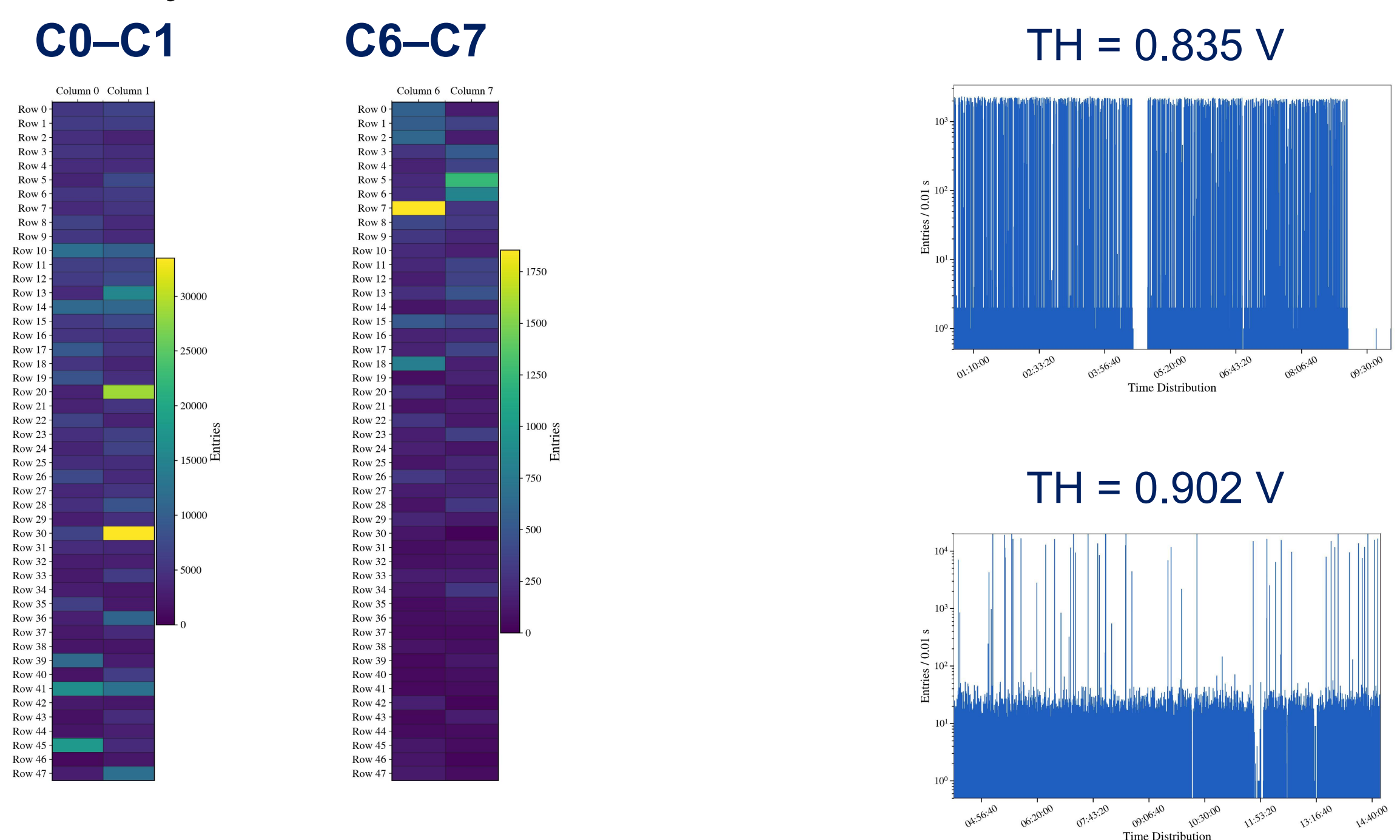


Beam-test waveforms and timing definitions

Single-pixel timewalk

2 Multi-pixel response and noise

Both tested double-columns, C0–C1 and C6–C7, recorded hits across all pixels. Local TDAC tuning changed pixel response, while non-uniformity and fake-hit bursts remained.

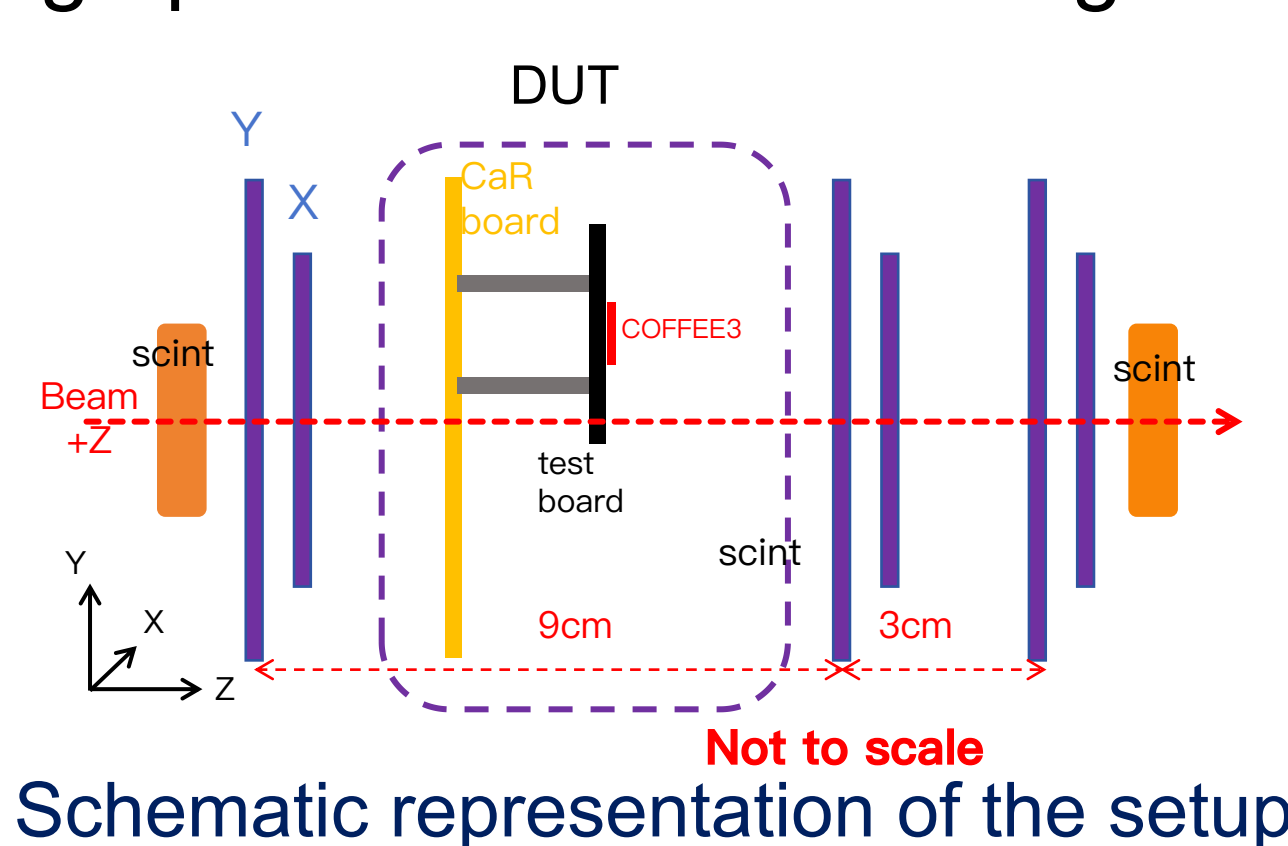


Hit maps after local TDAC adjustment

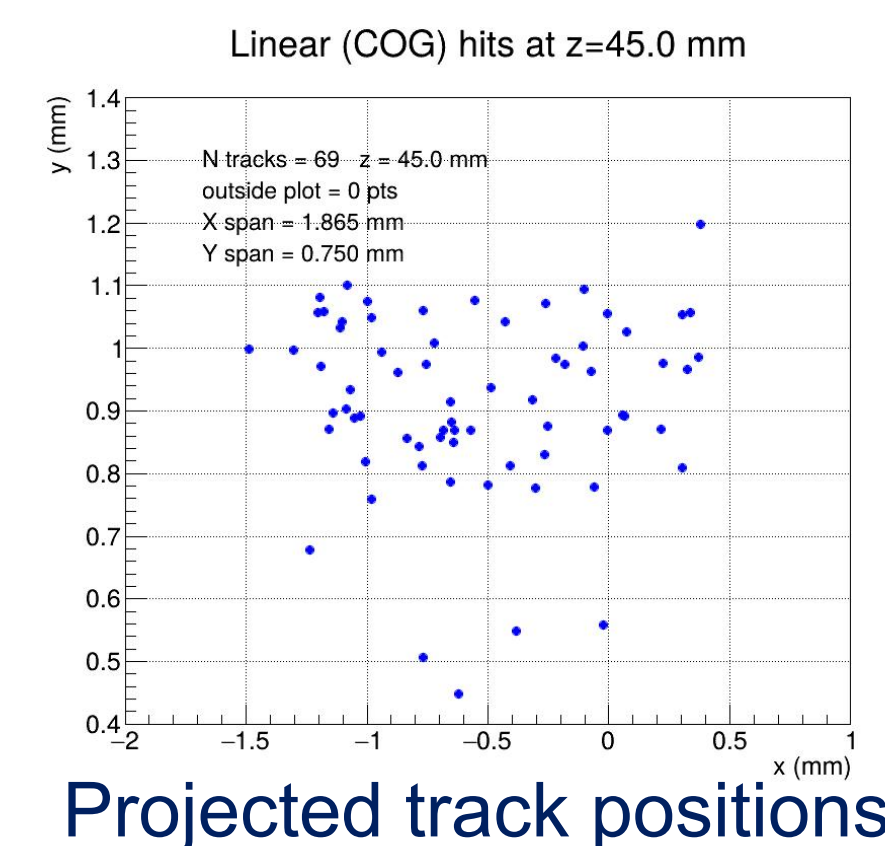
Higher TH suppresses sustained noise bursts.

3 Tracking with the silicon-strip monitor

Tracking confirms the expected pixel geometry: X pitch = $36.5 \pm 0.8 \mu\text{m}$ (design: 36 μm); Y separation is consistent with the 130.5 μm design pitch. Residuals are alignment-dominated.



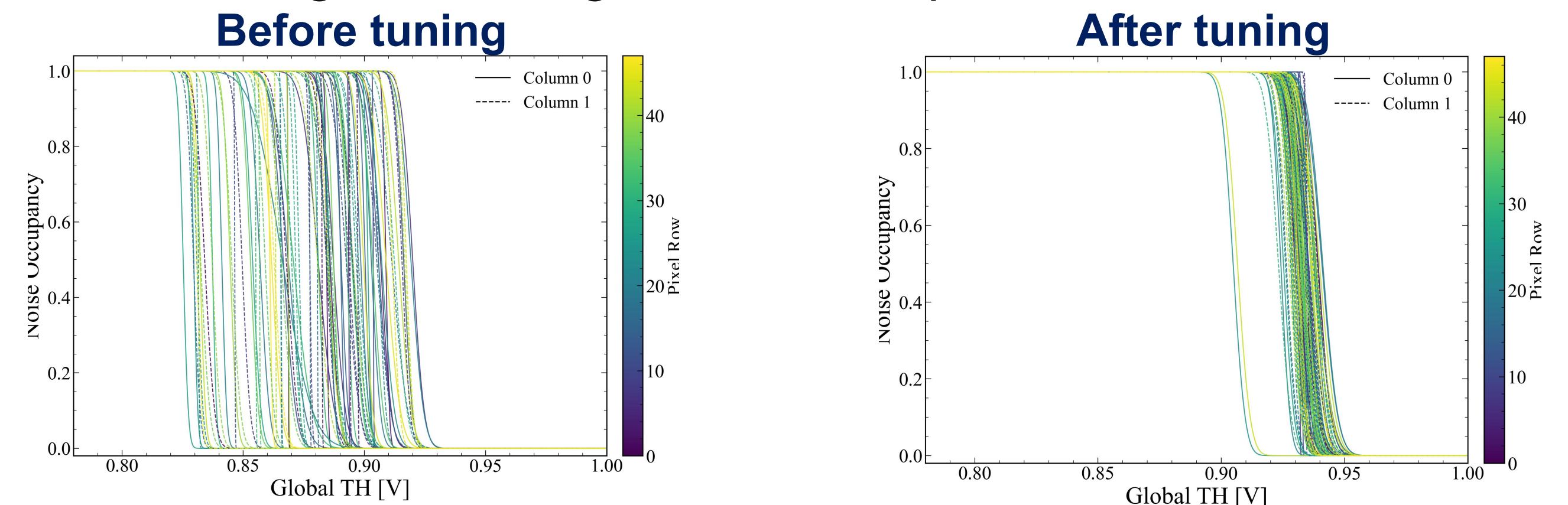
Schematic representation of the setup



Projected track positions

4 Threshold equalization after the beam test

4-bit TDAC tuning significantly improves threshold uniformity. For C0–C1, the noise S-curve spread decreases from $\sim 0.1 \text{ V}$ to $\sim 0.02 \text{ V}$ after individual tuning, confirming functional in-pixel TDACs.



Summary & Outlook

COFFEE3 records high-energy charged particles and demonstrates multi-pixel readout. Selected-event timing reaches a fitted core width of about 93 ns, and laboratory TDAC tuning reduces threshold dispersion. The tracking study also shows good spatial consistency between the reconstructed tracks and the tested pixel region. Further work will address timewalk, noise bursts and alignment, and quantify efficiency and timing for the next COFFEE prototype.