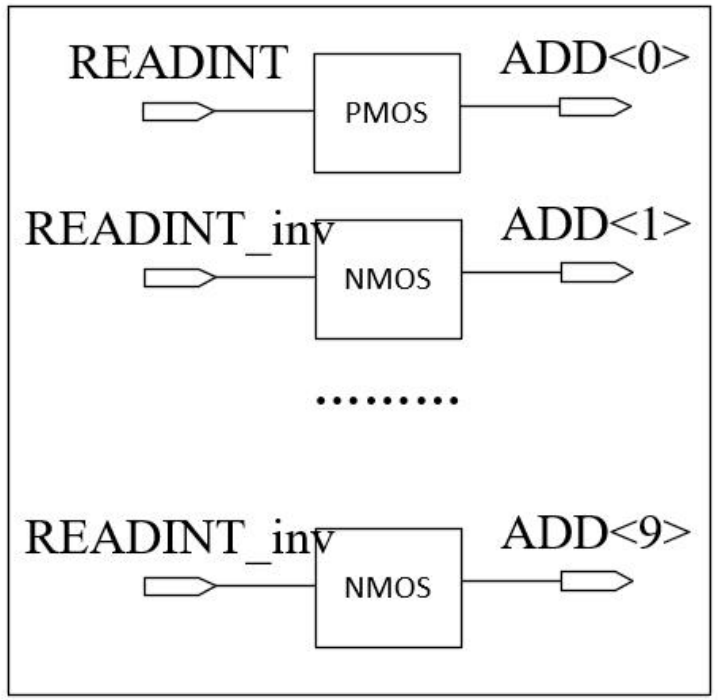
# 10.15

# ADDR延时

**ADDR延迟48ns,驱动项延迟21.94ns，预估驱动电阻为5.2kΩ左右**




**PMOS尺寸：W=660nm,L=100nm**

**此时驱动电阻为5.14KΩ**

**理论计算从输入到输出的50%延迟时间为21.89ns**

**NMOS尺寸：W=280nm,L=100nm**

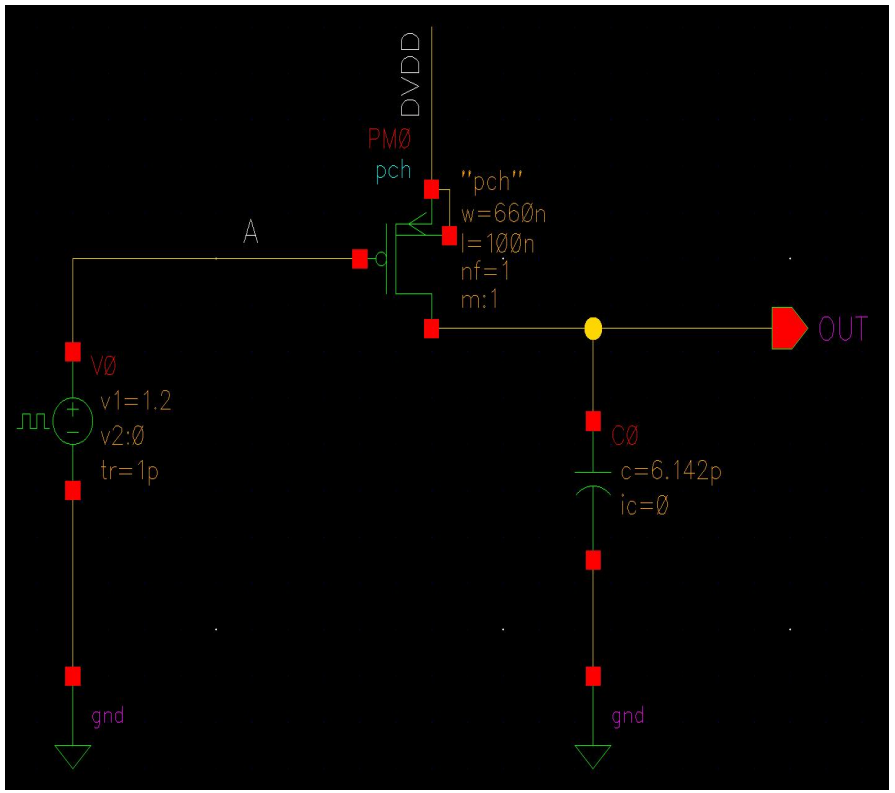
**此时驱动电阻为5.136KΩ**

**理论计算从输入到输出的50%延迟时间为21.86ns**

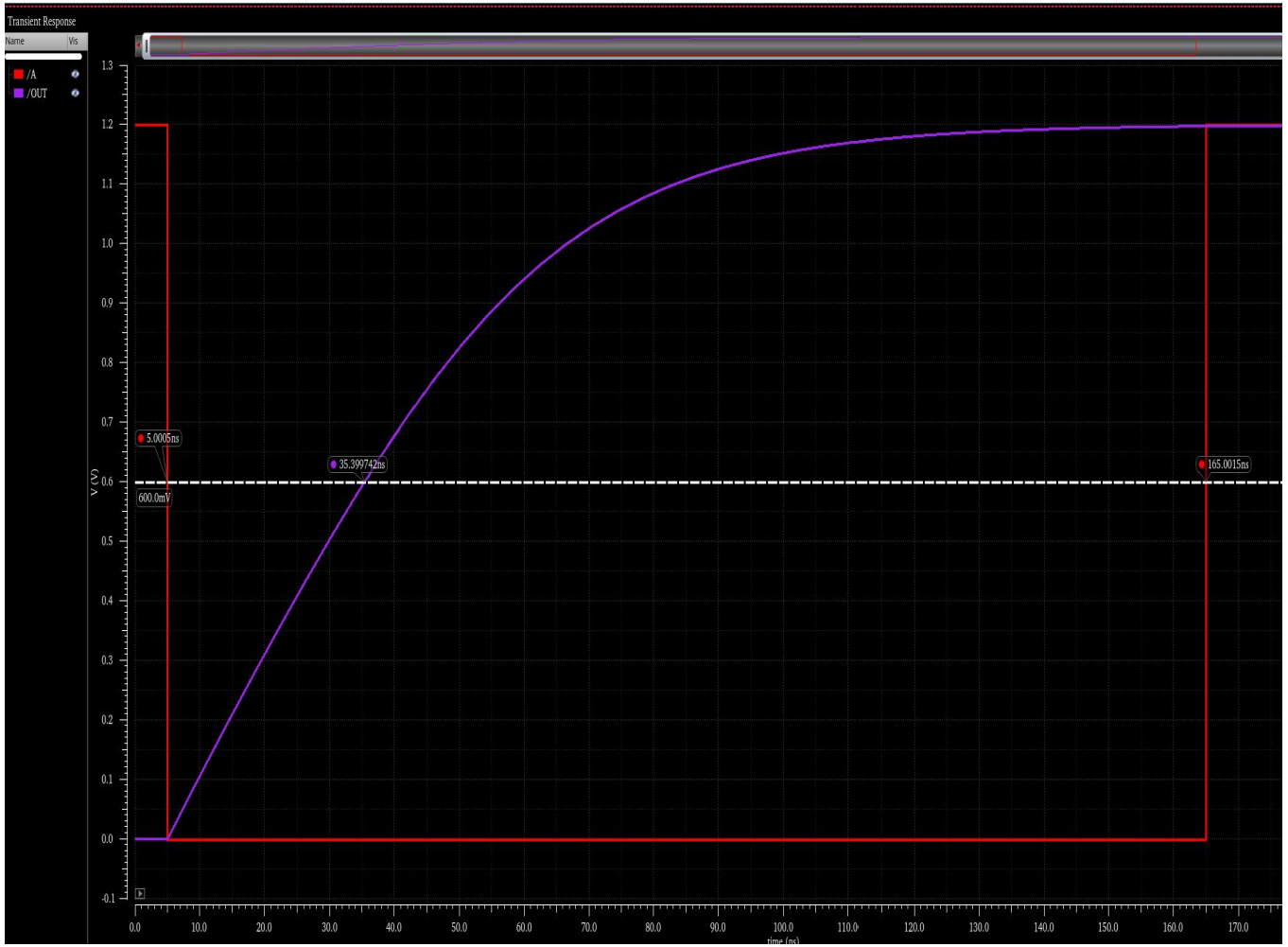
# ADDR延时

## PMOS仿真实测

### 电路搭建




### 仿真结果

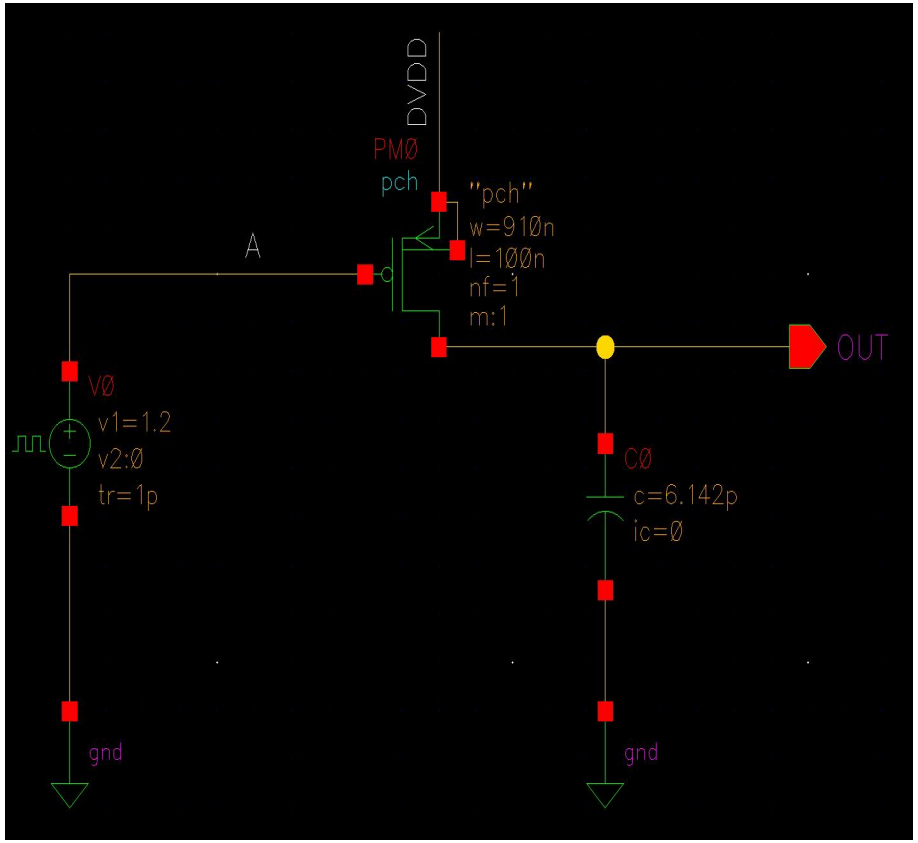



仿真测得延迟时间为30.40ns,与理论计算值有偏差，理论计算是恒定电阻模型，仿真中管子并不满足，管子落在了饱和区

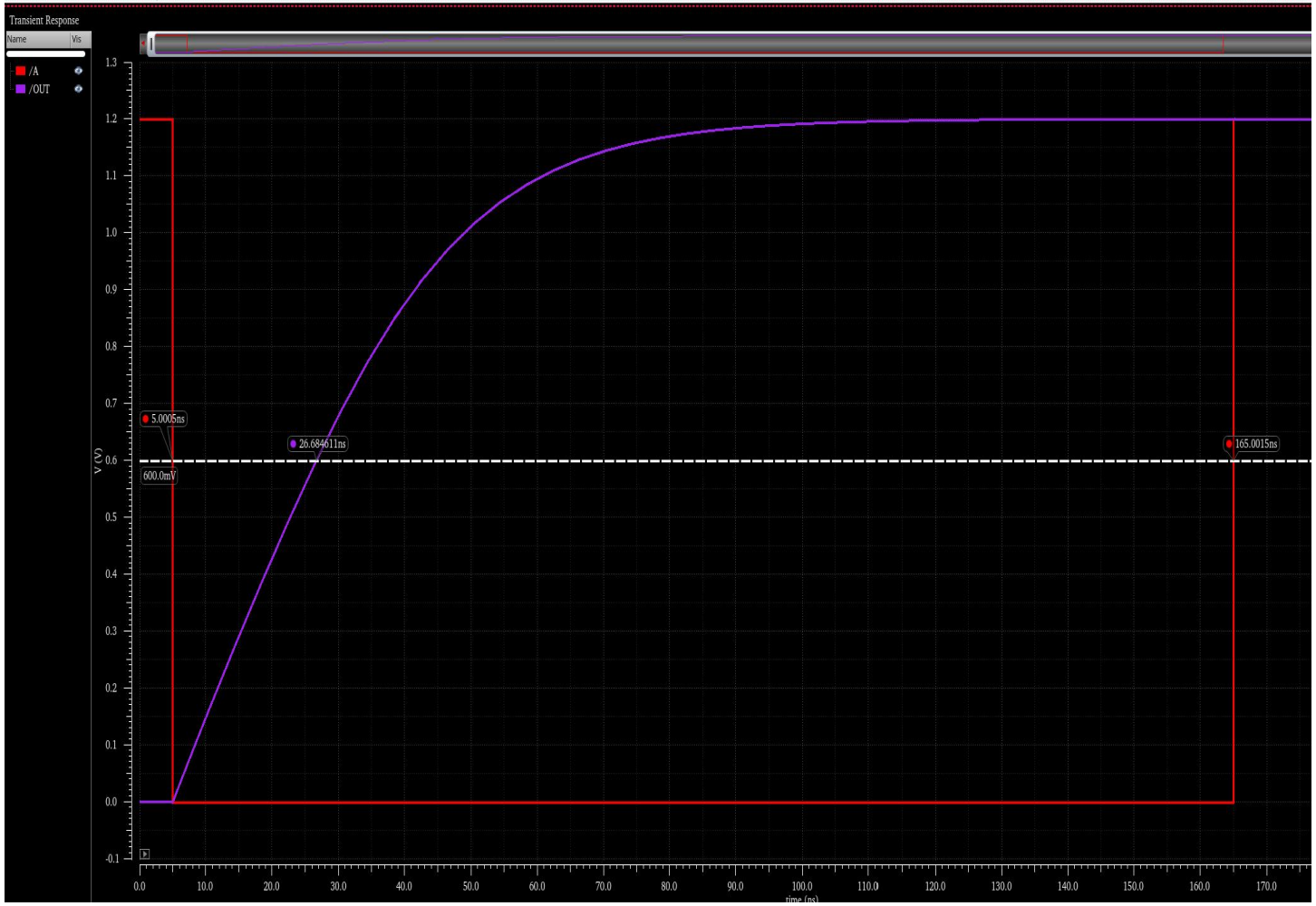
# ADDR延时

## PMOS仿真实测

### 电路搭建




### 仿真结果

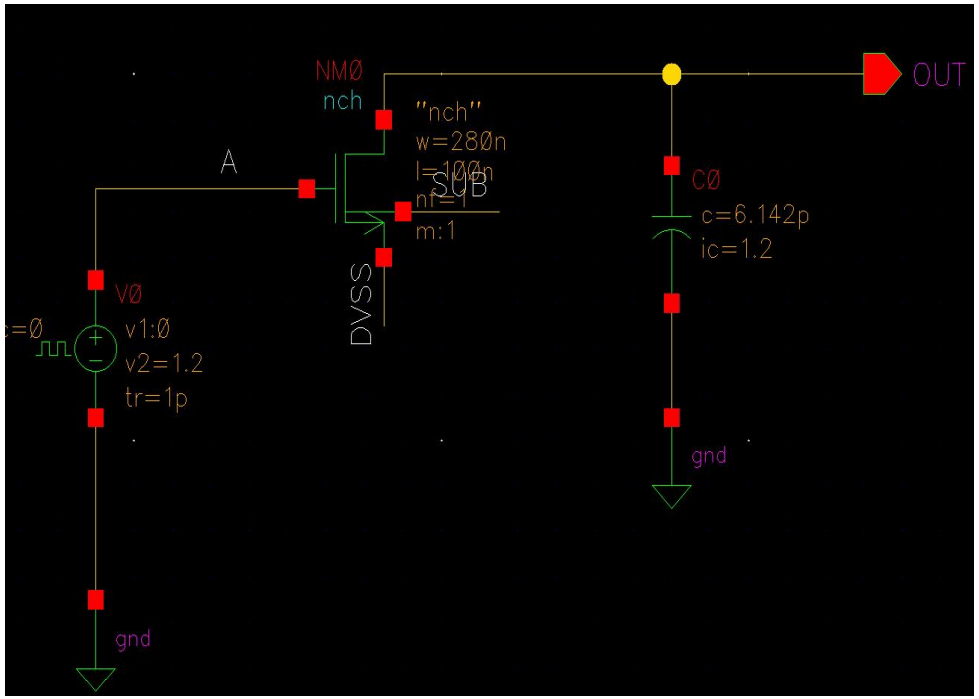



经计算仿真，将PMOS管的尺寸调节为W=910nm,L=100nm,此时延迟时间为21.68ns，满足要求

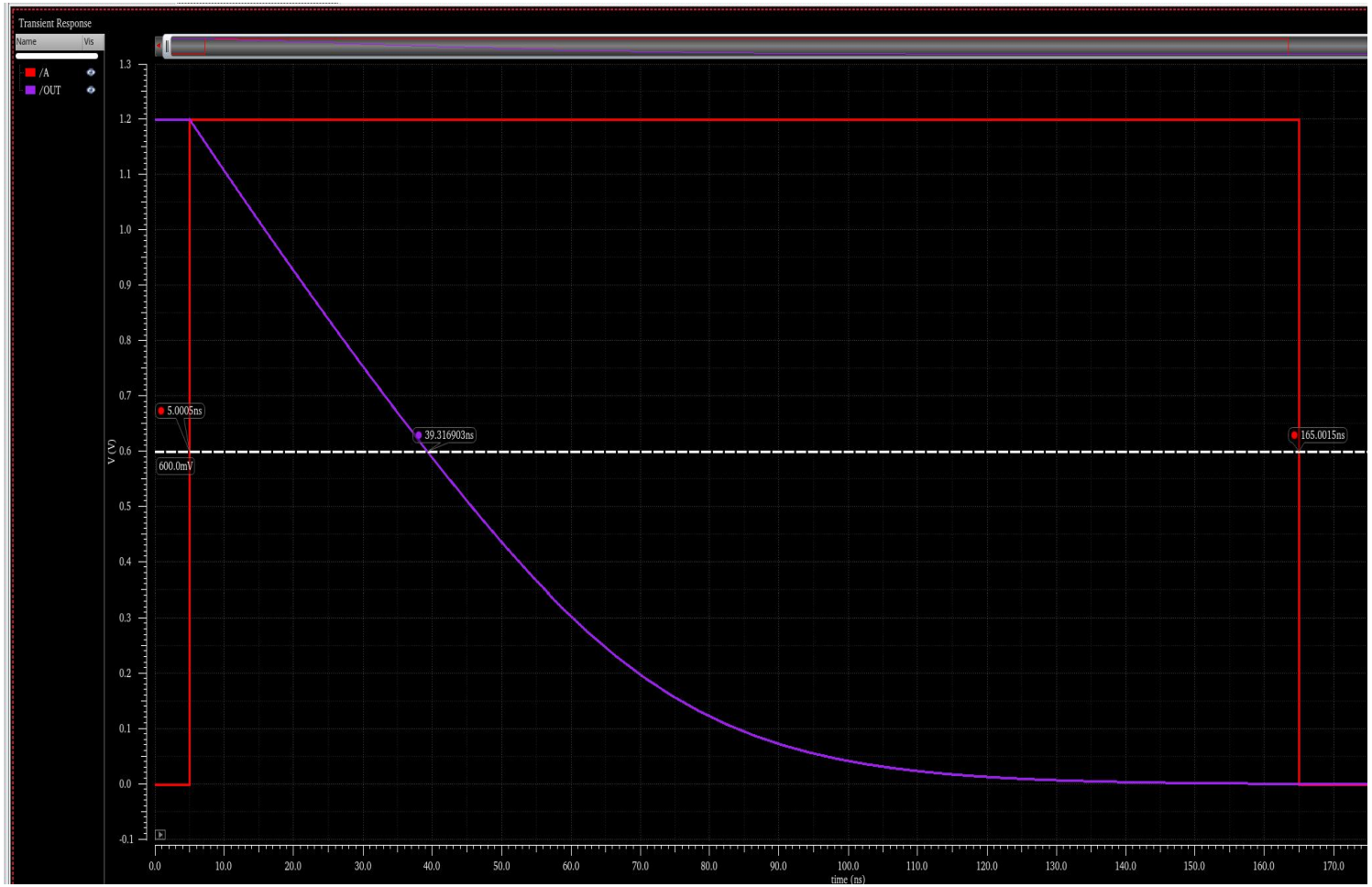
# ADDR延时

## NMOS仿真实测

### 电路搭建




### 仿真结果

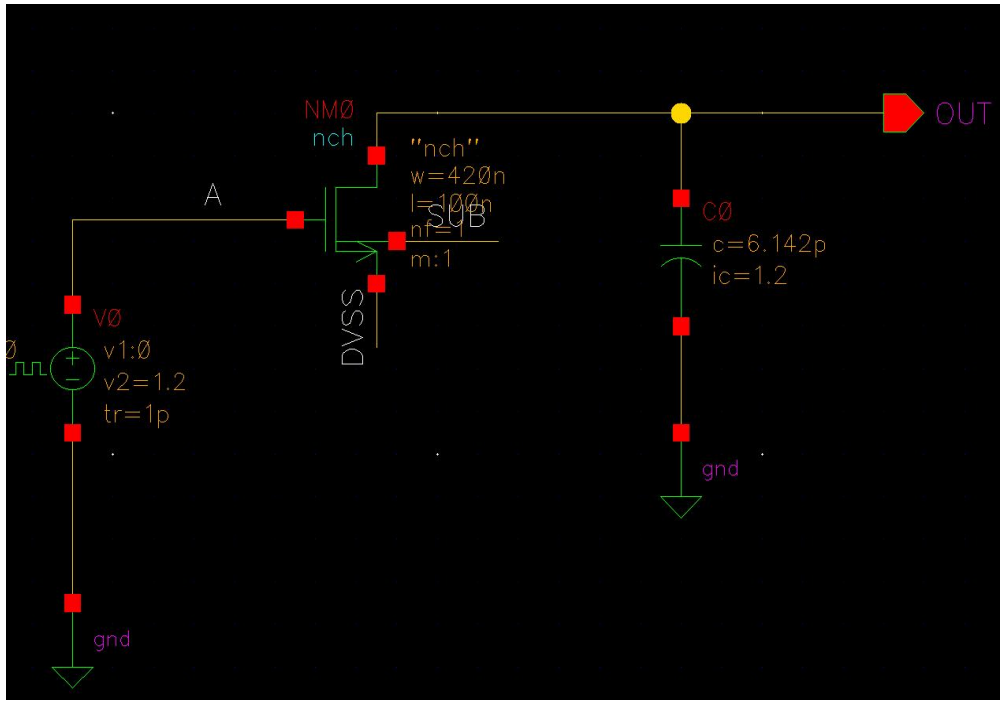



仿真测得延迟时间为34.32ns,与理论计算值有偏差，理论计算是恒定电阻模型，仿真中管子并不满足，管子落在了饱和区

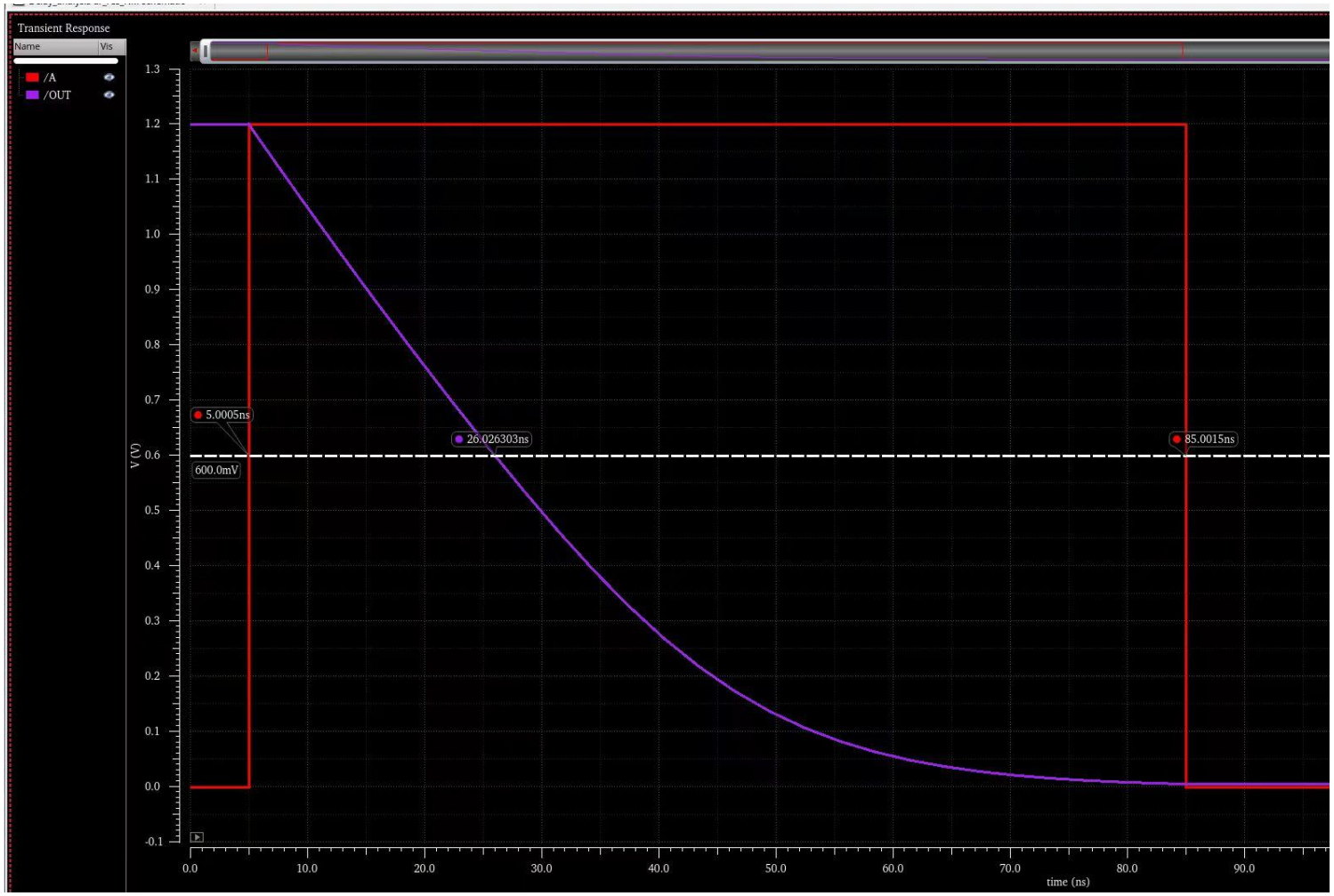
# ADDR延时

## NMOS仿真实测

### 电路搭建




### 仿真结果

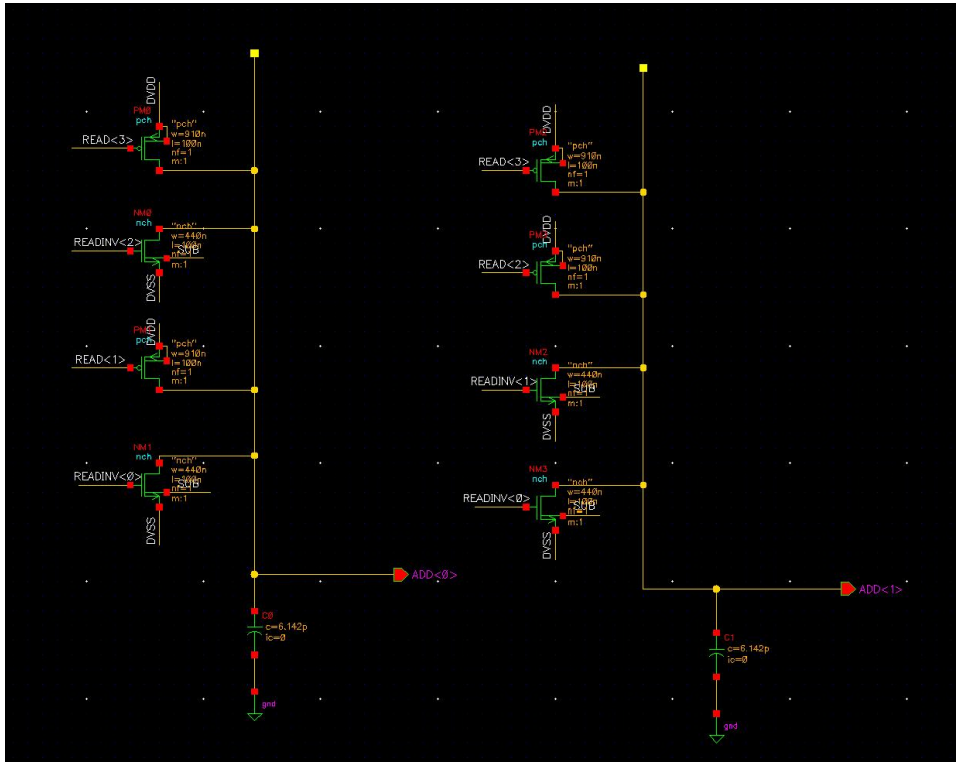



经计算仿真，将NMOS管的尺寸调节为W=420nm,L=100nm,此时延迟时间为21.03ns，满足要求

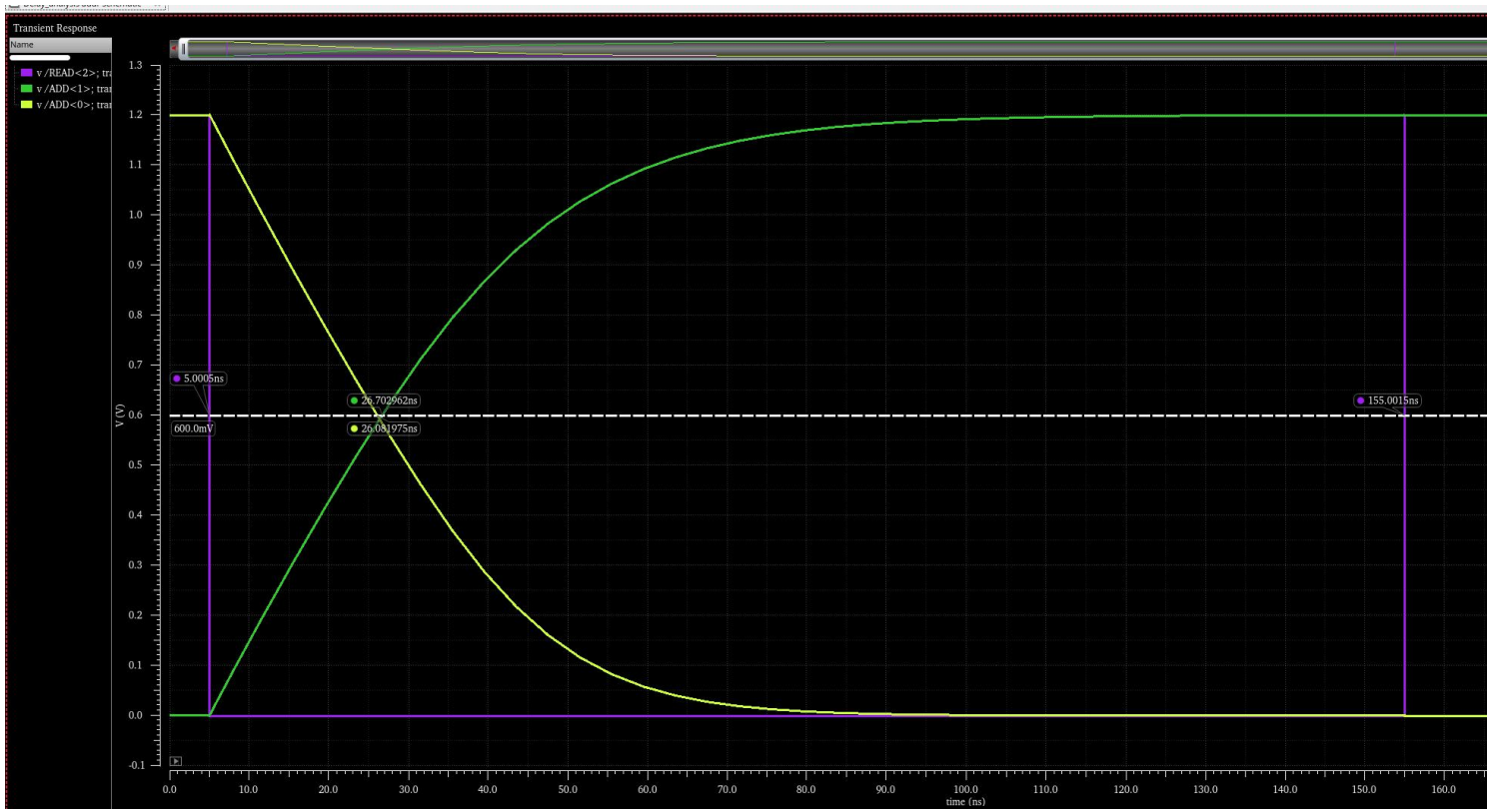
# ADDR延时

## 四像素两位地址仿真

### 电路搭建

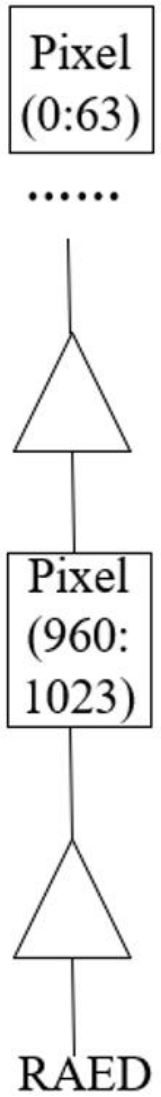



### 仿真结果




当第二个像素击中时，输出地址10，高位地址信号上升时间为21.70ns,低位地址信号下降时间为21.08ns,满足要求

# READ延时




## READ延迟32ns,预估驱动电阻为5kΩ左右

### Buffer尺寸

| | 第一级 | 第二级 |
|---|---|---|
| PMOS | W=330nm<br>L=100nm | W=670nm<br>L=100nm |
| NMOS | W=240nm<br>L=100nm | W=290nm<br>L=100nm |

**此时上拉驱动电阻为5.02KΩ**

**理论计算从输入到输出的50%延迟时间为30.2ns**

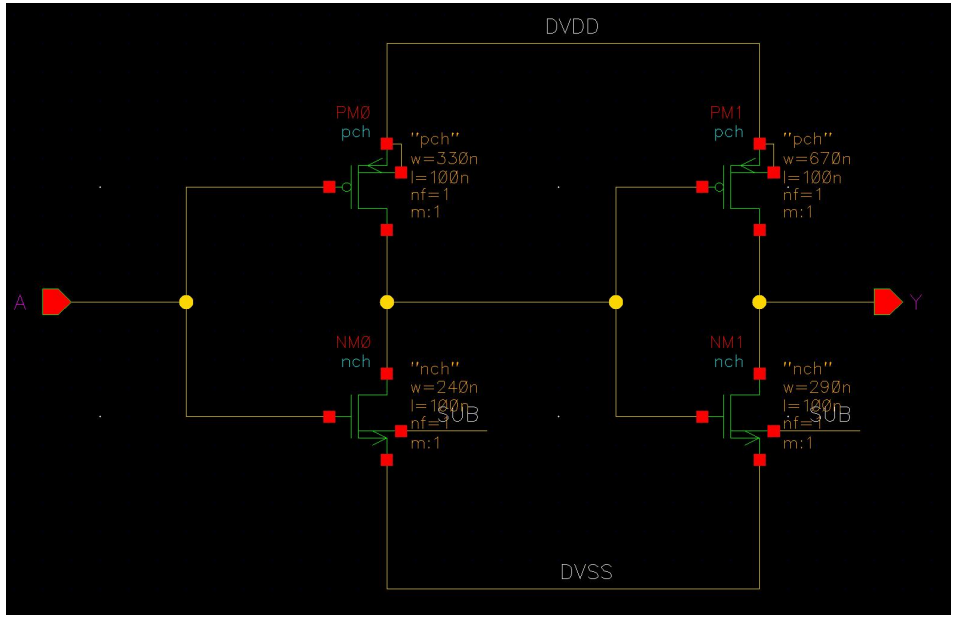
**此时下拉驱动电阻为4.99KΩ**

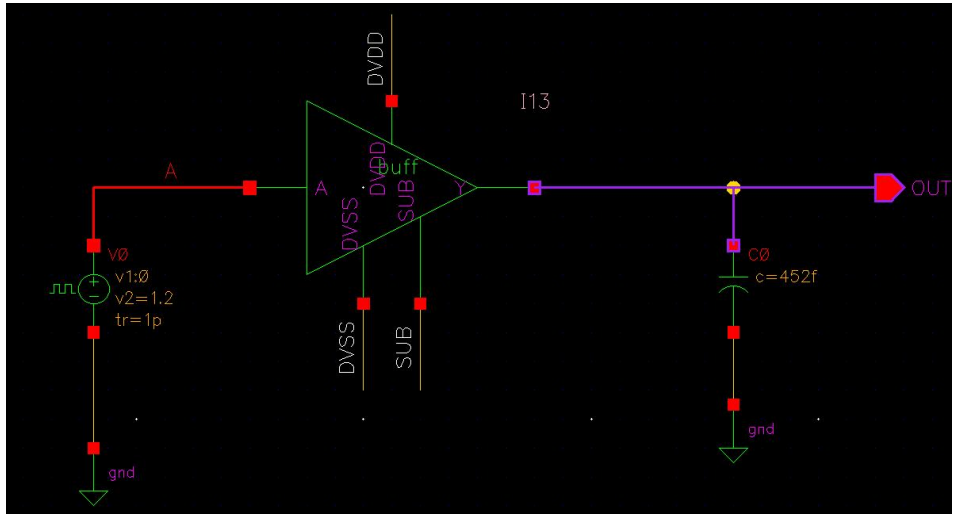
**理论计算从输入到输出的50%延迟时间为30.06ns**

# READ延时

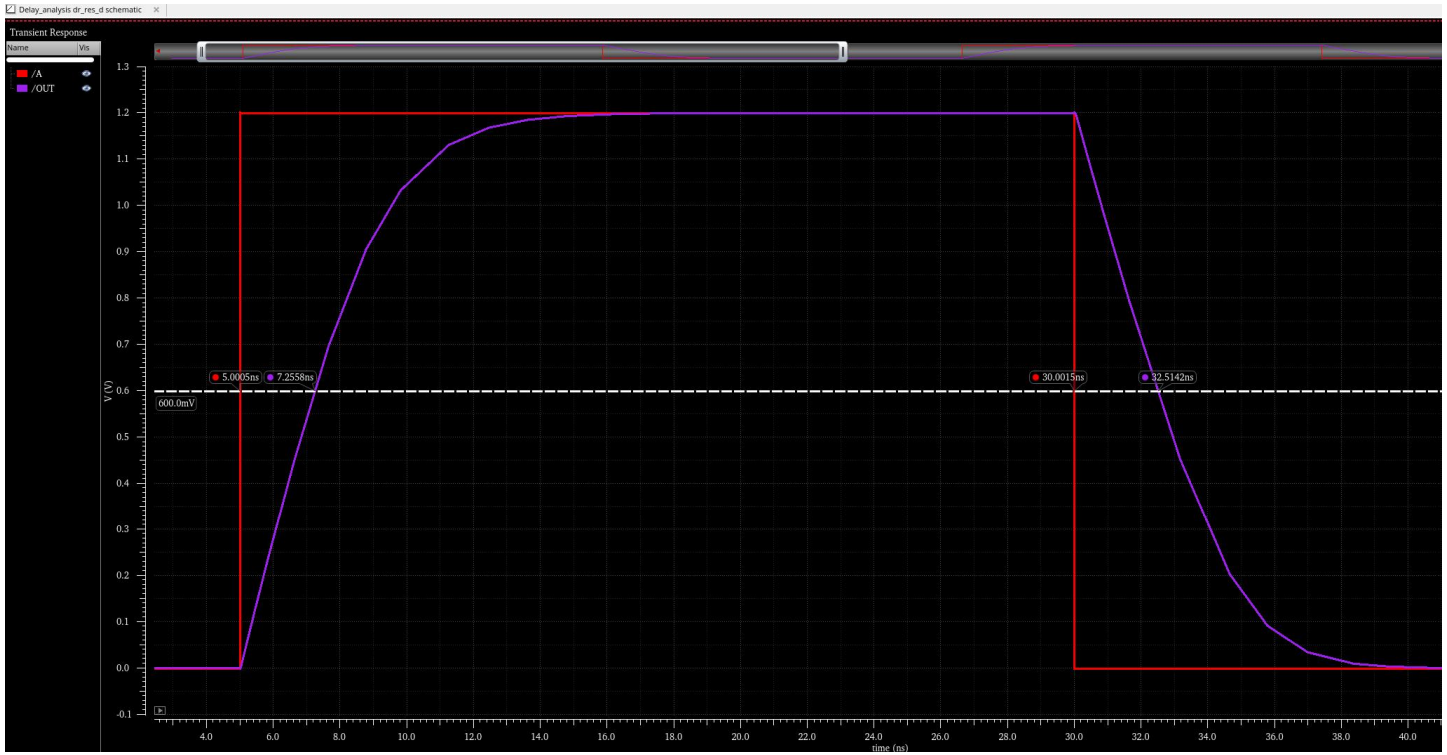
# BUFFER仿真实测

## 电路搭建




## 仿真结果

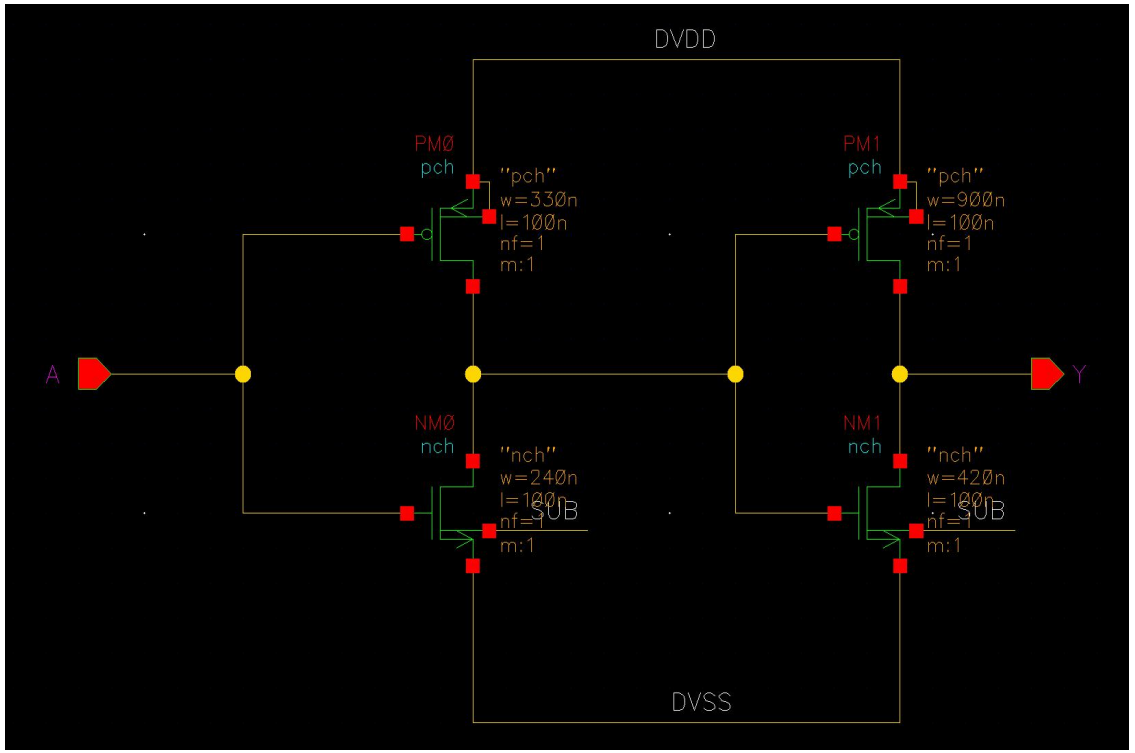



**仿真测得上升与下降延迟时间分别为41.15ns、45.27ns,与理论计算值有偏差**

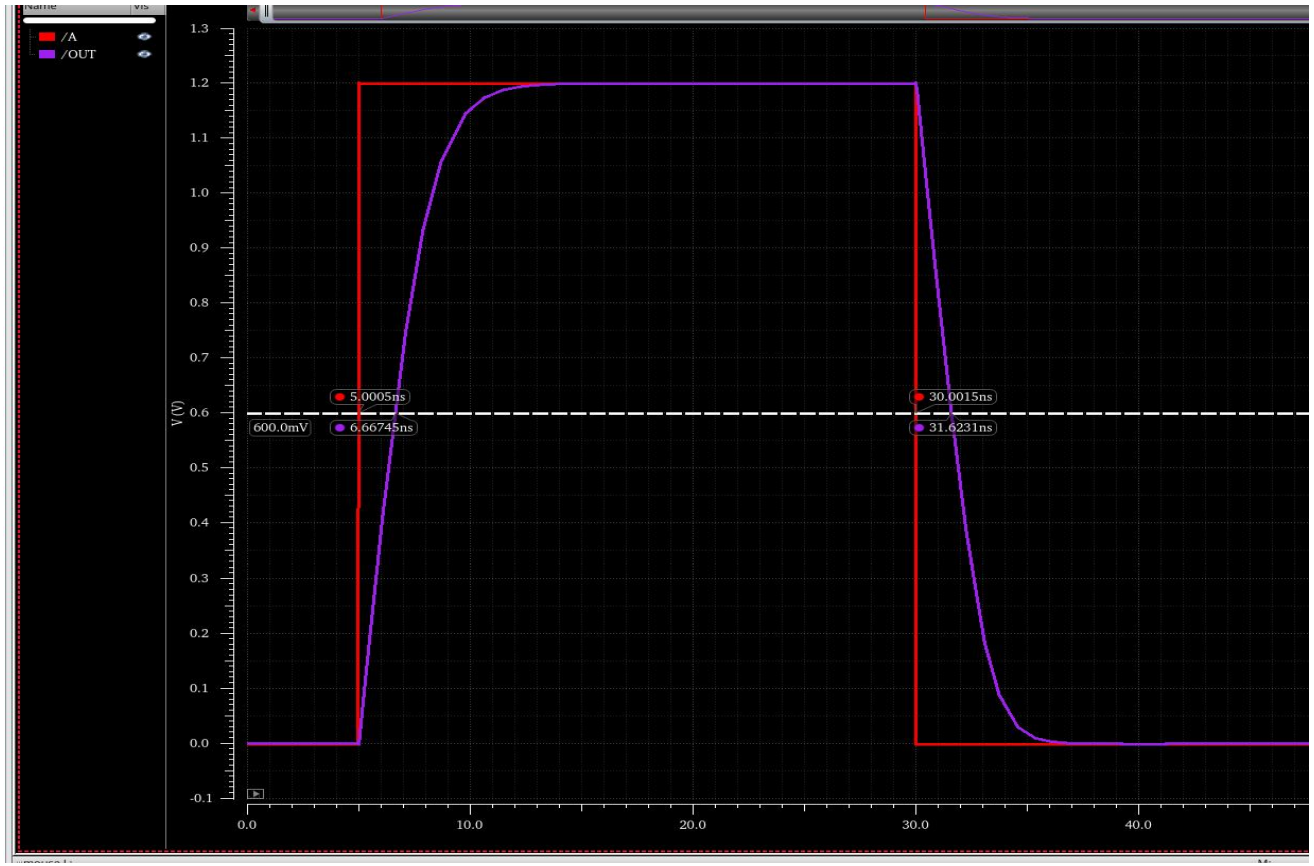
# READ延时

## BUFFER仿真实测

### 电路搭建




### 仿真结果

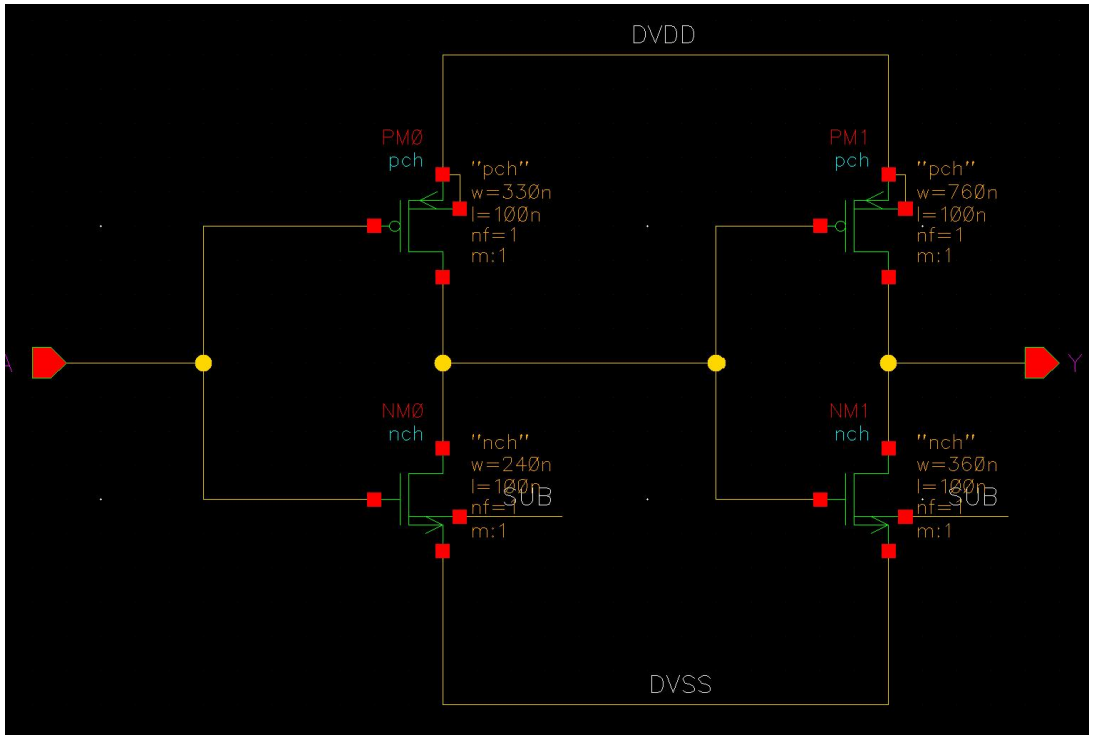



经计算仿真，将BUFFER的尺寸第二级PMOS调节为W=900nm,L=100nm;NMOS调节为W=420nm,L=100nm,此时上升和下降延迟时间分别为31.99ns和31.68ns，满足要求

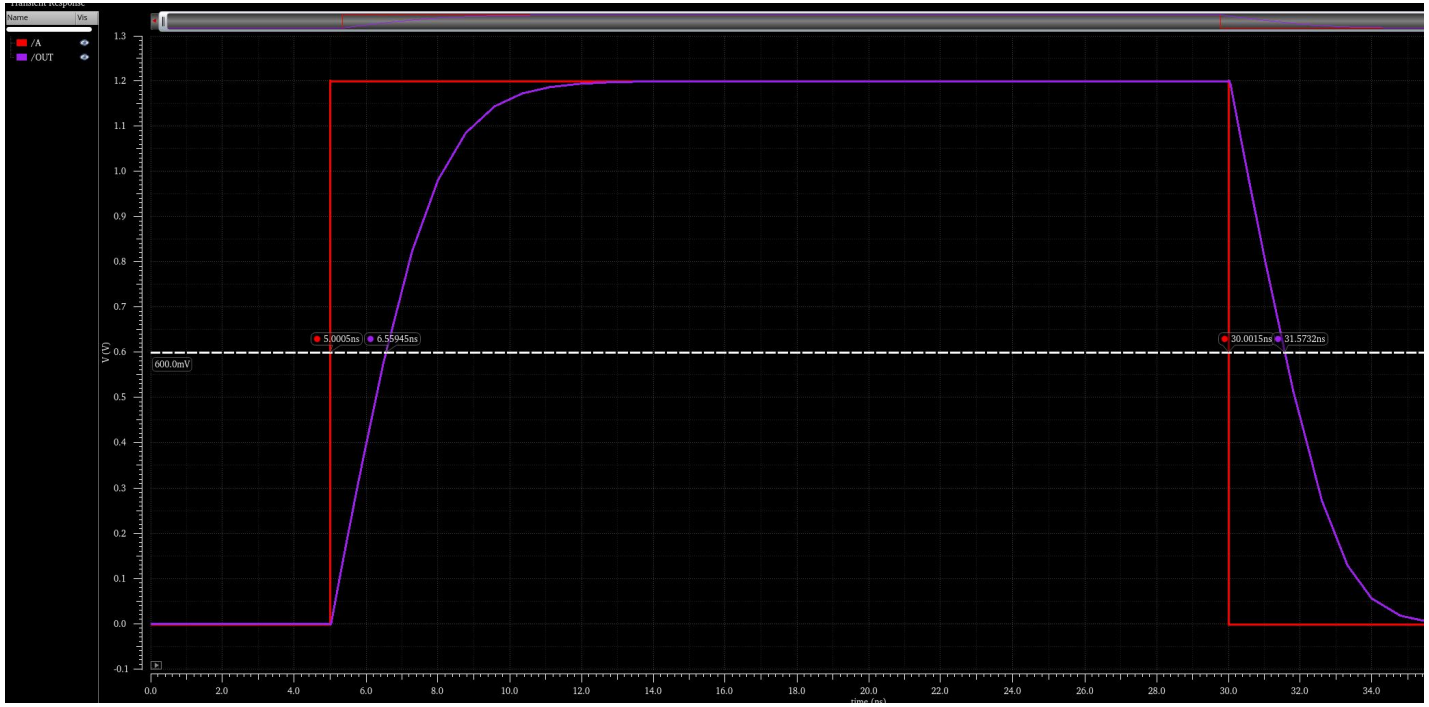
# FREEZE延时

## BUFFER仿真实测

### 电路搭建




### 仿真结果




经计算仿真，将BUFFER的尺寸第二级PMOS调节为W=760nm,L=100nm;NMOS调节为W=360nm,L=100nm,此时上升和下降延迟时间分别为29.61ns和29.83ns，满足要求