[B01]

Benchmarking APES against SAD for Single-Beam Background Simulations at BEPCII-U

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Abstract

Under identical machine settings and physics models, we benchmark APES (Accelerator Physics Emulation Studio) against SAD (Strategic Accelerator Design) for single-beam background simulations at BEPCII-U. Ring parameters, optical functions, loss distributions near the interaction point and background-particle lifetimes are compared: ring parameters agree to better than **1%**, optical functions and IP-region loss distributions show good agreement in both rings, and lifetime deviations lie within **one statistical error**.

Tracking particles of the same scale (10^5), APES's GPU tracking outruns SAD by **×32.959–33.433** for pure tracking and **×2.728–2.875** for the full ring-level simulation. After further optimization of APES's GPU tracking, specifically for background simulations, the speedups relative to SAD reach **×221–222** and **×15.4–15.6**, respectively.

Introduction

Accelerator-physics simulation is a fundamental basis for accelerator design, beam-dynamics studies and machine operation, and its accuracy and reliability directly affect machine performance and physics research. For beam-background studies, accurately predicting beam lifetimes and loss distributions requires simulation software that both describes the relevant physics processes reliably and supports large-scale particle tracking. APES (Accelerator Physics Emulation Studio), newly developed at the Institute of High Energy Physics, Chinese Academy of Sciences, exactly matches these needs[1]. To evaluate its single-beam background simulation capability on a real accelerator lattice, we benchmark APES against SAD (Strategic Accelerator Design)[2], which has been extensively used for beam-background studies at BEPCII[3].

In single-beam background studies at BEPCII-U[4,5], lost background particles originate mainly from three processes[6–8]: Touschek scattering, beam-gas bremsstrahlung and beam-gas Coulomb scattering. Both rings use identical machine and beam-parameter settings, and APES and SAD use exactly the same input parameters and settings; the calculated ring parameters for the electron ring (BER) are listed in Table 1.

Parameter	SAD	APES	Diff. (%)
Horizontal tune	7.505616	7.505697	+0.001081
Vertical tune	5.575804	5.575777	−0.000494
Synchrotron tune	3.822643×10^{-2}	3.822641×10^{-2}	−0.000064
Momentum compaction	1.657748×10^{-2}	1.649890×10^{-2}	−0.474022
Horizontal emittance (m·rad)	1.404505×10^{-7}	1.397897×10^{-7}	−0.470522
Longitudinal emittance (m)	6.756492×10^{-6}	6.749357×10^{-6}	−0.105593
Horiz. damping time (s)	1.300762×10^{-2}	1.303240×10^{-2}	+0.190527
Vert. damping time (s)	1.258763×10^{-2}	1.258701×10^{-2}	−0.004926
Long. damping time (s)	6.194632×10^{-3}	6.188384×10^{-3}	−0.100869

Table 1: Calculated ring parameters for the electron ring (BER); Diff. (%) = (APES − SAD)/|SAD| × 100%.

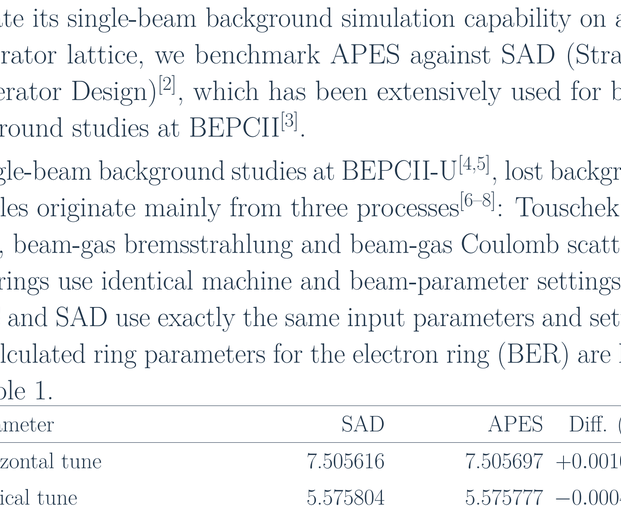


Figure 1: Optical functions along the BER: SAD vs. APES.
β_x, β_y beta functions
α_x, α_y alpha functions
η_x, $\eta_{x'}$ horizontal dispersion and its derivative

Touschek scattering is the intra-bunch scattering between particles: transverse momentum is converted into longitudinal momentum, pushing particles beyond the energy acceptance[9,10]. **Beam-gas bremsstrahlung** is the inelastic collision between a beam particle and a residual-gas nucleus: the particle loses energy by photon emission[11]. **Beam-gas Coulomb scattering** is the elastic deflection of beam particles by residual-gas nuclei: particles deviate transversely from the orbit[11].

Losses near the IP

Particles lost near the interaction point (IP) directly affect detector data taking and are therefore a key focus of this study.

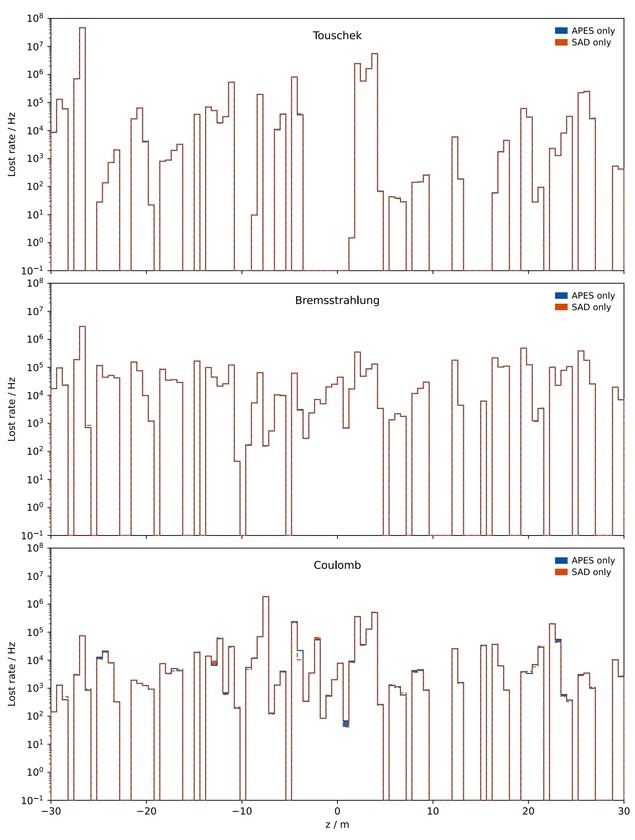


Figure 2: Longitudinal loss rates within ±30 m of the IP in the BER: APES vs. SAD.

Beam lifetimes

Table 2: Beam lifetimes over ten runs (hours): SAD vs. APES GPU.

Ring	Process	SAD (h)	APES GPU (h)	Agreement
BER	Touschek	15.404 ± 0.036	15.402 ± 0.020	0.017%
BER	Brem.	57.213 ± 0.005	57.215 ± 0.016	0.005%
BER	Coulomb	84.259 ± 0.399	84.318 ± 0.506	0.070%
BPR	Touschek	16.862 ± 0.038	16.865 ± 0.021	0.021%
BPR	Brem.	57.729 ± 0.004	57.734 ± 0.010	0.008%
BPR	Coulomb	87.025 ± 0.744	87.422 ± 0.671	0.456%

Values are ten-run means ± sample standard deviation (hours).

Lifetimes agree within one statistical error

Based on the mean lifetimes of ten independent runs, the lifetimes of the three background processes are compared for both rings: the difference of every case is smaller than one statistical error.

APES GPU Tracking Optimization

Within the background-simulation framework, APES's GPU tracking is optimized with four measures to raise the speedup.

Theta optimization. Skip rotation trigonometry at theta = 0

Device LTO (`-dlto`). Element-map functions inlined across compilation units

Particle compaction. Lost particles removed periodically

Single kernel. One launch for the whole ring

Speedups are relative to the previous GPU release, all at $\sim 10^5$ particles; the first three measures combine to **×6.6–6.8** for pure tracking, and to **×13–16** when particle compaction is enabled every 10 turns. In full ring-level runs of both rings, the optimized APES GPU tracking runs **×5.4–5.7** faster than before optimization and **×15.4–15.6** faster than SAD, with byte-identical output—the physics results are unaffected. The speedup is not a constant: it increases as the number of particles increases and saturates once the GPU is fully occupied.

GPU speedup

	prev GPU		new GPU	
Ring	Complete	Pure tracking	Complete	Pure tracking
BER	**2.728×**	**32.959×**	**15.6×**	**222×**
BPR	**2.875×**	**33.433×**	**15.4×**	**221×**

Complete = complete ring-level simulation; Pure = pure multi-turn tracking; both use $\sim 10^5$ particles. Values are ten-run mean cumulative times relative to SAD CPU; SAD uses a Xeon Gold 6140 CPU core, APES uses an NVIDIA V100 GPU.

Conclusions

Under identical BEPCII-U models and inputs, APES reproduces SAD's principal single-beam loss observables: ring parameters agree to better than **1%**, optical functions agree well, lifetime deviations lie within **one statistical error**, and the main IR loss patterns are consistent. GPU acceleration is considerable for tracking large particle ensembles ($\sim 10^5$ particles), reaching **×221–222** for pure tracking and **×15.4–15.6** for the complete simulation.

References
[1] W. Liu et al., "Advancements in the development of beam dynamics software APES for CEPC," Proc. IPAC'24, Nashville, TN, 2024, pp. 1021–1024.
[2] Y. Ohnishi et al., "Computer program complex SAD for accelerator design, simulation and commissioning," Proc. 16th Annual Meeting of Particle Accelerator Society of Japan, 2019, pp. 4–8.
[3] H.C. Shi et al., "Beam background simulation and experiment at BEPCII," Nucl. Instrum. Methods Phys. Res. A 1050 (2023) 168174.
[4] H. Geng et al., "Lattice design for BEPCII upgrade," Proc. IPAC'21, Campinas, Brazil, 2021, pp. 3756–3758.
[5] H. Geng et al., "An alternative design for BEPCII upgrade," Proc. IPAC'22, Bangkok, Thailand, 2022, pp. 1591–1593.
[6] N.-F. Zhou et al., "Monte Carlo simulation of BEPCII beam-related background (I): synchrotron radiation," Chin. Phys. C 28 (2004) 227–231.
[7] D.-P. Jin et al., "Monte Carlo simulation of the BEPCII/BESIII backgrounds: beam-gas interactions," Chin. Phys. C 28 (2004) 1197–1202.
[8] D.-P. Jin et al., "Monte Carlo simulation of the BEPCII/BESIII backgrounds: Touschek effects," Chin. Phys. C 30 (2006) 449–453.
[9] H. Bruck, *Circular Particle Accelerators*, LA-TR-72-10-REV, 1974.
[10] A. Piwinski, "The Touschek effect in strong focusing storage rings," arXiv:physics/9903034, 1999.
[11] H.C. Shi, "Analysis of beam background at electron-positron colliders in the tau-charm energy region," PhD thesis, University of Science and Technology of China, 2023.

[B02]

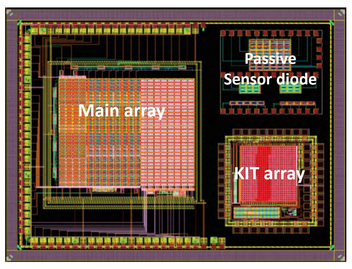
Radiation tolerance study of the first 55nm HV-CMOS pixel sensor

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Introduction

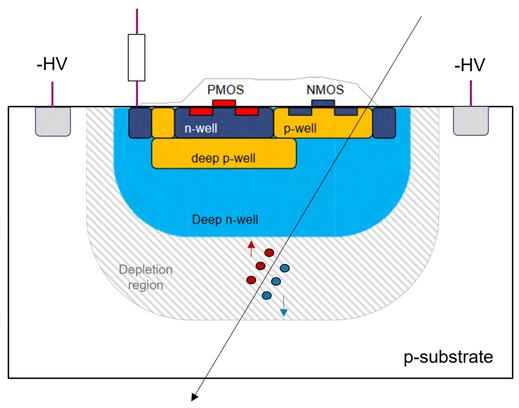
High-voltage CMOS (HV-CMOS) pixel sensors are promising candidates for tracking in future high-energy physics experiments. Developed in a commercial 55 nm HV-CMOS technology, the COFFEE2 prototype integrates pixel-level circuitry for sensor and analog front-end characterization alongside a full data-driven readout array.



To evaluate its radiation tolerance, COFFEE2 underwent proton irradiation at the Chinese Spallation Neutron Source (CSNS) and X-ray irradiation at Zhejiang University. Performance was assessed using S-curve scans and time-over-threshold (ToT) measurements as a function of threshold to characterize the effects of proton irradiation, X-ray total ionizing dose (TID), and chip power state during irradiation. These preliminary irradiation results provide initial validation of both the COFFEE2 design and the commercial 55 nm HV-CMOS process, demonstrating its viability for future detector applications.

Process Features

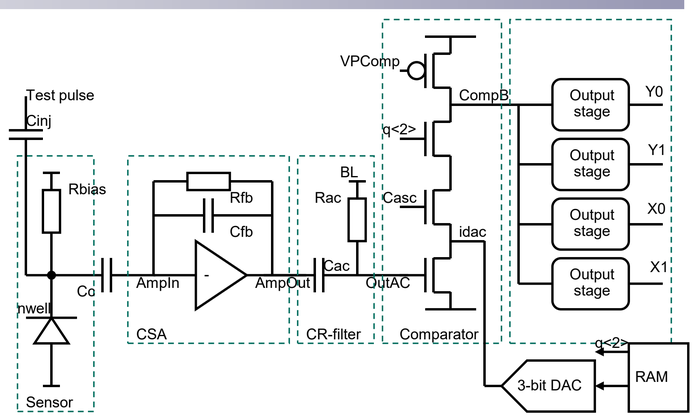
- Deep n-well — P substrate junction as collection electrode
- Triple-well process: N-well/P-well/Deep n-well
- P-type substrate resistivity: $10\Omega \cdot \mathrm{cm}$
- Guard ring: one inner N-well ring, with two P-well outer rings
- Substrate breakdown Voltage > 70V with frontside HV bias
- More design details:
  - *Z. Chen et al., Feasibility study of CMOS sensors in 55 nm process for tracking,* Nuclear Instruments and Methods in Physics Research A 1069 (2024) 169905.
  - *H. Zhang, et al., High voltage monolithic pixel sensor in 55 nm technology,* JINST 20 (2025) 03, C03023.



Working principle of HV-CMOS sensors.

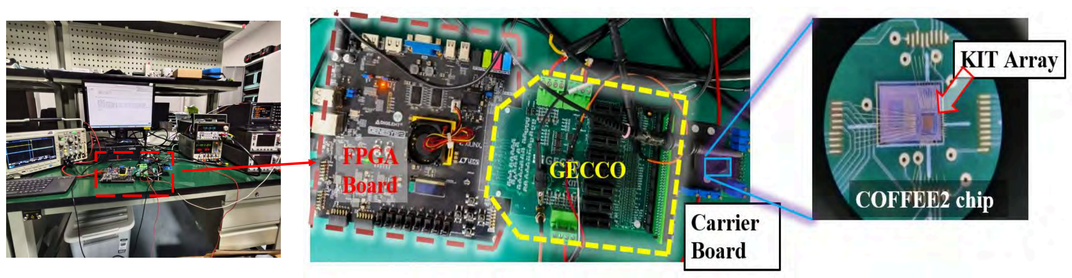
KIT Pixel Electronics

- Pixel electronics (25 μm × 25 μm)
  - Sensor diode
  - Charge Sensitive Amplifier (CSA)
  - CR filter
  - Comparator
  - RAM and tune DAC
  - Output stages
- Work principle
  - Charge collected by pixel n-well
  - Converted to voltage signal by Charge Sensitive Amplifier
  - Analog voltage pulse shaped and converted to digital signal by comparator
  - Output stage generates current
  - Current is sent via address line to the transimpedance amplifier outside matrix
  - Address lines have constant potential – no cross talk



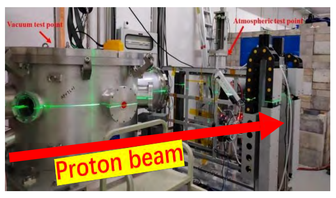
H. Zhang, etl. High voltage monolithic pixel sensor in 55nm technology JINST 20 (2025) 03, C03023

Bench test setup

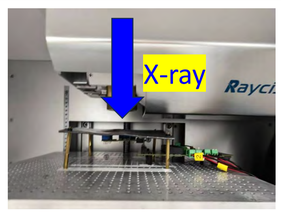


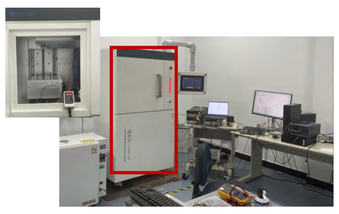
- Genesys2 FPGA Board
  - Translates commands from the PC into the precise low-level digital protocol
- GECCO Control Readout Board
  - It integrates power delivery and controls and supplies all required electrical
  - potentials for testing the chip
- Carrier Board (with wire-bonded COFFEE2 chip)
- Signal Generator
  - Provide charge injection to the chip through the GECCO board

Irradiation Test



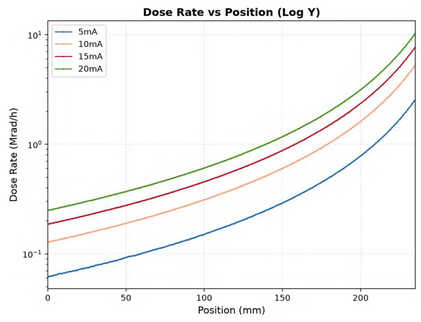
Proton irradiation at CSNS





X-ray irradiation at Zhejiang University (ZJU)

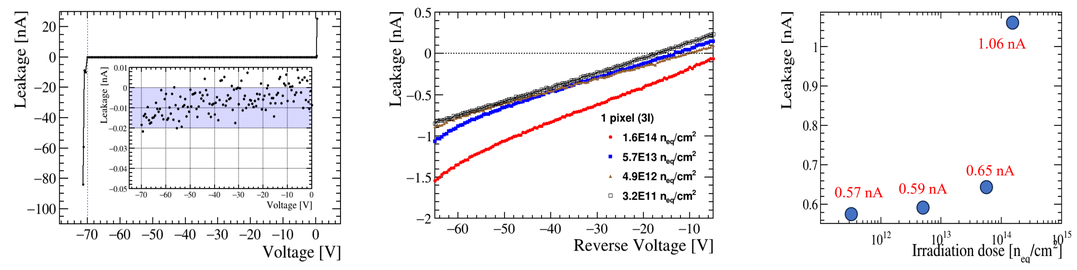
- Proton irradiations at China Spallation Neutron Source, reaching a maximum fluence exceeding $10^{15} \mathrm{n_{eq}/cm^2}$
- X-ray irradiation at Zhejiang University (ZJU) was performed at different operating voltages and currents to achieve different dose rates.
- The right panel shows the dose rate (Mrad/h) as a function of position at different currents, with the dose rate plotted on a logarithmic scale.



Main results

Proton-Induced I-V Changes

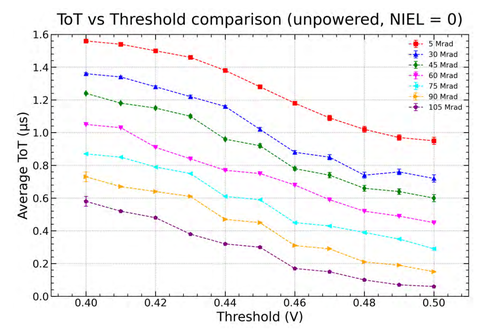
Under 50V setup, Leakage current increased from ~ 10 pA to ~ 1nA after irradiated. The magnitude of leakage current is proportional to the irradiation fluence



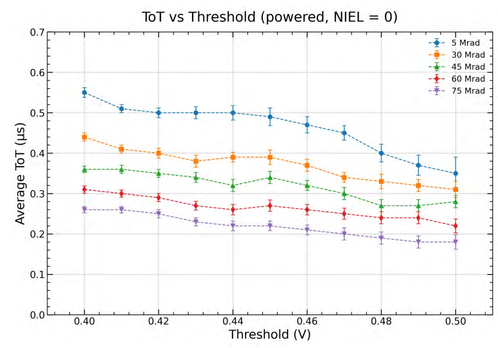
IV test results of COFFEE2 in different irradiation fluence

Irradiation Tolerance Evaluation

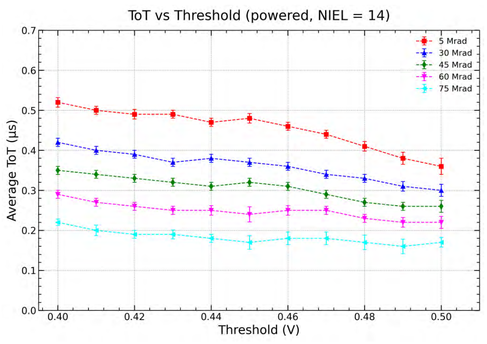
- Measuring time-over-threshold (TOT) as a function of threshold helps assess radiation tolerance by revealing irradiation-induced changes in the analog front-end response.
- Panels (a)–(c) show time-over-threshold (TOT) versus threshold at different X-ray doses (Mrad): (a) for an unpowered chip, (b) for a powered chip, and (c) for a powered chip previously irradiated with protons to a fluence of $10^{14}\ \mathrm{n_{eq}/cm^2}$



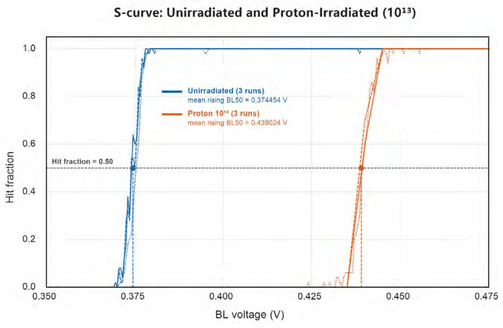
(a)



(b)



(c)



(d)

- S-curve measurements before and after irradiation reveal changes in threshold and noise, helping assess the stability of the chip's response to radiation.
- Panel (d) compares the S-curves of an unirradiated chip and a chip irradiated with protons to $10^{13}\ \mathrm{n_{eq}/cm^2}$, showing a threshold shift from 0.37 V to 0.43 V following irradiation.

Summary & Outlook

The radiation tolerance of COFFEE2, developed in a commercial 55 nm HV-CMOS process, was investigated through proton and X-ray irradiation. I–V measurements, time-over-threshold (TOT) versus threshold curves, and S-curve scans were used to assess performance under different fluences, TID levels, and chip power conditions. The preliminary results support the potential of COFFEE2 and the technology for future tracking detectors. Further studies will extend the irradiation range, quantify changes in threshold and noise, and evaluate long-term stability and full-array readout performance.

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Circular Electron-Positron Collider
ShangHai, China 2026.10.21- 10.26

中国科学院高能物理研究所
Institute of High Energy Physics, Chinese Academy of Sciences

Development Status & Plans of Serial Powering at IHEP

Tianyu Liang, Fan Hu, Tianyu Shi, Congcong Wang and Hui Zhang
Institution of High Energy Physics, Chinese Academy of Science, Beijing, China

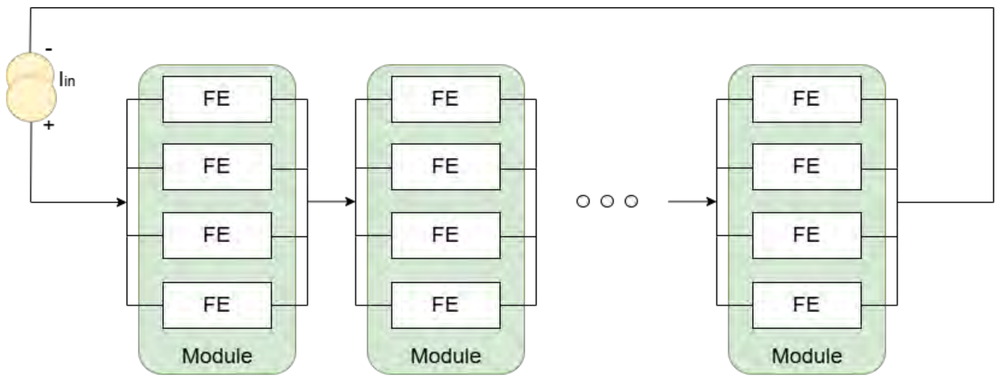
Indico Link

[B03]

Abstract

The increasing level of front-end integration in particle detector has placed new requirements for powering system, particularly in terms of material budget, power distribution, and system scalability. Serial powering, based on a constant current scheme with shunt-LDO regulars (SLDO), has been an attractive solution for large-scale detector systems and future collider upgrades. This contribution presents the development status and future plans of serial powering R&D at the Institute of High Energy Physics (IHEP), with applications to the LHCb Upstream Tracker and future Higgs-factory experiments such as CEPC.

Serial Powering Concept



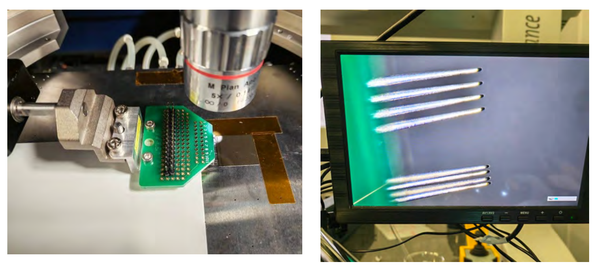
Serial powering diagram

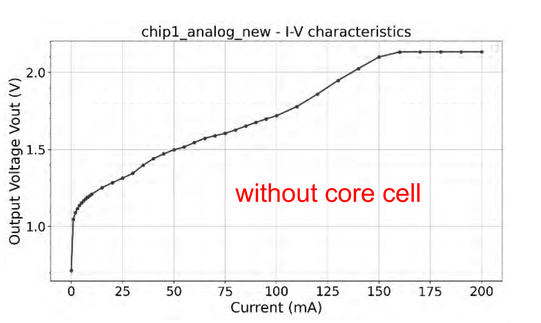
ATLASPix3-based SLDO Tests

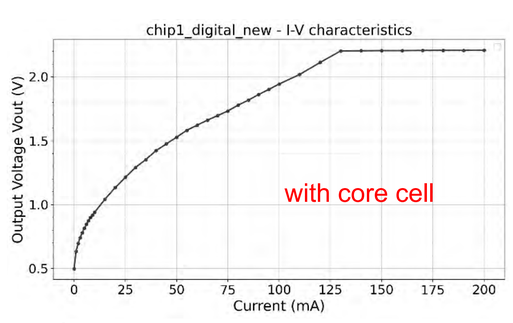
The SLDO performance of ATLASPix3 chips has been systematically investigated using dedicated probe card and Single-Chip Carrier (SCC) setups. Both **bare chip** and chip with **core cell** configurations have been characterized. Four ATLASPix3 chips assembled on SCCs have been operated in series, demonstrating stable voltage regulation and functional outputs. Besides, A 1×4 PCB based on a quad-flex layout has also been designed and produced for module-level serial-powering studies, with wire bonding and functional testing in progress.

Prob card test

- Testing bare chips with the probe card.
- Analog and digital output are both tested.
- Six chips are tested and show excellent I-V characterization.

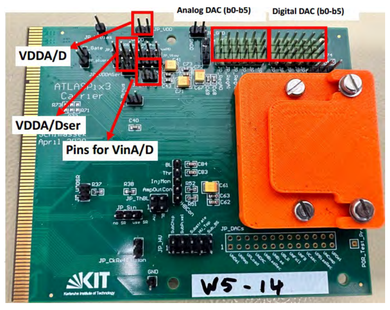


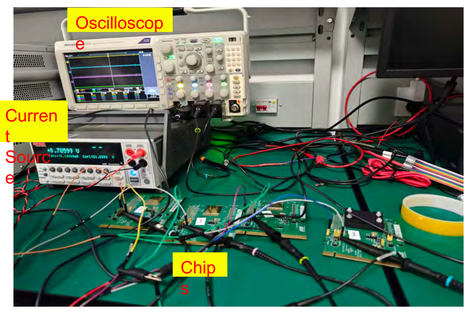




I-V Curve for a random chip

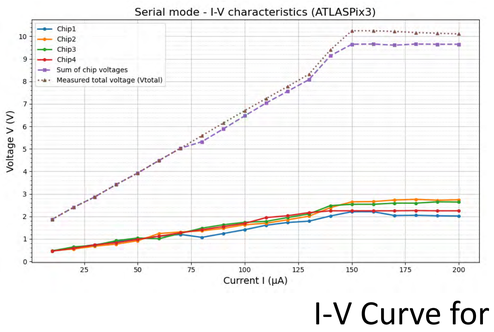
Single-Chip (multi) Carrier(s) test

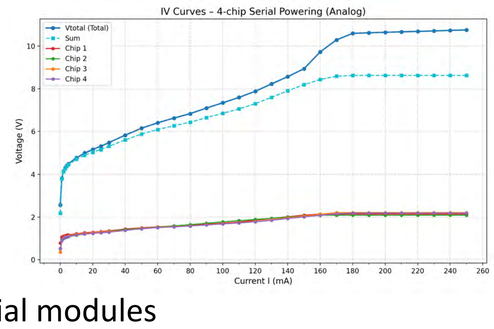




Photos of test setup

- Stable regulation is achieved in both cases
  - ✓ ~150 mA input current yields 2.2–2.8 V (without core cell)
  - ✓ ~160 mA input current yields 2.0 V (with core cell)
- Both scenarios demonstrate good regulation and fully meet our expectations



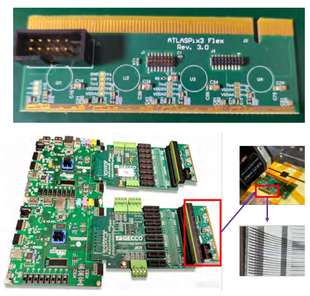


I-V Curve for 4 serial modules

1 x 4 PCB design and production

- A new layout 1×4 test board has been designed and produced suitable for LHCb experiment geometry based on Quad flex.
- ATLASPix Chip will wire bonded on 1 x 4 PCB and test the serial powering functionality

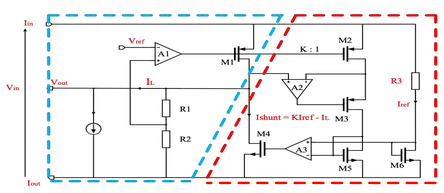
Photo of test board



COFFEE/CHiR Chips with SLDO design

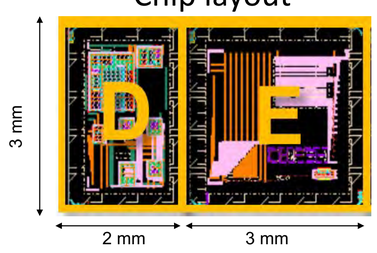
To develop CMOS pixel sensors in a 55~nm HVCMOS processing with serial powering module, two different SLDO architectures have been implemented in the CHiR chip, including an approach following the ATLASPix3 design and another based on the RD53 architecture. Device sizes and types have been optimized for the shunt and pass devices, while an overvoltage tolerant design extends the applicable input voltage range beyond the nominal 1.2~V technology limit to approximately 2~V. Simulations have demonstrated stable regulation for both a single SLDO and a four-chip serial chain. A dedicated CHiR test PCB has been designed, with measurements planned to characterize SLDO output regulation, serial-chain operation, and load-transient response.

Sensor development with SLDO

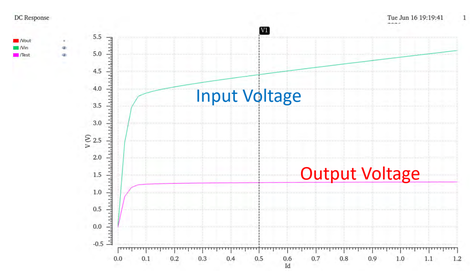


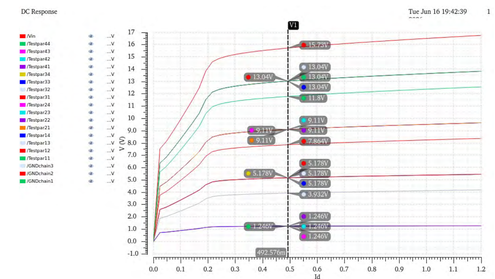
SLDO structure diagram

Chip layout



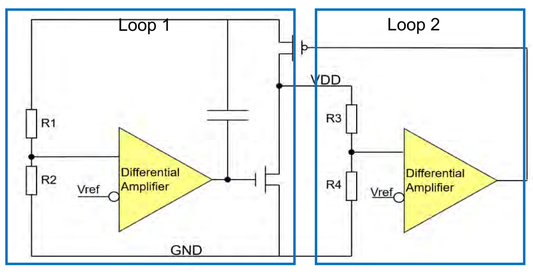
- Two different designs of SLDO implemented in CHiR with 55 nm HVCMOS process (latest COFFEE submission with modified process)





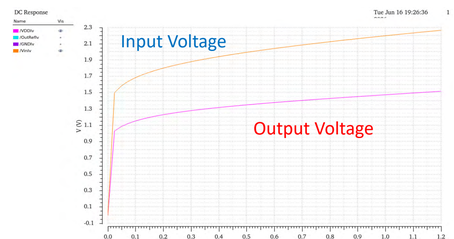
Simulations of both single and four-chip serial configurations.

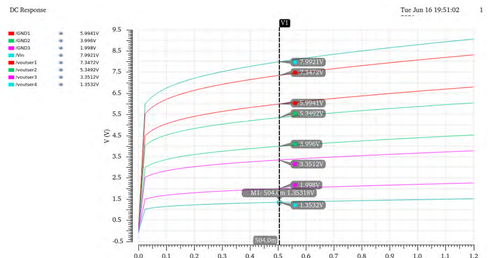
- Device types and dimensions optimised for both shunt and pass-device.
- Technology limitation: max input voltage = 1.2 V .
- Overvoltage-tolerant design extends capability to 2 V (55 nm process).
- Simulations validated for single SLDO and 4-chip serial chain.



The SLDO block provides separate regulation for VDDA and VDDD.

- Separat regulation modules for VDDA and VDDD.
- Enables constant-current operation mode
  - ✓Loop 1: defines shunt regulation
  - ✓Loop 2: regulates both VDDA and VDDD outputs
- Simulations performed for single SLDO and 4 chips serial chain

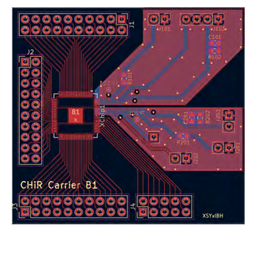




Simulations of both single and four-chip serial configurations.

PCB design and production for CHiR

- A test PCB for CHiR is designed and currently being production
- Full functional test plan prepared: SLDO output characterization, serial-chain regulation, and load transient response will be measured



Ongoing efforts & plans

The ongoing development aims to demonstrate serial powering at module level and establish a practical powering solution for future low-material-budget tracking detectors, while supporting long-term collaboration with the ATLASPix community and the development of serial powering technologies.

- ATLASPix3-based modules
  - ✓ wire-bonding of chips on the 1×4 PCB
  - ✓ full serial-powering functional tests
- CHiR-based tests:
  - ✓ Hardware, firmware and software: ongoing preparation for the module DAQ

CEPC PAIR-FLOW [B04]

IHEP | CHINESE ACADEMY OF SCIENCES

Fast Simulation of Incoherent Pair Backgrounds at the CEPC Using Conditional Flow Matching

Yanbang Tang · Haoyu Shi · Zhongjian Ma

Institute of High Energy Physics, Chinese Academy of Sciences, Beijing

135 ms/BX
A800 GPU generation

∼270,000×
vs. Guinea-Pig++ (1 CPU core)

2.8×10^{-5}
MMD on the test set

Physics-informed features: fast generation with close agreement to reference distributions.

01 Why a fast surrogate?

At $\sqrt{s} = 240$ GeV, CEPC beam–beam interactions produce ∼2,200 particles per bunch crossing (BX), with broad energy spectra and sharp forward peaks.

Bottleneck: Guinea-Pig++ takes ∼10 h/BX on one CPU core; detector studies need 10^4–10^5 BX.

Training data 5,000 BX; 10.8 million particles.
4,000 / 500 / 500 train / validation / test BX; split by BX to avoid leakage.

Processes: Breit–Wheeler 1.2%, Bethe–Heitler 18.3%, Landau–Lifshitz 80.5%.

02 Physics-informed features

Map 7 raw variables to 9 features, then standardize.

Input	Transform and purpose
Signed energy E	$\mathrm{sign}(E),\ \log_{10}\lvert E\rvert$ Compress five energy decades.
β_x, β_y	$\log_{10} p_T,\ \sin\phi,\ \cos\phi$ Separate scale and direction.
β_z	$\Phi^{-1}\left(\widehat{F}(\beta_z)\right)$ Resolve sharp peaks near ± 1.
Vertex x, y, z	Standardize each coordinate.

$\widehat{F}$: 50,000 training-data quantiles.
Φ^{-1}: standard-normal inverse CDF.

03 Process-conditional flow

Process c conditions the flow from noise u_0 to data u_1:

$$u_t = (1-t)u_0 + tu_1, \qquad t \sim \mathcal{U}(0,1)$$

$$\mathcal{L} = \mathbb{E}\left[\left\|v_\theta(u_t, t, c) - (u_1 - u_0)\right\|^2\right].$$

Network: 6×512 MLP with SiLU; 64D time and 64D process embeddings; 1.39M parameters.

Training: AdamW; 200 epochs; batch 4,096; ∼80 min on A800.

Generation: 100 midpoint ODE steps; sample joint process counts, generate particles, then invert preprocessing.

04 Speed and fidelity

Surrogate	MMD ↓	ms/BX
KDE	2.82×10^{-3}	6
Conditional FM	$\mathbf{2.8 \times 10^{-5}}$	**135**
Independent FMs	1.17×10^{-4}	219

Shared model: ∼101× lower MMD than KDE; 4.2× lower MMD and 1.6× faster than independent flows.

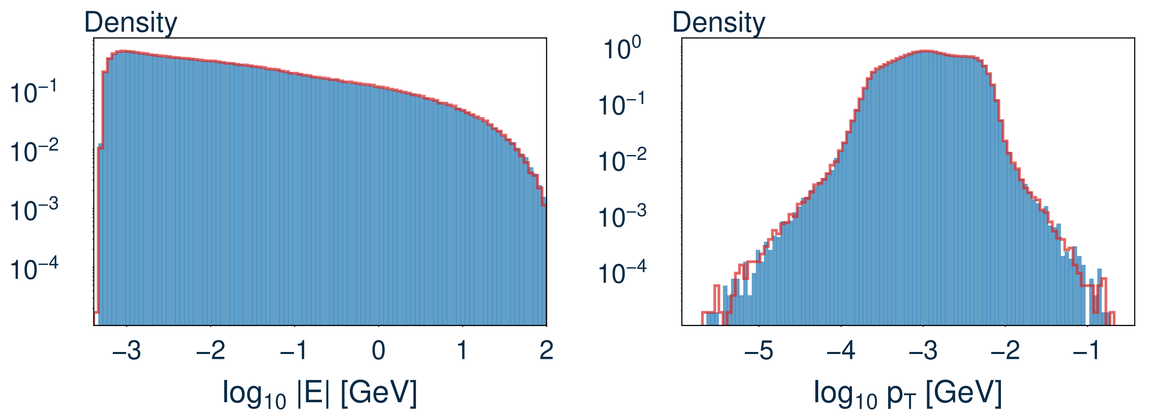
For 10^5 BX: ∼114 CPU-years of reference simulation → ∼3.75 GPU-hours.

Speedup: single-core CPU vs. A800 GPU; training excluded. FM on CPU: ∼4 s/BX.

05 Distribution fidelity

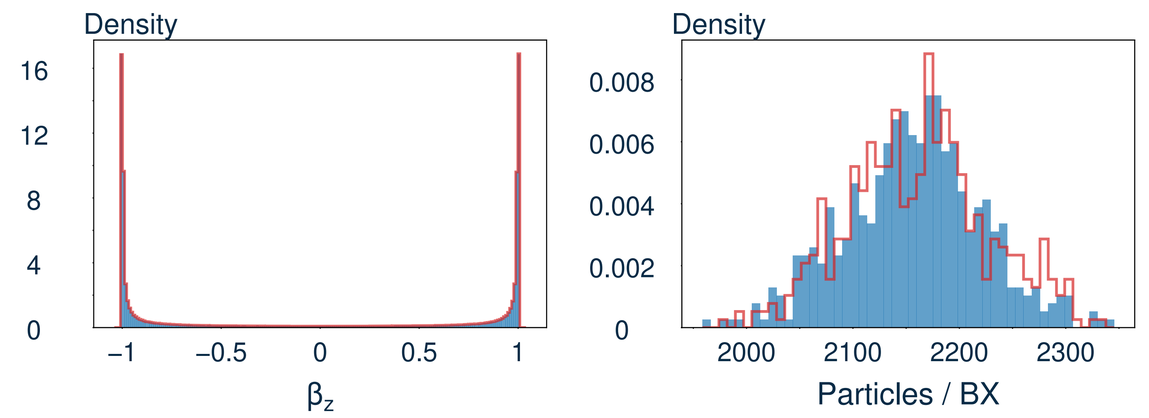
Guinea-Pig++ Conditional FM

Energy and transverse momentum



$|E|$: KS = 0.0009 p_T: KS = 0.0017

Longitudinal velocity and multiplicity



β_z: KS = 0.0132 Counts/BX: KS = 0.0500

Single-particle marginals: all nine reported KS values ≤ 0.0132; largest deviations are β_z (0.0132) and y (0.0117).

Particles/BX: reference 2156.9 ± 63.9; generated 2161.2 ± 68.2.
Multiplicity KS test: $p = 0.56$.

06 Preprocessing ablation

A 2×2 test: quantile normalization (QN) and p_T/ϕ decomposition.

KS	Full	No QN	No p_T/ϕ	Neither
β_z	0.013	0.056	0.014	0.056
p_T	0.002	0.001	0.008	0.006
θ	0.002	0.008	0.005	0.015

Both matter: QN resolves longitudinal peaks; p_T/ϕ preserves transverse structure.

07 Takeaway and next steps

Physics-informed features + one conditional flow: rapid CEPC pair-background generation with strong distribution fidelity.

Next validation targets

Beam-parameter conditioning; per-BX energy–momentum constraints; uncertainty quantification; Key4HEP / DD4hep integration.

Validated at one CEPC Higgs setting; broader beam settings and detector-level tests remain future work.

BX: bunch crossing FM: flow matching KS: Kolmogorov–Smirnov statistic MMD: maximum mean discrepancy

[B05]

A Unified Sensor-Front-End Optimization Framework for 55nm HV-MAPS

Bingchen Yan[1], Yang Zhou[1], Leyi Li[1,6], Jianpeng Deng[3], WeiGuo Lu[1], Pengxu Li[3], Xiaoxu Zhang[1,4], Xiaomin Wei[2], Mei Zhao[1], Yu Zhao[2], Zheng Wei[2], Yang Chen[5], Yujie Wang[5], Zhan Shi[5], Hongbo Zhu[3], Meng Wang[6], Jianchun Wang[1], Yiming Li[1]

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[3]Zhejiang University [4]Nanjing University, Nanjing, China [5]Dalian Minzu University, Dalian, China [6]Shandong University, Qingdao, China

Introduction

The CEPC Inner Tracker targets a timing resolution of approximately 3 ns and a power consumption below 150 mW/cm². This work presents a sensor–front-end co-optimization framework for MAPS in a domestic 55nm HV-MAPS process, where deep-well parasitic capacitance (Cw) dominates the front-end load.
A calibrated TCAD model decomposes the sensor capacitance and provides 3×3-pixel electric-field data, which is imported into Allpix² to simulate the collected charge and charge collection time. The AFE is optimized via gm/ID methodology under the extracted parameters to achieve sub-1 ns jitter with minimal power. This establishes a practical sensor-AFE co-optimization flow for CEPC ITK pixel chip development.

TCAD Capacitance Analysis

A 3 × 3 pixel array was modeled and simulated in TCAD to identify the contributions to the sensor capacitance. Capacitance decomposition shows that coupling to the P-well and deep P-well within the central pixel dominates, contributing approximately 229 fF out of a total of 262 fF (87%) .

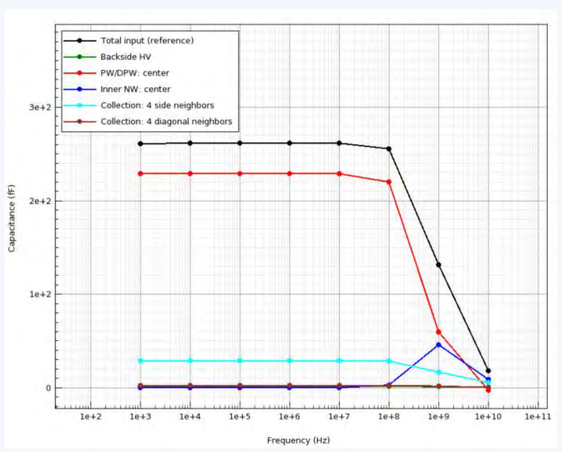


Fig. Dominant capacitance contributions.

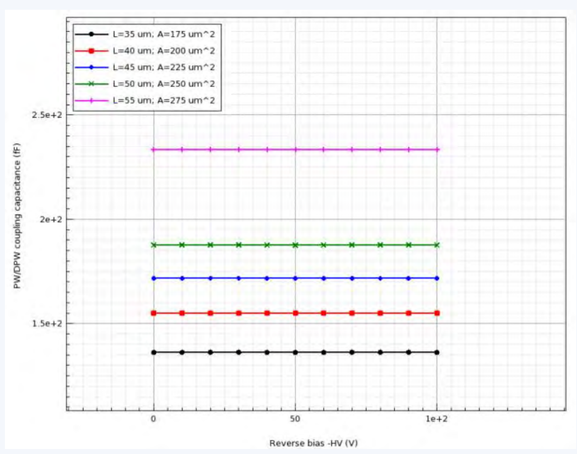


Fig. DPW area dependence.

The dependence on deep P-well area was further investigated through a geometry scan. The results clearly show that reducing the deep P-well area effectively lowers the sensor capacitance.

Allpix² Charge Collection Simulation

Signal collection was simulated in Allpix² using TCAD electric fields from a 3 × 3 pixel array, with normally incident 3 GeV protons, a −200 V bias, and a substrate resistivity of 2000 Ω·cm.

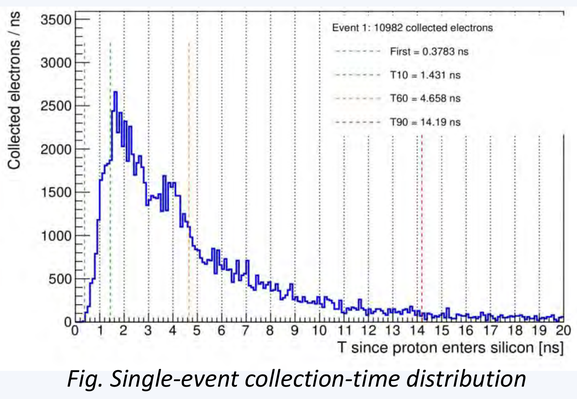


Fig. Single-event collection-time distribution

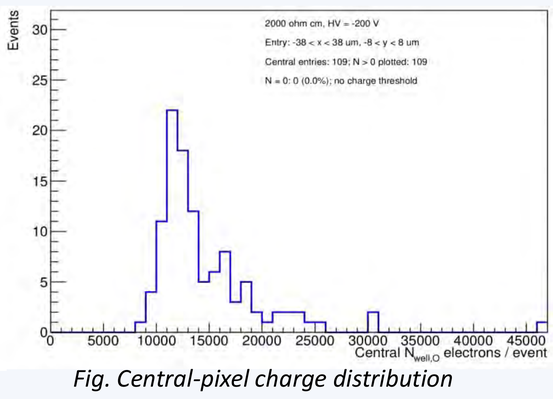


Fig. Central-pixel charge distribution

The collection-time distribution features a fast leading edge followed by a long tail. In a representative event, approximately 60% of the charge is collected within 5 ns. The collected-charge distribution for direct central-pixel hits mainly spans 8–25 ke⁻ , with a typical signal of 11–13 ke⁻ .
The rapid charge collection sets requirements on AFE bandwidth and response speed, while the collected-charge range guides the required input sensitivity and dynamic range.

From Requirements to AFE Design

$$C_{\mathrm{eq}} = C_d + \frac{C_c C_i}{C_c + C_i}$$

The Ceq, used throughout the following analysis, represents the effective capacitive load referred to the sensor collection node. Cd,Cc,Ci, and Cfb are the total sensor, coupling, amplifier input, and feedback capacitances, respectively.

1. Open-loop gain requirement

For a maximum relative gain loss $\delta_{\max}$

$$G_Q = \frac{1}{C_{\mathrm{fb}} + \frac{C_{\mathrm{eq}} + C_{\mathrm{fb}}}{A\alpha}} \qquad \delta = 1 - \frac{G_Q}{G_{Q,\mathrm{ideal}}} \le \delta_{\max} \qquad A \ge \frac{1-\delta_{\max}}{\alpha\delta_{\max}}\left(1 + \frac{C_{\mathrm{eq}}}{C_{\mathrm{fb}}}\right)$$

Larger Cd requires higher open-loop gain for the same tolerated signal loss.

2. Timing requirement and transconductance

For a single-pole response, timing jitter is approximately

$$\sigma_t \approx \frac{\mathrm{ENC}}{N_{\min}} \frac{\tau}{1-\eta}$$

With ENC = 200 e⁻ , N_{min} = 2000, and threshold fraction η = 0.5, subnanosecond jitter requires τ < 5 ns.

$$\tau \approx \frac{C_{\mathrm{eff,A}}}{\alpha\kappa g_{\mathrm{m,in}}\beta} \qquad C_{\mathrm{eff,A}} = C_{\mathrm{L,A}} + \frac{C_{\mathrm{fb}} C_{\mathrm{eq}}}{C_{\mathrm{eq}} + C_{\mathrm{fb}}} \qquad g_{\mathrm{m,in}} \gtrsim \frac{C_{\mathrm{L,A}}\left(1 + \frac{C_{\mathrm{eq}}}{C_{\mathrm{fb}}}\right) + C_{\mathrm{eq}}}{\alpha\kappa\tau_{\max}}$$

Larger C_{eq} demands higher g_m to preserve timing performance.

3. Low-noise requirement

For sufficient loop gain, the series-noise contribution and the input-transistor noise spectra are approximately given by:

$$\mathrm{ENC}_{\mathrm{series}} \approx \frac{C_{\mathrm{noise}}}{q} e_{\mathrm{n,rms}} \qquad C_{\mathrm{noise}} = \left(C_{\mathrm{d}} + C_{\mathrm{fb}}\right)\left(1 + \frac{C_{\mathrm{i}}}{C_{\mathrm{c}}}\right) + C_{\mathrm{i}} \qquad S_{\mathrm{v,th}} \approx \frac{4kT\gamma}{g_{\mathrm{m}}} \qquad S_{\mathrm{v,1/f}} \approx \frac{K_{\mathrm{eff}}}{WLf}$$

4. Power constraint

$$g_m \approx \sqrt{2\mu C_{\mathrm{ox}} \frac{W}{L} I_D}, \qquad I_D = \frac{g_m}{g_m/I_D}, \qquad P_{\mathrm{AFE}} \approx V_{\mathrm{DD}} \sum I_D.$$

Improving timing performance and reducing noise often require higher power consumption. Reducing Cd simultaneously relaxes gain, speed, and noise constraints, making capacitance reduction a key route to power-efficient sensor–AFE co-optimization.

AFE Simulation Results

Simulations are performed with a 200 fF input sensor capacitance, covering 2k–20k electrons.

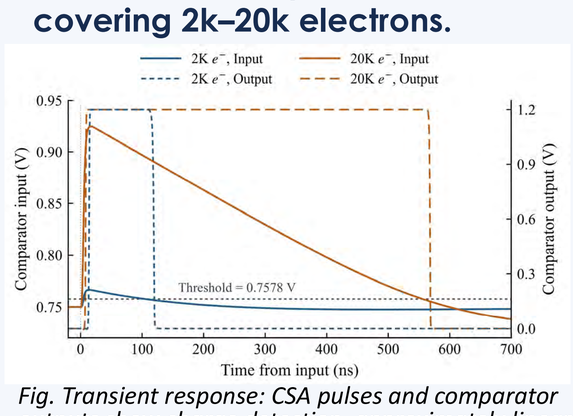


Fig. Transient response: CSA pulses and comparator outputs show charge detection, approximately linear discharge, and no saturation at 20k electrons.

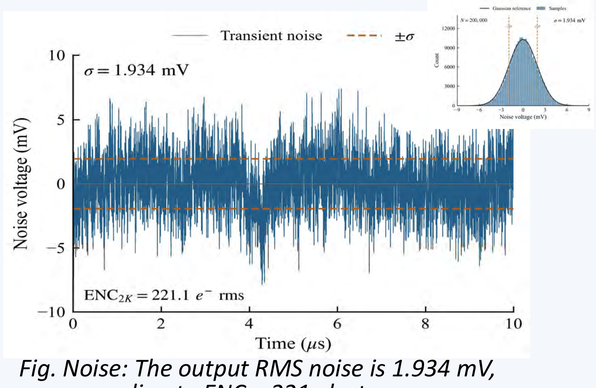


Fig. Noise: The output RMS noise is 1.934 mV, corresponding to ENC ≈ 221 electrons.

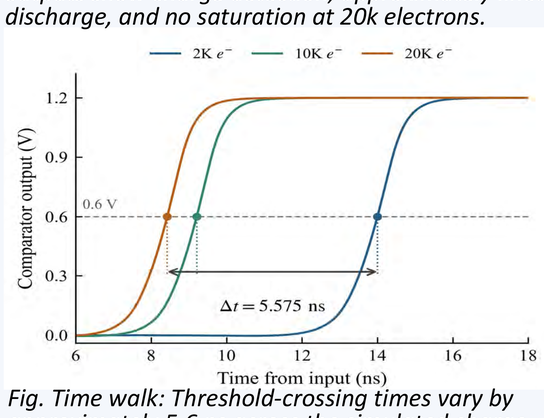


Fig. Time walk: Threshold-crossing times vary by approximately 5.6 ns across the simulated charge range.

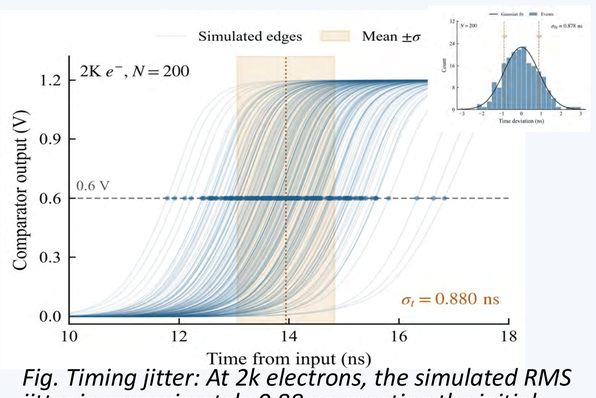


Fig. Timing jitter: At 2k electrons, the simulated RMS jitter is approximately 0.88 ns, meeting the initial subnanosecond target.

Summary & outlook

This work establishes a sensor–AFE co-design flow linking TCAD, Allpix², and analog front-end simulations. With sensor capacitance as the key design variable, the analysis identifies its dominant contributions (DPW) and evaluates its influence on AFE gain, response speed, and noise.
The work also defines a systematic path from experimental requirements to circuit performance targets and transistor sizing, providing a methodological foundation for further parameter optimization and design iterations.

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[B06]

Quantum Entanglement in Top–Antitop Pairs at Electron–Positron Colliders Across Energy Scales

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1. Introduction

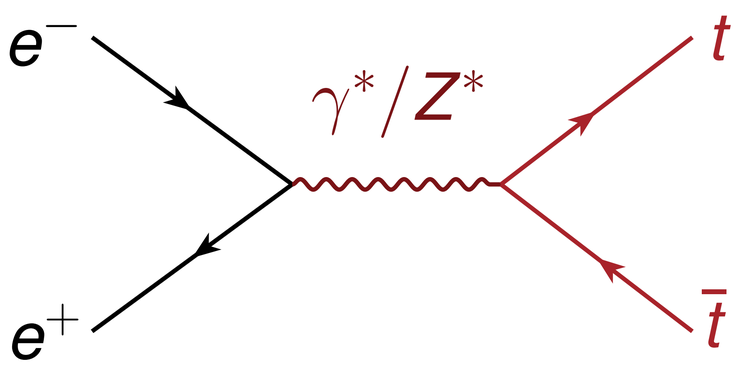
Quantum information at colliders. Entanglement is usually tested with photons and atoms. Colliders allow such tests at the TeV scale [1].

Top quarks as qubits. The top quark is so heavy that it decays before its spin is randomized, so a $t\bar{t}$ pair is a **two-qubit system**. Its entanglement was proposed for the LHC [2] and **observed in 2024** [3, 4].

Lepton colliders. In $e^+e^- \to t\bar{t}$ the collision energy is precisely known and the spin structure is well studied [5, 6]. New tools give the spin state of every event [7].

This work. Analytic LO results exist [6]. Here we validate the per-event Density Mode [7] against them and follow the **position** and **height** of the entanglement peak from 350 GeV to 3 TeV.

2. The process



The pair is produced through a photon or a Z boson (leading order, unpolarized beams). θ is the angle between the top quark and the electron beam.

3. Quantum-information observables

The spin state of the pair is a 4×4 density matrix ρ.

Concurrence [8] — degree of entanglement (0 = none, 1 = maximal):

$$C = \max\bigl(0,\ \lambda_1 - \lambda_2 - \lambda_3 - \lambda_4\bigr)$$

$\lambda_1 \geq \cdots \geq \lambda_4$: square roots of eigenvalues of $\rho(\sigma_y \otimes \sigma_y)\rho^*(\sigma_y \otimes \sigma_y)$.

Purity — how mixed the state is (1 = pure state):

$$P = \mathrm{Tr}\,\rho^2$$

Negativity [9] — based on the partial transpose:

$$N = \tfrac{1}{2}\bigl(\|\rho^{T_B}\|_1 - 1\bigr)$$

4. Method

1. Simulated $e^+e^- \to t\bar{t}$ with the **Density Mode of MadGraph5_aMC@NLO** [7], which gives the spin density matrix of every event.
2. 9 energies (350, 365, 500, 700, 1000, 1500, 2000, 2500, 3000 GeV), 10 000 events each.
3. A Python pipeline computes C, P, N and $\cos\theta$ for every event, and finds the **peak position** and **peak height** of C.
4. All results agree with an independent analytic calculation to better than 10^{-4}.

5. Results: entanglement vs. angle

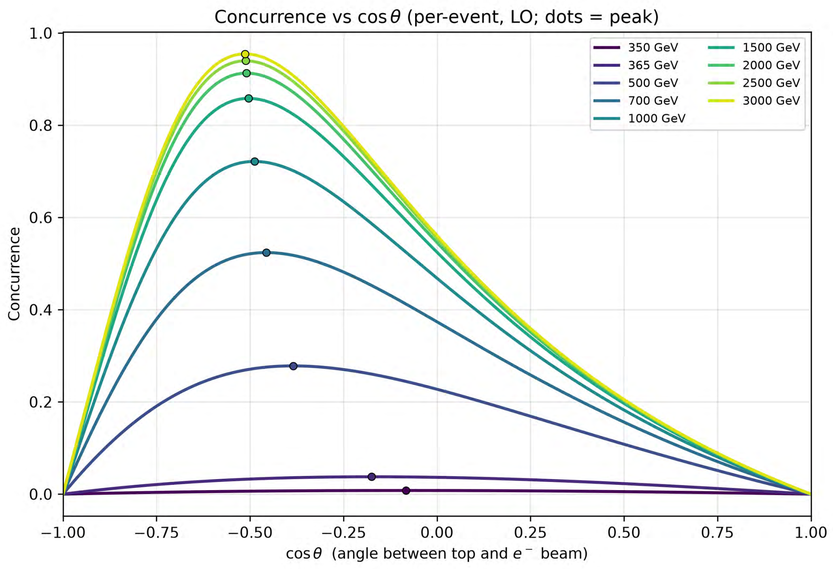


Fig. 1. Concurrence vs. $\cos\theta$ (dots: peaks).

- **350 GeV:** almost no entanglement ($C_{\max} \approx 0.008$).
- **3 TeV:** strong entanglement ($C_{\max} = 0.955$).
- Maximum at $\theta \approx 120°$ ($\cos\theta \approx -0.5$), not 90°: the Z couples differently to left- and right-handed particles [6].

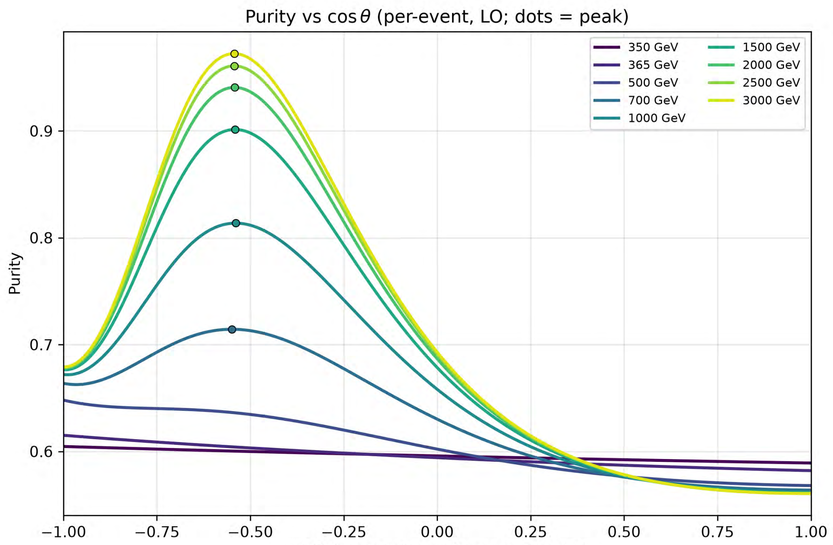


Fig. 2. Purity vs. $\cos\theta$.

- High energy: purity peaks at nearly the same angle and approaches 1.

References

[1] A. J. Barr *et al.*, Prog. Part. Nucl. Phys. 139, 104134 (2024).
[2] Y. Afik, J. R. M. de Nova, EPJ Plus 136, 907 (2021).
[3] ATLAS Collab., Nature 633, 542 (2024).
[4] CMS Collab., Rep. Prog. Phys. 87, 117801 (2024).
[5] S. Parke, Y. Shadmi, PLB 387, 199 (1996).
[6] F. Maltoni *et al.*, JHEP 09 (2024) 001.
[7] V. Durupt *et al.*, JHEP 04 (2026) 103.
[8] W. K. Wootters, PRL 80, 2245 (1998).
[9] G. Vidal, R. F. Werner, PRA 65, 032314 (2002).
[10] CEPC Study Group, CEPC input to the European Strategy for Particle Physics Update 2026 (2025).
[11] Y. Afik *et al.*, arXiv:2504.00086 (2025).

6. Results: peak position and height

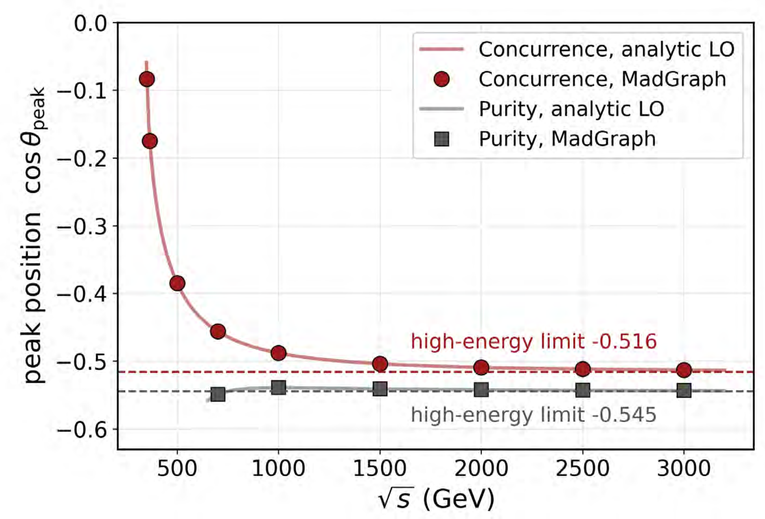


Fig. 3. Peak angle vs. energy (points: simulation, lines: analytic). At 350 GeV $C \approx 0$, so the peak angle is poorly defined.

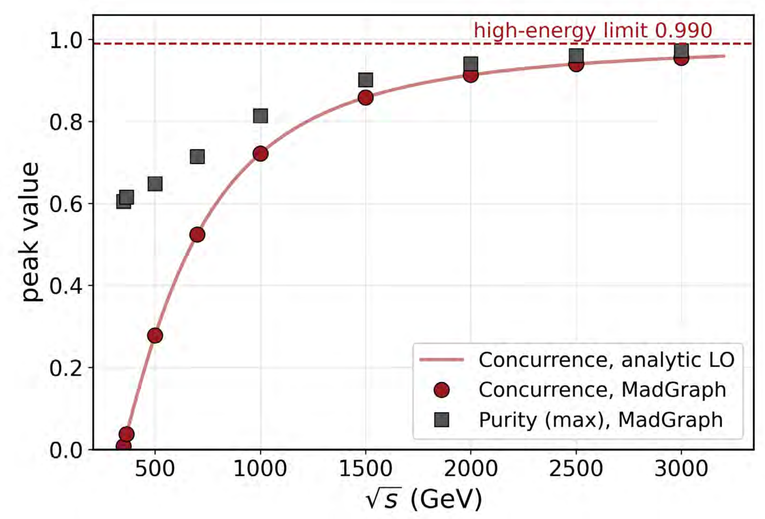


Fig. 4. Maximum concurrence (and purity) vs. energy.

$\sqrt{s}$ [GeV]	350	500	1000	1500	2000	3000
$\cos\theta_{\mathrm{peak}}$	−0.08	−0.38	−0.49	−0.50	−0.51	−0.51
$C_{\max}$	0.01	0.28	0.72	0.86	0.91	0.95

Main result

The best **angle** is already set by ∼1 TeV, but the **amount** of entanglement keeps growing up to 3 TeV.

7. What this means for CEPC

CEPC will produce top pairs at about 360 GeV, just above threshold [10]. The tops are almost at rest, so the entanglement is **small** ($C_{\max} \approx 0.04$ at 365 GeV); $C > 0.7$ needs about 1 TeV. CEPC can still measure the full spin state precisely [11]. All values: LO, parton level.

8. Conclusion and outlook

- Near threshold: almost separable ($C_{\max} \lesssim 0.04$). High energy: strong entanglement.
- Best angle ($\theta \approx 120°$) settles early; the amount keeps growing.
- **Next:** polarized beams, Bell tests, and higher-order effects.

I would like to thank Prof. Mehmet Burcin Unlu for his support, and Ozyegin University for the opportunity to carry out this project within the Summer Research Internship 2026.

[B08]

First beam test results of COFFEE3, an HV-CMOS Pixel Prototype for the CEPC Inner Tracker

Yuman Cai[1], Jianpeng Deng[2], Leyi Li[1,4], Pengxu Li[2], Qinze Li[1], Yiming Li[1], Kang Liu[1], Weiguo Lu[1], Boxin Wang[1], Congcong Wang[1], Jianchun Wang[1], Xiaomin Wei[3], Zhiyu Xiang[6], Zijun Xu[1], Yuan Yuan[1], Xiaoxu Zhang[1,5], Mei Zhao[1], Yang Zhou[1], Hongbo Zhu[2]

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[3]Northwestern Polytechnical University, Xi'an 710129, China [4]Shandong University, Qingdao, Shandong 266237, China
[5]Nanjing University, Nanjing 210093, China [6]Central South University, Changsha 410083 China

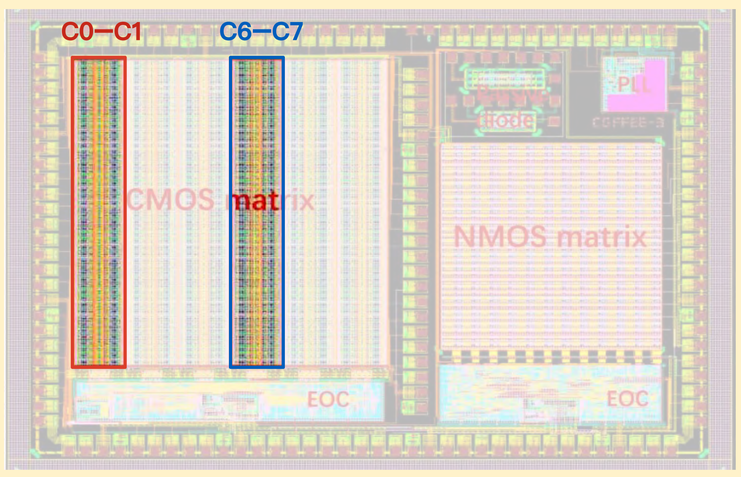
CMOS SENSOR IN FIFTY-FIVE NM PROCESS

Introduction

COFFEE3 is a 55 nm HV-CMOS pixel sensor prototype developed for the CEPC inner tracker. Following laboratory characterization, two beam-test campaigns were carried out at the CERN SPS in May and July 2026. This poster presents particle response in two double-columns, timing and timewalk measurements on a test pixel, and tracking with a silicon-strip beam monitor. Laboratory threshold tuning and high-threshold hit bursts motivate further calibration and design studies.

COFFEE3 Chip Design

- Chip size: 4000 × 3000 μm²
- CMOS array: 48 rows × 12 columns
- Pixel pitch: 36 × 130.5 μm²
- Tested double-columns: C0–C1 and C6–C7
- Two CSA variants and 4-bit pixel TDACs
- In-pixel timing and peripheral readout

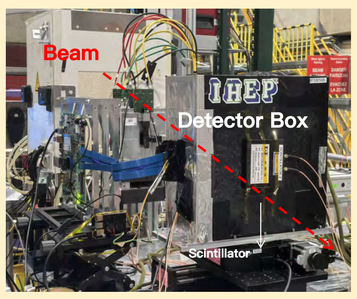


COFFEE3 chip layout

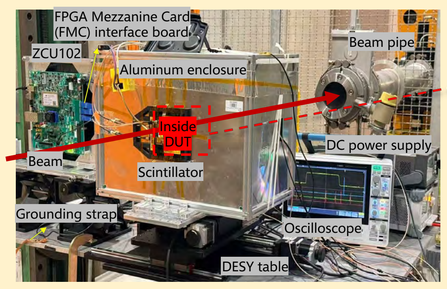
Beam-Test Setup

- May 2026: SPS H6, 200 GeV hadrons
- Tracking references: 6-layer silicon-strip beam monitor
- Trigger: two scintillators in coincidence with COFFEE3

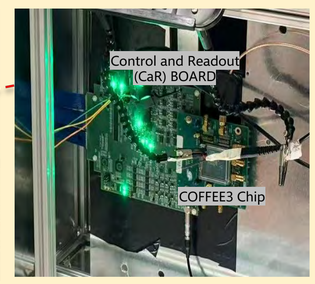
- July 2026: SPS H8, 180 GeV hadrons
- Timing references: three scintillators
- Beam intensity: ~2 × 10⁶ particles/spill



May: tracking setup



July: beam-test setup

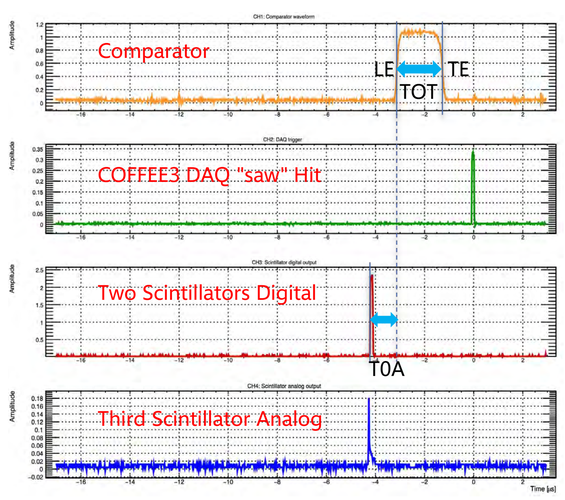


DUT and CaR board

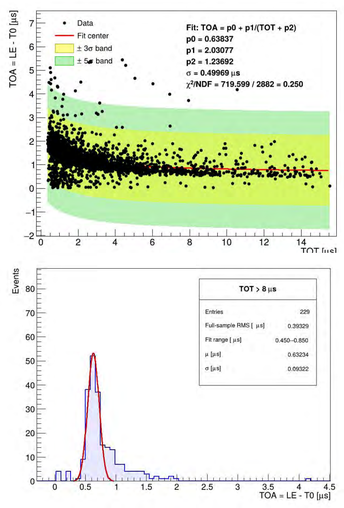
Test Results

1 Single-pixel timing and timewalk

Timing measurements are performed on a test pixel: TOA = LE − T0 and TOT = TE − LE. For TOT > 8 μs, the fitted TOA core has σ ≈ 93 ns. Measured times include test-system delays and do not represent intrinsic chip timing.



Beam-test waveforms and timing definitions

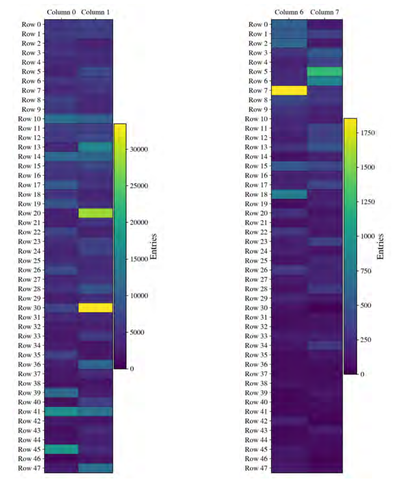


Test-pixel timing

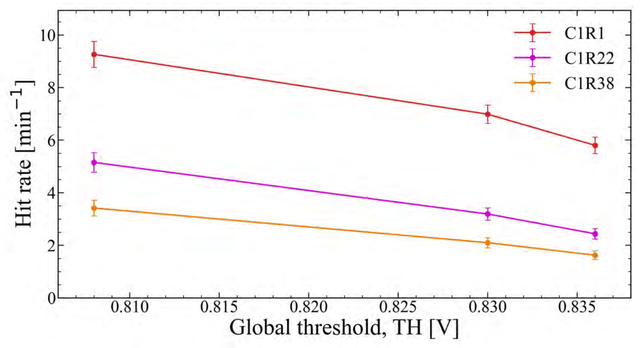
2 Multi-pixel response and threshold scan

All 192 pixels in the two tested double-columns, C0–C1 and C6–C7, respond to particle hits. For representative pixels, the particle-hit rate decreases as the global threshold increases.

C0–C1 C6–C7



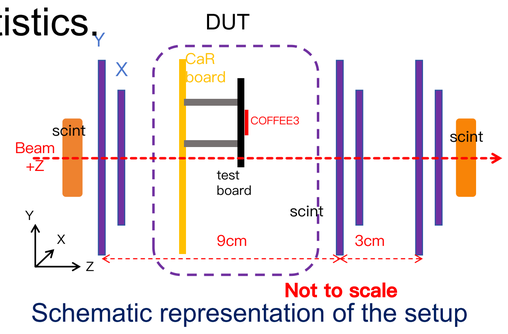
Beam-test hit maps
96 pixels per double-column



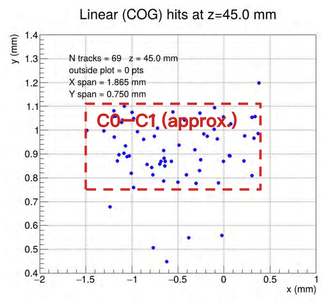
Particle-hit rate versus global threshold
Three representative pixels

3 Tracking with the silicon-strip monitor

Tracking confirms the expected pixel geometry: X pitch = 36.5 ± 0.8 μm (design: 36 μm); Y separation is consistent with the 130.5 μm design pitch. Further study on spatial resolution is limited by statistics.



Schematic representation of the setup

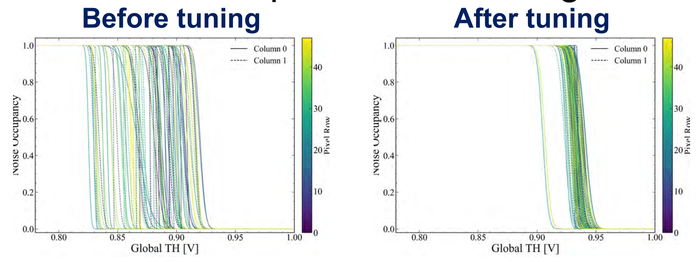


Projected track positions

4 Future study for COFFEE3

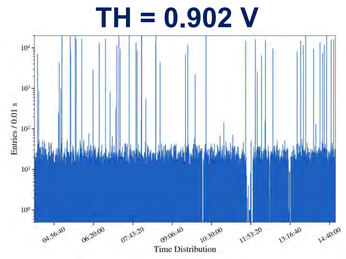
Laboratory TDAC tuning on the first double-column (96 pixels) reduces the S-curve spread from ~0.10 V to ~0.02 V. Next: tune before beam tests, investigate high-threshold hit bursts and use the results to improve future designs.

Before tuning After tuning



Laboratory TDAC tuning on the first double-column

TH = 0.902 V



High-threshold hit bursts

Summary & Outlook

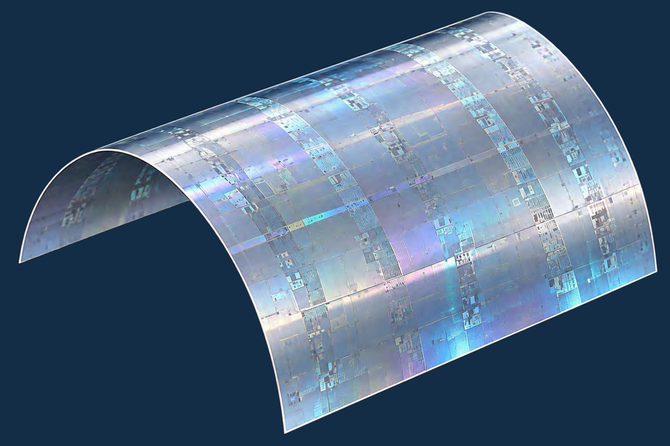
COFFEE3 demonstrates particle response and array readout in all 192 tested pixels. Test-pixel measurements show timewalk and a ~93 ns TOA core width for TOT > 8 μs, including test-system contributions. Laboratory TDAC tuning improves threshold uniformity in the first double-column, reducing the S-curve spread from ~0.10 V to ~0.02 V. Track projections agree with the pixel geometry. Further work will investigate high-threshold hit bursts and quantify efficiency and intrinsic timing performance.

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[B09]

Simulation and Beam-Test Studies of TaichuPix

for the CEPC Vertex Detector



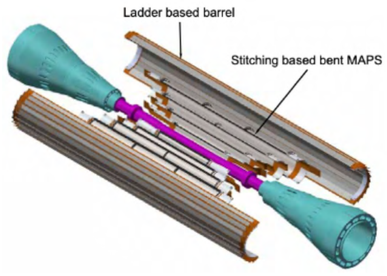
Hancen Lu, Zhijun Liang, Ying Zhang
Institute of High Energy Physics, Chinese Academy of Sciences

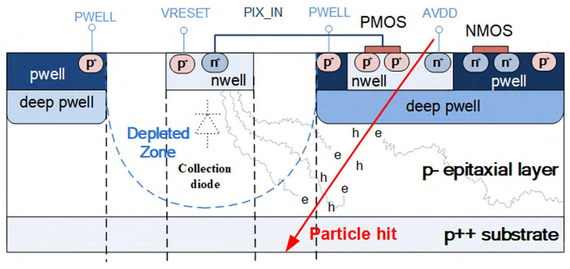
CEPC Vertex Detector R&D

CEPC vertex detector and TaichuPix

01

Precision vertexing at CEPC supports flavour tagging and heavy-flavour physics. Large incidence angles enhance charge sharing among neighbouring pixels.
TaichuPix-3 is a monolithic active pixel sensor in a 180 nm CMOS imaging process. [3]





25 µm pitch 1024 × 512 pixels
DESY test, 150 µm chip: resolution <5 µm, efficiency >99.5%. [3]

Illustrative vertex concept [4]. TaichuPix cross-section, not to scale. [3]

Simulation and digitization

02

Allpix² combines Geant4 energy deposition with electron/hole drift and diffusion in imported 3D fields. Endpoint charges feed threshold digitization and eight-connected clustering. Shockley–Ramo signal diagnostics remain a separate validation step. [1,2]

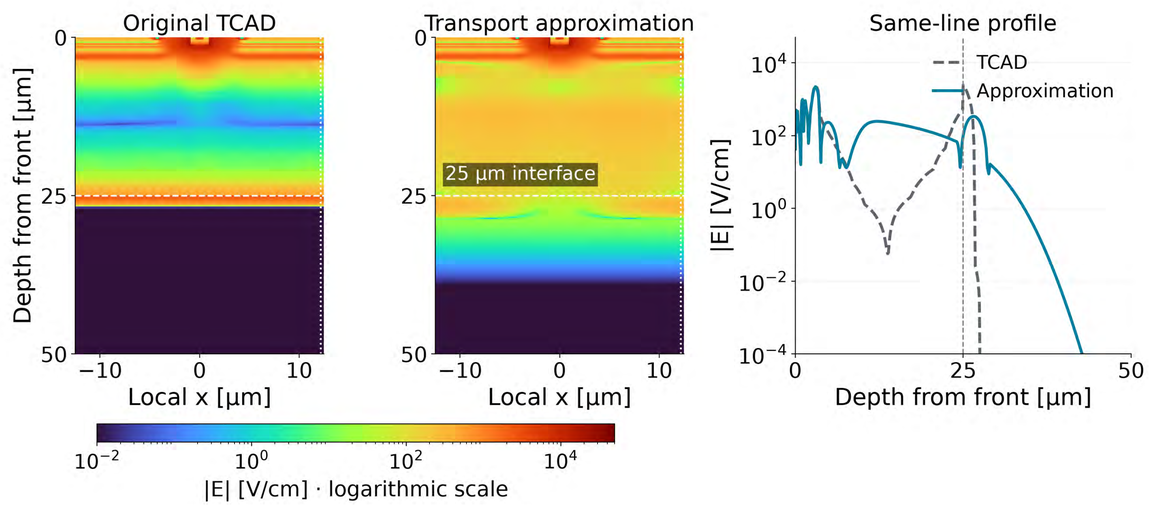
Current endpoint study	Fixed configuration
Beam / angles	2.5 GeV e⁻; 0°, 60°, 65°, 70°, 80°
Statistics / silicon	1000 per angle; 25 + 25 µm
Node / P-well / temperature	+1 / 0 V; 293 K
Packet / step / integration	50 e / 1 ps / 3 µs
Threshold / spread / noise	368 / 50 / 20 e; no reflection

Angles are measured from the sensor normal. Full 50 µm silicon includes 25 µm of epitaxial silicon and 25 µm of substrate.

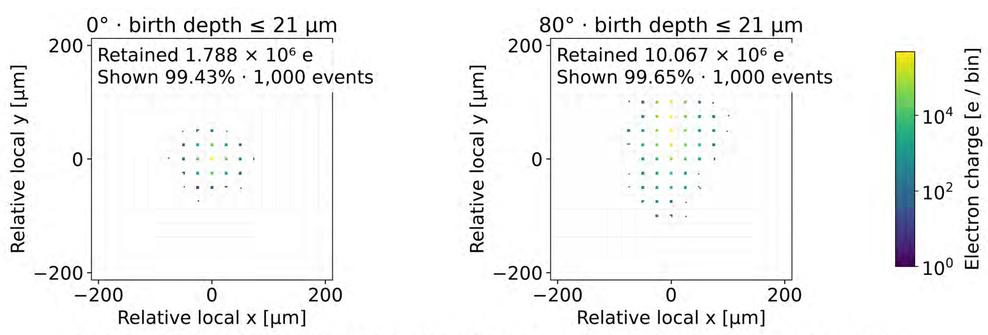
TCAD baseline and approximate field

03

The n10 TCAD baseline has a sharp field feature at the 25 µm epitaxial/substrate interface. The approximation combines a screened surface field, a smooth concentration-gradient potential (L = 5 µm sensitivity case) and weak focusing.
A = 0.10 V and D = 24 µm were **selected using 0° BSRF** cluster-size and width distributions. The scan penalized an endpoint electron fraction outside 30–40% and any-hit probability below 99%. The selected field gave 55.9% before depth selection in the 100-event selection sample. Independent calibration remains pending.



Section y = −0.2348 µm, profile x = 12.153 µm; depth = −TCAD Z. Dashed line: 25 µm interface. This approximation changes interface and bulk response. A self-consistent process/device solution remains pending.



Allpix transport before electronics threshold; 2.5 µm square bins; fixed original event centroid.
21 µm is a birth-depth selection, not a depletion depth. Response uses no new field or trajectories.

Selected endpoint electrons (birth depth ≤21 µm), weighted by collected charge. The empirical depth selection adds no new trajectories or field changes.

[1] S. Spannagel et al., NIM A 901 (2018) 164. [2] S. Agostinelli et al., NIM A 506 (2003) 250.
[3] T. Wu et al., NIM A 1059 (2024) 168945. [4] H. Lu et al., arXiv:2503.05415 (2025).

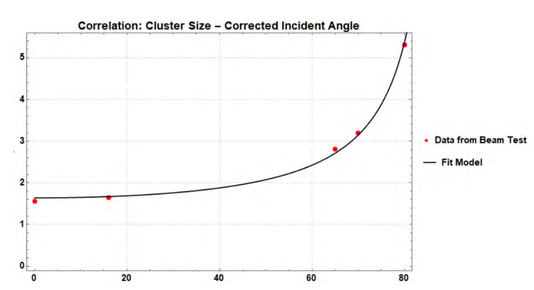
Earlier beam-test parameterization

04

Previous beam-test measurements suggest an empirical parameterization of mean cluster size versus incidence angle. [4]

$$\langle C \rangle(\theta) = a \sec\theta + b$$

a = 0.783 ± 0.022 b = 0.856 ± 0.069
Historical fit: $R^2 = 0.9995$



Historical beam-test fit, not a validation of the present simulation. Its corrected-angle convention does not calibrate the current beam angles.

BSRF beam test and simulation

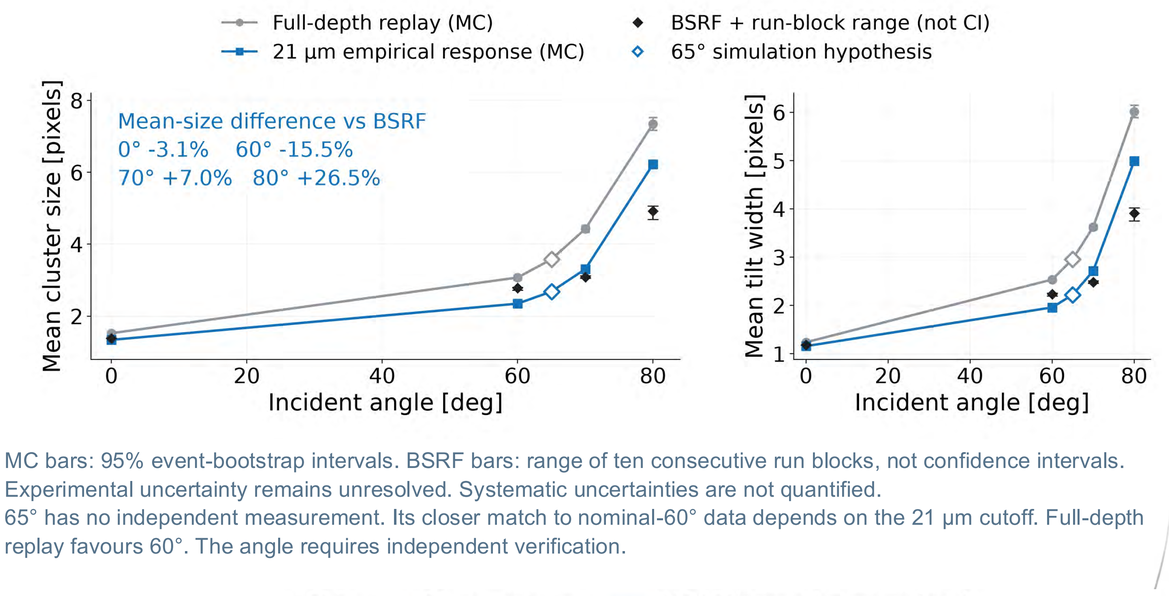
05

BSRF: ITHR32, nominal 0°, 60°, 70° and 80°, provisional DUT plane 2. Allpix²: 2.5 GeV electrons, 1000 events at each of 0°, 60°, 65°, 70° and 80°, with fixed field and readout.

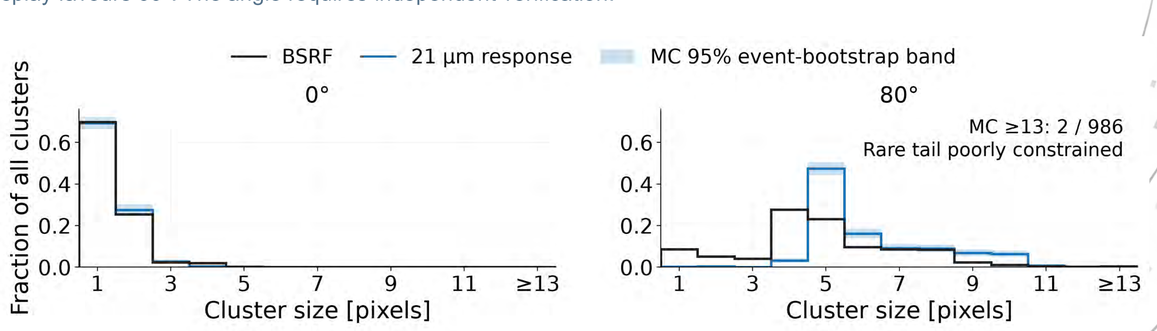
The 18/21/24 µm scan reused 0°/80° samples. The 21 µm choice balanced a 30–40% electron-fraction target with hit retention and BSRF comparisons. This empirical, model-dependent choice is **not an independent prediction**.
After transport, it selects collected electrons born within 21 µm of the front. Original hole contributions stay unchanged. The **effective collected-electron fraction** divides selected electrode-endpoint electrons by all electrons generated in the full 50 µm silicon. The cutoff is not a measured depletion depth and differs from the 25 µm epitaxial thickness and D = 24 µm focusing depth.

Angle	Effective e⁻ fraction	Seed med. [e]	⟨C⟩ sim.	⟨C⟩ BSRF
0°	38.33%	1048	1.342	1.385
60°	39.34%	1677	2.349	2.781
65°	38.38%	1767	2.686	N/A
70°	39.04%	1887	3.309	3.092
80°	39.19%	2377	6.225	4.921

Eight-connected components are formed per generated event in simulation and within each stored cluster ID in data. Means include all non-empty components. Zero-hit events contribute none. Event selections are not matched.



MC bars: 95% event-bootstrap intervals. BSRF bars: range of ten consecutive run blocks, not confidence intervals. Experimental uncertainty remains unresolved. Systematic uncertainties are not quantified.
65° has no independent measurement. Its closer match to nominal-60° data depends on the 21 µm cutoff. Full-depth replay favours 60°. The angle requires independent verification.



Conclusions and outlook

06

Mean cluster size differs from BSRF by −3.1% (0°), −15.5% (60°), +7.0% (70°) and +26.5% (80°). These data-informed comparisons remain model dependent.
At 80°, the two 500-event halves give means of 6.34 and 6.11. Only two clusters have ≥13 pixels, so rare tails remain poorly constrained.
Next steps: self-consistent TCAD with dopant diffusion, matched event selections, independent depth-response constraints and Ramo/front-end validation.

The collected-electron fraction is distinct from a Ramo signal efficiency.

[B10]

Heating film design and temperature-sensing methods for VTX thermal mockups

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Institute of High Energy Physics, Chinese Academy of Sciences

Abstract

We have developed resistive heating films to simulate the heat loads generated by pixel sensors and readout electronics in the vertex detector. Two designs have been fabricated for thermal mockups of the first and fourth detector layers. The films consist of high-resistivity heating elements encapsulated in polyimide and operate at low supply voltages. Dedicated flexible printed circuit (FPC) boards attached to the films carry PT100 platinum thin-film resistance temperature detectors (RTDs). Adapter boards connect the sensing channels to data-acquisition modules. We present the experimental setup and preliminary air-cooling results for two assembly configurations. In parallel, we are developing silicon dummy chips as an alternative for thermal studies.

Heating film design

We designed two heating films for the first and fourth vertex-detector layers. The first-layer sensor module (Figure 1) routes all power connections, I/O signals and services through the Left-end Readout Block (LRB), forming a localized high-heat region. The first-layer film therefore contains high- and low-heat regions (Figure 2a). The fourth-layer film comprises two independently powered sections, each with a high-heat region at one end (Figure 2b).

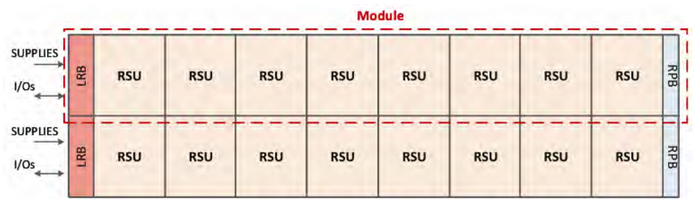
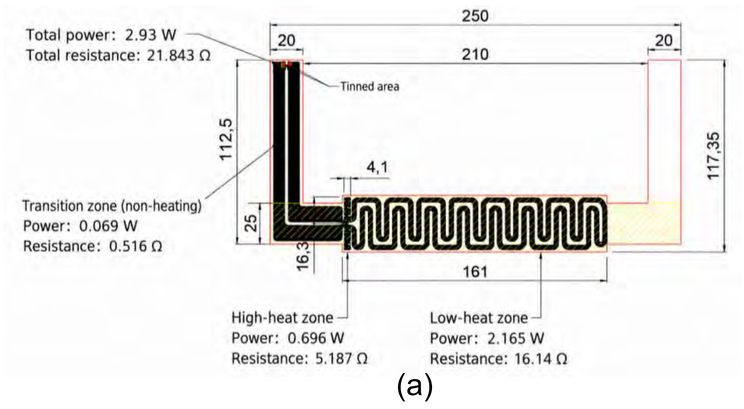
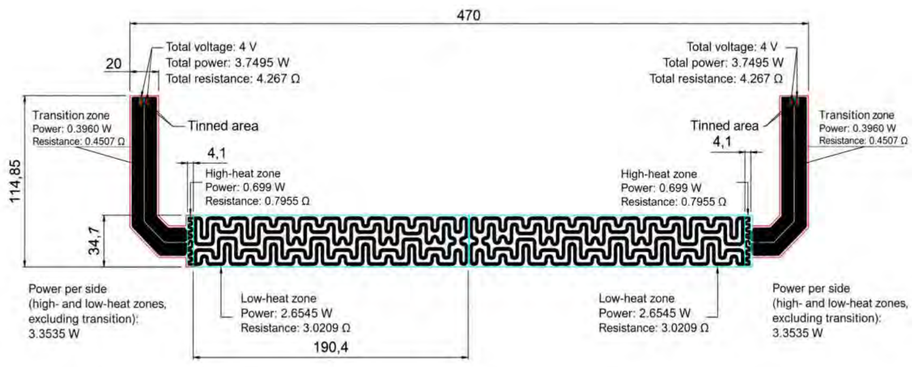


Figure 1. Sensor module for the first vertex-detector layer



(a)



(b)

Figure 2. First- and fourth-layer heating film layouts

FPC sensor board design

We designed two FPC boards using Vishay PTS060301B100RP100 platinum RTDs. Their Class F0.3 tolerance is ±(0.3 + 0.005|T|) °C, where T is the temperature in °C.

The first-layer board has 11 sensing points (Figure 3a) for temperature profiling with airflow from the left. Three-wire connections use two traces on one RTD terminal and one on the other to reduce lead-resistance errors. Signals pass through 24-pin FPC connectors. Polyimide stiffens both FPC tails, and stainless steel reinforces the connector regions. The fourth-layer board has 18 sensing points (Figure 3b), with nonuniform spacing based on simulation results.

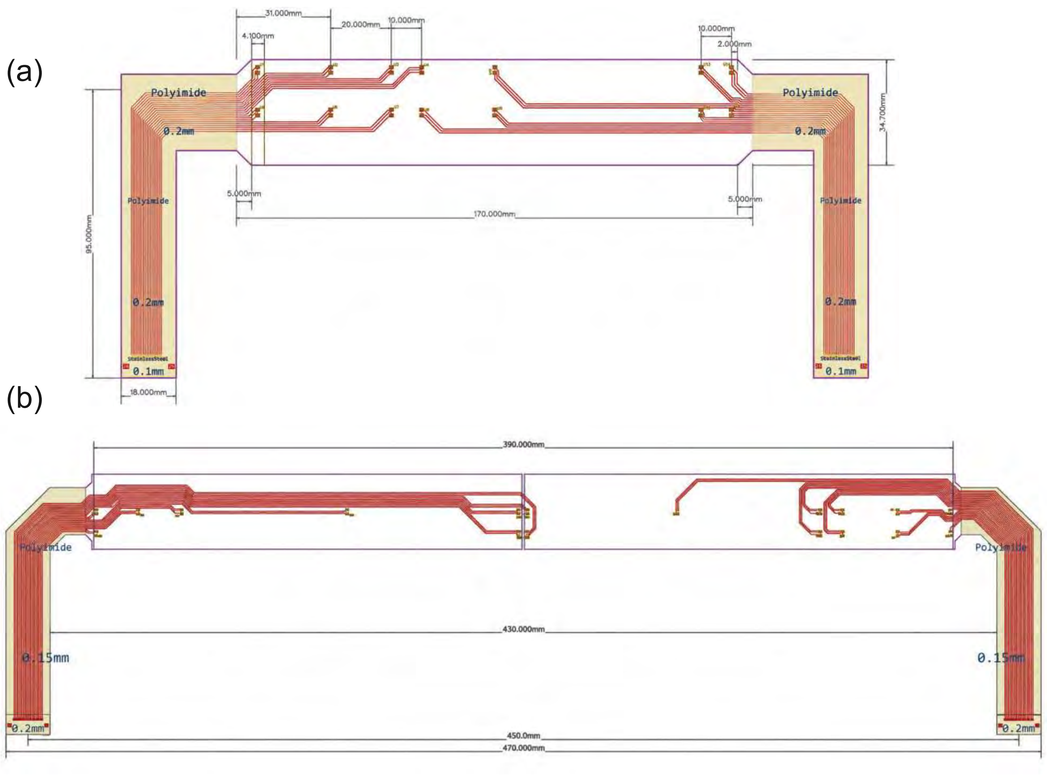
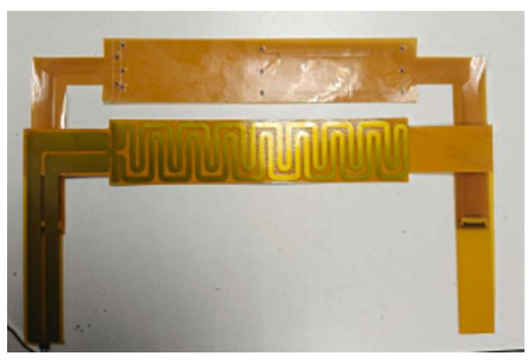


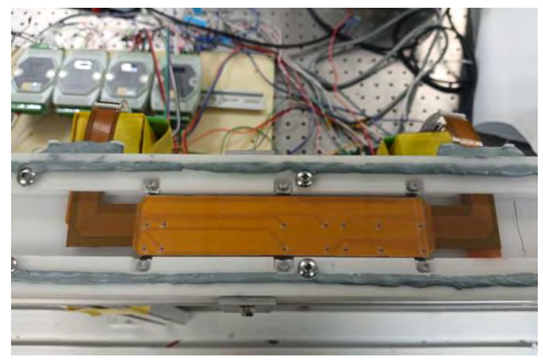
Figure 3. First- and fourth-layer FPC layouts

Air-cooling test

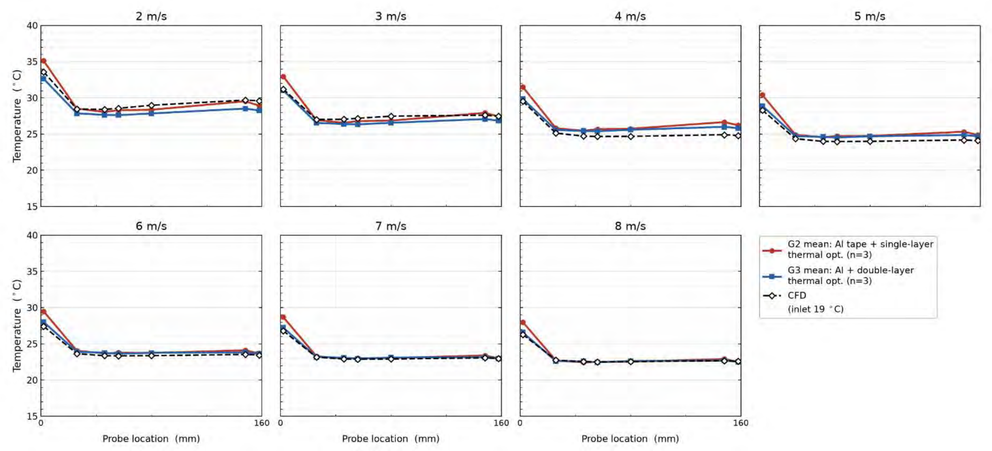
We conducted preliminary air-cooling tests with the first-layer heating film and FPC sensor board (Figure 4). After assembling the heater using aluminium and adhesive layers, we installed it in a thermal mockup. We compared two configurations: aluminium tape with 3M 9448A double-sided tape, and aluminium with two layers of 3M 8805 thermally conductive tape. We tested both configurations at different air velocities and compared the measured temperature profiles with computational fluid dynamics (CFD) simulations.



(a)



(b)



(c)

Figure 4. Air-cooling test setup and test results

Silicon dummy chip design

We are developing two silicon dummy chips, A and B (Figure 5), each measuring 34.7 mm × 80 mm, to better reproduce the thermal behavior of actual sensors. Both designs use serpentine aluminium heaters with a nominal thickness of 2 μm. Each chip contains four independently powered low-heat sections, each with two parallel branches. At 12 V, these sections provide a nominal average power density of 40 mW/cm². Chip A also includes a separately powered, 4.1 mm-long high-heat region designed to dissipate 696 mW at 9.3 V. Chip B provides low-heat coverage across its full area.

Table 1 summarizes the trace geometry and nominal current densities.

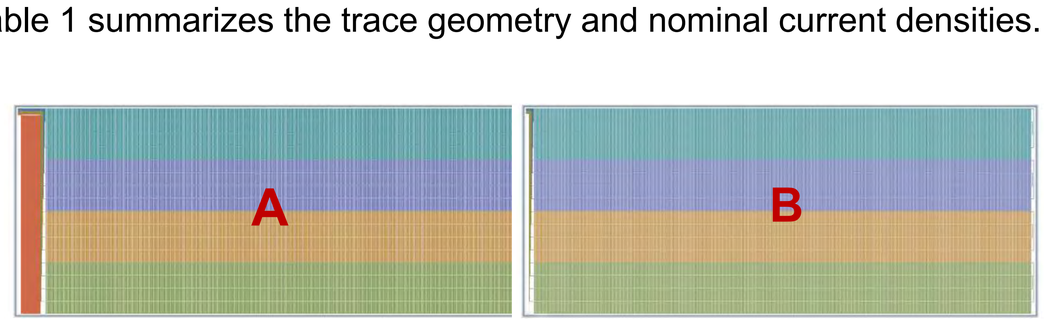


Figure 5. Silicon dummy chips A and B

Parameter	High-heat region	Chip A low-heat	Chip B low-heat
Trace width, w (μm)	97.28	40	40
Clear spacing (μm)	11.42	53.734	63.074
Cross-sectional current density, J (kA/cm²)	38.47	13.72	14.46
Linear current density, K (mA/μm)	0.7693	0.2743	0.2892

Table 1. Trace geometry and nominal current densities

[B11]

A Compact Silicon Microstrip Tracking System

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Institute of High Energy Physics, Chinese Academy of Sciences, Beijing, China

Abstract

Silicon microstrip detectors offer high spatial resolution and scalable architectures, making them attractive for charged-particle tracking, beam monitoring, and detector prototyping. We present the development and initial characterization of a compact p-on-n silicon microstrip detector system. A module comprises a 192-channel sensor with a sensitive area of approximately 26 mm × 40 mm, three 64-channel IDE1140 front-end ASICs, dedicated bias and control electronics, and FPGA-based data acquisition using a Xilinx ZCU102. The current single-module prototype supports front-end configuration, calibration, programmable sampling delay, and internal or external triggering. At a bias voltage of 50 V, the typical common-mode-reduced channel noise is approximately 3.5 ADC counts, and cosmic-ray measurements show clear particle-induced clusters.

System Architecture

The readout system integrates a silicon microstrip sensor, a dedicated front-end board (FEB), and a Xilinx ZCU102-based DAQ platform. The FEB provides sensor biasing, leakage-current monitoring, and analog signal digitization. The ZCU102 implements front-end control, trigger handling, and data acquisition.

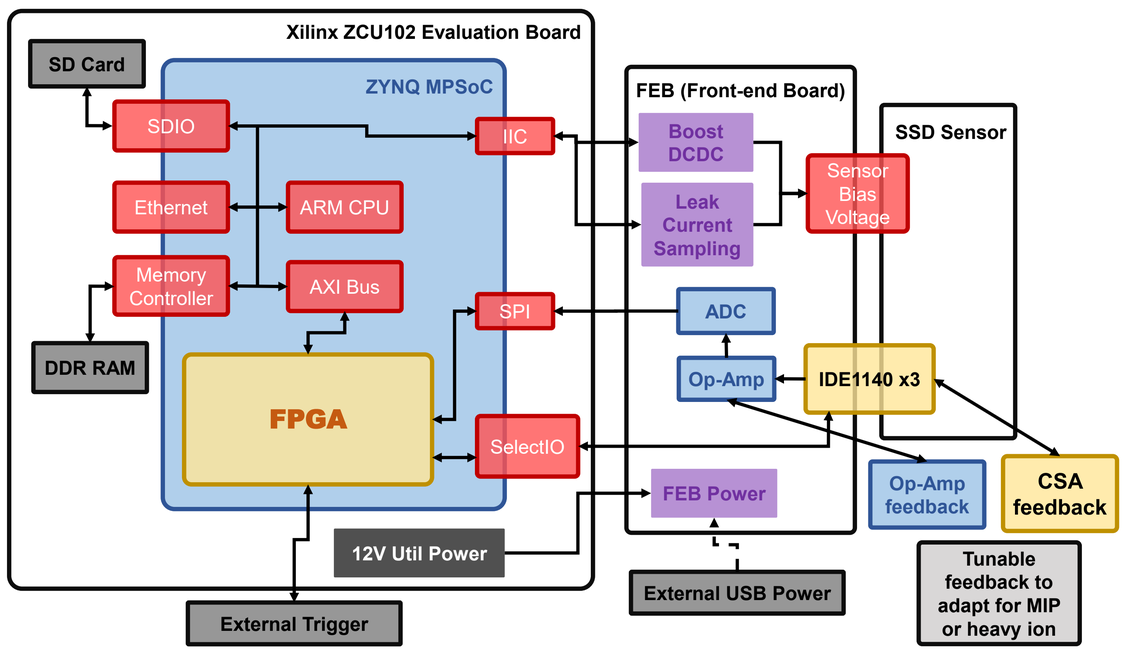


Figure 1. Architecture of the single-module readout system, showing the ZCU102 DAQ platform, front-end electronics, sensor interfaces, and power and trigger connections.

Detector Module and Front-End Electronics

The detector module integrates a 192-channel p-on-n silicon microstrip sensor (AMS L0 baby sensor) with an active area of about 26×40 mm² and three 64-channel IDE1140 front-end ASICs. The front-end electronics provide signal conditioning, digitization using a 14-bit ADC rated at 2.5 MSPS, and adjustable sensor biasing over 0–80 V. An FMC-to-RJ45 adapter board is alternative for connecting the readout electronics to the ZCU102-based DAQ system.

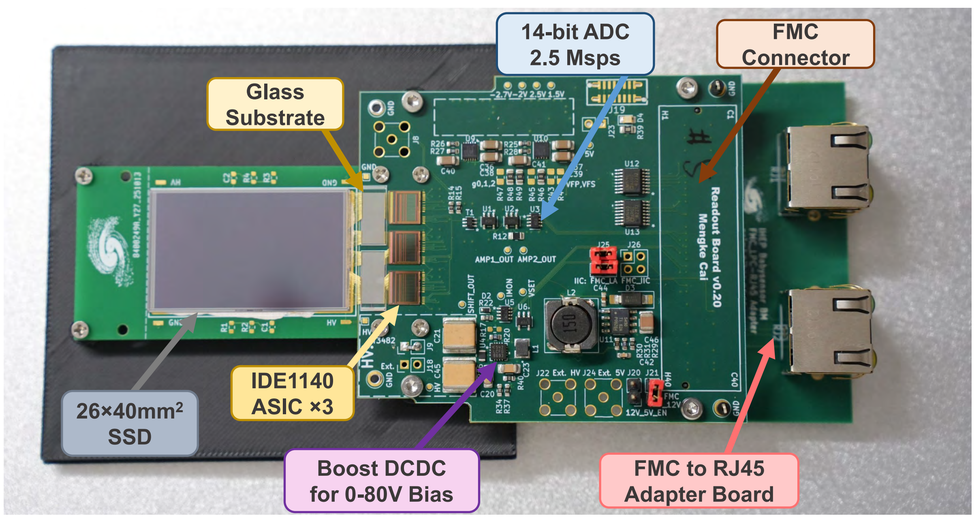


Figure 2. Assembled silicon microstrip detector module and front-end electronics.

ADC Signal Decomposition and Correction

The raw ADC value comprises a channel pedestal, an event-dependent common-mode offset, random noise, and signal:

$$ADC_i^j = Pedeatal_i + CM_{a(i)}^j + Noise_i^j + Signal_i^j$$

where i and j are the channel number and event number. $a(i)$ represents the ASIC channel i connects to.

Pedestals are determined from dedicated pedestal runs. For each event, the common-mode offset is estimated separately for each ASIC using the median pedestal-subtracted channel value.

After pedestal and common-mode noise subtraction, the corrected strip response retains the particle signal and residual noise.

Electronics Characterization

Pedestal data were acquired with the sensor shielded from light in auto-trigger mode at a sensor bias of 50V using 20,000 triggers. Common-mode offsets were estimated separately for each ASIC using the median channel value. The typical channel RMS after common-mode correction was approximately 3.5 ADC counts.

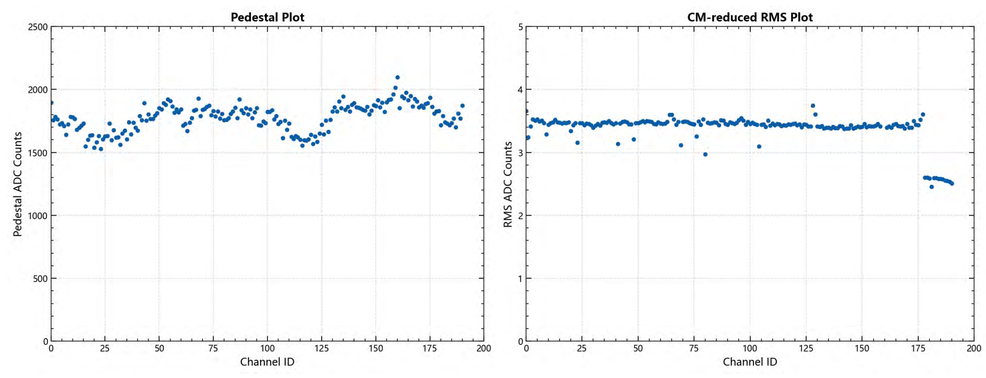


Figure 3. Pedestal and common-mode-reduced RMS distributions measured in auto-trigger mode at a sensor bias of 50 V.

Cosmic-Ray Measurements

Cosmic-ray measurements were performed with a single silicon microstrip module operated at a bias voltage of 50 V. A coincidence signal from two scintillators provided the external trigger. The sensor was shielded from ambient light during data acquisition.

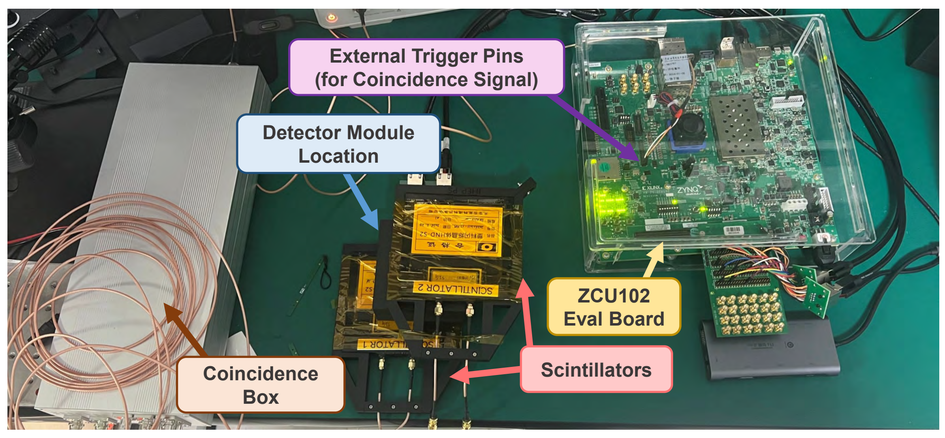


Figure 4. Cosmic-ray test setup shown with the light shielding removed. The sensor was shielded from ambient light during data acquisition.

Signals were corrected for pedestal and common-mode offsets. Cluster selection used a 5σ seed threshold and a 3σ side threshold, where σ is the mean common-mode-reduced RMS of channels remaining after bad and dead channels were excluded.

Figure 5. Representative cosmic-ray event and cluster value distribution in the cosmic-ray data. The cluster signal is the sum of the corrected strip signals within each selected cluster

Conclusions & Outlook

- Silicon-microstrip-DAQ system for cosmic-ray, testbeam, and education purpose.
- A very compact design: SSD+FMC+FPGA-board.
- Looking for more economic solutions for readout ASIC and DAQ platform.

The 2026 International Workshop on the High Energy Circular Electron Positron Collider, Shanghai

October 22-26, 2026

[B12]

Module Prototyping for the CEPC/AGORA Inner Tracker

Xiaomin Deng[1,2], Xingyu Tong[1], Yiming Li[1], Xuhao Yuan[1], Congcong Wang[1]

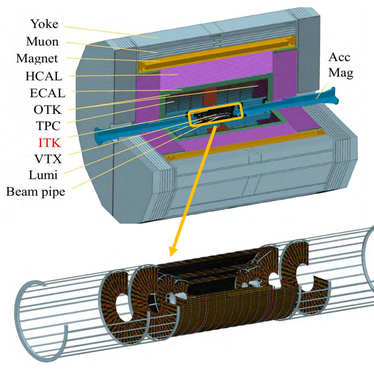
[1]Institute of High Energy Physics,CAS [2]University of Chinese Academy of Sciences

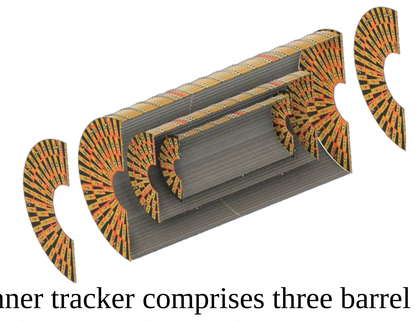
Abstract

Utilizing advanced 55 nm HVCMOS technology, the Inner Tracker (ITK) is a key component of the AGORA detector tracking system, originally proposed for the CEPC. The ITK features a highly modular design, with each basic module integrating up to 14 sensor chips. Pending the availability of full-size chips, prototyping efforts have commenced with dummy sensors that replicate the geometric dimensions and material composition of the final chips. Concurrently, a suite of customized assembly tools has been designed, and the assembly workflow is being established. This poster will present the latest progress in module prototyping.

1. Introduction

The HV-CMOS Inner Tracker (ITK) is a key subsystem of the tracking system. It employs monolithic HV-CMOS pixel sensors fabricated using 55 nm CMOS technology to achieve high spatial resolution, a low material budget, and excellent mechanical stability.

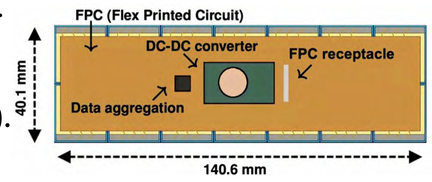




The inner tracker comprises three barrel layers and four endcap layers, with a total active area of 20 m² and 47,024 sensors in total.

➢ITK Module design from CEPC TDR

- Sensor layout: 14 sensors (2 rows × 7 columns).
- Module size: 140.6 × 40.1 mm².
- Electrical connections: Wire bonds to the Flexible Printed Circuit (FPC).
- FPC functions: Power, data, clock, and command signal routing.
- Integrated electronics: DC–DC converter and data aggregation chip.



➢R&D Plan for ITK Module Prototyping

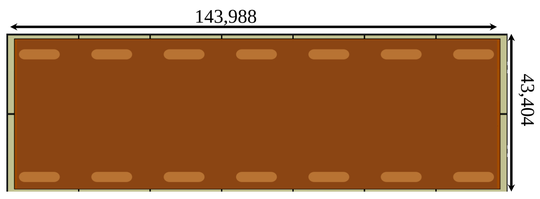
- Mechanical Prototyping: Develop and validate the assembly process.
- Thermal-Mechanical Prototyping: Assess thermal-mechanical stability.
- Functional Prototyping: Validate functionality and readout performance.
- Module Qualification: Evaluate overall performance and reliability.

This poster focuses on the first step of the R&D program: **Mechanical Prototyping,** which includes:

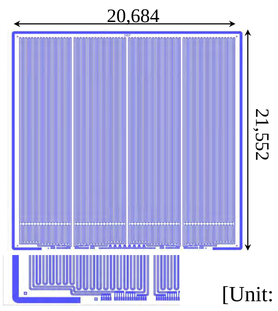
- Development of customized assembly tools.
- Establishment of the module assembly process.
- Fabrication of dummy modules using dummy sensors.

2. Dummy module design

Dummy module is designed to replicate the geometry and mechanical structure of the final ITK module, enabling the development and validation of assembly procedures before functional sensors become available.



[Unit: μm]



[Unit: μm]

➢Dummy sensor: Dummy COFFEE v2

- Same size as the final chip
- With metal traces for thermal study
- With real pads and pattern to facilitate assembly

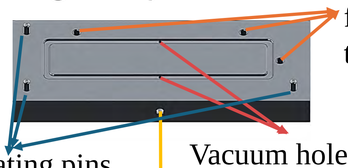
➢Dummy hybrid: Designed based on the dummy sensor size.

- Flexible, heat-resistant, electrically insulating polyimide (PI) substrate for FPC.
- With metal traces to allow wire bonding

3. Assembly tools

Customized assembly tools were designed for manual prototype assembly.

■ Jig for hybrid



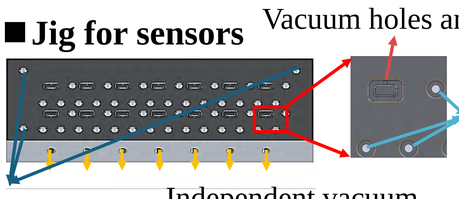
locating holes for positioning the hybrid

locating pins

Vacuum holes and grooves for holding the hybrid

Connect the vacuum pump

■ Jig for sensors



Vacuum holes and grooves

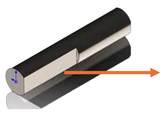
locating holes

Independent vacuum for each sensor

locating holes for positioning the chip

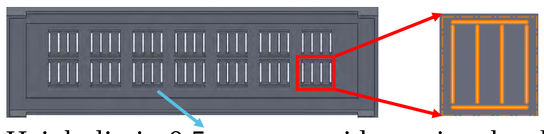
■ pins

To position the hybrid/sensor.



Partially flatted

■ Stencil for glue application

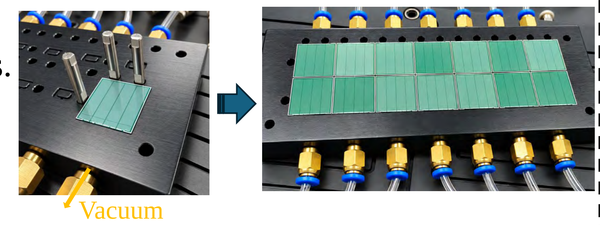


Height limit: 0.5mm, to avoid pressing the chip.

4. Assembly procedure

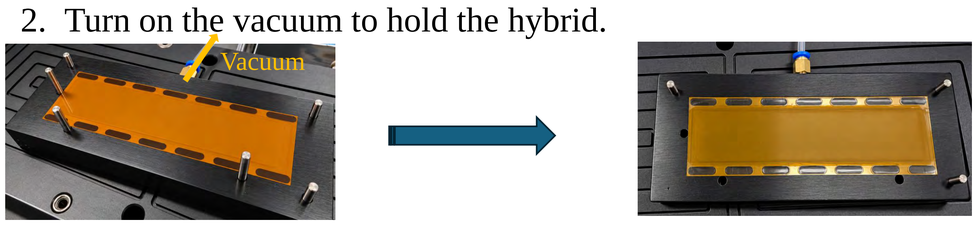
➢Step 1. Sensor positioning

1. Position the sensor using locating pins.
2. Turn on the vacuum to hold the chip.
3. Repeat steps for all 14 sensors.



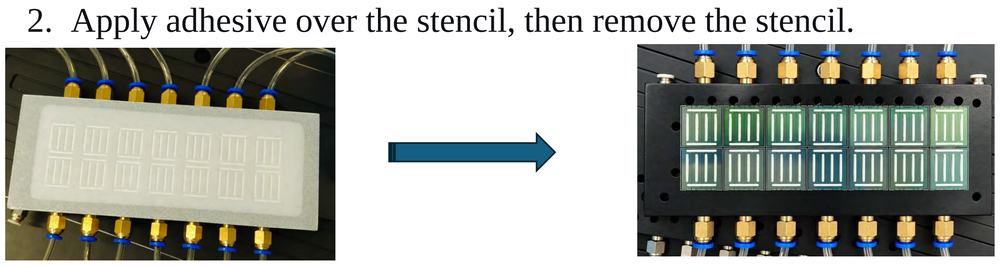
➢Step 2. Hybrid positioning

1. Position the hybrid using three locating pins.
2. Turn on the vacuum to hold the hybrid.



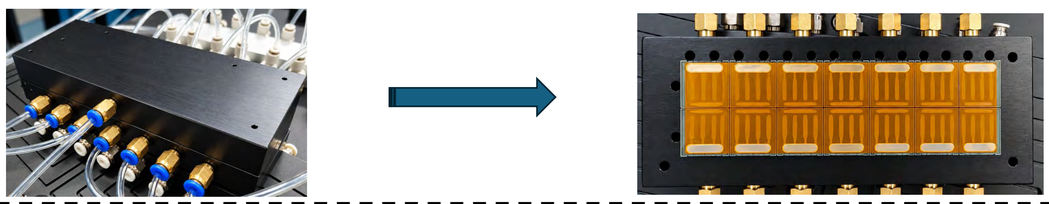
➢Step 3. Adhesive application

1. Place the stencil over the sensors.
2. Apply adhesive over the stencil, then remove the stencil.



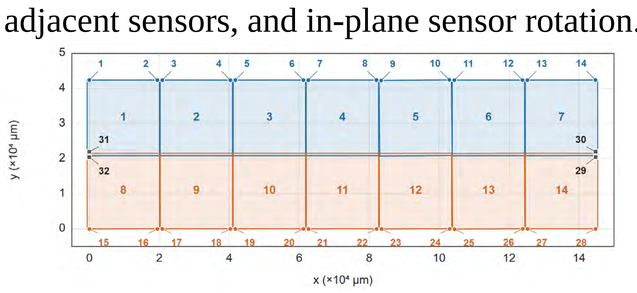
➢Step 4. Module assembly

1. Align and mate the adhesive-applied sensors and hybrid.
2. Turn off the vacuum on the hybrid jig and remove it after adhesive curing.



5. Prototype validation

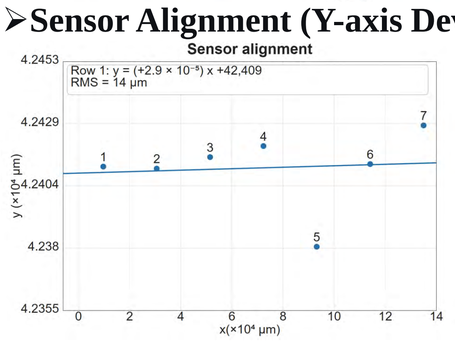
For the assembled module, the positions of 32 exposed fiducial targets on the sensor surfaces are measured to evaluate sensor alignment, gaps between adjacent sensors, and in-plane sensor rotation.

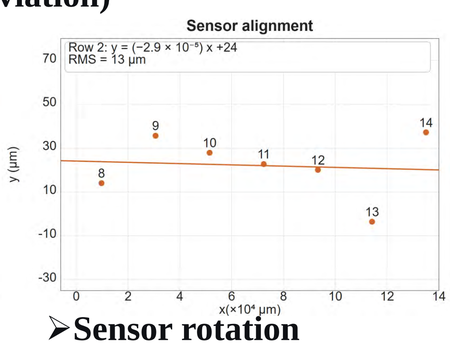




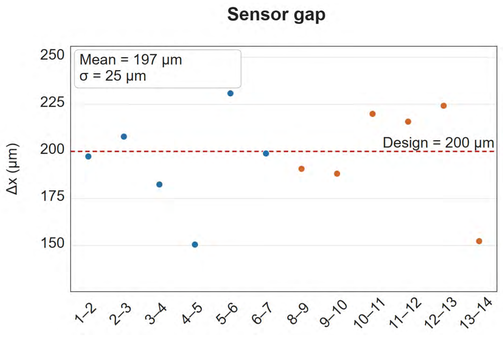
The Quick Vision Apex enables high-precision, non-contact optical measurement for accurate dimensional inspection.

➢Sensor Alignment (Y-axis Deviation)

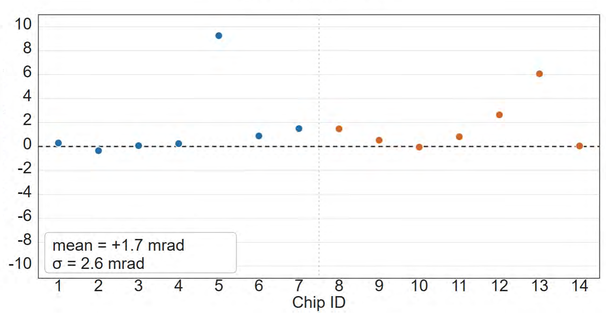




➢Sensor gap along X-axis



➢Sensor rotation



6. Current status & Outlook

➢Current Status

- ✓ Customized tools for manual assembly have been designed.
- ✓ The assembly workflow has been initially established.
- ✓ Dummy sensors have been produced for module prototyping.
- ✓ The first dummy module has been assembled using dummy sensors.

➢Outlook

- ☐ Automatic assembly using gantry system to be investigated for mass production.
- ☐ Assess bonding integrity and mechanical stability.
- ☐ Integrate dummy electronics and thermal loads.
- ☐ Evaluate thermal performance, deformation, and cooling efficiency.

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[B13]

A Methodology for Determining Pixel Chip Circuit Parameters from Vertex Detector Design Requirements

Hao Xiong[1], Ying Zhang[2], Zhijun Liang[3], Ziying Liu[4], Yunpeng Lu[5]

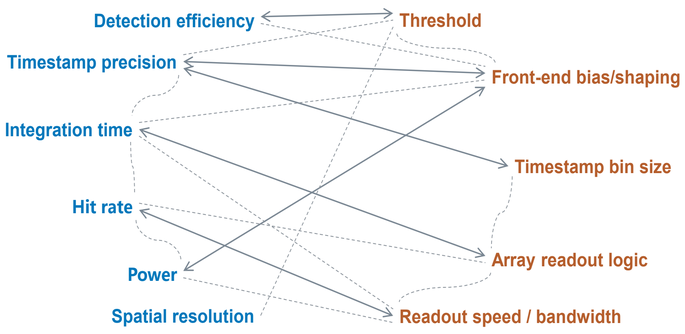
The Institute of High Energy Physics of the Chinese Academy of Sciences

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We present a quantitative methodology for determining pixel-chip circuit parameters from vertex-detector design requirements. Collected-charge statistics and threshold-crossing response connect power, threshold and integration time to timestamp precision and occupancy.

01 Background & Design Targets

Precision electroweak, Higgs and flavour studies at CEPC/FCC-ee require precise impact-parameter measurements and secondary-vertex reconstruction. The AGORA vertex detector must combine fine spatial resolution, high efficiency and a low material budget. Charge sharing, discriminator threshold and front-end response speed affect spatial resolution, detection efficiency, timing, power consumption and readout requirements. These coupled trade-offs motivate a unified method for selecting compatible circuit parameters.



Coupling Between Detector Performance Requirements and Circuit Parameters

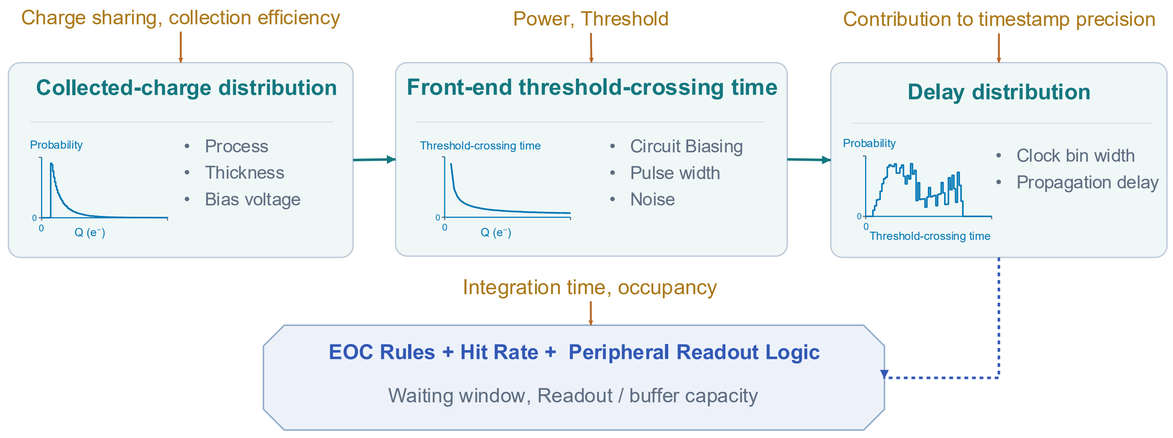
AGORA vertex-detector requirements

Requirement	Target
Spatial Resolution	~ 3 μm
Power density	≤ 40 mW/cm²
Integration time	< 1 μs
Timestamp precision	< 100 ns
Pixel hit rate	~ 200 MHz/cm²
Material budget per layer	< 0.2% X_0

02 Methodology

Propagate collected-charge statistics through the threshold-crossing response to obtain a delay distribution. Combine its timing contribution with the EOC rules, background hit rate and readout organisation to infer compatible front-end settings, waiting windows and readout capacity.

$$Q \sim f_Q \quad \longrightarrow \quad t = d(Q; P, Q_{\mathrm{th}}) \quad \longrightarrow \quad f_t$$



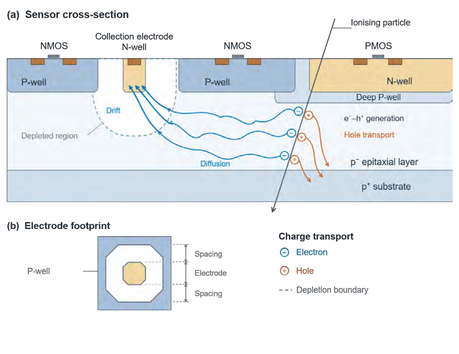
03 Methodology illustrated with a simplified model

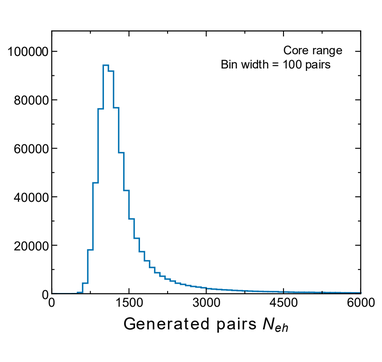
A Sensor and collected-charge statistics

Ionisation creates carriers that reach the collection node by drift and diffusion.

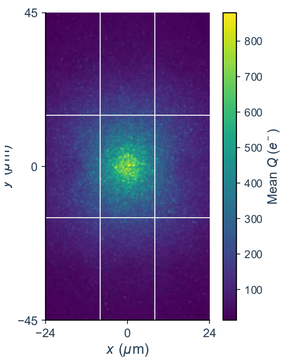
Energy-loss fluctuations and charge sharing shape the collected-charge distribution.

A simple 3×3 pixel array model supplies the example for this methodology demonstration.

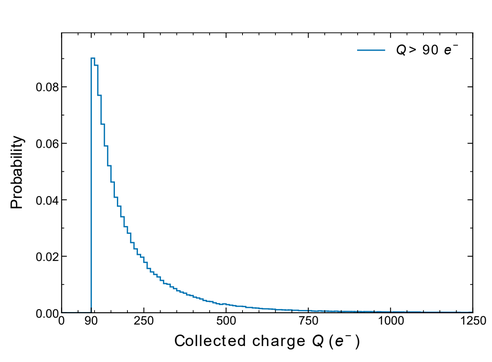




Generated charge



Collection map



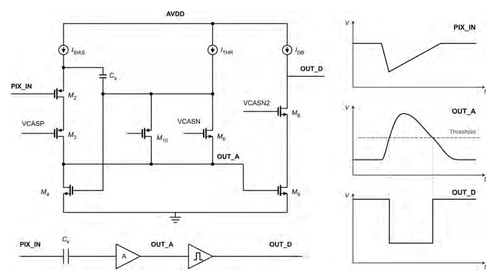
Collected $Q > 90\,e^-$

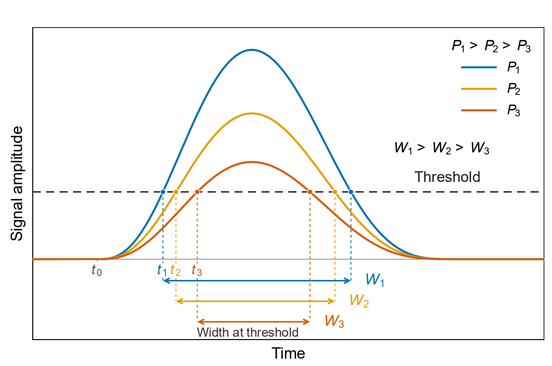
B Analogue front-end response

A source follower and amplifier drive a leading-edge discriminator.

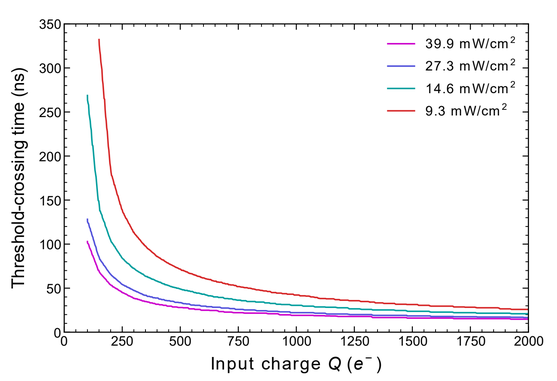
Higher power or a lower threshold shortens crossing time in this reference circuit.

The simulated charge-to-time curves provide the mapping used below.





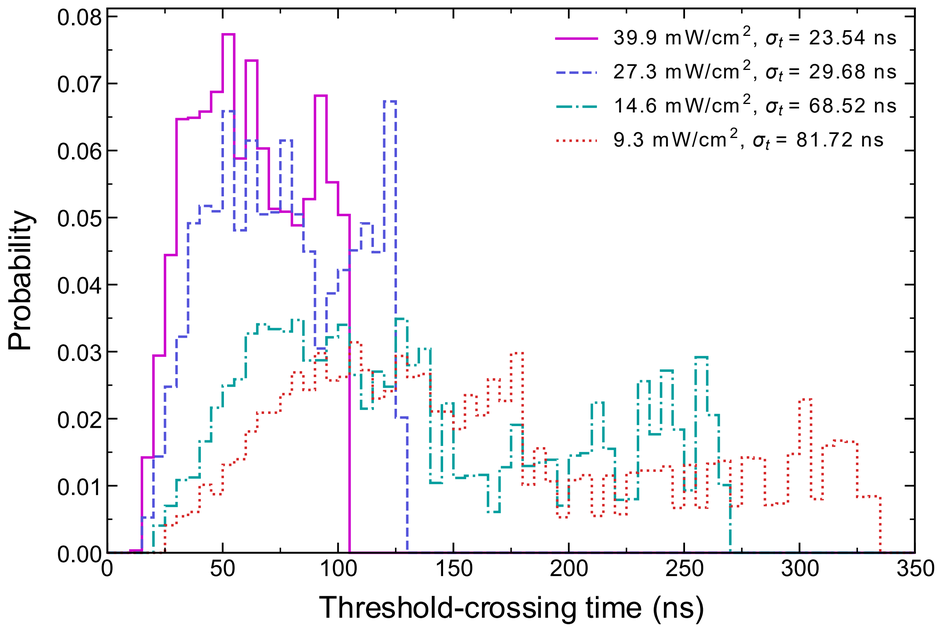
Analog Front-End Signal



Charge-to-time curves

C Delay statistics and timestamp precision

Mapping the collected-charge distribution through the simulated front-end response gives the threshold-crossing-time distribution. For a design with 14.6 mW/cm² power density and a 100 e⁻ threshold, the time-walk contribution to timestamp precision is 68.5 ns.

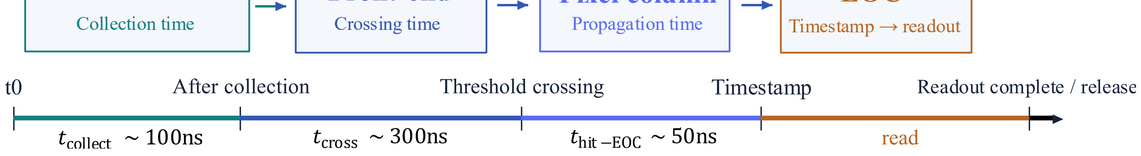


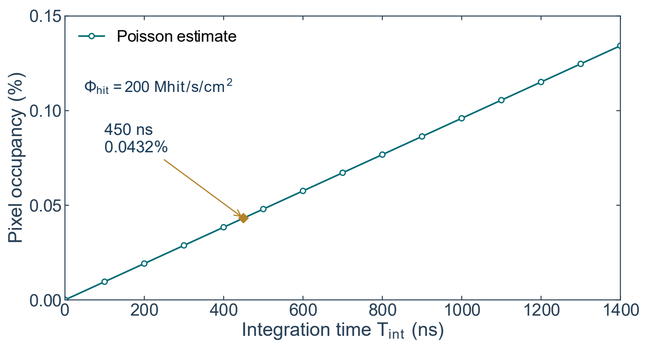
D Integration time and occupancy

Integration time is the difference between the timestamp and the true event time.

For the PRECISE architecture under development, a 450 ns integration time gives an estimated 0.0432% pixel occupancy at 200 Mhit/s/cm². The occupancy allowed by track reconstruction can conversely constrain the integration-time range.

$$t_{\mathrm{int}} = t_{\mathrm{collect}} + t_{\mathrm{cross}} + t_{\mathrm{hit-EOC}} \approx 450\ \mathrm{ns}$$





04 Outlook

Future work will incorporate the actual sensor structure and transient charge collection into a process-specific TCAD–Geant4 model to obtain accurate and reliable distributions of collected charge and threshold-crossing time.

Subsequent measurements will validate the performance of the complete PRECISE sensor–front-end–readout chain and assess the feasibility of the proposed methodology.

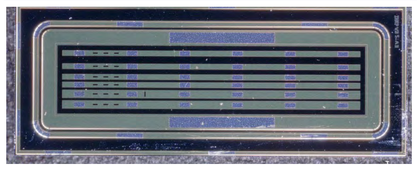
[B14]

Neural-Network-Based Position Reconstruction for Strip AC-LGADs

Weiyi Sun, Ke Li, Mengzhao Li, Zhijun Liang, Mei Zhao

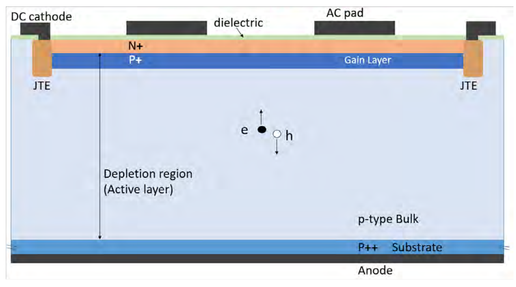
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Strip AC-LGAD sensor

AC-Coupled Low Gain Avalanche Diode



Structure of a Strip AC-LGAD sensor

Questions

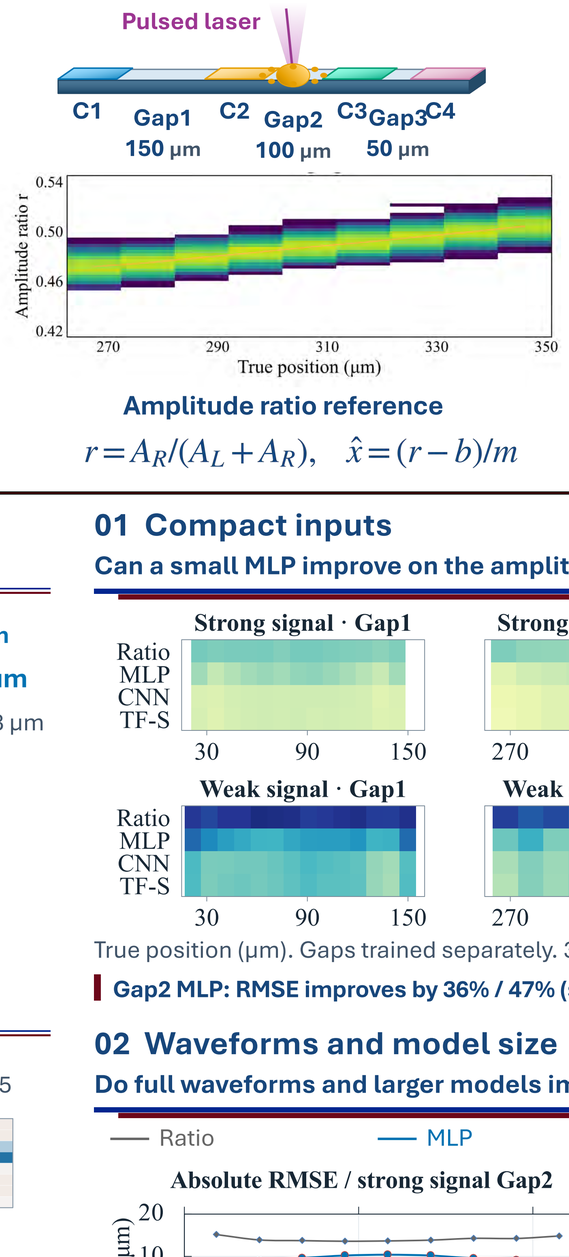
1 Can a small network with few amplitudes beat the ratio method?

2 Do full waveforms and larger networks improve reconstruction?

3 Can ToA and ToT improve amplitude-based reconstruction?

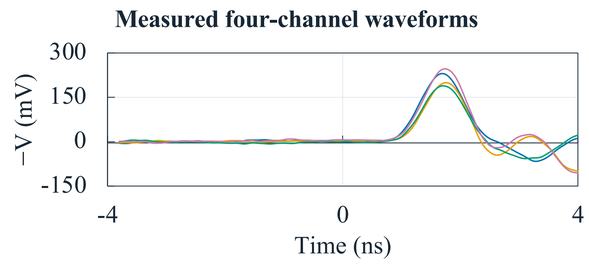
4 Can a model predict a gap excluded from training?

Experiment: TCT Laser Scan



Amplitude ratio reference

$$r = A_R/(A_L + A_R), \quad \hat{x} = (r - b)/m$$

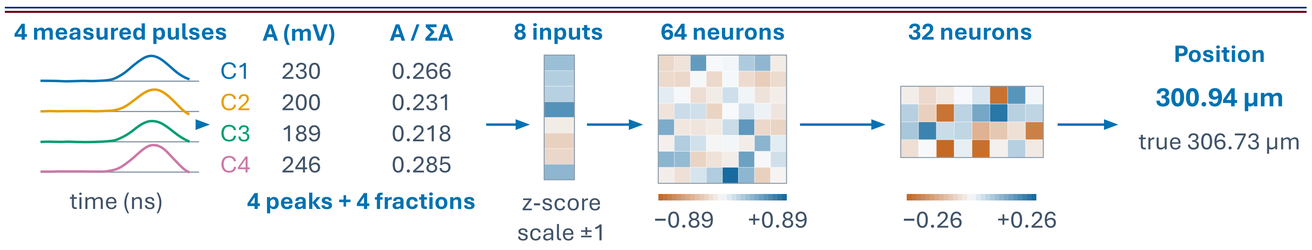


4 channels × 197 samples, 50 ps per sample

Gap2 RMSE: 14.14 µm strong
31.75 µm weak

MLP: compact amplitude features

Eight features encode position



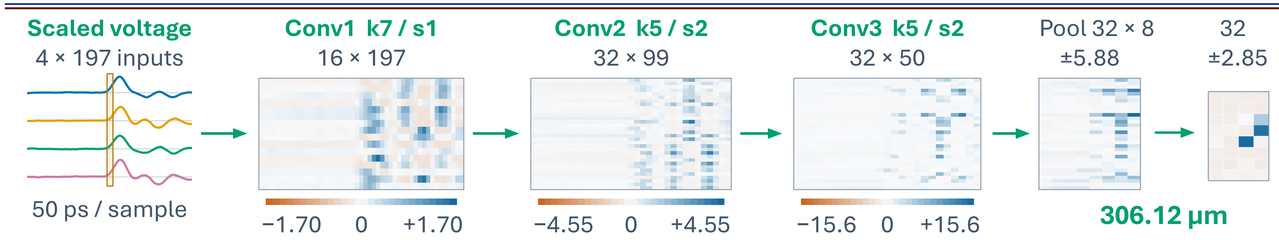
8 → 64 → 32 → 1 SiLU 2,689 parameters

$$h' = \mathrm{SiLU}(Wh + b)$$

h: features. W, b: learned weights and offsets.
Colours represent measured features and neuron activations.

Joint-channel CNN

Pulse shapes reveal more than amplitudes



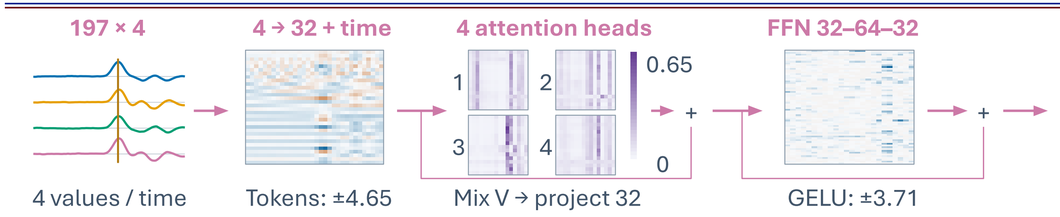
Time-local filters mix all four channels. 16,465 parameters.

$$H' = \mathrm{SiLU}(K * H + b)$$

K: learned filters. *: convolution over nearby samples.
The feature maps show an actual event at successive layers.

Time Transformer

Relationships across distant samples



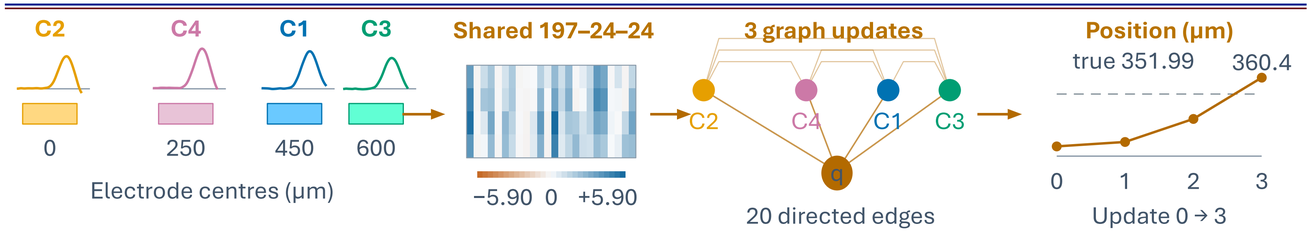
2 blocks, 4 heads, width 32, GELU. 17,345 parameters.

$$\mathrm{Attention}(Q, K, V) = \mathrm{softmax}(QK^T/\sqrt{8})\,V$$

Q, K: similarity. V: carried features.
Each attention head has width 8.

Anchored GNN

Electrode geometry support transfer to an unseen gap



Shared waveform encoder and 3 graph updates. 20,259 parameters.
AGNN-d0 removes radial messages but retains electrode anchors.

$$\hat{x}' = \hat{x} + 0.5\,\mathrm{mean}_i[(c_i - \hat{x})\,w_i]$$

c: electrode centres. x-hat: estimated hit.
w: learned weight between −1 and 1.

Train on Gap1 + Gap3, then predict Gap2.
Curves: seed means. Whiskers: seed range. Black: ideal.

Input definitions and training convention

Input	Numbers supplied to the position model
TT	ToA + ToT
A8	4 peaks + 4 peak fractions
TT+A	TT + 4 peaks
S16	Peaks, areas, relative ToA + validity flags
P16	16 learned principal components
CNN / TF-S	All four waveforms (788 samples)

CFD = 0.5 of each channel's own peak. TDC step = 20 ps.

Conclusions and outlook

1 RMSE Improvement: MLP 36% / 47%, TF 56% / 59% (strong / weak).

2 Larger models give no material gain in the matched capacity tests.

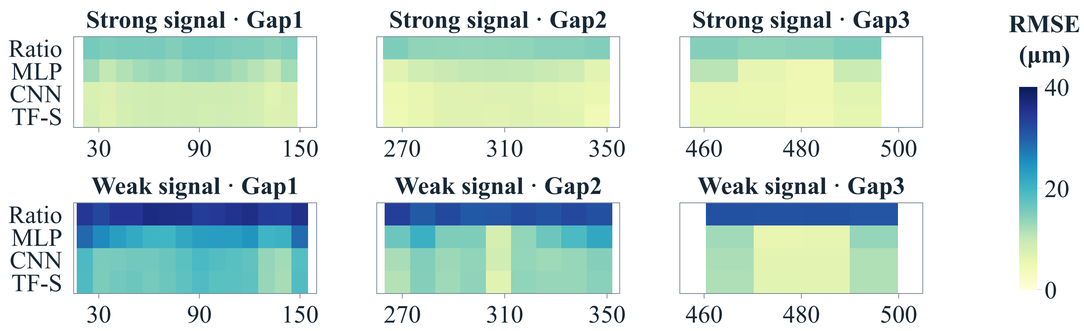
3 Timing alone is weak here. Amplitude or area information is needed.

4 Robust cross-gap observables remain to be found.

5 Small models show FPGA potential. Hardware tests remain necessary.

01 Compact inputs

Can a small MLP improve on the amplitude ratio?

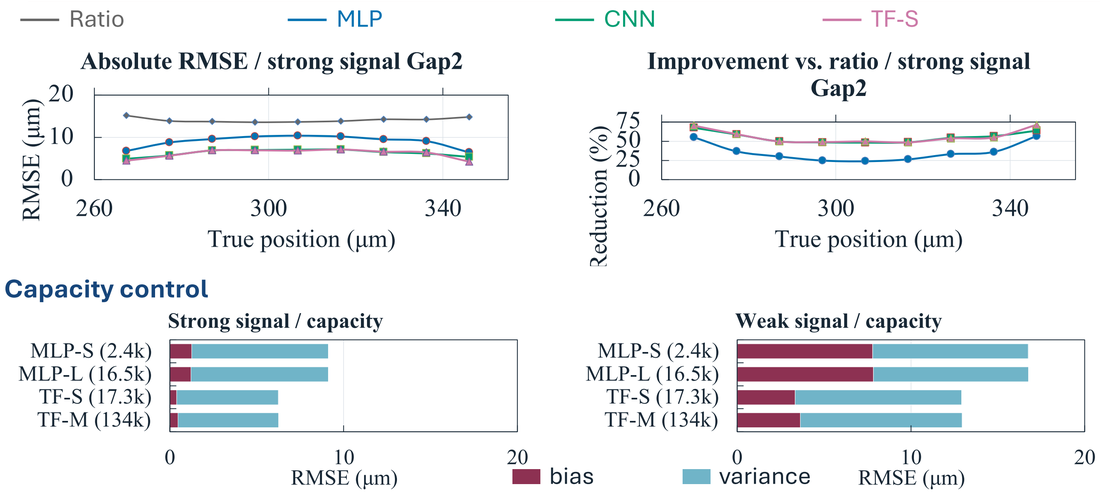


True position (µm). Gaps trained separately. 3 seeds. Gap3: 4 validation positions.

Gap2 MLP: RMSE improves by 36% / 47% (strong / weak).

02 Waveforms and model size

Do full waveforms and larger models improve accuracy?



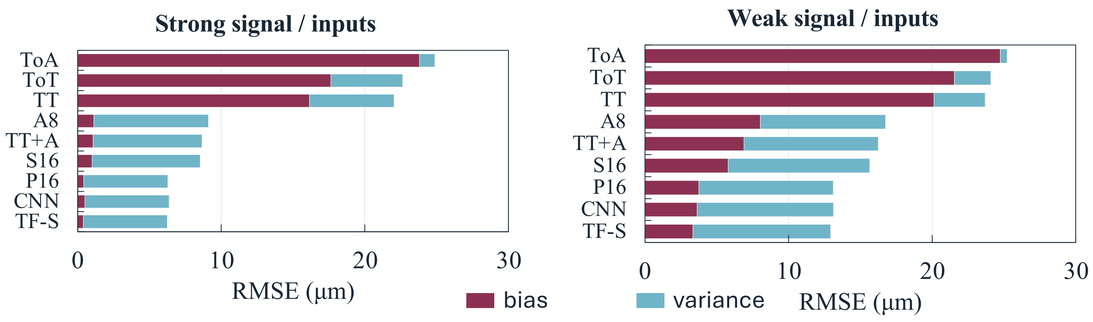
Capacity control

MLP-S/L: same four peaks. TF-S/M: same full waveforms.

Waveforms help. Larger models give no material gain.

03 Timing information

Can ToA and ToT improve amplitude-based reconstruction?



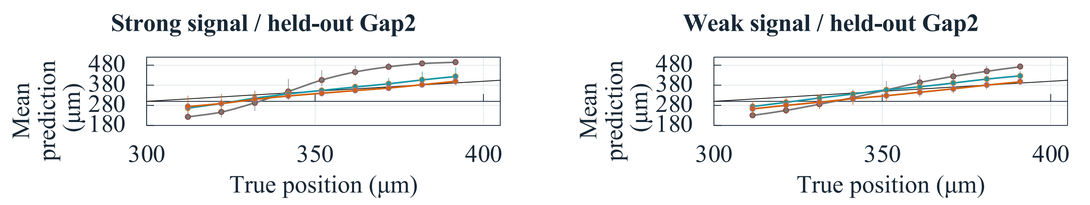
Total bar length = RMSE.

TT+A vs. A8: 4.9% / 3.0% lower RMSE (strong / weak).

Timing alone gives poor position sensitivity.

04 Cross-gap transfer

Train on Gap1 + Gap3. Can the model predict Gap2?



Gap2 RMSE (µm)	CNN-4L	AGNN	AGNN-d0
Strong	95.0	43.6	37.3
Weak	104.9	60.6	60.0

Anchors help, but bias and seed sensitivity remain.

Reference

[1] M. Tornago et al., Resistive AC-Coupled Silicon Detectors
NIM A 1003, 165319 (2021). arXiv:2007.09528.

[2] A. Aoki et al., Machine Learning-Based Reconstruction for Resistive Silicon Sensors.
JINST 21, C08015 (2026). arXiv:2607.11585.

[2] F. Siviero et al., Machine learning for precise hit position reconstruction in Resistive Silicon Detectors.
JINST 19, C01028 (2024).

[4] V. G. Satorras et al., E(n) Equivariant Graph Neural Networks.
ICML, PMLR 139, 9323–9332 (2021). arXiv:2102.09844.

Simulation of the Influence of JTE and p-Stop Geometry on the Breakdown Voltage of Long RSD/LGAD Sensors

[B15]

Authors: Violetta Maier, Nikolay Atanov, Alexandr Putilin et al.

1. RSD-LGAD Sensor Concept

Modern detector systems for particle physics, such as the Outer Tracker (OTK) of the future Circular Electron-Positron Collider (CEPC), aim to improve both time and spatial resolution while reducing the amount of material in the detector and simplifying its readout electronics. One possible approach is the use of large-area RSD-LGAD sensor strips. Such sensors can provide particle position information using multiple adjacent readout pads. Increasing the strip length and the number of strips per module allows a larger area to be covered with fewer readout channels.

A conventional LGAD matrix consists of discrete n^{++} cathodes separated by edge-termination structures, such as the Junction Termination Extension (JTE) and p-stop. These structures introduce insensitive dead regions between pixels, thereby reducing the fill factor. AC-coupled RSD-LGAD sensors (here after referred to as AC-LGADs) (Fig. 1, left) [1] address the dead-region problem by employing a continuous n^{+} layer. In an AC-LGAD, the metal readout electrodes are electrically isolated from the resistive layer by a thin dielectric passivation layer, providing capacitive coupling to the readout electronics. These structures have demonstrated promising performance, as reported in [2], achieving a time resolution of 25-30 ps and a spatial resolution of 10 μm. Further improvements in signal shape and time and spatial resolution may be achieved using DC-coupled RSD-LGAD sensors [3, 4]. In a DC-RSD LGAD, the dielectric layer beneath the electrodes is absent. The metal pads form a direct electrical contact with the resistive layer, providing DC coupling [3] (Fig. 1, right).

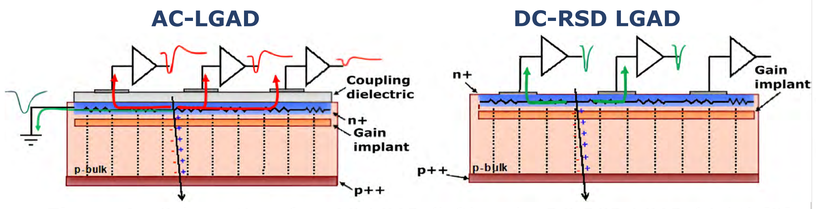


Figure 1 *- Schematics of an AC-LGAD (left) and a DC-RSD LGAD (right) [3]*

One of the key characteristics of a semiconductor sensor is its breakdown voltage. A higher breakdown voltage extends the sensor's operating range and enables stable operation at higher bias voltages. Therefore, achieving a high breakdown voltage while maintaining a simple sensor structure is highly desirable. In this work, the influence of structural parameters on the breakdown voltage of a DC-RSD LGAD was investigated. Thestudy was first performed for a structure with a length of 400 μm, followed by an investigation of the effect of the most influential parameter on the breakdown voltage of a longer structure.

2. DC-RSD LGAD 2D Model

There are many ways to arrange electrodes on the sensor surface. These configurations are described in detail in [2, 3, 5]. In this work, we consider a 2D model of a strip DC-RSD LGAD sensor implemented in Synopsys Sentaurus TCAD, based on the structure of the AC-coupled RSD-LGAD sensor described in [5]. We assume continuous strips with a large width in the cross-section (Fig. 2), ranging from 400 μm to one centimeter.

- passivation surface layer (oxide).

- resistive layer (n^{+} type doping, N=1 x 10^{18} см$^{-3}$).

- gain layer (p - type doping, N = 1 x 10^{16} см$^{-3}$).

- p^{-} epitaxial layer (p^{-} type doping, N=1 x 10^{12} см$^{-3}$).

- anode (p^{++} type doping, N = 1 x 10^{19} см$^{-3}$).

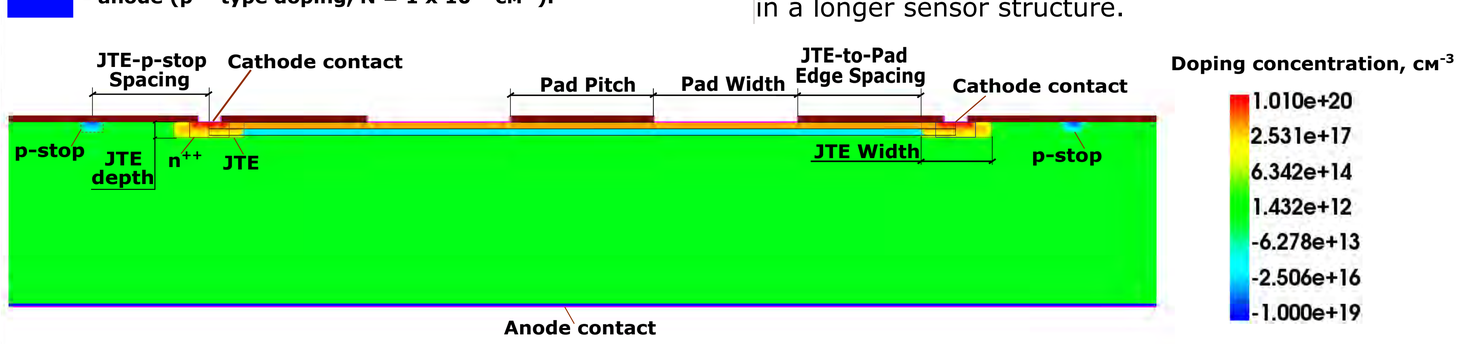


Figure 2 *- 2D Structure of the DC-RSD-LGAD Sensor*

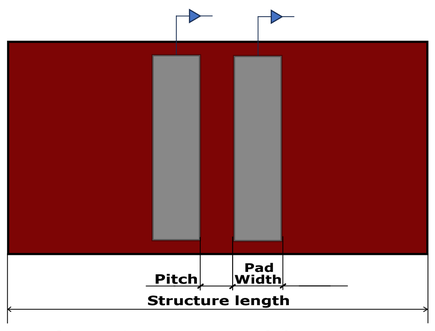


Figure 3 *- Top View of the DC-RSD LGAD Sensor*

The length of the structure means the dimension illustrated in Figure 3.

3. Tasks

The main objectives of this study are:
1. To investigate the dependence of the breakdown voltage on the width of the Junction Termination Extension (JTE) in a DC-RSD LGAD sensor with a structure length (Fig. 3) of 400 μm.
2. To evaluate the influence of the JTE depth on the breakdown voltage at the same structure length.
3. To determine how the distance between the JTE and the p-stop region affects the breakdown voltage.
4. To investigate the influence of the electrode pad width on the breakdown voltage.
5. To evaluate the effect of the pad pitch on the breakdown voltage.
6. To determine how the distance between the JTE edge and the electrode pad edge affects the breakdown voltage.
7. To identify the geometrical parameter with the greatest influence on the breakdown voltage and investigate its effect in a longer sensor structure.

4. Method for the Breakdown Calculation

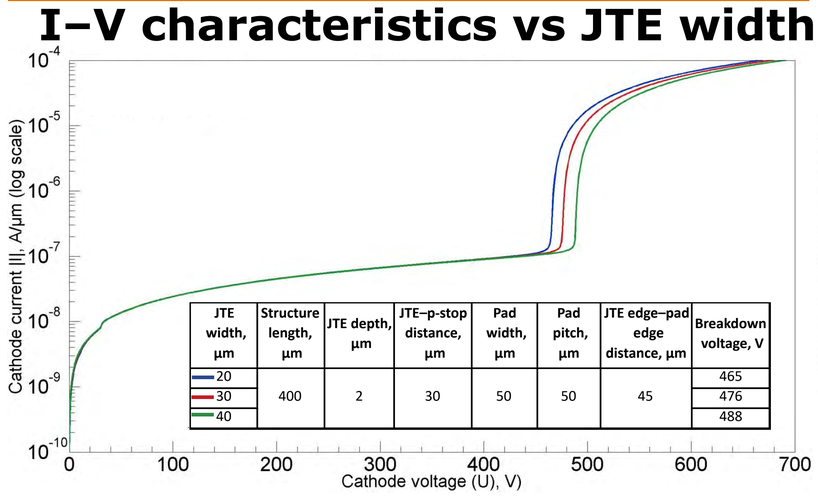
The breakdown voltage was determined as the maximum of the second derivative of the logarithm of the current with respect to voltage:

$$\frac{d^2(\ln I)}{dU^2}$$

The voltage at which this curve reaches its maximum is taken as the breakdown voltage.

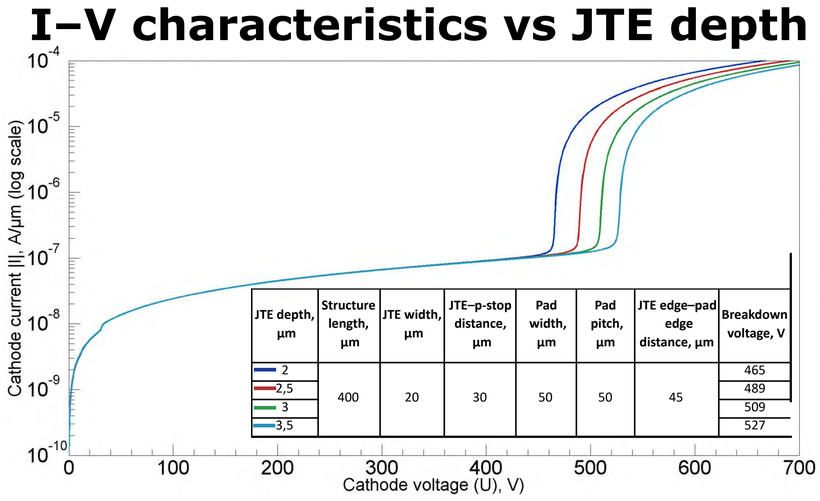
5. Results

I–V characteristics vs JTE width



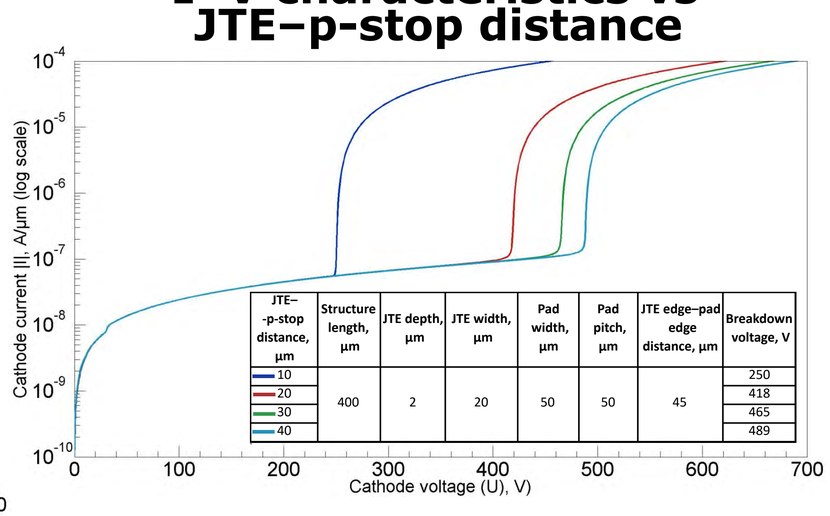
JTE width, μm	Structure length, μm	JTE depth, μm	JTE–p-stop distance, μm	Pad width, μm	Pad pitch, μm	JTE edge–pad edge distance, μm	Breakdown voltage, V
20	400	2	30	50	50	45	465
30							476
40							488

I–V characteristics vs JTE depth



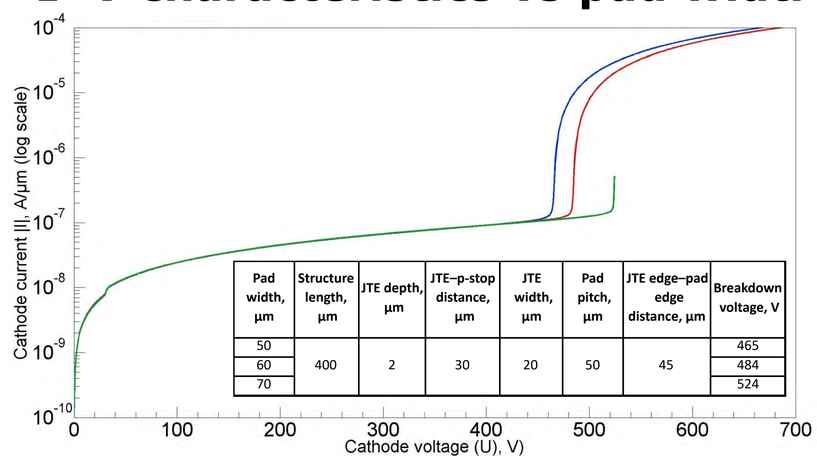
JTE depth, μm	Structure length, μm	JTE width, μm	JTE–p-stop distance, μm	Pad width, μm	Pad pitch, μm	JTE edge–pad edge distance, μm	Breakdown voltage, V
2	400	20	30	50	50	45	465
2,5							489
3							509
3,5							527

I–V characteristics vs JTE–p-stop distance



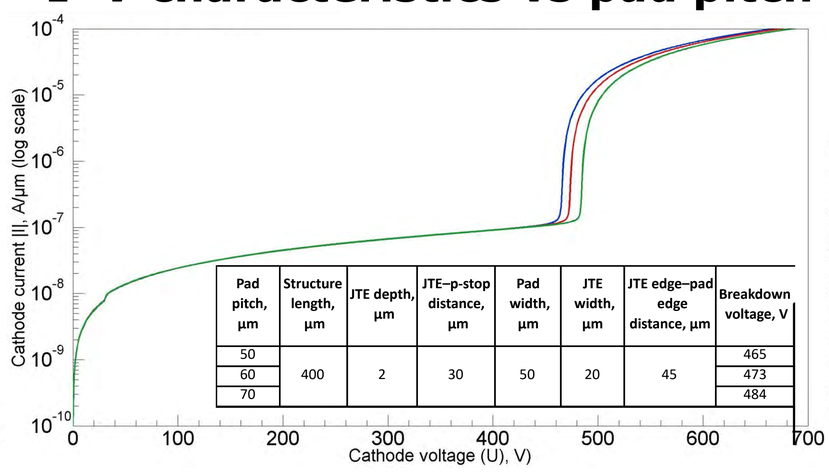
JTE–-p-stop distance, μm	Structure length, μm	JTE depth, μm	JTE width, μm	Pad width, μm	Pad pitch, μm	JTE edge–pad edge distance, μm	Breakdown voltage, V
10	400	2	20	50	50	45	250
20							418
30							465
40							489

I–V characteristics vs pad width



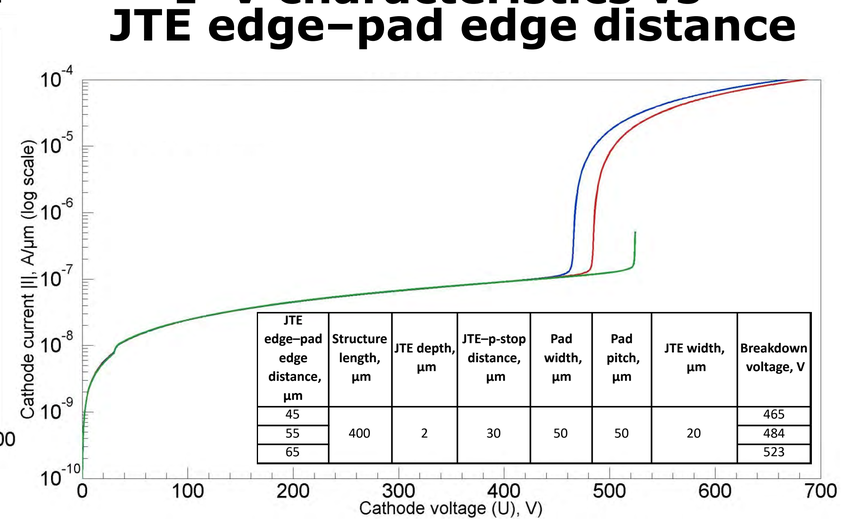
Pad width, μm	Structure length, μm	JTE depth, μm	JTE–p-stop distance, μm	JTE width, μm	Pad pitch, μm	JTE edge–pad edge distance, μm	Breakdown voltage, V
50	400	2	30	20	50	45	465
60							484
70							524

I–V characteristics vs pad pitch



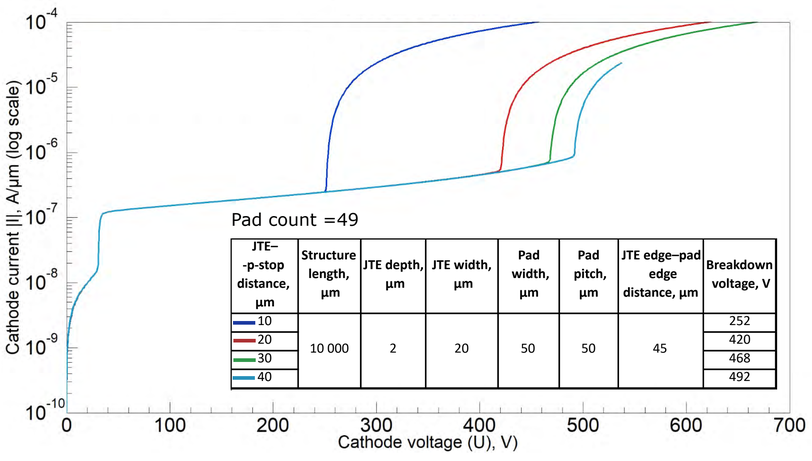
Pad pitch, μm	Structure length, μm	JTE depth, μm	JTE–p-stop distance, μm	Pad width, μm	JTE width, μm	JTE edge–pad edge distance, μm	Breakdown voltage, V
50	400	2	30	50	20	45	465
60							473
70							484

I–V characteristics vs JTE edge–pad edge distance



JTE edge–pad edge distance, μm	Structure length, μm	JTE depth, μm	JTE–p-stop distance, μm	Pad width, μm	Pad pitch, μm	JTE width, μm	Breakdown voltage, V
45	400	2	30	50	50	20	465
55							484
65							523

I–V characteristics vs JTE–p-stop distance



JTE–-p-stop distance, μm	Structure length, μm	JTE depth, μm	JTE width, μm	Pad width, μm	Pad pitch, μm	JTE edge–pad edge distance, μm	Breakdown voltage, V
10	10 000	2	20	50	50	45	252
20							420
30							468
40							492

6. Conclusions

1. The breakdown voltage increases with increasing values of all investigated geometrical parameters within the studied ranges.
2. The distance between the JTE and p-stop regions has the strongest influence on the breakdown voltage. Increasing this distance from 10 to 40 μm raises the breakdown voltage from approximately 250 to 489 V. However, the increase becomes progressively smaller at larger distances.
3. The JTE depth also has a significant effect on the breakdown voltage. Increasing the depth from 2 to 3.5 μm raises the breakdown voltage from 465 to 527 V. The incremental increase in breakdown voltage decreases as the JTE depth increases.
4. The pad width and the distance between the JTE edge and the pad edge have comparable effects on the breakdown voltage, increasing it by approximately 59 V and 58 V, respectively, over the investigated ranges.
5. The JTE width and pad pitch have the weakest influence among the investigated parameters, with breakdown voltage increases of approximately 23 V and 19 V, respectively.
6. For the 10,000 μm-long structure, the breakdown voltage increases from 252 V at a JTE–p-stop distance of 10 μm to 492 V at 40 μm. This trend is consistent with the results obtained for the 400 μm-long structure, suggesting that the influence of the JTE–p-stop distance persists in longer sensors.

7. References

1. W. Sun et al., "The Performance of AC-coupled Strip LGAD developed by IHEP," Nucl. Instrum. Methods Phys. Res. A, vol. 1062, p. 169203, 2024.
2. M. Tornago et al., "Resistive AC-Coupled Silicon Detectors (RSD): Principles of operation and first results," Nucl. Instrum. Methods Phys. Res. A, vol. 1003, p. 165319, 2021.
3. F. Moscatelli et al., "Measurements and TCAD simulations of innovative RSD and DC-RSD LGAD devices for future 4D tracking," Nucl. Instrum. Methods Phys. Res. A, vol. 1064, p. 169380, 2024.
4. R. Arcidiacono et al., "Innovative DC-coupled Resistive Silicon Detector for 4D tracking," Nucl. Instrum. Methods Phys. Res. A, vol. 1080, p. 170796, 2025.
5. X. Zhang et al., "Design of AC-coupled low gain avalanche diodes (AC-LGADs): a 2D TCAD simulation study," J. Instrum., vol. 17, no. 09, p. C09014, 2022.

UP bare stave design and thermal study

Tiange Li (李天歌), Heng Ma, Zhongfu Xia, Yi Yang and Jiesheng Yu @ Hunan University
Hanbing Liu, Kai Liu and Zhijie Wang @ Lanzhou University
Xuhao Yuan and Jianchun Wang @ IHEP

[B16] **Shanghai, October 22 ~ 26, 2026**

on behalf of UP wp3 group

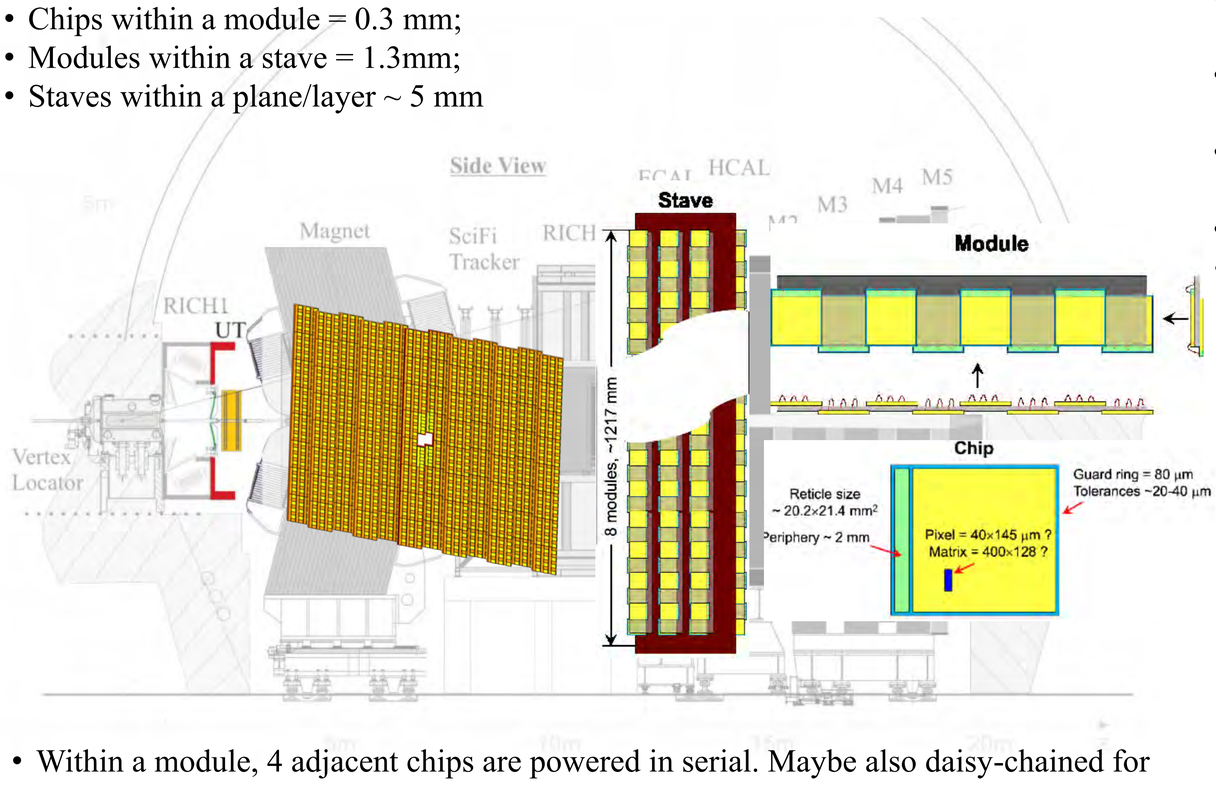
Upstream Pixel of LHCb

Layout:

- 1536 silicon sensors, organised in 4 planes, 48 vertical staves and 48 modules.

Detection overlap:

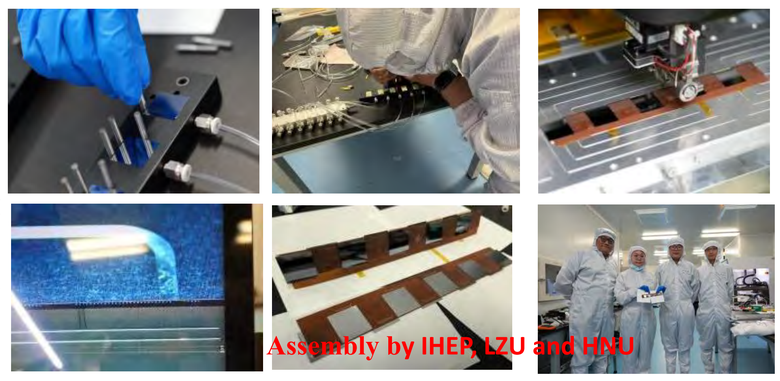
- Chips within a module = 0.3 mm;
- Modules within a stave = 1.3mm;
- Staves within a plane/layer ~ 5 mm

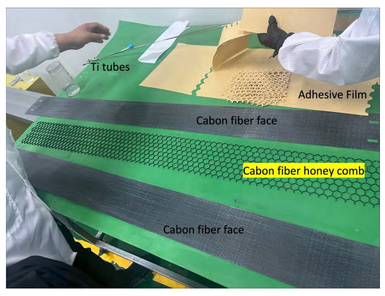


- Within a module, 4 adjacent chips are powered in serial. Maybe also daisy-chained for output e-link. They should have the same e-link/chip configuration.

First module and UP bare stave production

- **Jigs** based now. Using gantry for high precision **later**
  Designed by IHEP & LZU
- Chips positioning according to **D-shape** pins, with **vacuum** fixing
- **Align** the upper and lower jigs using positioning holes.
- Using **five-point method** to glue hybrid and chips.
- Wait for one day until the glue cures.
- Also with **wire bonding tests**: Two layers of the chips are both bonded => looks good

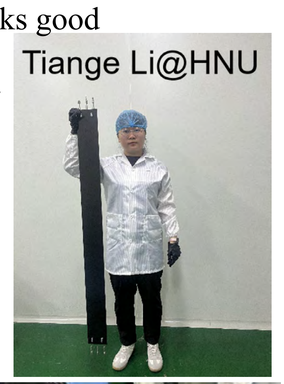


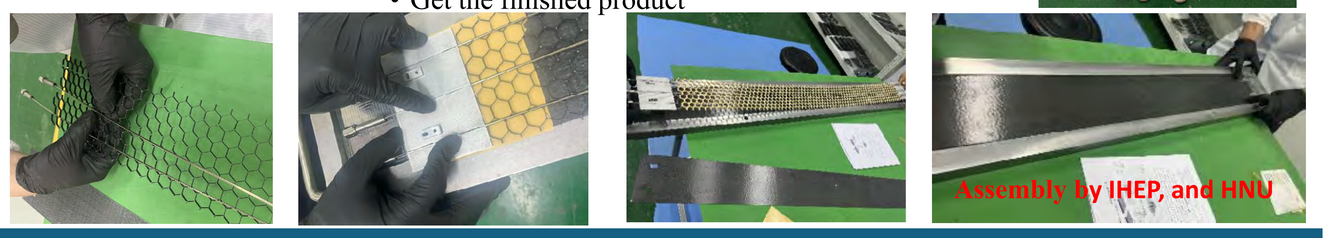


UP bare stave

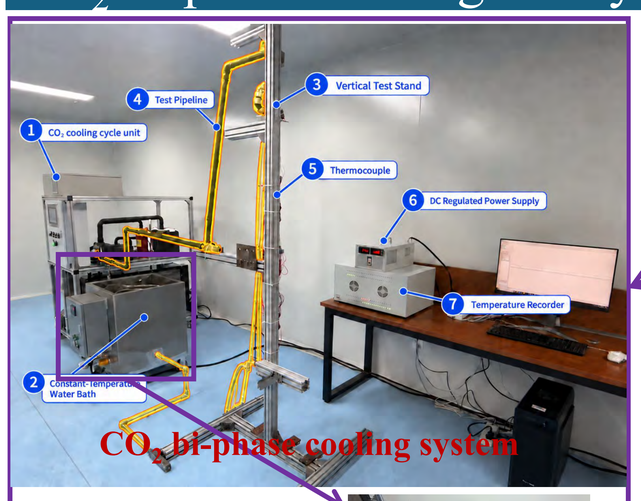
First **full-size bare stave prototype** from manufacturer

- Two CF facing + CF comb + 3x Ti tubes + 2x Al end of stave
- Ready for QA test + thermal/mechanical studies …
- Place the titanium tube into the carbon fiber comb.
- Fix the aluminum plates at both ends.
- Place the carbon fiber into the Jig
- High-temperature and high-pressure curing
- Get the finished product





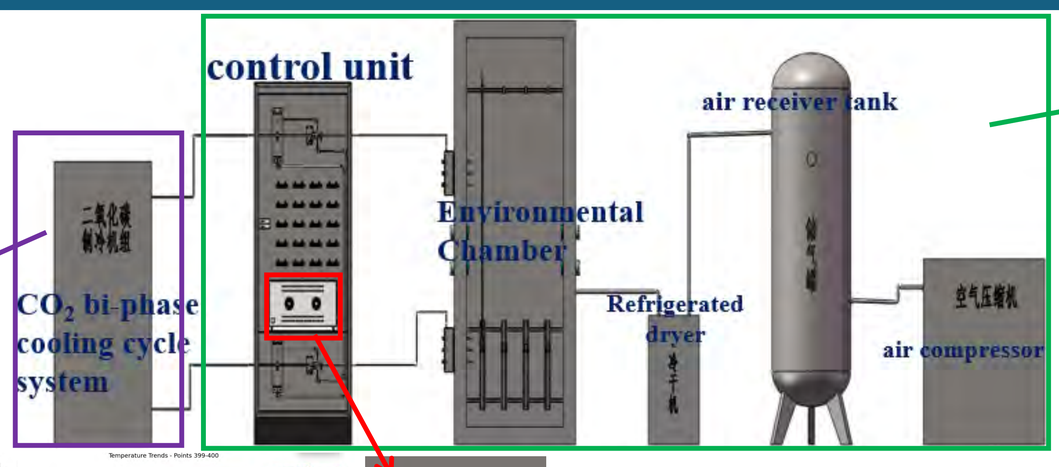
CO_2 bi-phase cooling test system

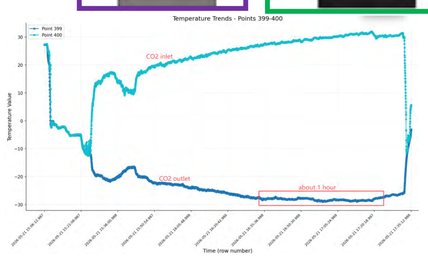


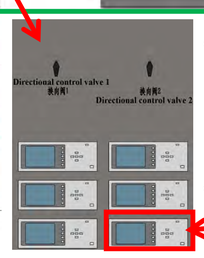
- Constant temperature water bath ensures that the thermal load of the entire loop remains constant.



Constant-Temperature Water Bath





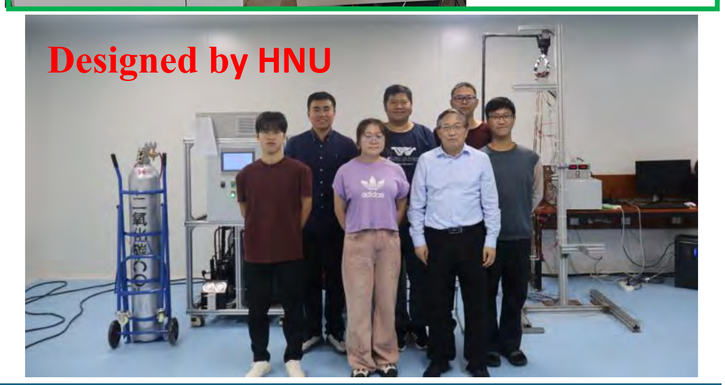


- **Directional control:** The flow direction of the liquid carbon dioxide in one of the three titanium tubes on the carbon fiber board can be changed.
- The outside of the environmental chamber is connected to a **temperature recorder**

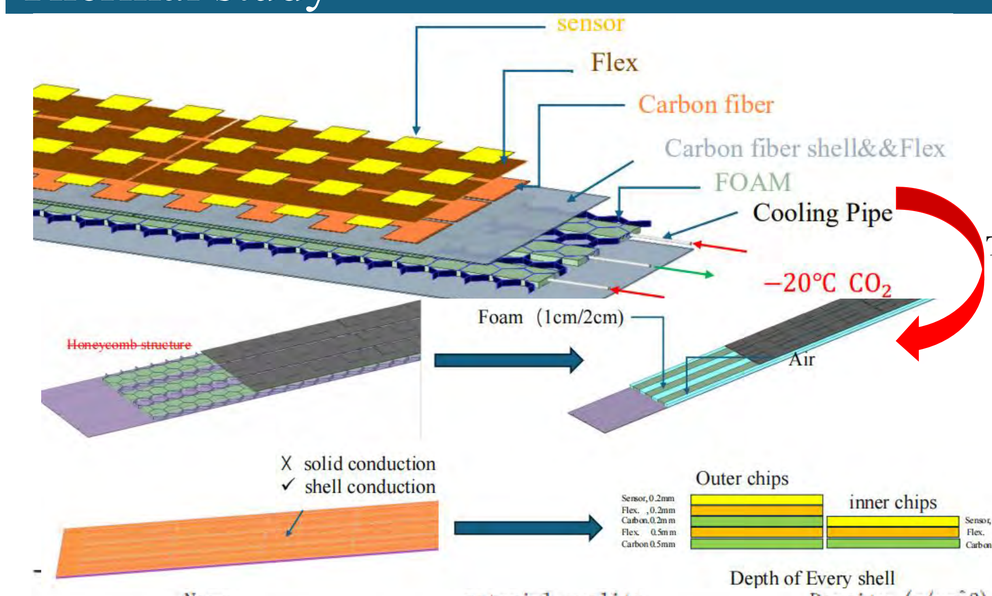
- The unit has passed the preliminary test and achieved stable output at -30°C.



- Internal space: 2.5m* 0.8m* 0.8m (4 staves together)
- Temperatures: -30°C to 40°C
- Humidity: 10% to 80% RH.

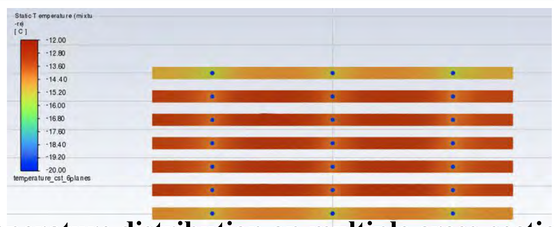


Thermal study

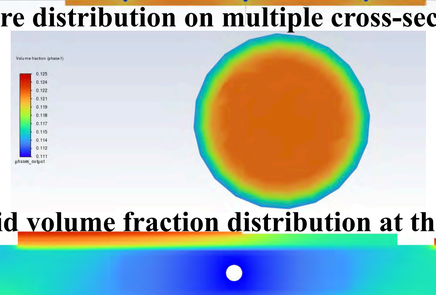


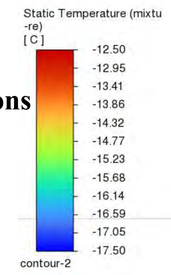
Name	material quality	Density (g/cm^3)	specific heat(J/Kg K)	Thermal conductivity(W/mK) W/mK
Carbon fiber	carbon fiber plate	1.43	1130	105(z)
Support	foam	0.56	710	55
Flex	polyimide	1.42	1000	0.4
Sensor	silicon	2.33	703	149
Cooling pipe	titanium	4.43	526	6.7

Name	Density(g/cm^3)	specific heat(J/Kg K)	Thermal conductivity(W/mK)	Viscosity(kg/m s)	molecular weight(kg/mol)	Standard state enthalpy (J/kgmol)
Co2 (liquid)	0.9183	2446	0.109	9.657e-05	44	0
Co2 (Gas)	0.103	1828	0.021	1.575e-05	44	1.67e+07

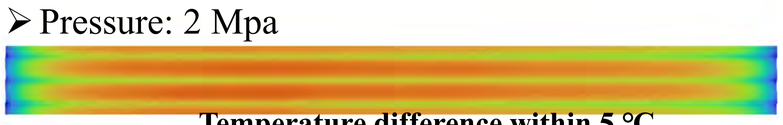


Model simplify

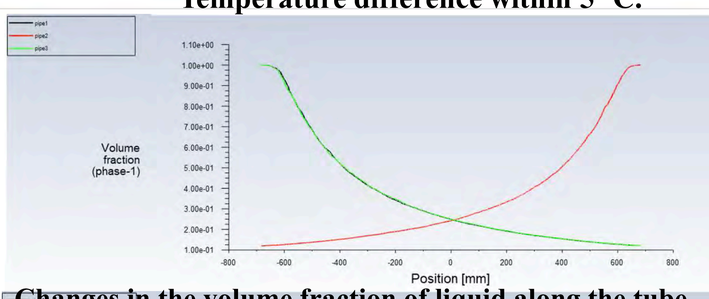




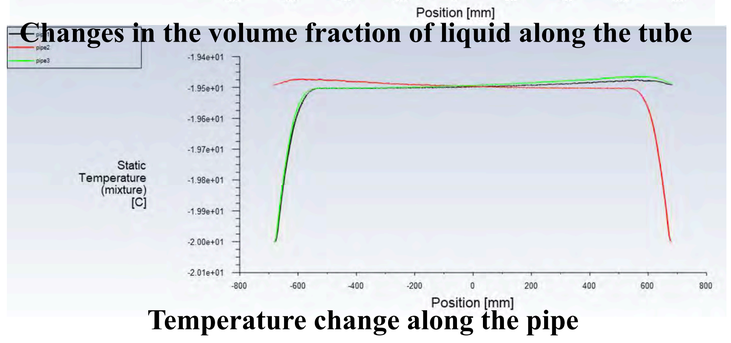
- **Power 2400W, flow rate 1.5g/s, sponge width 2cm**
  - Chips thermal power: 200 mW/cm²
  - flex power: 40 mW/cm²
  - UP box temp: 26.8 ℃
  - CO_2 input temp: -20℃,
  - Pressure: 2 Mpa



Temperature difference within 5 ℃.



Changes in the volume fraction of liquid along the tube



Temperature change along the pipe

Conclusions

- A relatively mature cooling system has been built (designed by Hunan University).
- Mechanical prototype assembly and bare stave assembly have been completed.
- Thermal simulation test on the structure of carbon fiber honeycomb for bare stave.
- Simulation result: the temperature difference within 5 ℃.

Next

- **Cooling experiment:**
  - Three titanium tubes with heating films attached are added to the test thermal load to test whether there is uneven liquid distribution in the pipeline.
- **Temperature Uniformity Test**
  - Test Uniformity on a Single Module and the Entire Stave.
  - Test uniformity under different flow directions of liquid carbon dioxide in the titanium tube.

