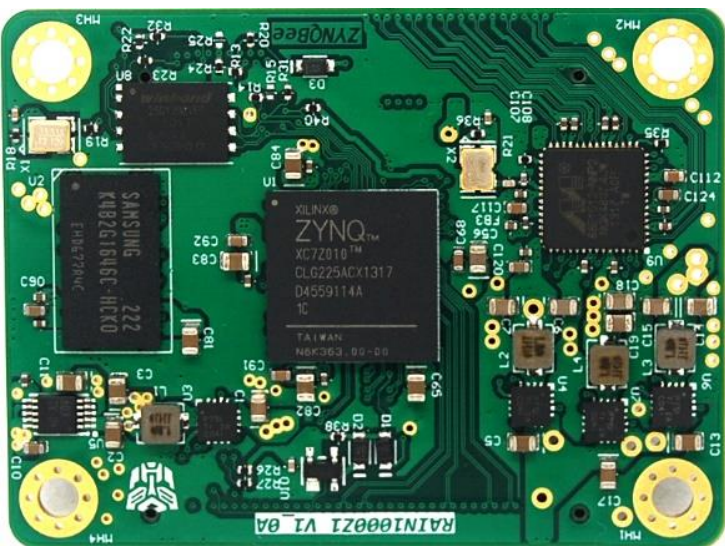




# 基于ZYNQ的 千兆以太网接口读出模块 ZYNQBee的研制



NSCAL  
Tsinghua University

NED2014, 兰州, 8月14日

第十七届全国核电子学与核探测技术学术年会

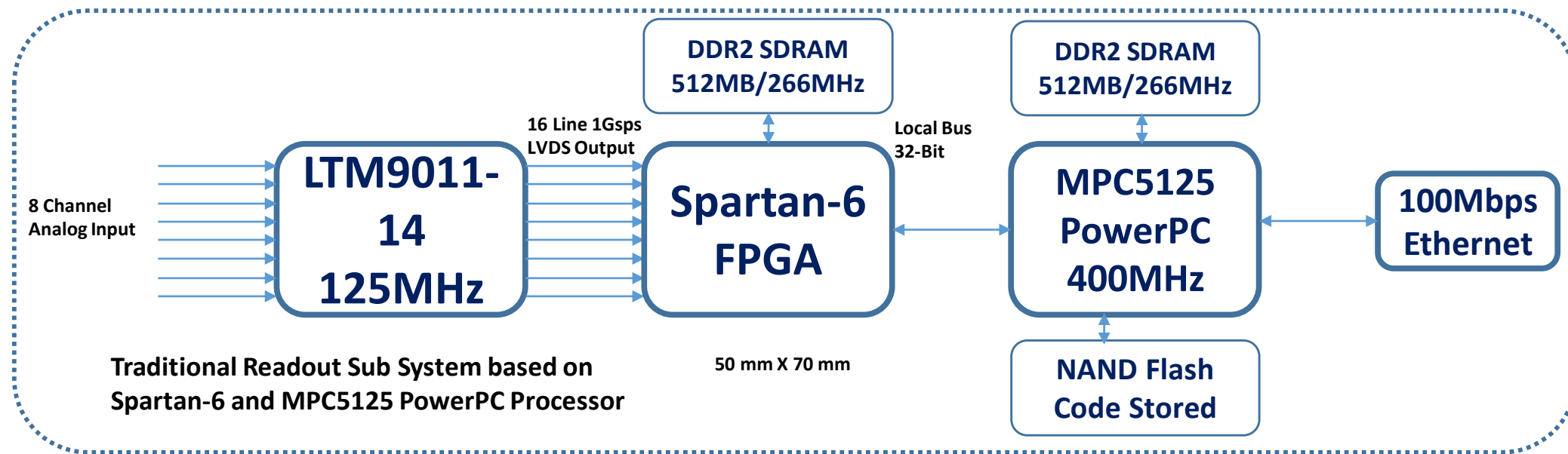
清华大学 工程物理系

薛涛, 龚光华, 曾鸣, 宫辉, 李荐民



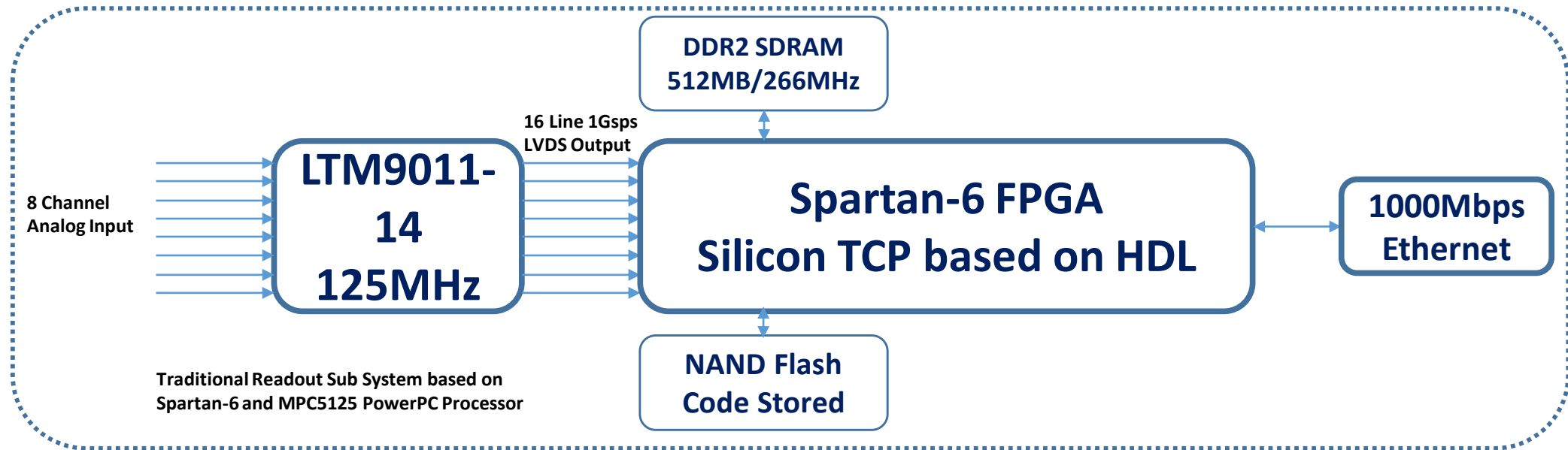
中国锦屏地下实验室  
China Jinping Underground Laboratory

# 传统读出电子学的架构



- 传统上读出电子学使用FPGA+MPU的架构，FPGA处理与FADC等前端高速模拟数字转换电路的接口以及高速数据的缓存；而MPU处理以太网等高速网络以及慢控制接口的实现，通过数据总线（Local Bus，PCI Bus等）与FPGA接口并且从FPGA获取数据，通过以太网发送数据到PC阵列。
- FPGA+MPU架构从之前的VME板卡以及到后来的专用板卡，一直是数据读出系统的典型结构。
- FPGA+MPU的优点是系统灵活，开发简单，也可以分成单独的VHDL硬件语言设计和基于嵌入式Linux的C语言设计以及Socket TCP/IP编程，有利于开发人员分别开发和研制。
- FPGA+MPU的缺点在于系统占用PCB面积较大，功耗较大，一般要分别使用2家以上芯片厂家的芯片来使用，FPGA与MPU之间的数据带宽也堪忧，读出系统的性能越来越受限于两者之间的带宽限制。

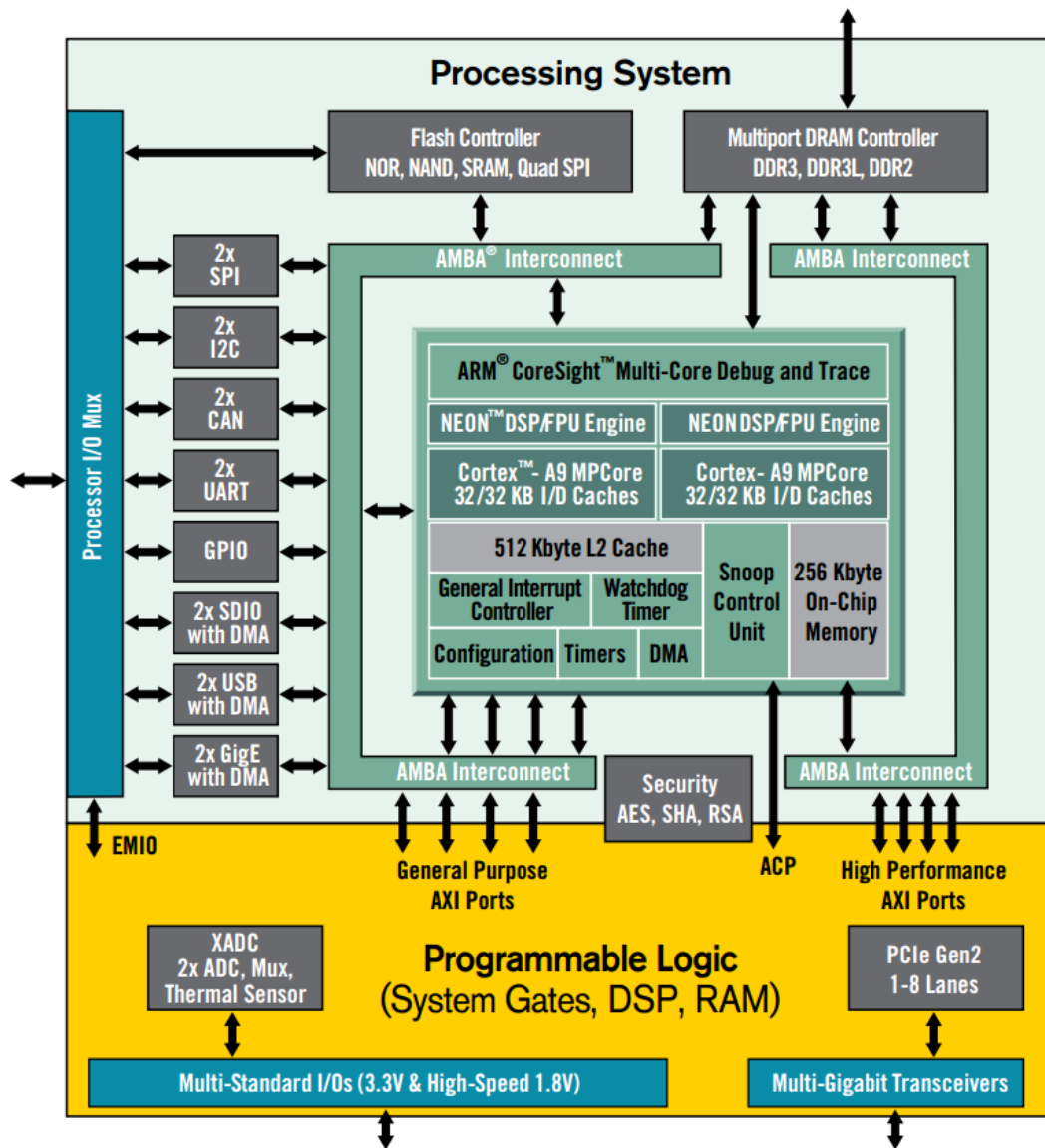
# 读出电子学的转变



- **FPGA**成本的降低以及性能的提高，很多精通VHDL设计以及TCP协议的科研开发人员开始使用单独的**FPGA**芯片来完成模拟到数字转换芯片的接口以及数据缓存和软核实现TCP协议，直接发送数据到以太网，比如使用在SuperK的SiTCP。
- **FPGA**单芯片架构的优势在于硬件系统的简化和传输速率的大幅提高，一般来讲在**1000Mbps**物理带宽的线路上可以达到**950Mbps**的数据带宽。
- **FPGA**单芯片架构的劣势在于TCP协议部分VHDL代码的复杂性，大多数学生和研究人员并不具备自己开发和维护基于VHDL代码的TCP协议的能力，商业的需要付费，并且属于黑盒子，系统的灵活性受到很大限制。系统易用性相比较基于传统架构下嵌入式Linux系统中的TCP Socket编程还有差距。

# Hardware, Software, and I/O Programmable SoC

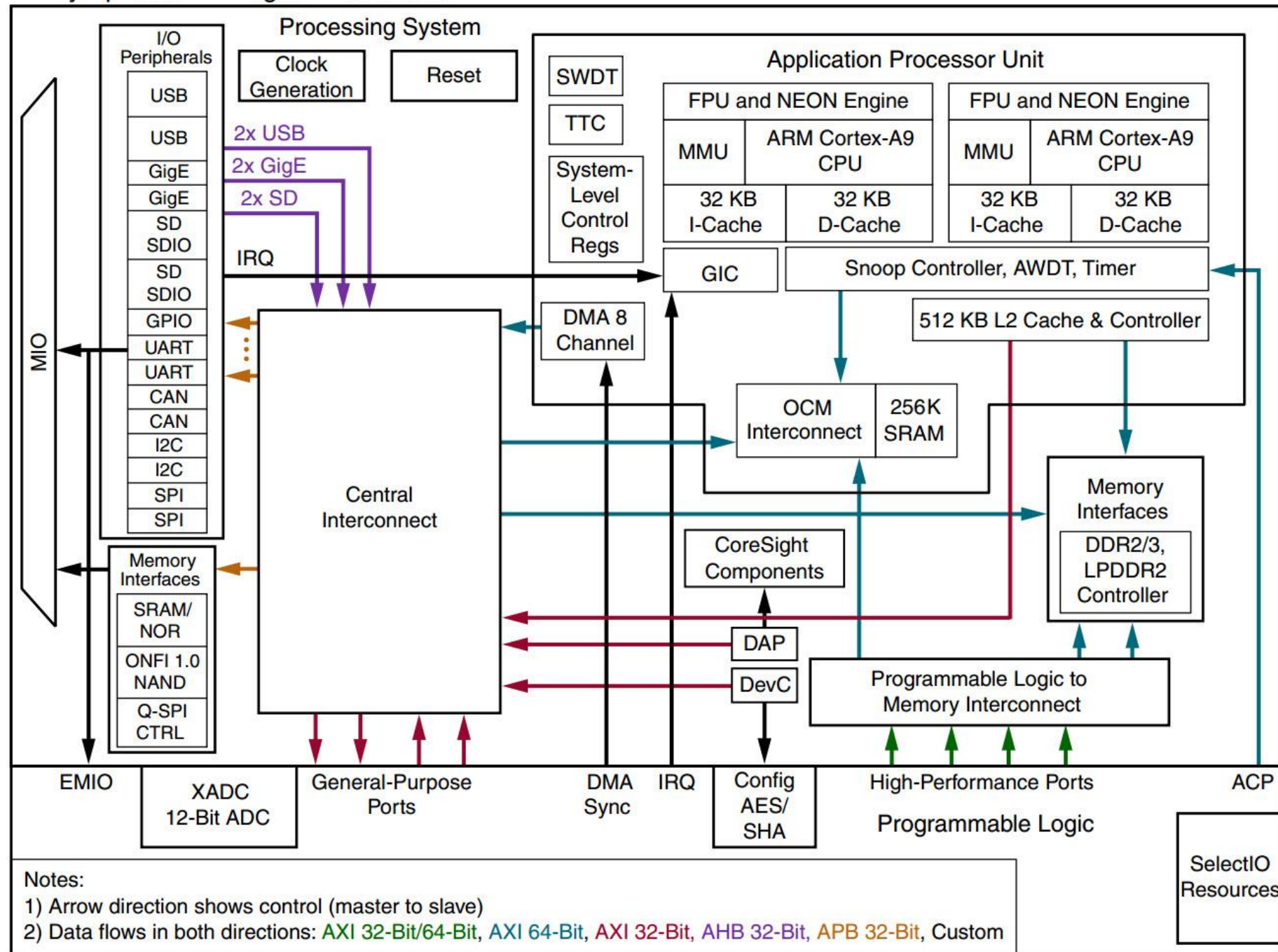
# ZYNQ系列 FPGA+ARM架构



- 28nm工艺制造，功耗相对于之前的Spartan-6以及Virtex-6或者Virtex-4Pro（内含PowerPC 405的MPU内核）有了极大降低。
- 7系列FPGA加上双核最高1GHz Cortex-A9 ARM内核，以及DDR3-533的高性能能缓存接口。
- 极其丰富和高性能高带宽的PS（Processor System）与PL（Programmable Logic）之间的互联，包括2路32位AXI从设备接口，2路32位AXI主设备接口，4路64位可配置带1KB缓存的高速AXI从设备接口以及1路64位AXI ACP接口。
- 非常小的封装形式，最小封装为CLG225封装，球间距0.8mm，外形尺寸为13mmX13mm，非常适合紧凑型应用的某些场合的板卡和模块。
- 丰富的外围接口，双千兆网络接口，USB，SD卡等接口，可以运行嵌入式Linux以及uCOS等RTOS，并且Xilinx提供了一体化的开发应用环境Vivado以及wiki来支持开源开发。



# XA Zynq-7000 All Programmable SoC



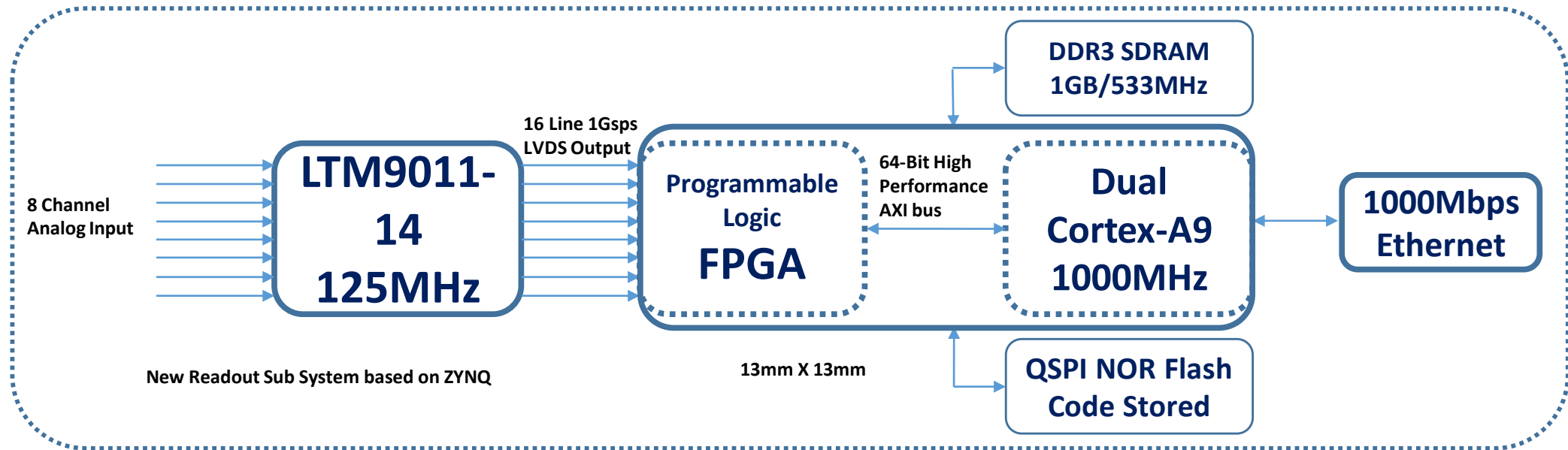
# ZYNQ系列FPGA+ARM架构

Zynq®-7000 All Programmable SoC															
Device Name	Z-7010		Z-7015		Z-7020		Z-7030			Z-7045			Z-7100		
Part Number	XC7Z010		XC7Z015		XC7Z020		XC7Z030			XC7Z045			XC7Z100		
Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™														
Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor														
Maximum Frequency	866 MHz						Up to 1 GHz <sup>(1)</sup>								
L1 Cache	32 KB Instruction, 32 KB Data per processor														
L2 Cache	512 KB														
On-Chip Memory	256 KB														
External Memory Support <sup>(2)</sup>	DDR3, DDR3L, DDR2, LPDDR2														
External Static Memory Support <sup>(2)</sup>	2x Quad-SPI, NAND, NOR														
DMA Channels	8 (4 dedicated to Programmable Logic)														
Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO														
Peripherals w/ built-in DMA <sup>(2)</sup>	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO														
Security <sup>(3)</sup>	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot														
Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory, AXI 64b ACP, 16 Interrupts														
Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA		Artix-7 FPGA		Artix-7 FPGA		Kintex®-7 FPGA			Kintex-7 FPGA			Kintex-7 FPGA		
Programmable Logic Cells (Approximate ASIC Gates <sup>(4)</sup> )	28K Logic Cells (~430K)		74K Logic Cells (~1.1M)		85K Logic Cells (~1.3M)		125K Logic Cells (~1.9M)			350K Logic Cells (~5.2M)			444K Logic Cells (~6.6M)		
Look-Up Tables (LUTs)	17,600		46,200		53,200		78,600			218,600			277,400		
Flip-Flops	35,200		92,400		106,400		157,200			437,200			554,800		
Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)		380 KB (95)		560 KB (140)		1,060 KB (265)			2,180 KB (545)			3,020 KB (755)		
Programmable DSP Slices (18x25 MACCs)	80		160		220		400			900			2,020		
Peak DSP Performance (Symmetric FIR)	100 GMACs		200 GMACs		276 GMACs		593 GMACs			1,334 GMACs			2,622 GMACs		
PCI Express® (Root Complex or Endpoint)	—		Gen2 x4		—		Gen2 x4			Gen2 x8			Gen2 x8		
Analog Mixed Signal (AMS) / XADC <sup>(2)</sup>	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs														
Security <sup>(3)</sup>	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration														
Commercial (0C to 85C)	-1												NA		
Extended (0C to 100C)	-2, -3												N/A		
Industrial (-40C to 100C)	-1, -2												-1, -2		
Package Type <sup>(5)</sup>	CLG225 <sup>(1)</sup>	CLG400	CLG485 <sup>(7)</sup>		CLG400	CLG484	SBG485 <sup>(7)</sup>	FBG484	FBG676	FFG676	FBG676	FFG676	FFG900	FFG900	FFG1156
Size (mm)	13x13	17x17	19x19		17x17	19x19	19x19	23x23	27x27	27x27	27x27	27x27	31x31	31x31	35x35
Pitch (mm)	0.8	0.8	0.8		0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Processing System User I/Os (excludes DDR dedicated I/Os) <sup>(6)</sup>	32	54	54		54	54	54	54	54	54	54	54	54	54	54
Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	150		125	200	50	100	100	100	100	100	212	212	250
Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	—	—	—		—	—	100	63	150	150	150	150	150	150	150
Serial Transceivers	—	—	4		—	—	4	4	4	4	8	8	16	16	16
Maximum Transceiver Speed (Speed Grade Dependent)	N/A	N/A	6.25 Gb/s		N/A	N/A	6.6 Gb/s	6.6 Gb/s	6.6 Gb/s	12.5 Gb/s	6.6 Gb/s	12.5 Gb/s	12.5 Gb/s	10.3125 Gb/s	10.3125 Gb/s





# 基于Zynq的读出电子学的架构

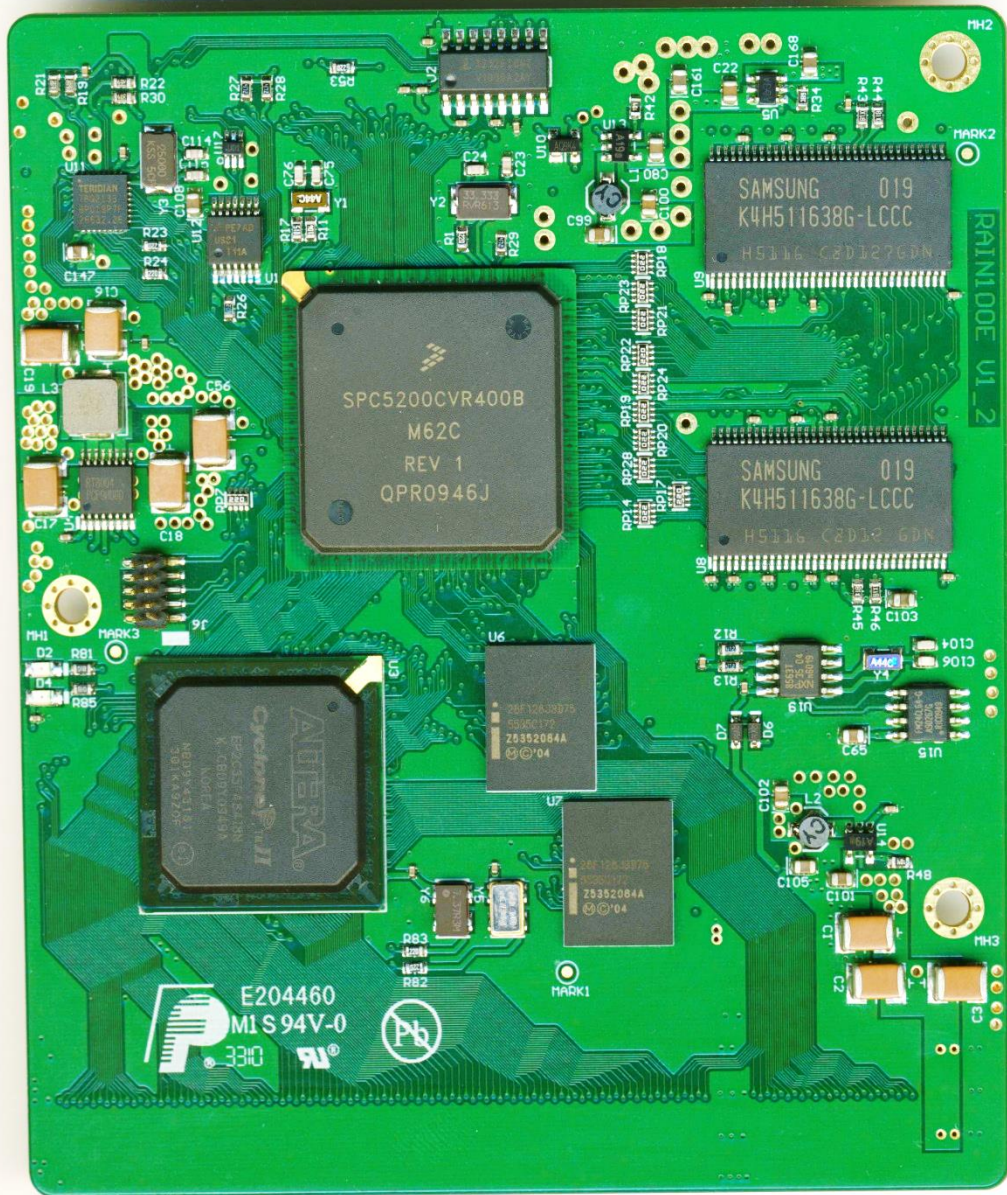


- 基于Zynq架构的新型读出电子学的设计大大简化了传统FPGA+MPU架构读出电子学的设计，系统在单片上既有FPGA，又包含了双核的高性能ARM MPU。
- 相对较低的功耗和较小的尺寸，非常具有灵活性，对电源盒散热系统的设计业带来很大的好处，在紧凑型系统中应用广泛。
- 533MHz的DDR3接口SDRAM能为系统提供足够带宽和容量的缓存，因为DDR的原因，实际的时钟沿是1066MHz，时钟间隔达到了1ns，对于PCB布线和阻抗匹配设计有了新的要求，当然，随着整个FPGA和MPU的发展，这个趋势是不可避免的。
- 丰富的外围接口，比如双千兆网，USB以及SD卡接口，QSPI的NORFLASH等。

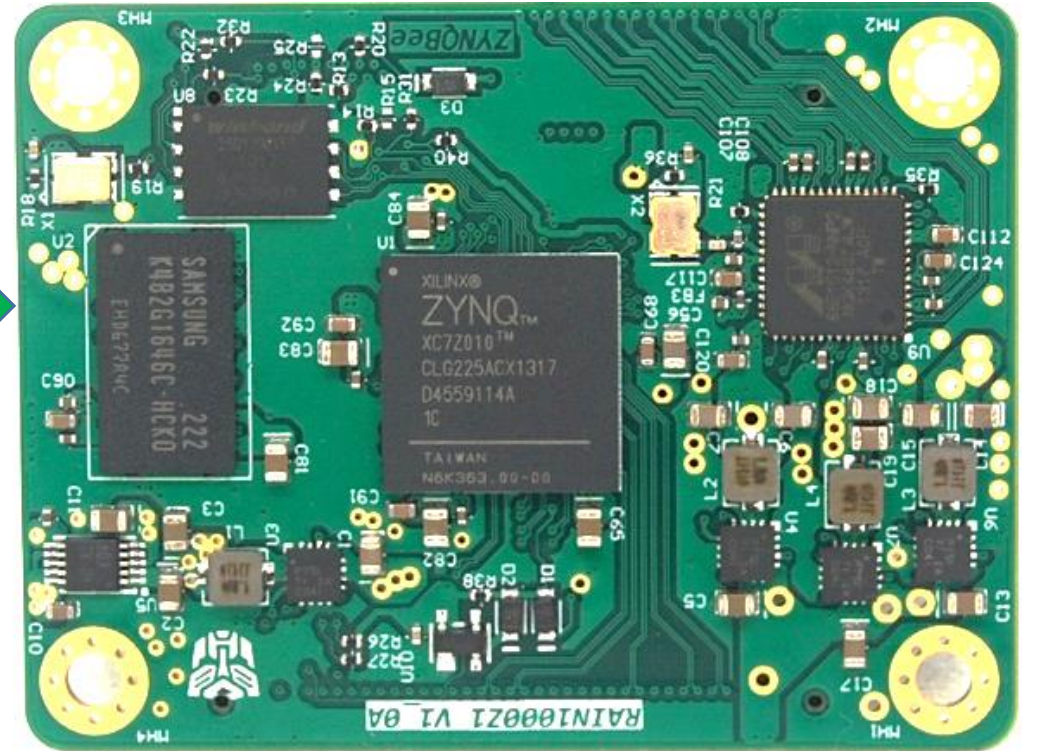


# 变革

92mmX107mm



42mmX56mm



# 变革

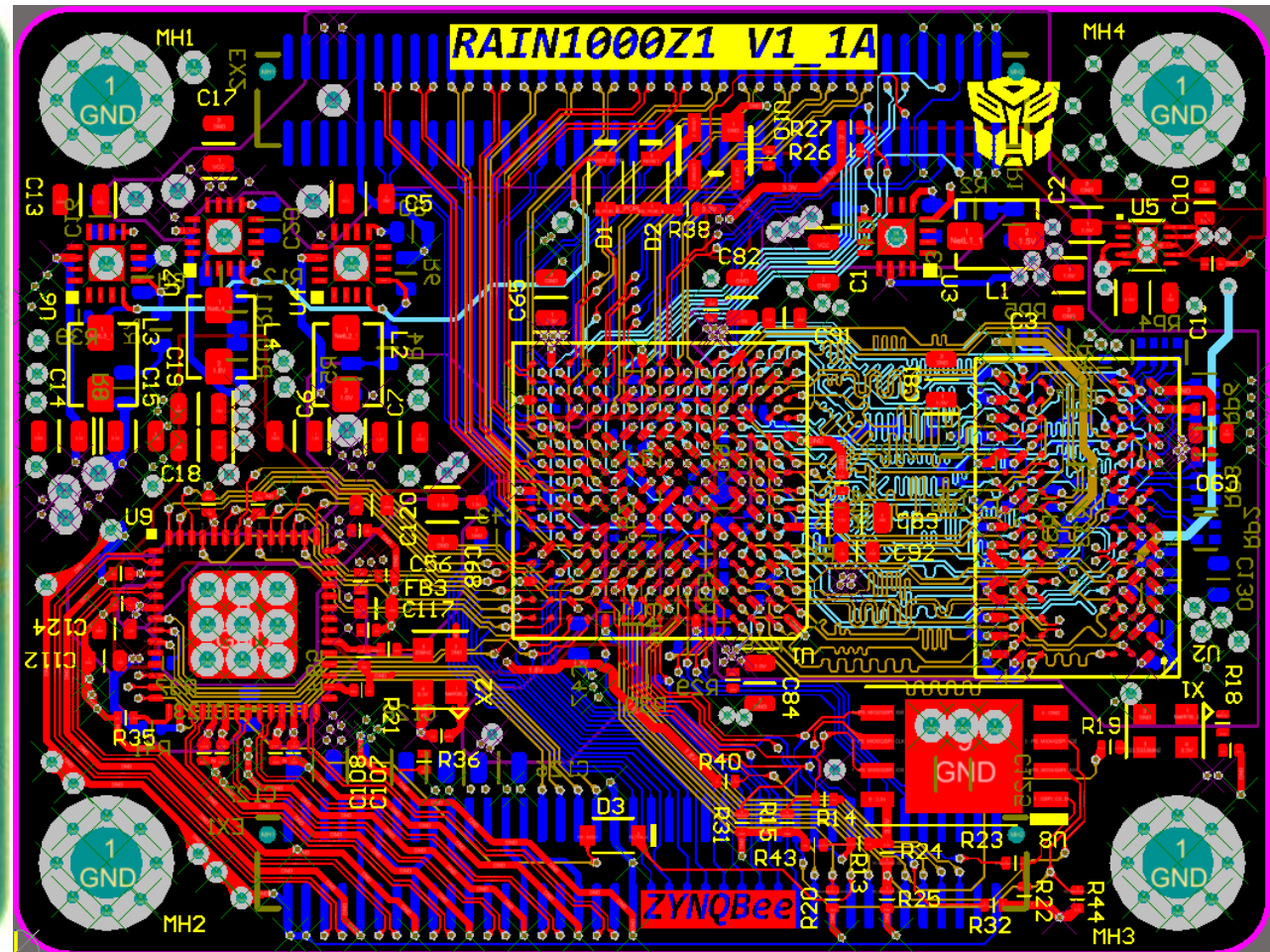
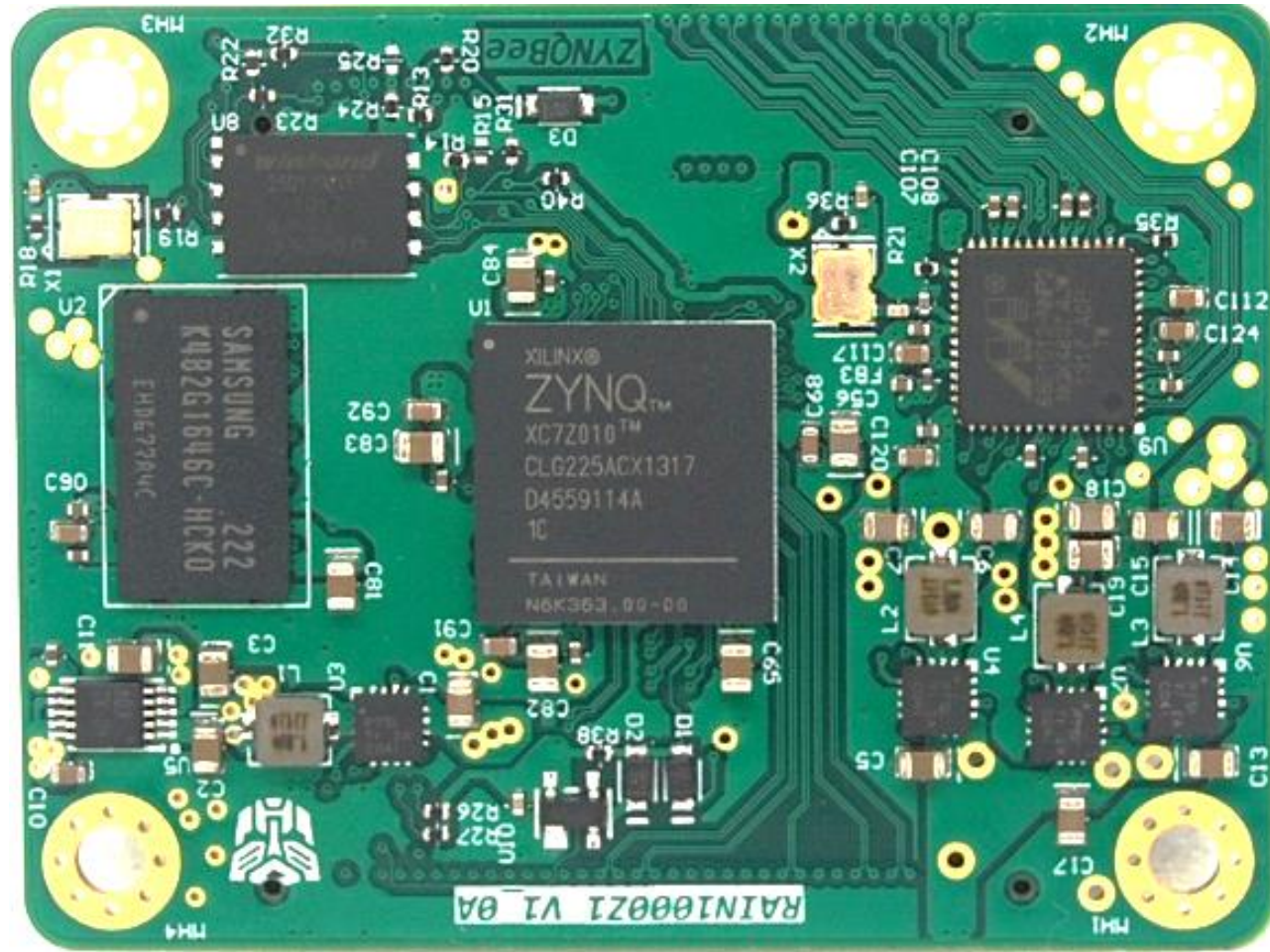
- 92mmX107mm
- MPC5200B，运行在400MHz，带有100Mbps以太网接口，DDR SDRAM接口是266MHz
- FPGA使用Atlera Cyclone EP2C35
- FPGA与MPU之间打数据接口是33MHz，32bit的PCI接口
- 运行嵌入式Linux，可以支持RT



- 42mmX56mm
- Zynq系列的XC7Z010，运行在666MHz，带有1路1000Mbps以太网接口，DDR3 SDRAM运行在533MHz
- FPGA是7系列Kintex架构，支持LVDS达到1250Mbps DDR接口，FPGA逻辑容量相当于Spartan-6的XSL25
- FPGA与MPU之间，也就是PS与PL之间有高速150MHz，64bit带1KB缓存的极其高性能接口
- 运行嵌入式Linux，可以支持RT，双核之中，第二个核心可以运行uCOS等RTOS来更好的支持RT



# ZYNQBee的读出电子学模块的设计



- 基于Zynq系列的最小尺寸，容量和架构的XC7Z010 CLG225封装的芯片，我们设计了一款读出电子学模块来用于核电子学研究的数据读出，主要是为配合研究生做ASIC测试，各种探测器FADC数据的读出等的研究工作。
- 系统包含了ZYNQ处理器以及DDR3 SDRAM，QSPI的128Mbits NORFLASH，千兆以太网PHY采用Marvell的88E1512，可以支持CAT5e的非屏蔽双绞线铜缆或者光纤。



# ZYNQBee的读出电子学模块的设计挑战-阻抗匹配

Saturn PCB Design, Inc. - PCB Toolkit V6.31 - www.saturnpcb.com

File Program Function Tools Help | Contact Saturn PCB Design, Inc.

Fusing Current Embedded Resistors PPM Calculator Crosstalk Calculator Wavelength Calculator  
Via Properties Conductor Properties Bandwidth & Max Conductor Length Differential Pairs Padstack Calculator Mechanical Properties  
Conductor Spacing Conductor Impedance Conversion Data Planar Inductors PDN Impedance

Conductor Impedance  
Conductor Width (W)  mils  
Conductor Height (H)  mils  
W/H = 1.000  
T/H = 0.087

Formula Restrictions:  
 $0.1 < W/H < 2.0$   
 $T/H < 0.25$

Options

Base Copper Weight  
 0.25oz  
 0.5oz  
 1oz  
 1.5oz  
 2oz  
 2.5oz  
 3oz  
 4oz  
 5oz

Units  
 Imperial  
 Metric

Substrate Material Selection  
FR-4 STD  
Er

Temp Rise   
Temp in (°F)

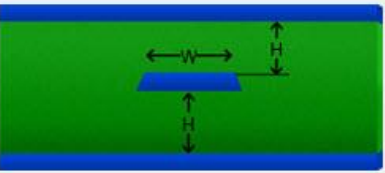
Ambient Temperature   
Temp in (°F)

Plating Thickness  
 Bare PCB  
 0.5oz  
 1oz  
 1.5oz  
 2oz  
 2.5oz  
 3oz



Passive Circuits  
 Microstrip  
 Microstrip Embed  
 Stripline  
 Stripline Asym  
 Coplanar Wave

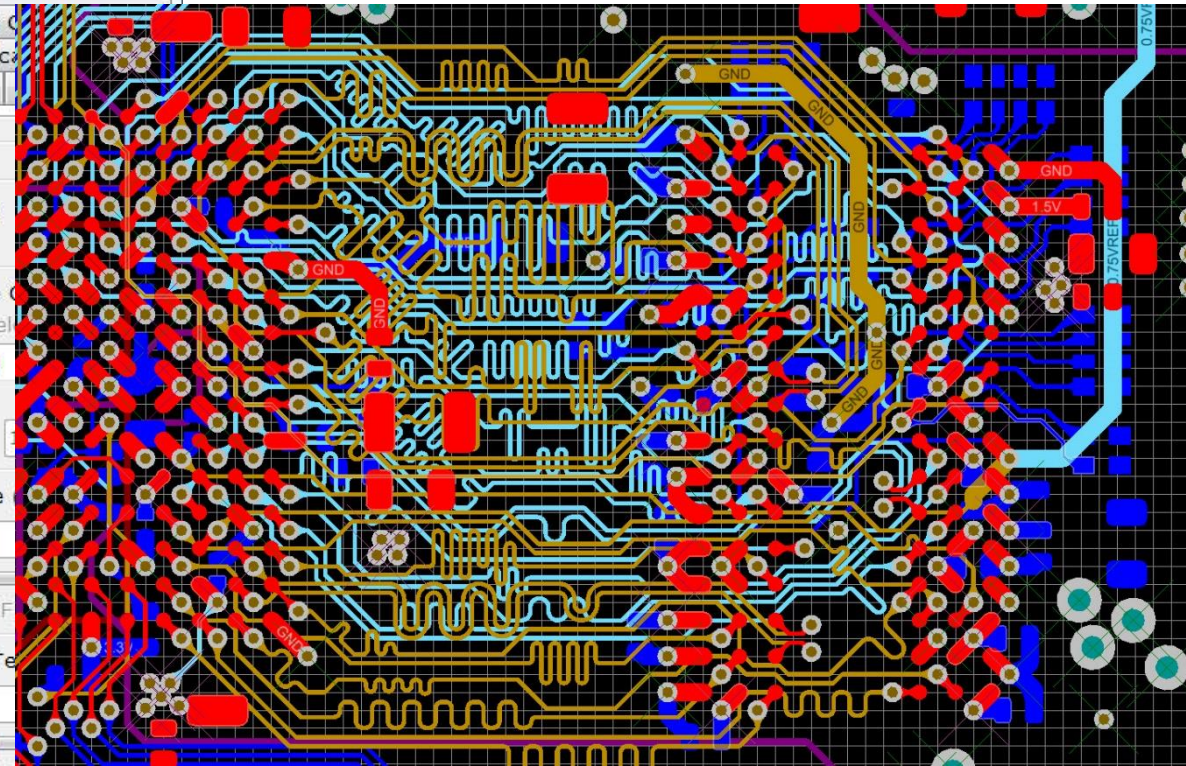
Information  
Total Copper Thickness 0.35 mils  
VIA Thermal Resistance N/A  
Conductor Temperature  
Temp in (°C) = N/A  
Temp in (°F) = N/A

Zo   
Lo   
Co   
Tpd



**SATURN**  
PCB DESIGN, INC.  
Turnkey Electronic Engineering Solutions

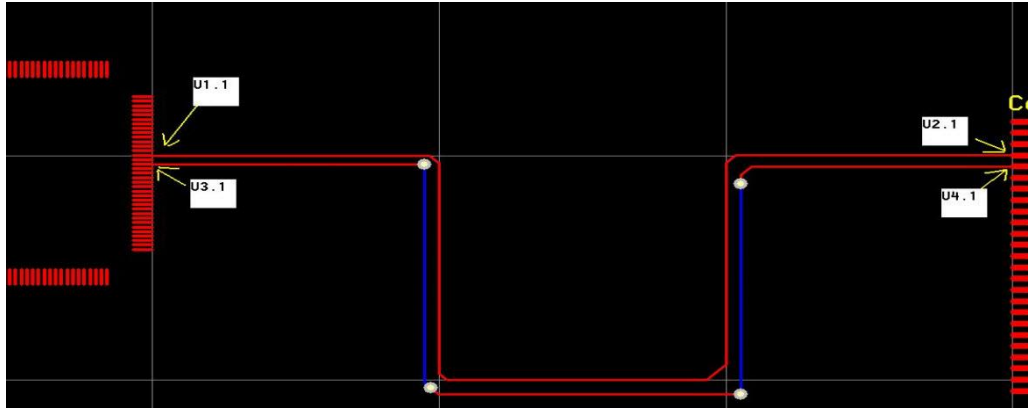
 



- Zynq的DDR3 SDRAM接口可以达到533MHz的速度，也就是时钟沿1ns就会有一次数据变化，基于Zynq的40欧姆阻抗设计需求，需要在硬件PCB设计时注意DDR3阻抗的匹配以及同一个Lane的length match。



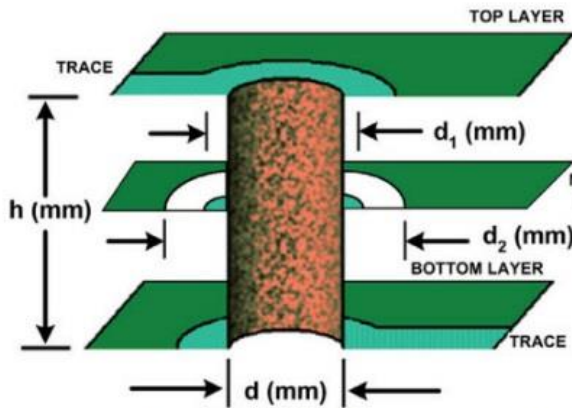
# ZYNQBee的读出电子学模块的设计挑战-等长控制



Component: Vias

Purpose: Interconnect traces on different layers

Problem: Inductance and Capacitance



$$L(nH) \approx \frac{h}{5} \left[ 1 + \ln \left( \frac{4h}{d} \right) \right]$$

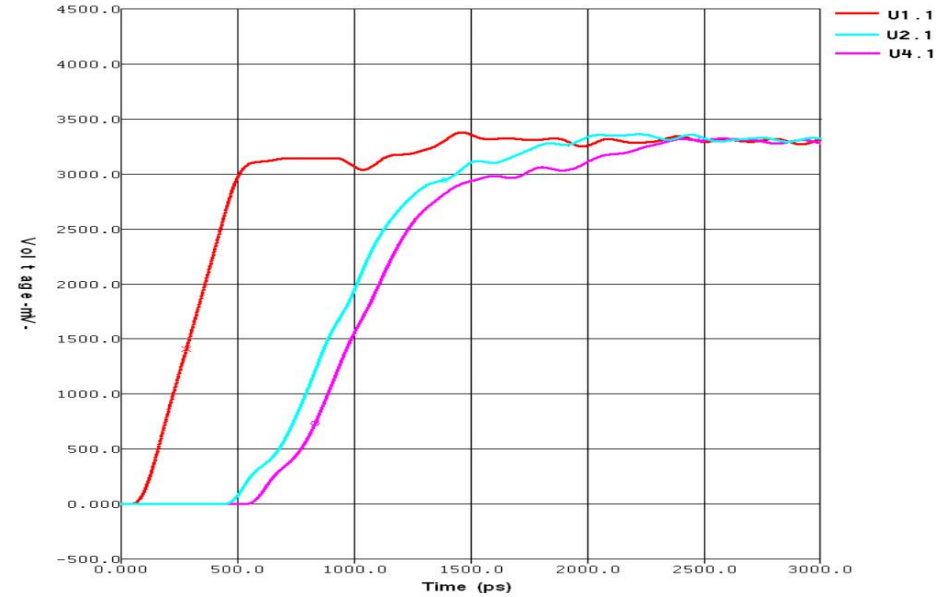
$$C(pF) \approx \frac{0.0555 \epsilon_r h d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6 \sqrt{\frac{L(nH)}{C(pF)}} \quad T_p(ps/cm) = 31.6 \sqrt{L(nH)C(pF)}$$

0.4mm (0.0157") via with 1.6mm (0.063") thick PCB has ~ 1.2nH

1.6mm (0.063") Clearance hole around 0.8mm (0.031") pad on FR-4 has ~ 0.4pF

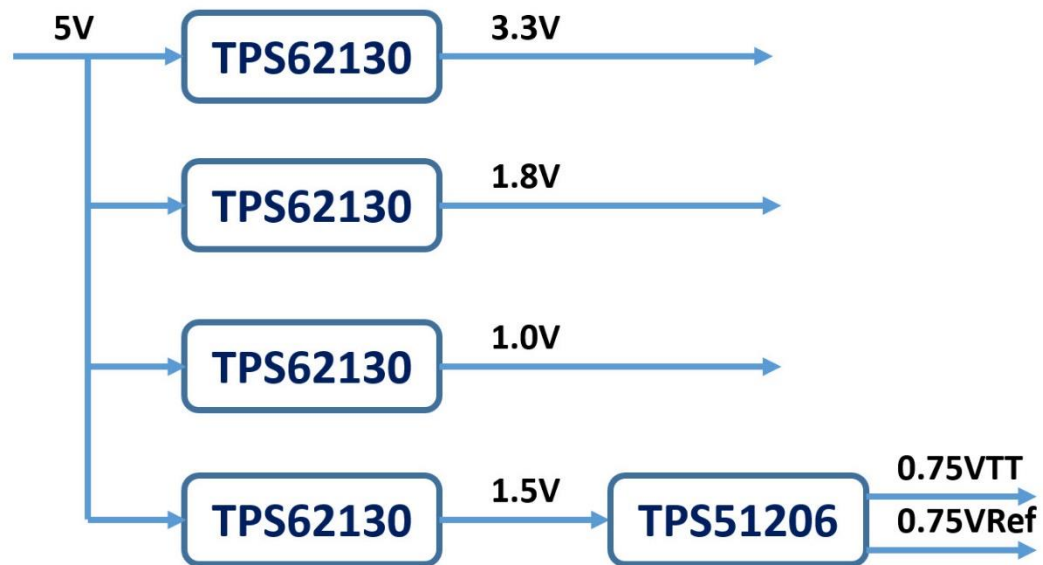
$\epsilon_r$  = PCB material permeability (FR-4 ~ 4.5)



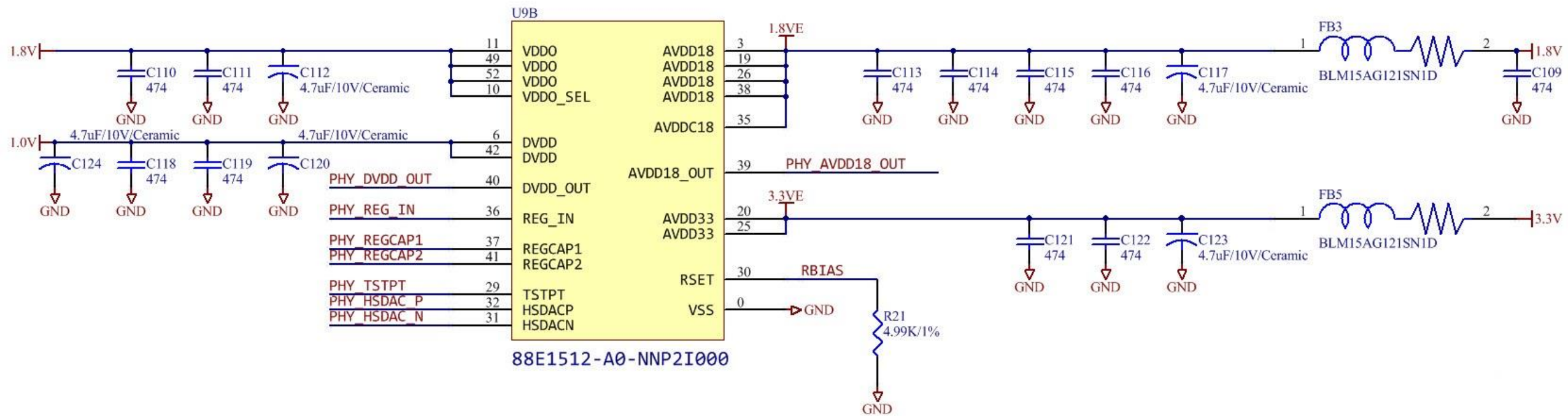
- 200ps delay added.
- 同一个Lane尽量在同一个midlayer



# ZYNQBee的读出电子学模块的设计挑战-电源设计

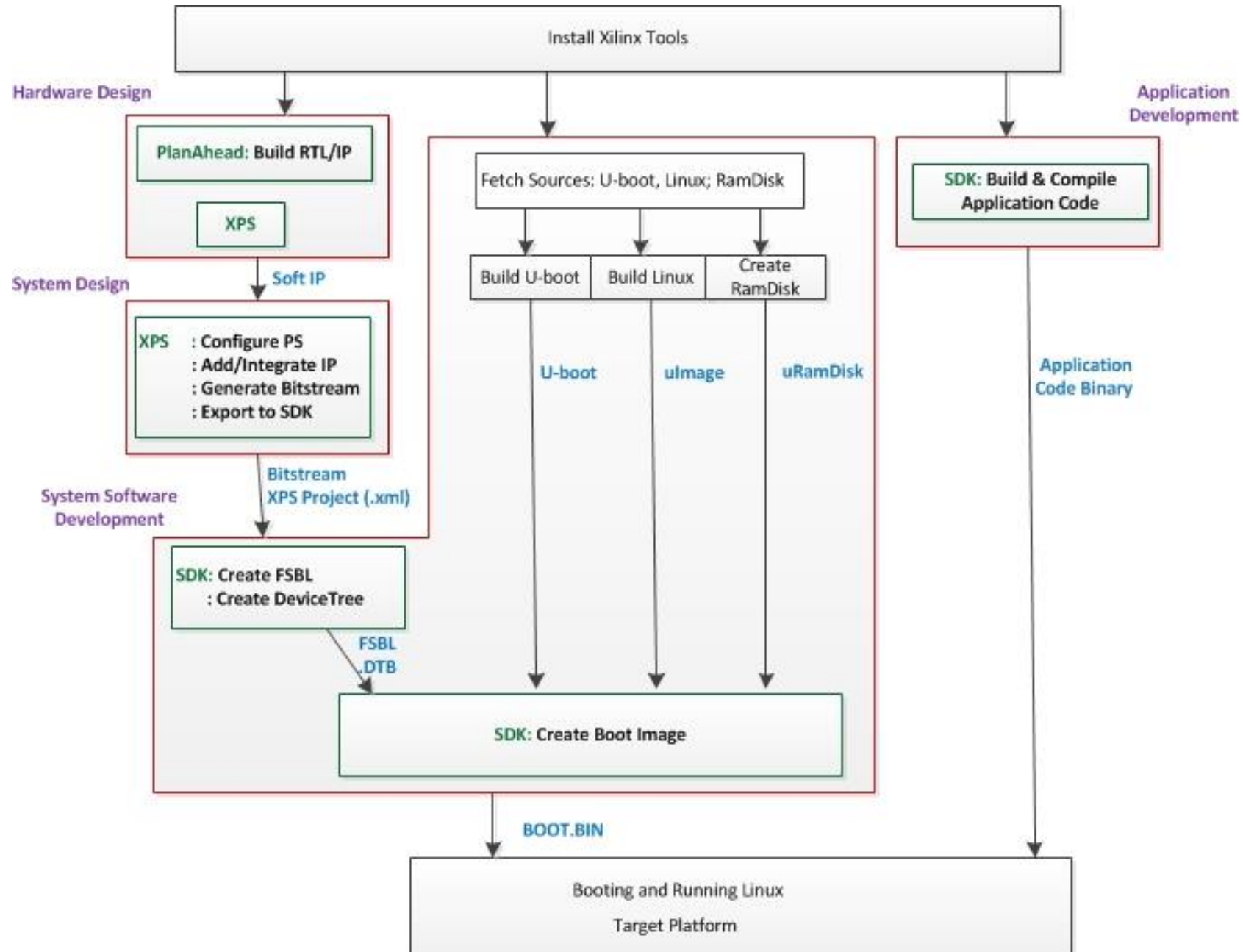


- 使用TI公司的QFN16超小封装的TPS62130配合Vishay公司的高性能超小封装金属膜一体成型IHL系列电感，能够提供持续3A的电流，并且达到90%以上的效率。
- 选用Marvell公司的以太网PHY 88E1512，优点在于这颗PHY的电源电压和Zynq保持一致，简化了电源设计，并且这颗PHY能够提供铜缆和光纤两种物理介质接口。





# ZYNQBee的读出电子学模块的软件设计



# ZYNQBee的读出电子学模块的软件设计

Re-customize IP

ZYNQ7 Processing System (5.3)

Documentation Presets IP Location Import XPS Settings

Page Navigator << DDR Configuration Summary Report

Zynq Block Design  
PS-PL Configuration  
Peripheral I/O Pins  
MIO Configuration  
Clock Configuration  
**DDR Configuration**  
SMC Timing Calculation  
Interrupts

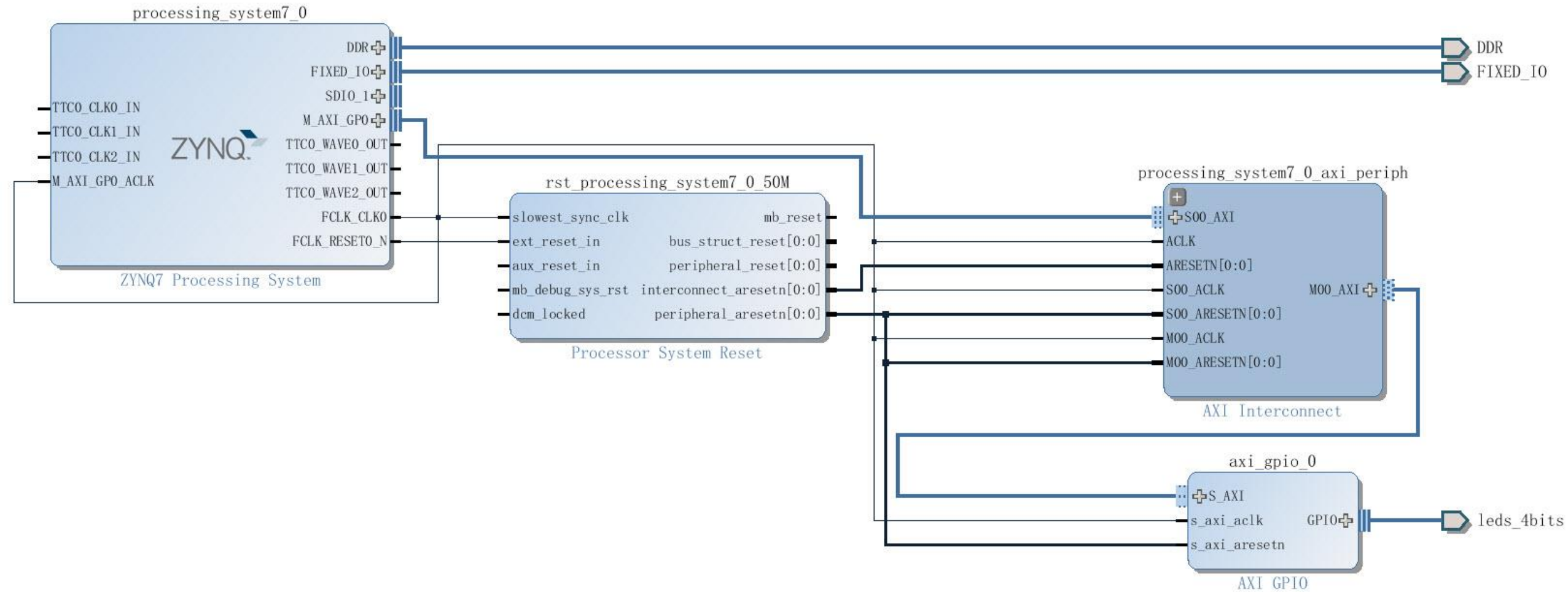
Enable DDR

Search: Q-

Name	Select	Description
<b>DDR Controller Configuration</b>		
Memory Type	DDR 3	Type of memory interface. Refer to UG585 Zynq Technical Reference Manual (TRM) for a detailed list of supported memory controllers.
Memory Part	MI41J128M16 HA-15E	Memory component part number. For unlisted parts choose "Custom". This will enable user input in the "Memory Part Configuration" section.
Effective DRAM Bus Width	32 Bit	Data width of DDR interface, not including ECC data width. Refer to UG585 for a detailed list of supported DDR data widths.
ECC	Disabled	Enables error correction code support. ECC is supported only for an effective data width of 16 bits.
Burst Length	8	Minimum number of data beats the controller should use when communicating with the DDR component.
DDR	533.333313	Memory clock period. The allowed freq range is (200.000000 : 534.000000) MHz.
Internal Vref	<input checked="" type="checkbox"/>	Enables internal voltage reference source. Disable to use external Vref pins as voltage reference.
Operating Temperature (C)	Normal (0-85)	Intended operating temperature range. Controls the DDR refresh interval.
<b>Memory Part Configuration</b>		
DRAM IC Bus Width	16 Bits	Width of individual DRAM components.
DRAM Device Capacity	2048 Mbits	Storage capacity of individual DRAM components.
Speed Bin	DDR3_1066F	Speed bin of the individual DRAM components.
Bank Address Count (Bits)	3	Number of bank address pins.
Row Address Count (Bits)	14	Number of row address pins.
Col Address Count (Bits)	10	Number of column address bits.
CAS Latency (cycles)	7	Column Access Strobe (CAS) latency in memory clock cycles. It refers to the amount of time it takes for data to appear on the pins of the memory module
CAS Write Latency (cycles)	6	CAS write latency setting in memory clock cycles.
RAS to CAS Delay (cycles)	7	tRCD. Row address to column address delay time. It is the time required between the memory controller asserting a row address strobe (RAS), and then asserting the column address strobe...
Precharge Time	7	tRP. Precharge Time is the number of clock cycles needed to terminate access to an open row of memory and open access to the next row.
tRC (ns)	49.5	Row cycle time (ns)
tRASmin (ns)	36.0	Minimum number of memory clock cycles required between an Active and Precharge command
tFAW (ns)	49.5	Defines the number of activates that can be performed within a certain window of time.
<b>Training/Board Details</b>		
<b>DRAM Training</b>		
Write leveling	<input checked="" type="checkbox"/>	Enables Write Leveling calibration, which adjusts write DQS relative to the DDR clock.
Read gate	<input checked="" type="checkbox"/>	Enables Read Gate calibration, which adjusts valid RD DQS window.
Read data eye	<input checked="" type="checkbox"/>	Enables Read Data Eye calibration, which adjusts the read DQS to the center of read DQ.
<b>DQS to Clock Delay (ns)</b>		
DQS0	0.025	DQS to Clock delay [0] (ns). The DQS path delay subtracted from the clock path delay.
DQS1	0.028	DQS to Clock delay [1] (ns). The DQS path delay subtracted from the clock path delay.
DQS2	-0.009	DQS to Clock delay [2] (ns). The DQS path delay subtracted from the clock path delay.
DQS3	-0.061	DQS to Clock delay [3] (ns). The DQS path delay subtracted from the clock path delay.
<b>Board Delay (ns)</b>		
DQ[7:0]	0.41	Board delay [0] (ns). The midpoint of data (DDR_DQ, DDR_DM) trace delays averaged with the midpoint of clock (DDR_CK, DR_CK_ID) trace delays for byte lane 0.
DQ[15:8]	0.411	Board delay [1] (ns). The midpoint of data (DDR_DQ, DDR_DM) trace delays averaged with the midpoint of clock (DDR_CK, DR_CK_ID) trace delays for byte lane 1.
DQ[23:16]	0.341	Board delay [2] (ns). The midpoint of data (DDR_DQ, DDR_DM) trace delays averaged with the midpoint of clock (DDR_CK, DR_CK_ID) trace delays for byte lane 2.
DQ[31:24]	0.358	Board delay [3] (ns). The midpoint of data (DDR_DQ, DDR_DM) trace delays averaged with the midpoint of clock (DDR_CK, DR_CK_ID) trace delays for byte lane 3.
Additive Latency (ns)	0	Additive latency (ns). Increases the efficiency of the command and data bus for sustainable bandwidths

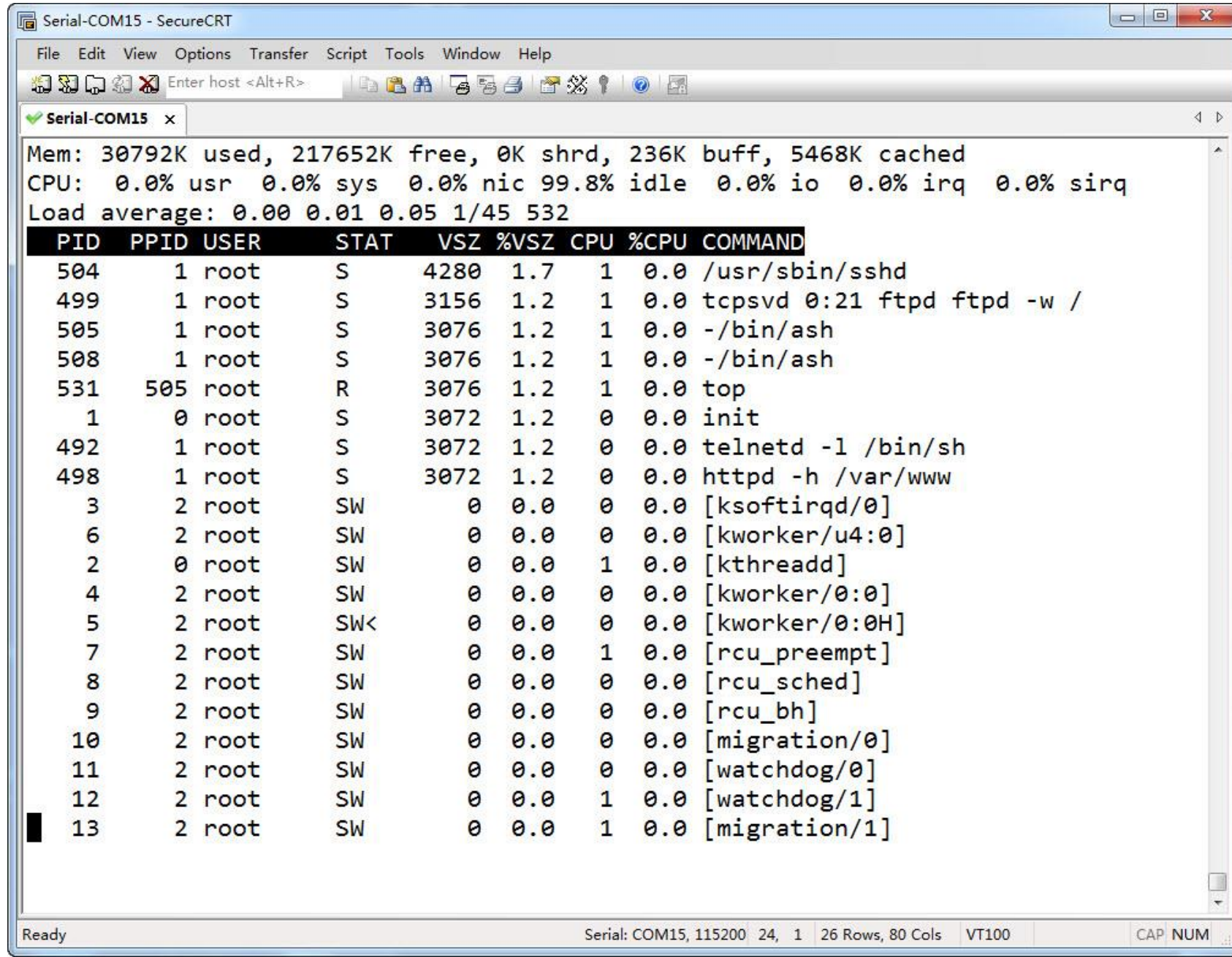
OK Cancel

# ZYNQBee的读出电子学模块的软件设计





# ZYNQBee的读出电子学模块的软件设计



Serial-COM15 - SecureCRT

File Edit View Options Transfer Script Tools Window Help

Enter host <Alt+R>

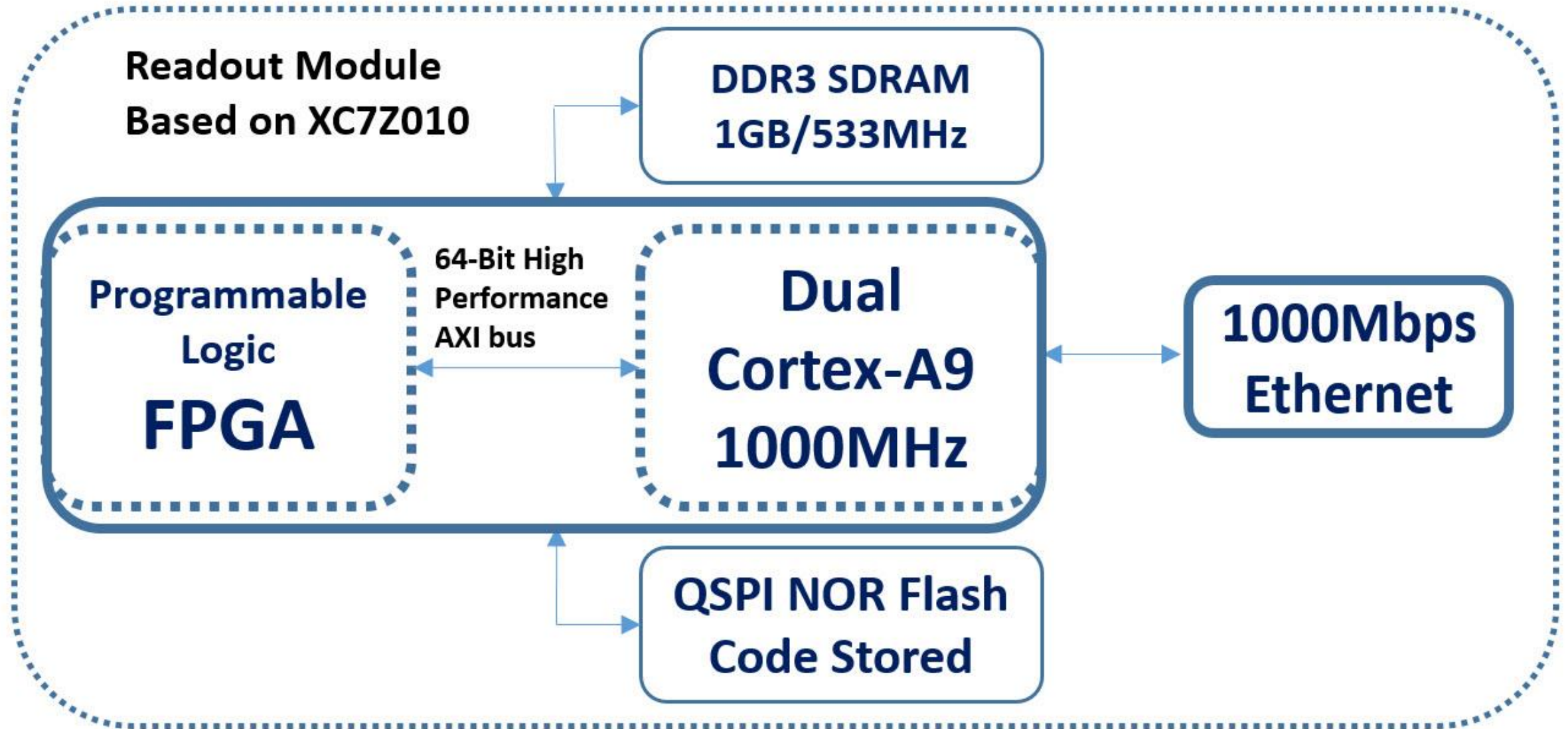
Serial-COM15 x

```
Mem: 30792K used, 217652K free, 0K shrd, 236K buff, 5468K cached
CPU:  0.0% usr  0.0% sys  0.0% nic 99.8% idle  0.0% io  0.0% irq  0.0% sirq
Load average: 0.00 0.01 0.05 1/45 532
```

PID	PPID	USER	STAT	VSZ	%VSZ	CPU	%CPU	COMMAND
504	1	root	S	4280	1.7	1	0.0	/usr/sbin/sshd
499	1	root	S	3156	1.2	1	0.0	tcpsvd 0:21 ftpd ftpd -w /
505	1	root	S	3076	1.2	1	0.0	-/bin/ash
508	1	root	S	3076	1.2	1	0.0	-/bin/ash
531	505	root	R	3076	1.2	1	0.0	top
1	0	root	S	3072	1.2	0	0.0	init
492	1	root	S	3072	1.2	0	0.0	telnetd -l /bin/sh
498	1	root	S	3072	1.2	0	0.0	httpd -h /var/www
3	2	root	SW	0	0.0	0	0.0	[ksoftirqd/0]
6	2	root	SW	0	0.0	0	0.0	[kworker/u4:0]
2	0	root	SW	0	0.0	1	0.0	[kthreadd]
4	2	root	SW	0	0.0	0	0.0	[kworker/0:0]
5	2	root	SW<	0	0.0	0	0.0	[kworker/0:0H]
7	2	root	SW	0	0.0	1	0.0	[rcu_preempt]
8	2	root	SW	0	0.0	0	0.0	[rcu_sched]
9	2	root	SW	0	0.0	0	0.0	[rcu_bh]
10	2	root	SW	0	0.0	0	0.0	[migration/0]
11	2	root	SW	0	0.0	0	0.0	[watchdog/0]
12	2	root	SW	0	0.0	1	0.0	[watchdog/1]
13	2	root	SW	0	0.0	1	0.0	[migration/1]

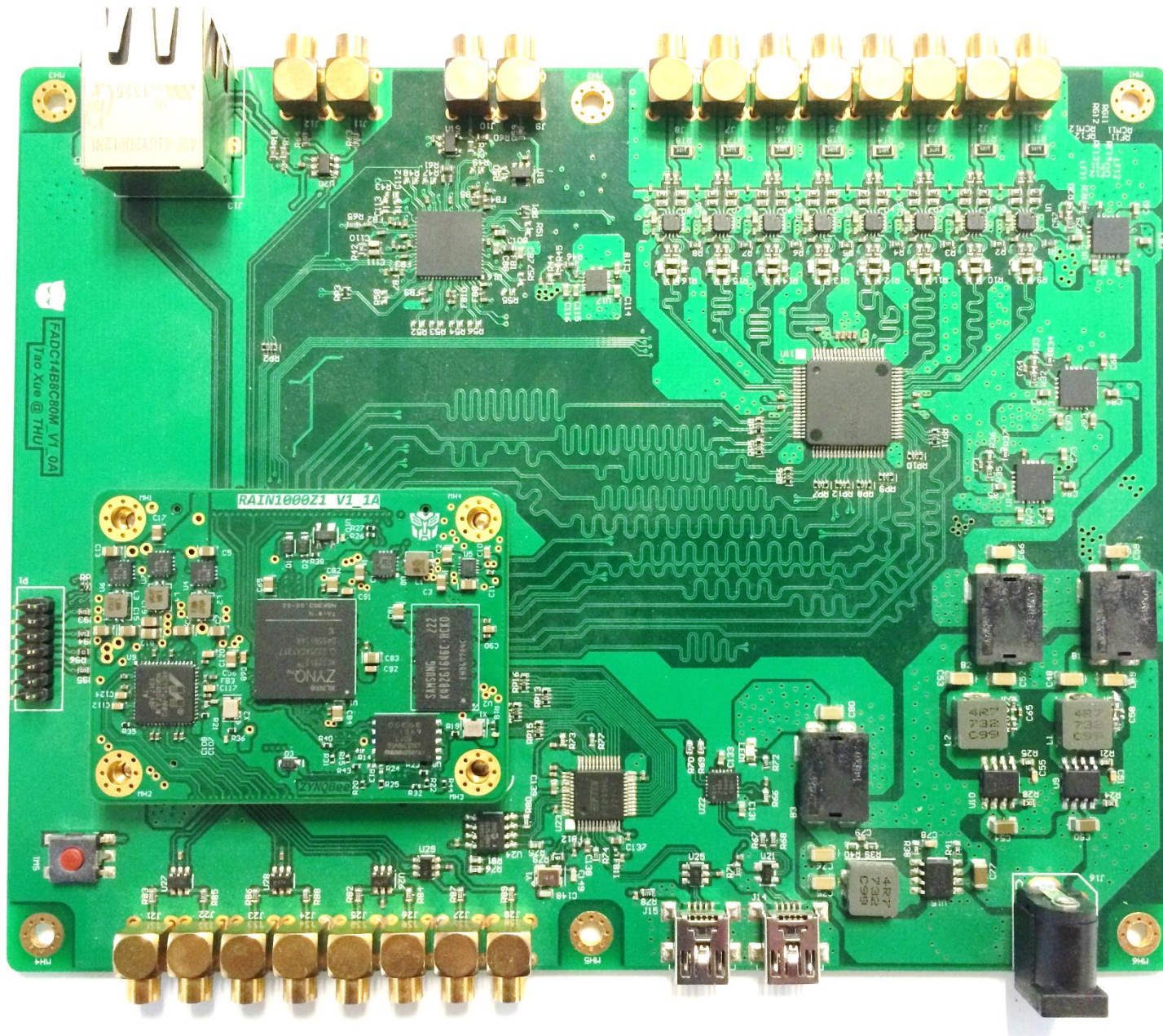
Ready Serial: COM15, 115200 24, 1 26 Rows, 80 Cols VT100 CAP NUM

# ZYNQBee的读出电子学模块的应用设计

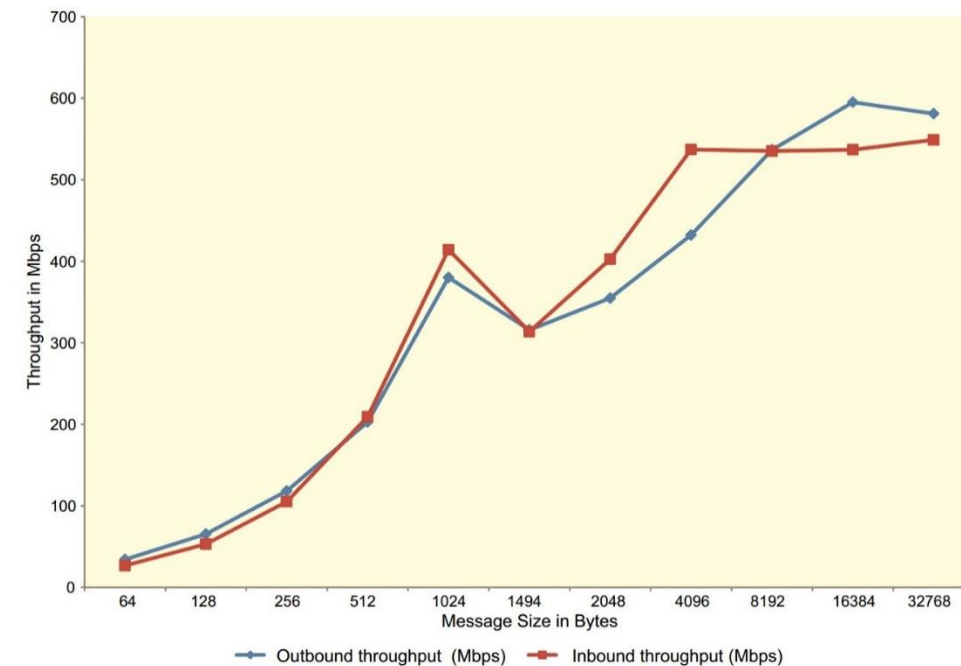




# ZYNQBee的读出电子学模块的应用设计

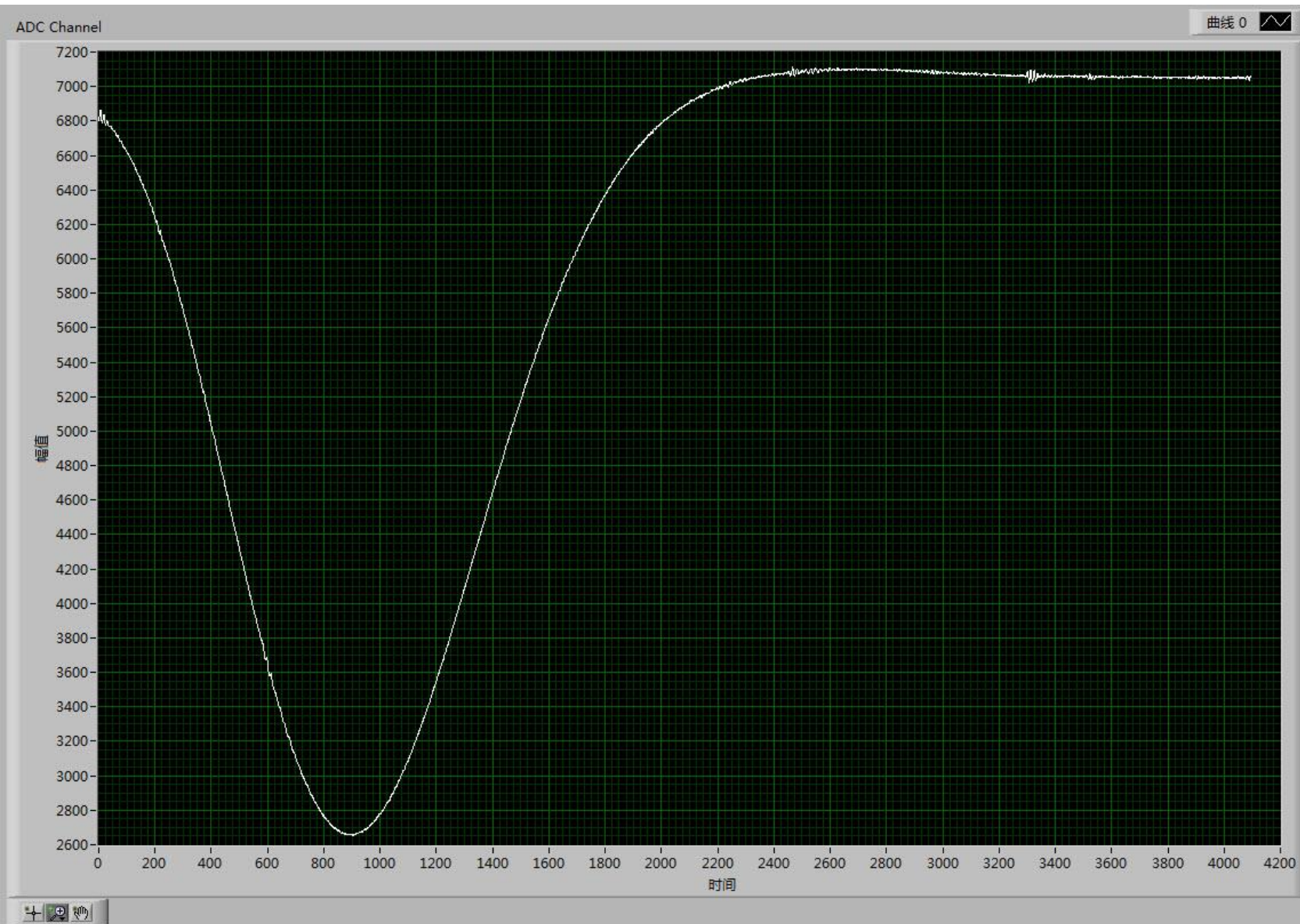


- 8通道14位80Mbps采样的原型系统，用于HPGe探测器的数据读出。
- 读出模块使用ZYNQBee，时钟使用LMK40806B产生FADC需要的时钟。

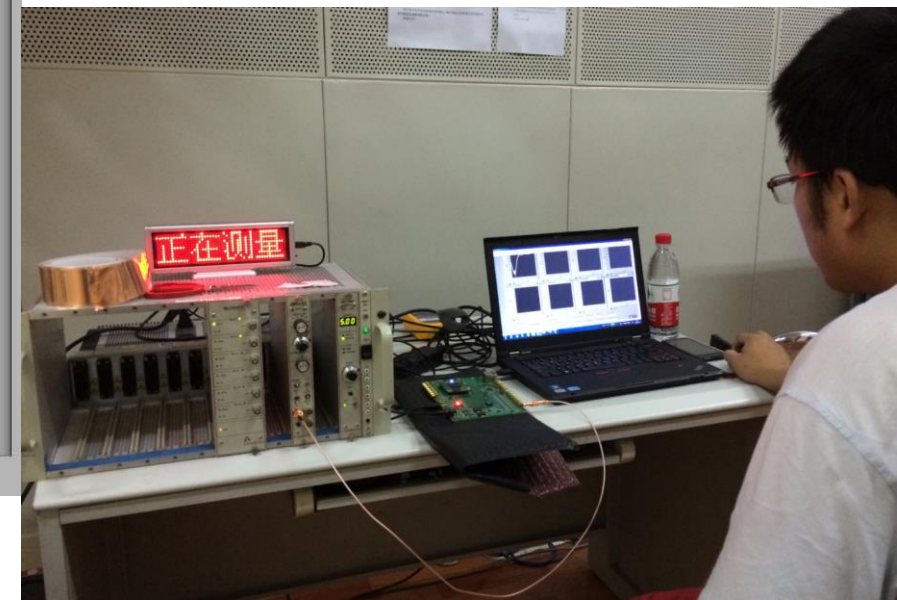




# ZYNQBee的读出电子学模块的应用设计

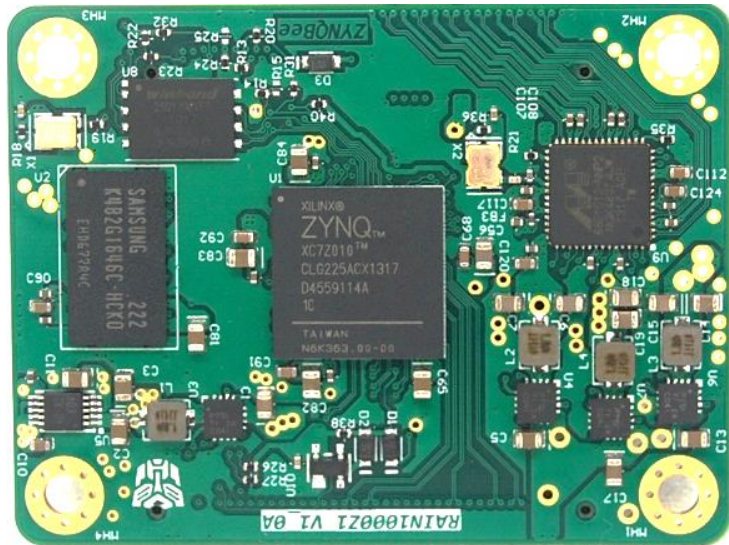


- 在CJPL锦屏地下实验室采集到的HPGe输出的波形信号。





# 小结



**NSCAL**  
Tsinghua University

- 基于Zynq的读出电子学模块为新架构的读出系统提供了一个新的选择。
- 相对于传统的FPGA+MPU双芯片解决方案，Zynq架构的读出电子学架构具有功耗低，尺寸小，性能高，价格低的特点，非常适合用于紧凑型读出系统的设计。
- 相对于基于FPGA单芯片的VHDL类型TCP协议实现的读出系统，Zynq具有更大的灵活性和易用性。