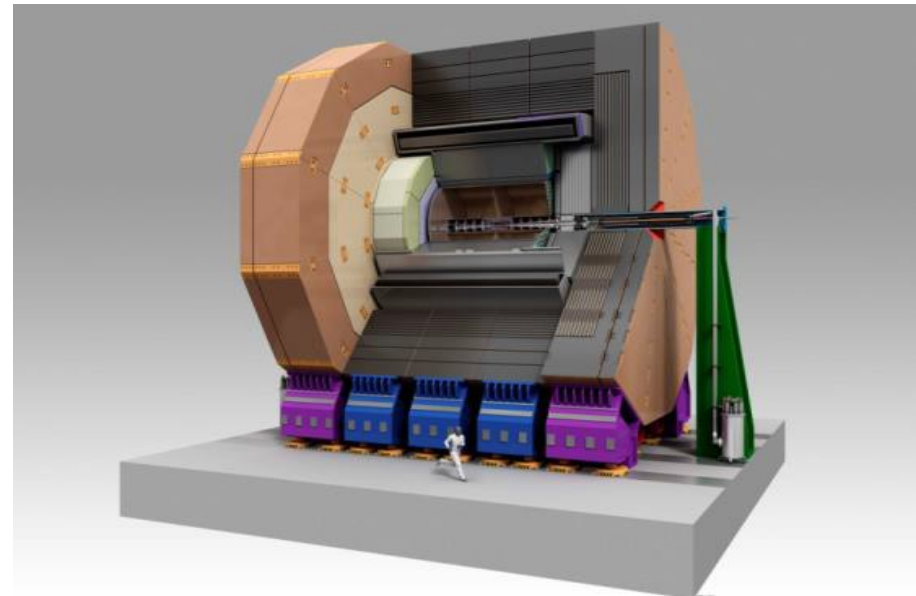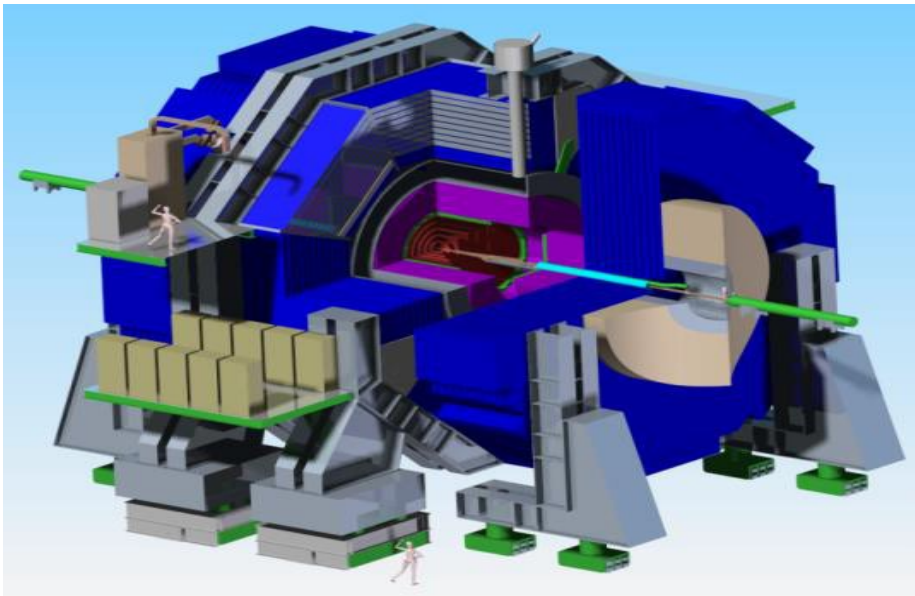# Overview of Silicon Detectors

Weiming Yao (LBNL)

CEPC workshop at SJTU, Sept 12-13 2014

Outline

- Introduction

- Silicon Basics

- Why Silicon Detectors

- Variety of Silicon Technologies

- Radiation damages

- Conclusion

- Disclaim:

- It would not be possible to cover all aspects of si-detectors in this short talk. Many plots are borrowed from various presentations at conferences based on my preference.

- All the errors are mine.

Introduction

- A new boson was discovered at 125 GeV by ATLAS and CMS in 2012 that looks consistent with SM Higgs boson.

- A new collider is required to study it as LEP did for W/Z

- Understanding the Higgs boson in ultimate precision are crucial for probing new physics beyond the Standard Model.
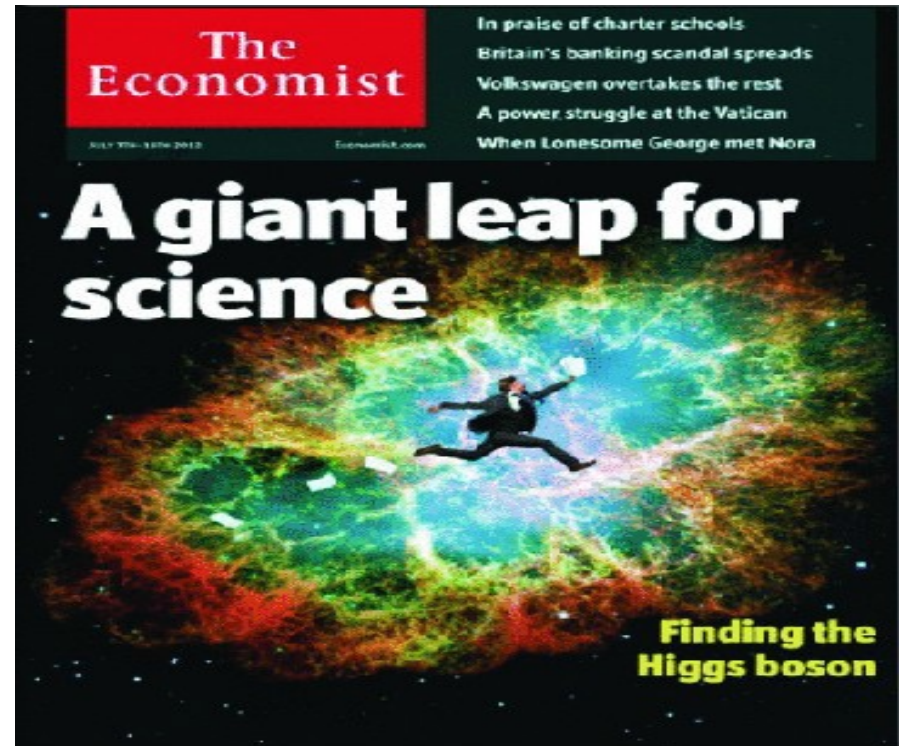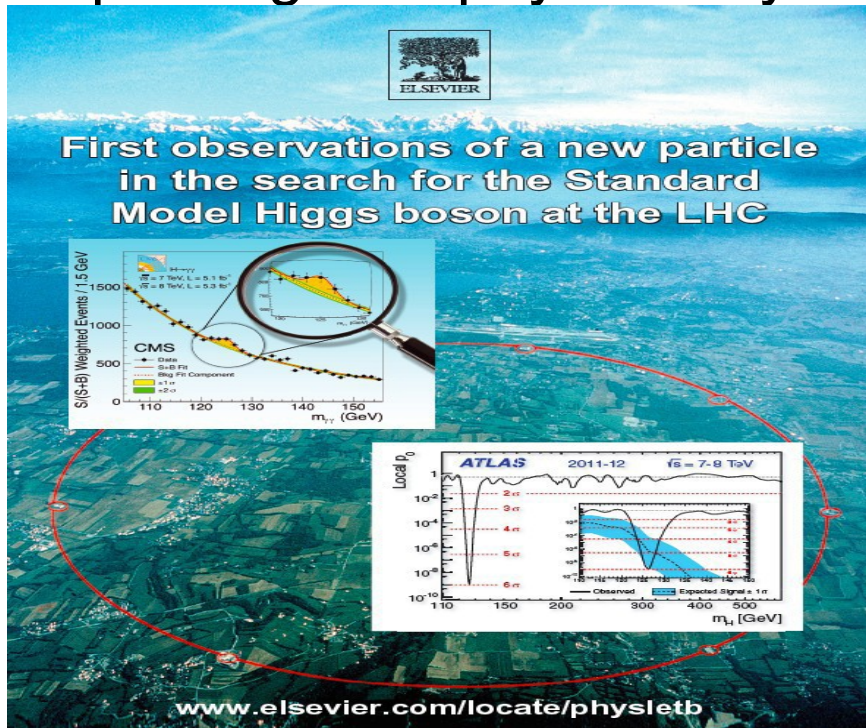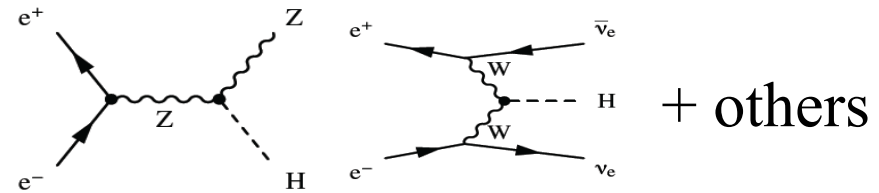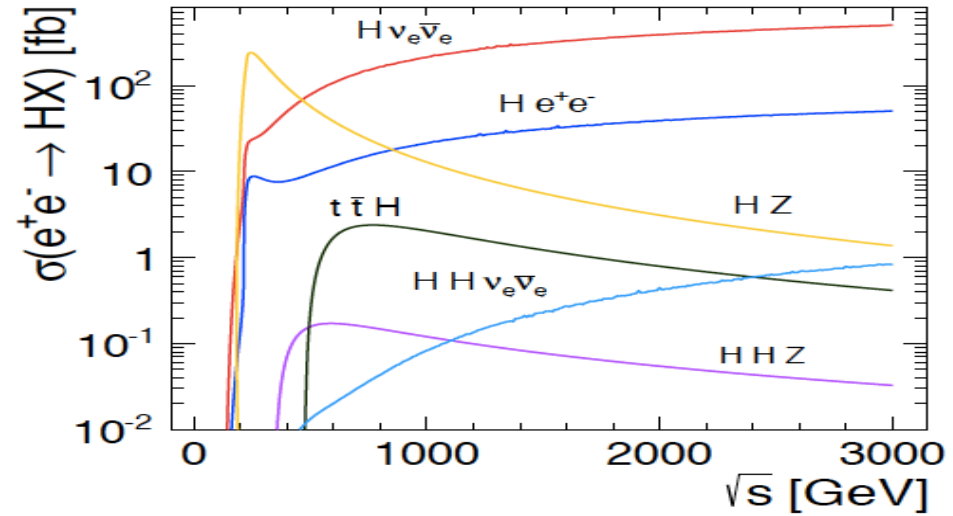
Physics Case: for e+e- collider

- Benchmarks for ~250 GeV Collider:
  - ILC, CLIC, CEPC
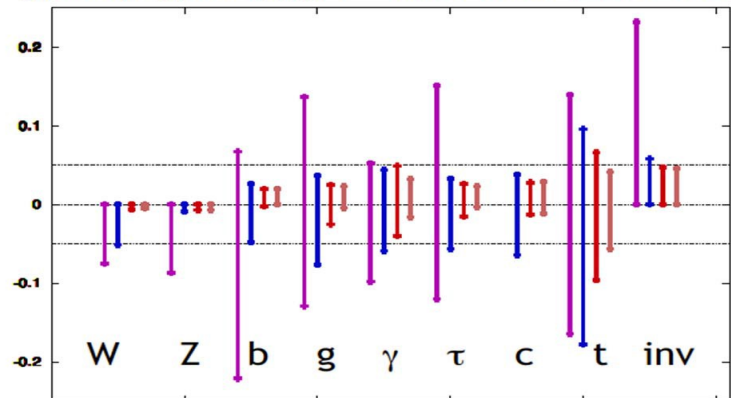 - Clean, well defined initial stat.

- Precise measurements:
  - Higgs mass, Cross section
  - Branching ratios

- Require a Tracker:
  - Excellent momentum resolution
  - Superb vertex capabilities for Heavy flavor tagging including C-tagging ($\sigma_{d0} < 5um$).

- LHC projection with 3 ab^{-1}/exp:
  - $\Delta M_H \sim 0.1$ GeV & $\Delta \Gamma_H \sim 0.1$ GeV

ILC vs CEPC mechine environment

- There are two detector designs exist for ILC: SID and ILD, backed up by lots of past and ongoing detector research and development.
- The running conditions at CEPC will drive the choice of detector technologies.

|	ILC at 500 GeV	CEPC at 250 GeV
Luminosity(cm^2s^{-1})	2×10^{34}	1.76×10^{34}
Beam crossing	554 ns	3.33 µs
#BX/Train	1312	
Train/beam repetition rate	5 Hz	300KHz
σx/σy	476/6(µm)	74.3/0.16(µm)
σz	300 µm	2.42 mm

Silicon Basics

- Silicon: type IV elements, has 1.1eV gap

- Charged particle crossing silicon to create multiple pairs of electric charges.

- Asymmetric diode junction between 2 types of silicon:
  - P(+): Si with some of B ("dopant")
  - N(+): Si doped with some of P, As

- External field applied (bias):
  - Electric field E is formed inside Si
  - Charges move to electrode: signal

- Advantage: Fast(few ns), precise(~10 μm), and compact.

- Disadvantage: expensive, difficult...

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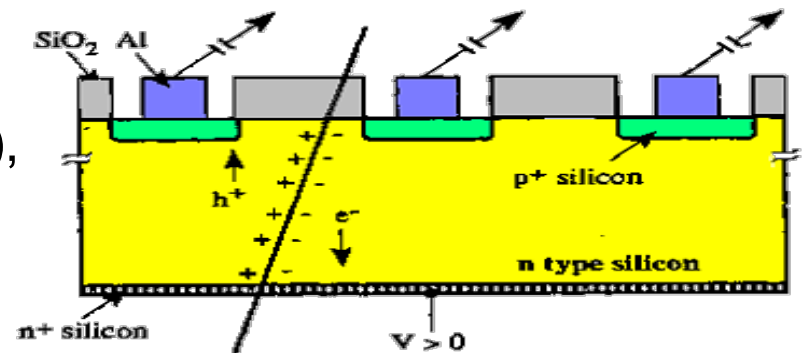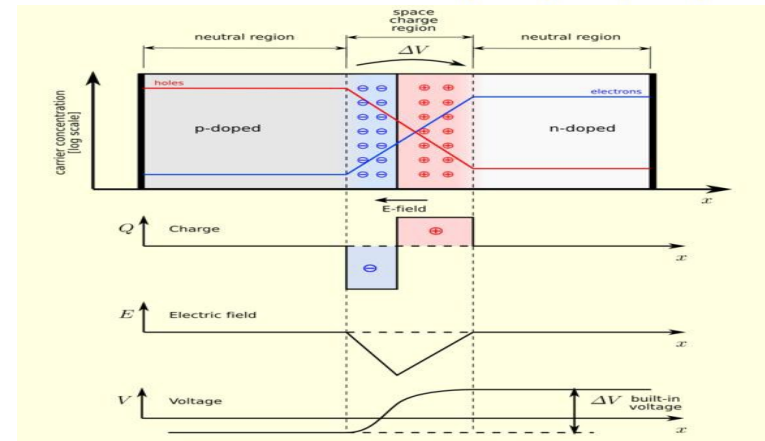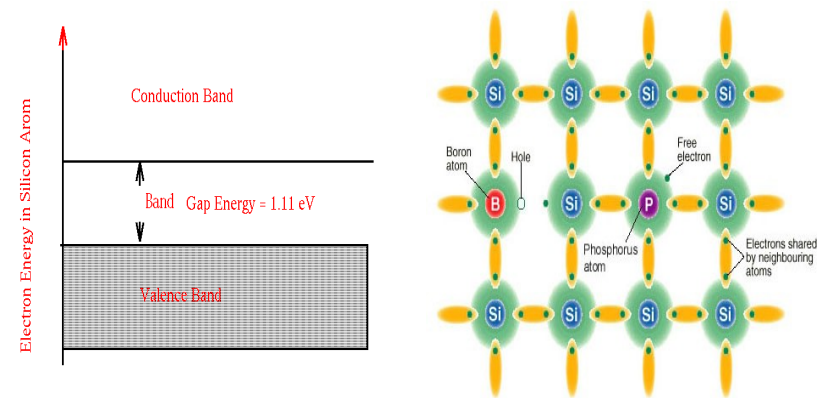
Silicon Detector

- Silicon sensors: where charge is generated by incident particles and is collected by the electrodes.

- Front-end electronic: amplify and read out the signal at the electrodes after suppression the noise hits.

- Cooling: dissipate heat generated by electronic and reduce the leakage current.

- Mechanical structure: everything has to be mounted on a supporting structures and aligned properly.
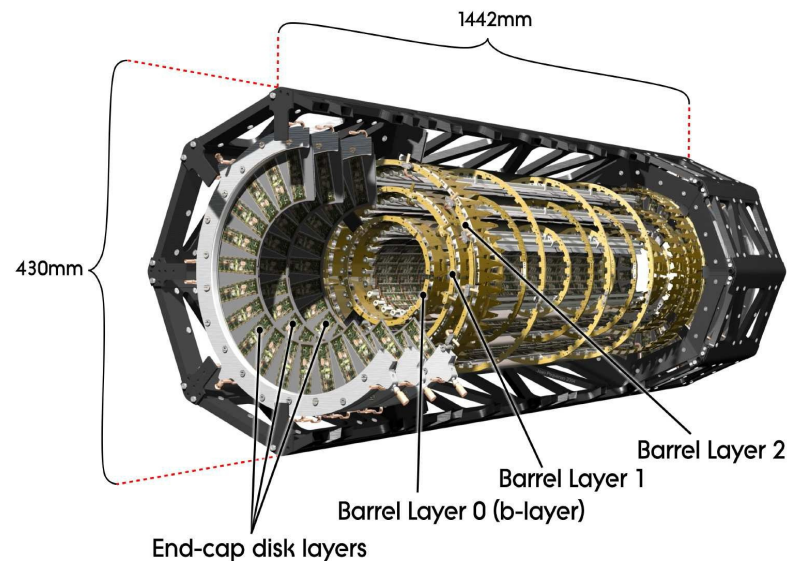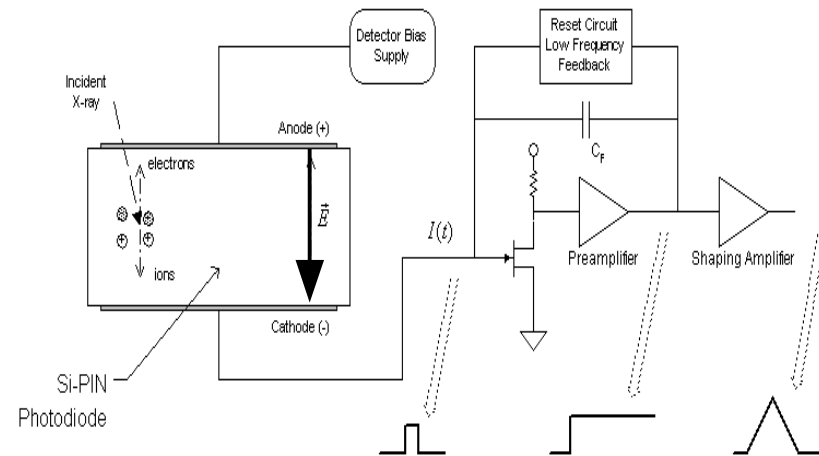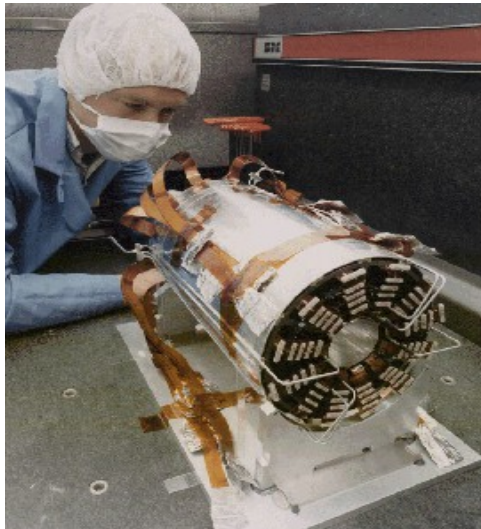
Why Silicon Detector ?

- Silicon detectors: kind of solid-state ionization chamber with superb spatial resolution and can handle very high rates.

- Silicon strip detector concepts started in the 80s, but expensive & difficult.

- Increased commercial use of Si-photolithography and availability of very large scale integration(VLSI) electronics lead to a boom for Si-Detectors in the 90s.

- Nearly all HEP experiments use Silicon detectors as innermost high-precision tracking device.
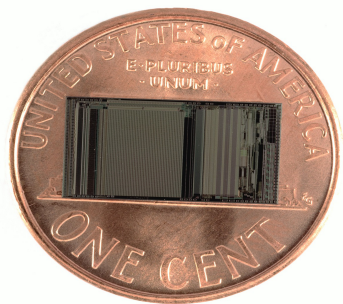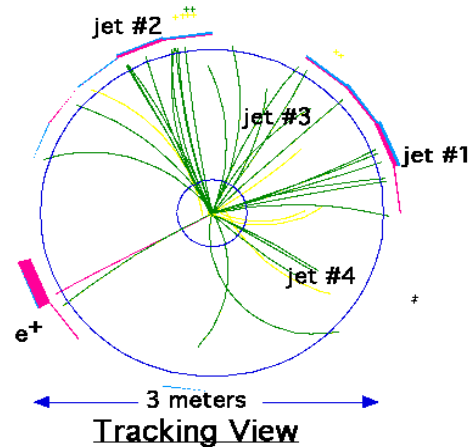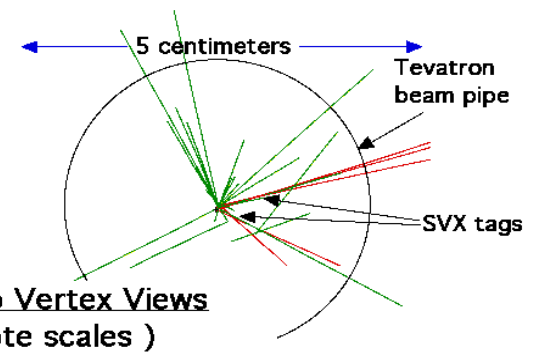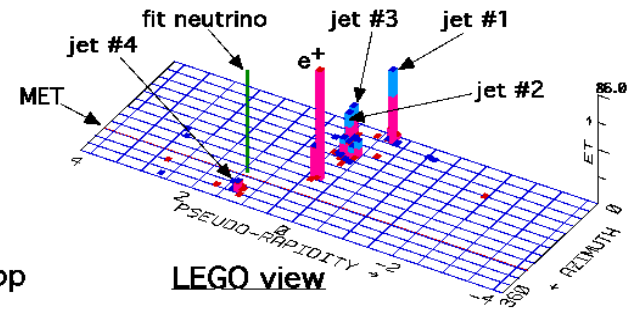
Top quark Discovery at Tevatron

• SVX was the first high rate silicon vertex detector built by CDF to identify the b-quark from Top decay that helped to discover the top quark in 1995.

TTbar→WbWb
→lυb jj b

TWO jets tagged by SVX

fit top mass is 170 +- 10 GeV

e^+, Missing E_t, jet #4 from top

jets 1,2,3 from top (2&3 from W)

fit neutrino   jet #3   jet #1
jet #4 e^+ jet #2
MET   86.0
PSEUDO-RAPIDITY   AZIMUTH θ
LEGO view

SVX Detector
SVX Chip

jet #2
jet #3
jet #1
jet #4
e^+
3 meters
Tracking View

5 centimeters   Tevatron beam pipe
SVX tags
Two Vertex Views
(note scales)

Primary Vertex   Secondary Vertex Ellipses
5 mm

Silicon detectors in collider experiments

Present/Recent Experiments: ATLAS,CMS,LHCb,ALICE,CDF,D0,BaBar, Belle
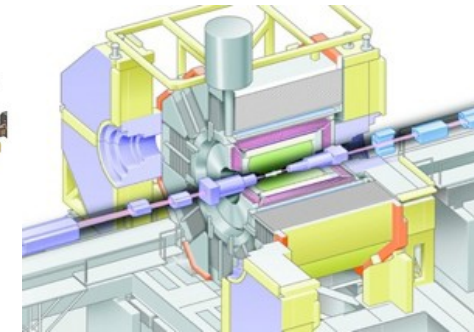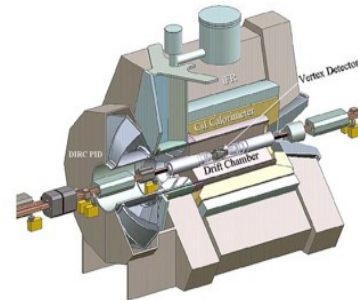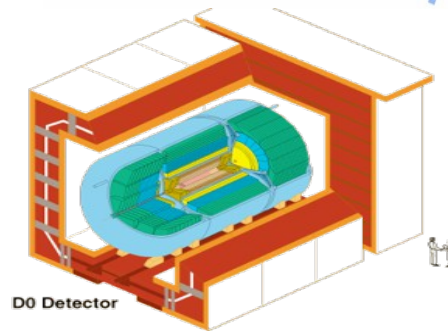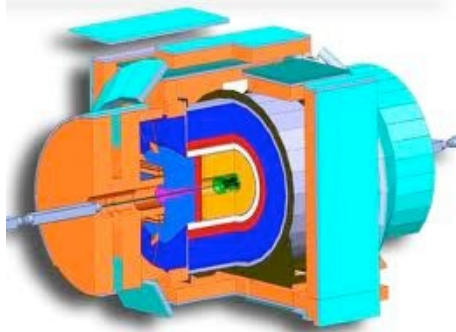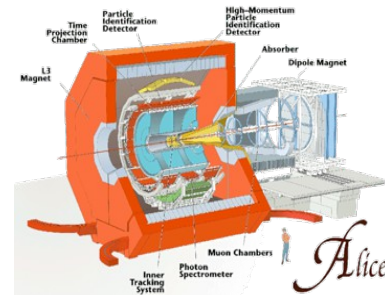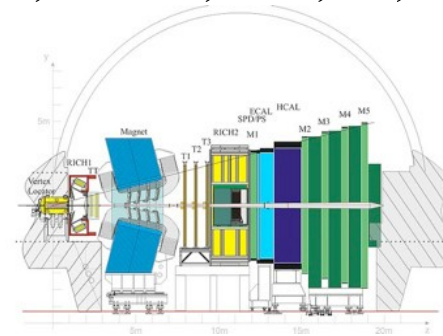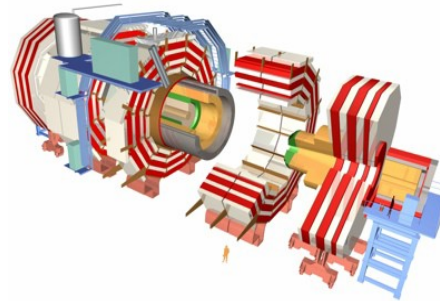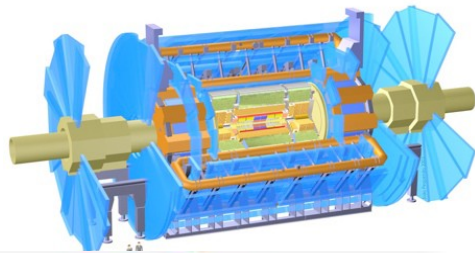
Future Experiments: Belle II,HL-LHC,ILC,CLIC, CEPC...

+ ...
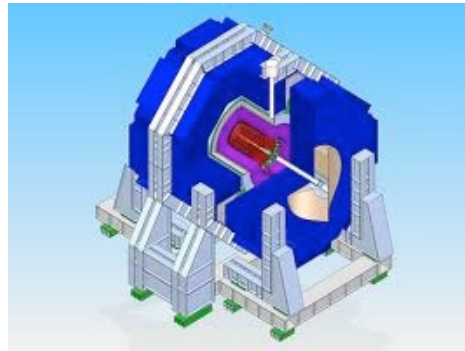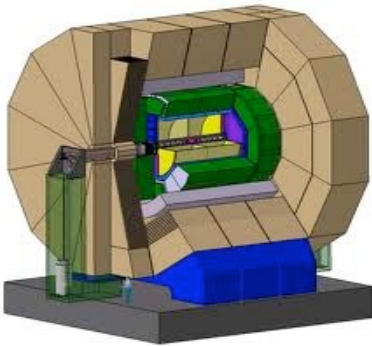
What drives the present and future developments

•Today's silicon trackers are playing critical role for tracking and secondary vertex reconstruction in high rate of interactions and track density at high luminosity environment (HL-LHC).

•Design specs are driven by Physics goals:

- – Hermetic, high efficiency covering the full solid angle
- – Good space resolution and low power
- – High radiation torelance, detection close to IP.
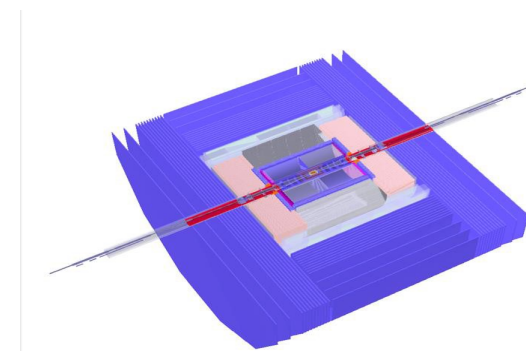- – Material budget including sensor, cooling, cabling
- – Fast, triggable up to 40MHz
- – Reliability, inaccess for several years

•No unique solution to all problems that require to compromise

- – Technology difficulties,
- – Space, material, and   budget constrains.

Evolution of Readout Electronics

- Large channel count, complexity require custom readout chips (ASICs)

- Experimental conditions have often driven the development of a variety of readout architectures, but limited by the available IC processes.

- Chip complexity increases with process evolution(3µm to 65-130nm CMOS)

- Integrated analog-digital signals on the same chip, but S/N remains an issue for longer strips and irradiation.

The State of the Art (FEI4)
26880 pixels, 30 µW/pixel
3000 transistors/pixel

FEI3

20mm

SVX'
1990

SVX2
1996

SVX3
1998

SVX4
2002
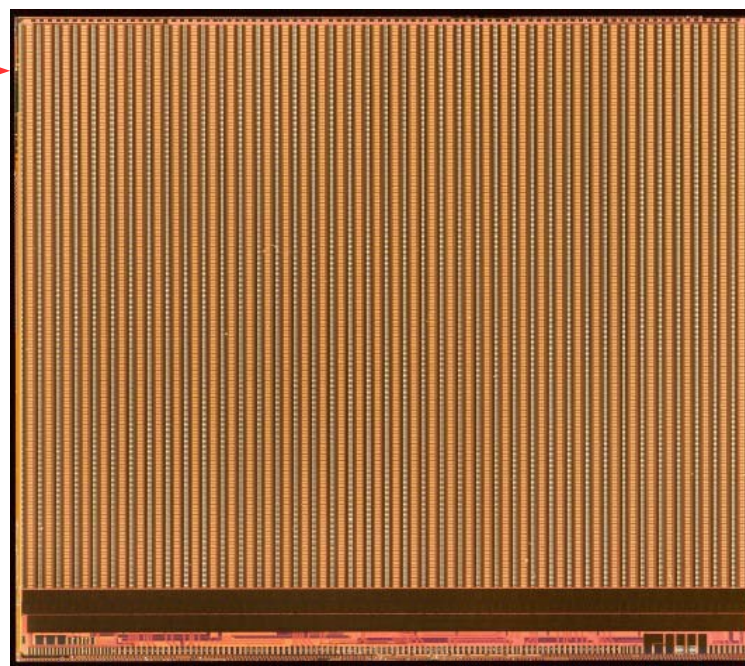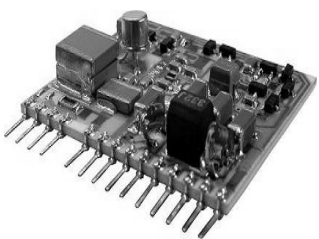
Vertex Detector Requirements for Precision Higgs Physics

- Efficient tagging of b, c, tau from Higgs through precise determination of displaced vertices is essential for ILC or CEPC detectors
  - $\sigma(d0)$ ~5 um, requires single point resolution $\sigma=5$ μm
    - small pixels 20x20 μm^2
  - Low material budget: x<0.15%X0/layer
    - Requires thin Silicon ~100 μm, including supports
    - Low-power ASICS (~50 mW/cm^2) + air-flow cooling
  - Close to IP at 14 mm to reduce extraploation error from MS.
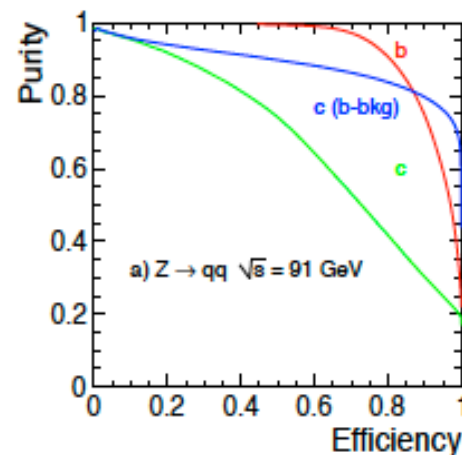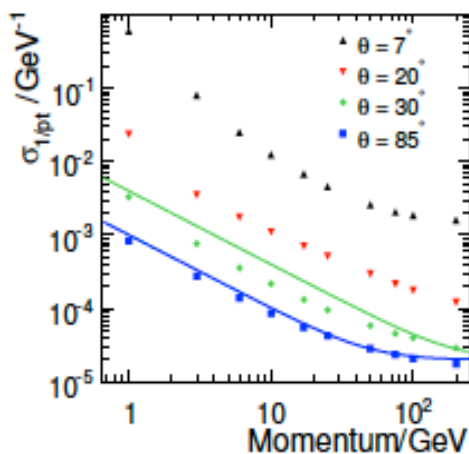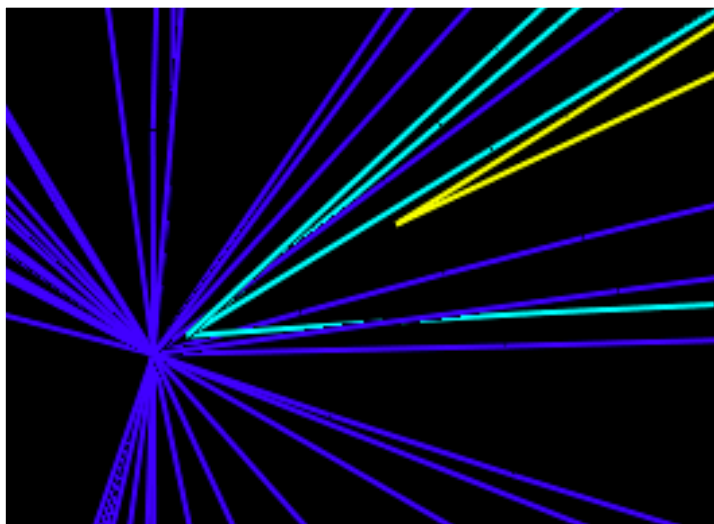
Vertex Detector Concepts for ILC

- Systematic optimization of geometries
  - Low background occupancies
  - Detector performance

- Barrel/endcap geometry
  - 3 double layers or 5 single layers
  - First layer at 14 mm from IP

- Insertable Vertex detector
  - Replace technology choice late
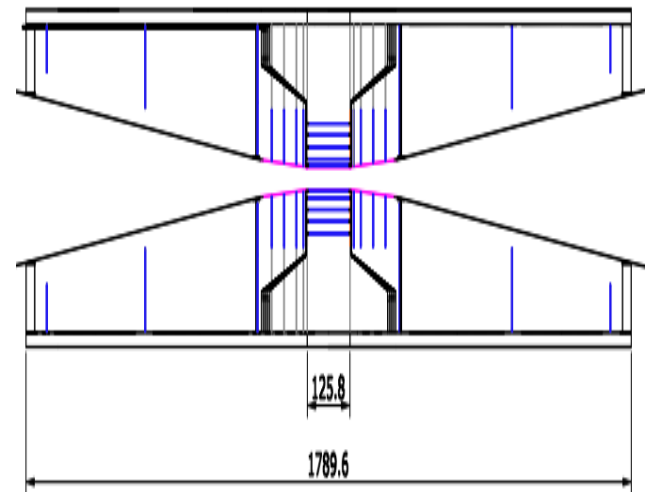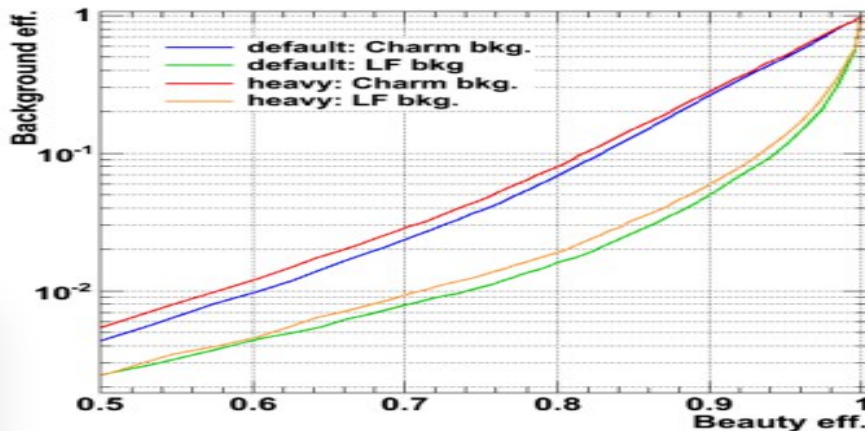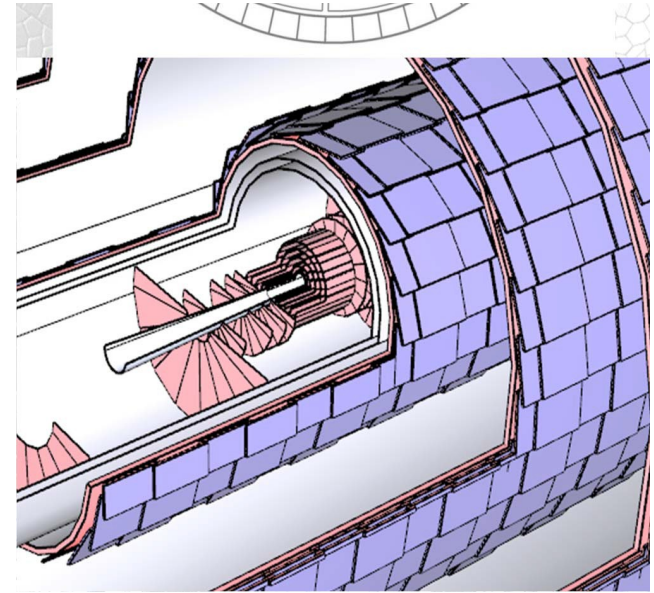
Silicon Pixel Detectors

- Basic concept: Segment a diode in 2-dimensions becomes pixels
    - Increased two-dimensional resolution to increase channel numbers
    - Use Less power than strip detector

- First pixel detectors were CCDs derived from digital cameras.

- CCDs: relative slow, low noise, low mass, not torelate out of time.

- Hybrid pixel: FE IC and sensor joined by a bump bond, fast, Rad. Hard.

- Monolithic Active Pixel (MAP): electronics and charge collection in a thin epitaxial layer, diffusion, moderate speed, low noise, low mass.

Three Phase CCD Clocking

Figure 1

15
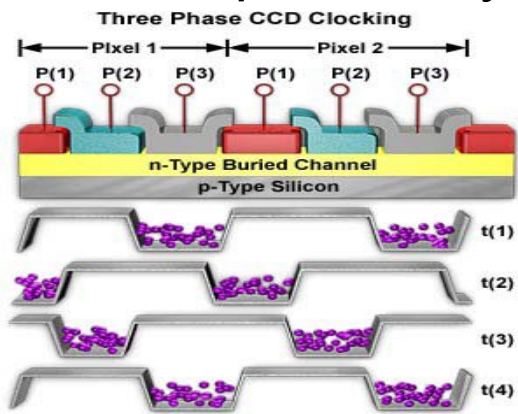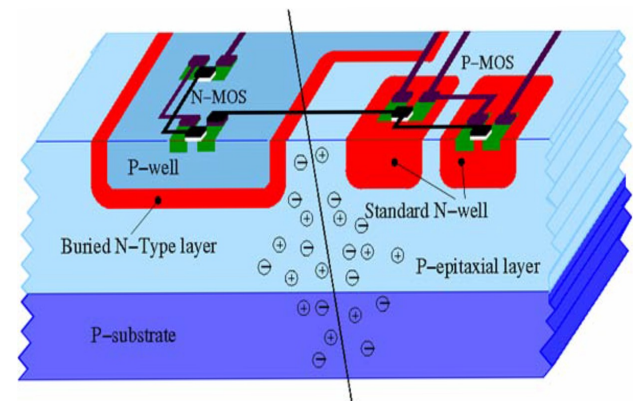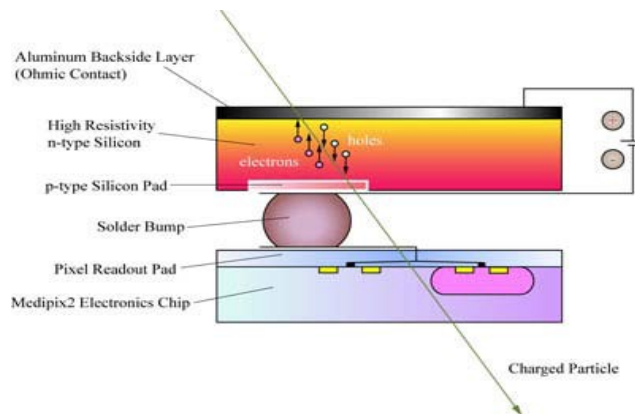
Monolithic Pixel Detectors

- Monolithic pixel detectors are interesting options for low radiation, low rate environments and have been adopted for the STAR HFT, Belle, ALICE ITS upgrade, and possibly for ILC.

- The application in high radiation areas will require radiation hard options which can sustain the high rates and provide adequate time resolution.

- The advantage of low cost and the availability of large wafer diameters could have a significant cost impact for larger trackers

- Ideally one would like to achieve, but no single soulution to all yet
  – Low capacitance (low power)
  – Good S/N
  – Good time resolution, high rate capability
  – Full depletion (High radiation tolerance)

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Silicon On Insulator (SOI)

- SOI wafer with high resistivity sensor & thin CMOS chip connected via oxide

- Fully depleted thick sensing region with low C, offers good Q/C

- Implantation of p+/n+ to the substrate is done after making halls in the top Si and oxide (BOX). Then contacts are formed to connect sensor with readout

- Advantages: no mechanical bump bonding, smaller pixel size, less power, and radiation tolerant.
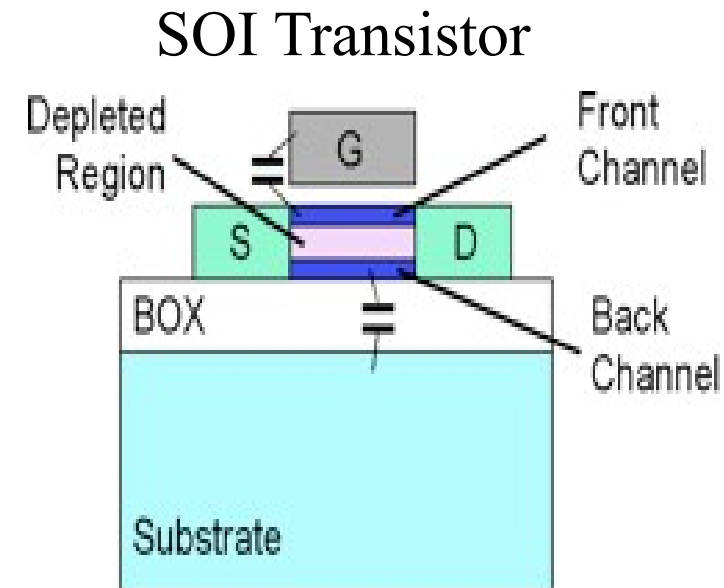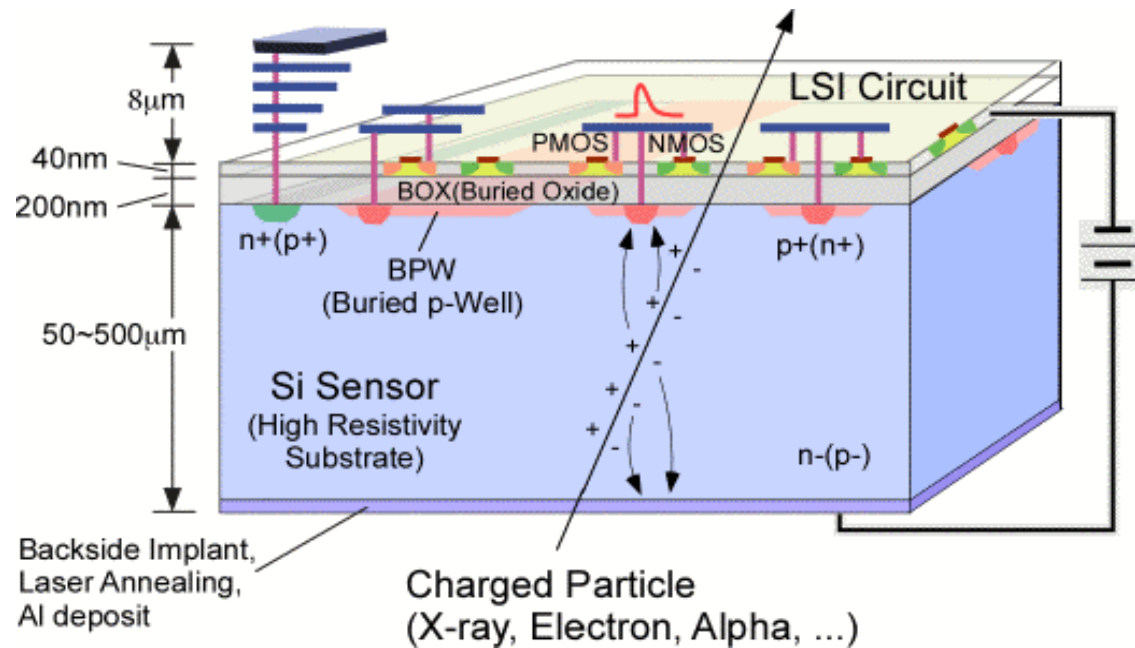
SOI Transistor

The DEPleted Field Effect Transistor(DEPFET)

•DEPFET is the design choice for the pixel detector for Belle II.

•Each pixel is a p-channel FET integrated in a completely depleted bulk

•A deep n-implant creates a potential minimum for electrons under the FET gate

•Drain current is proportional to electrons collected by gate with gain 500pA/e- .

•DEPFET is thin(50 um) with 25x25 pixels, readout with 20-100 us, smaller intrinsic noise and Low power consumption.
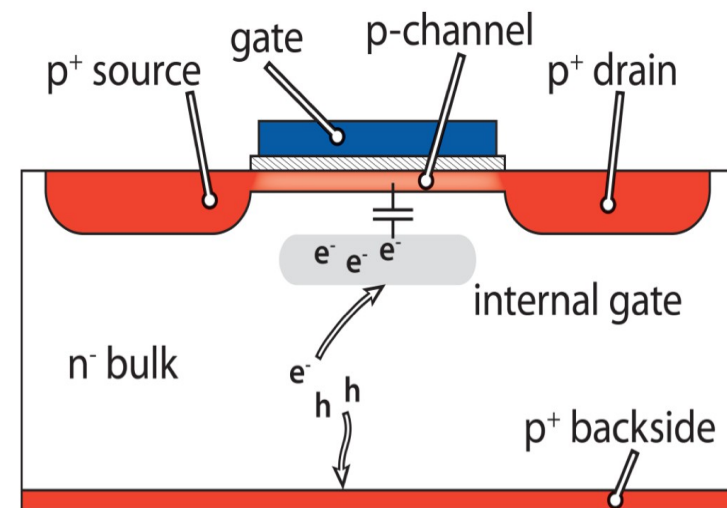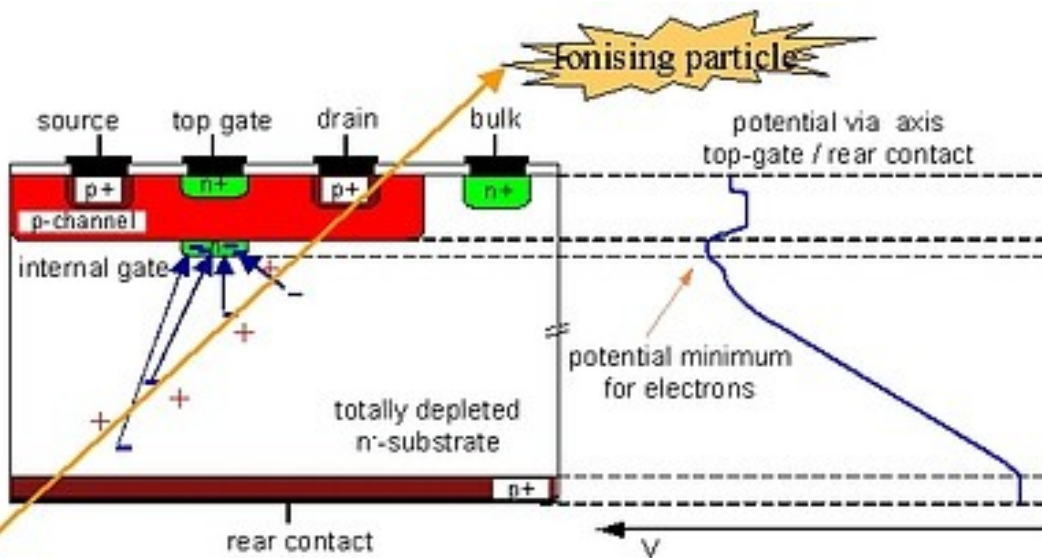
3D Detector and ICs

- Several Key technologies from the same IC world are making 3D fabrication reality.

- Through Silicon via (TSV):
  - Deep Reactive Ion Etch (DRIE) is most used method to etch hols in silicon.
  - Any size hole is possible(0.1-800 um) with very high aspect ratio (100:1).
  - Eliminates need for wirebonds
  - Eliminates dead regions between chips.
  - Increased reliability, reduced material

- Active Edge as electrode to reduce edge eff.:
  - Use support wafer and Plasma Dice
  - Dope and grow field oxide on Edges

Bosch Process Principle

F + ions   SiF$_4$

Si   SF$_6$ Plasma

-CF$_2$-

Si   C$_4$F$_8$ Plasma

Thin fluoro-carbon polymer film (passivation)

Scalloping   SF$_6$ Plasma

19
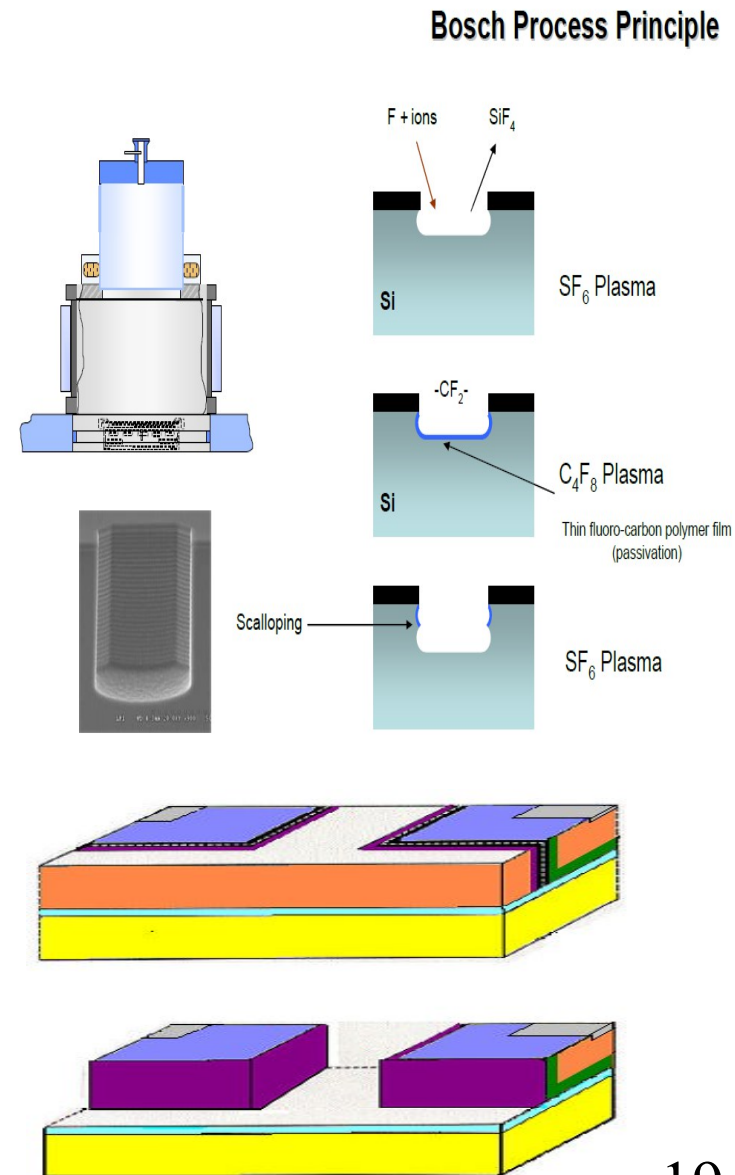
3D with Active Edges

- Proposed in late 90's by S. Parker and C. Kenney

- Combining traditional VLSI processing and MEMS (Micro Electro Mechanical Systems) technologies

- Electrodes are processed inside the detector bulk instead of being implanted on the Wafer's surface.

- The edge is an electrode: No dead area at edges, Efficient Wafer use

- Advantages: fast, higher radiation tolerance.

- 3d module is currently used by ATLAS IBL in the forward region.

20
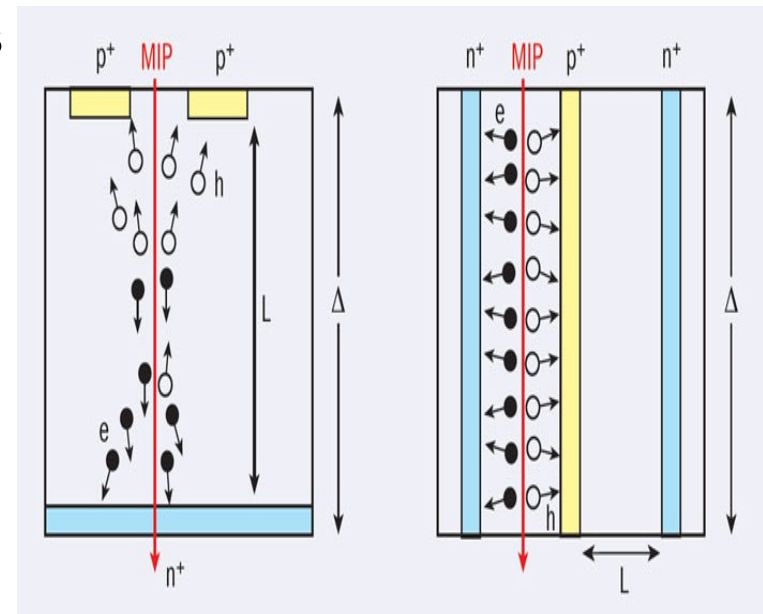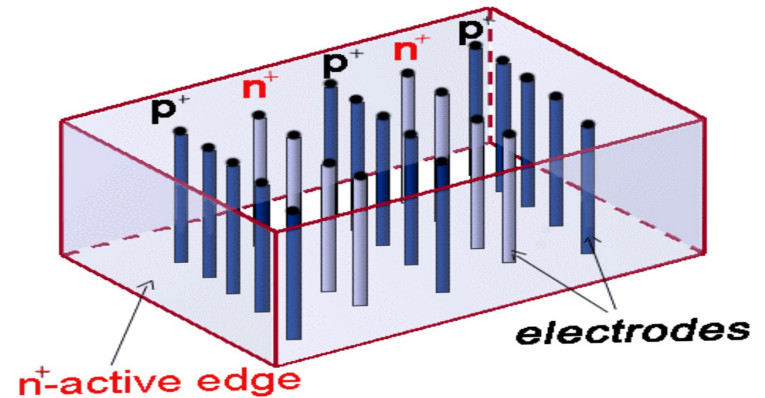
Vertical Integrated Circuits-3D

- Vertical integration of thinned and bonded silicon tiers with vertical interconnects between the IC layers

- Technology driven by industry: offers potential for transformational new detectors.

- Fermilab designed Vertical Integrated Pixel (VIP) chip for ILC pixel detector, through MIT-LL process

- First chip was functional with 48x48, 28x28 μm^2 pixels, redesign for 1000x1000 array was submitted VIP-2A, MIT-LL

- Provides analogy and binary readout.

- 7-bit time stamping of pixel hit

- Token passing readout scheme,Sparse readout

- Chip divided into 3 tiers (~7 µm/tier)
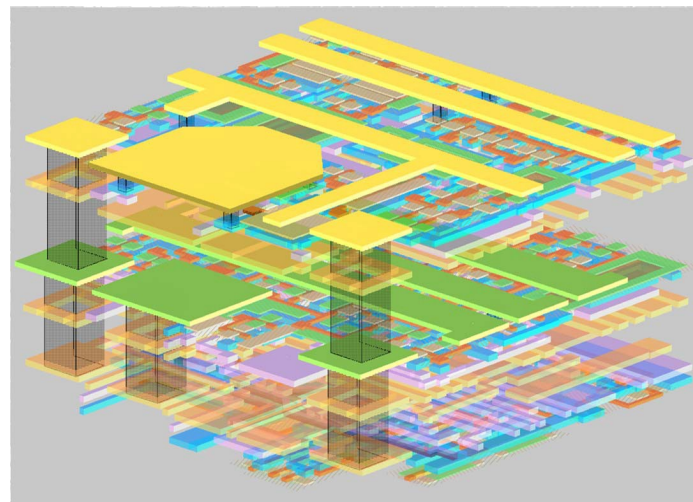
Strip-Detector Technologies

• The "Silicon Microstrip" detector was introduced in the late 1970's and is the basis of all precision tracker in use today.

•Arrays of diode strips can be patterned on silicon wafer(single-Side or double side) using micro-lithographic techniques

•S/N remains issue for long strip and radiation hardness.

Principles of operation
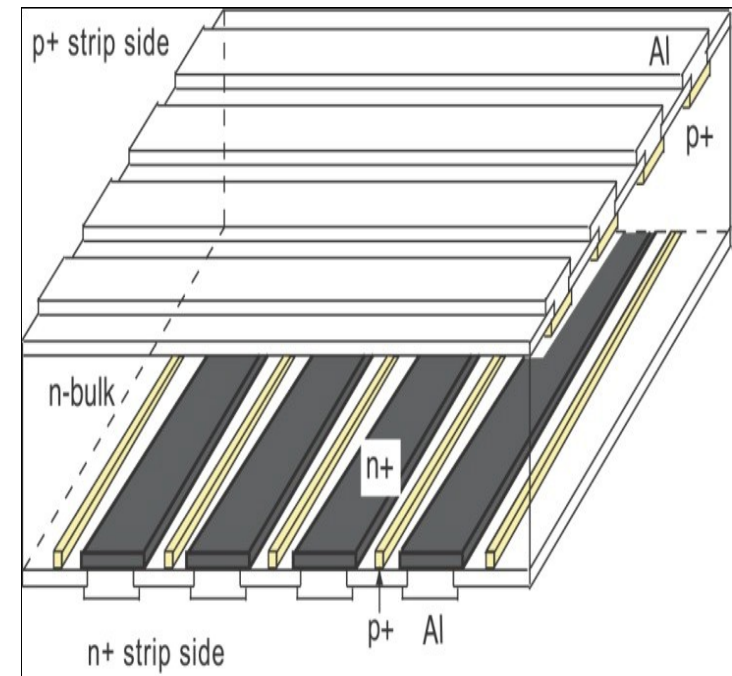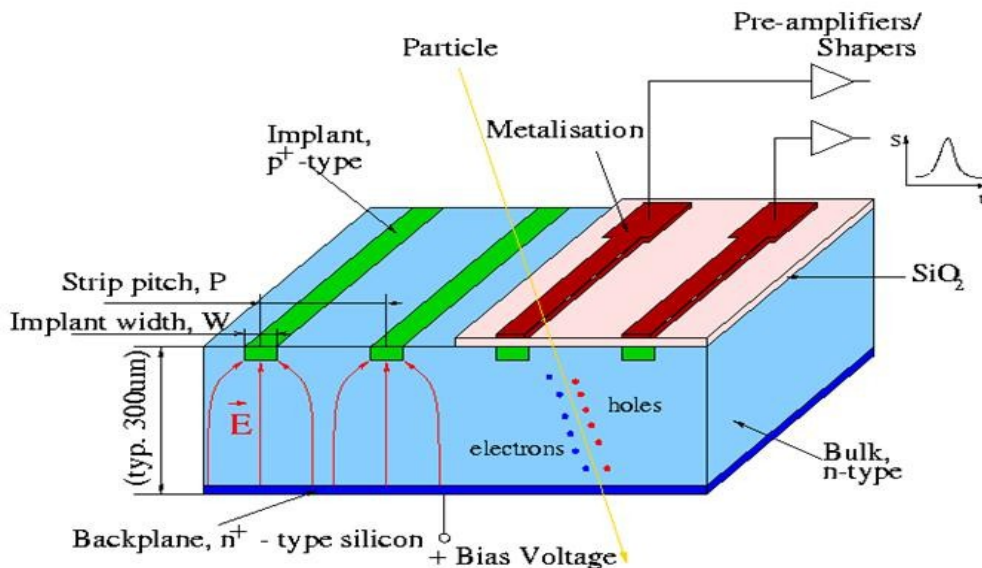
SID Silicon Strip Tracker

- All silicon tracker

  - Silicon micro-strip sensors 10x10cm

- 5 barrel layers and 4 disks

- Gas cooled ~400 W total

- Material budget

  - <20% of X0 in active layer

- KpiX – a readout system on a chip

  - A 1024 channel system to be bump bounded directly to large Si sensors

  - Optimized for ILC, with multi-hit during the train, and digitization and readout

  - Front-end power down during inter-train (mean power <20 uW per channel)

  - Pixel level trigger, trigger bunch # recorded
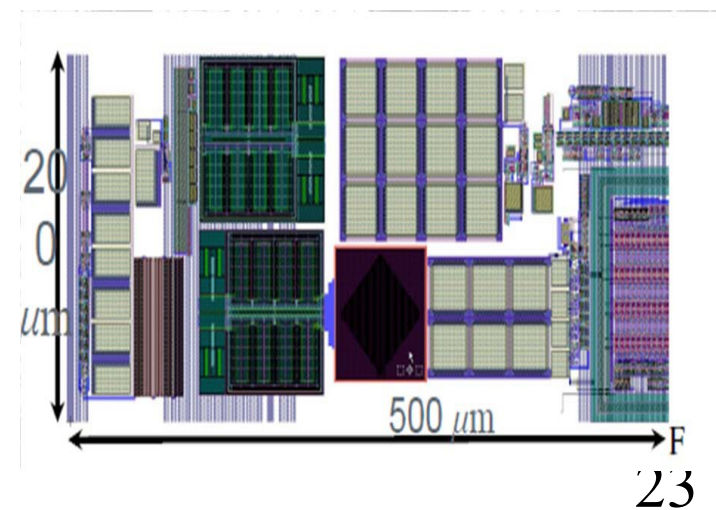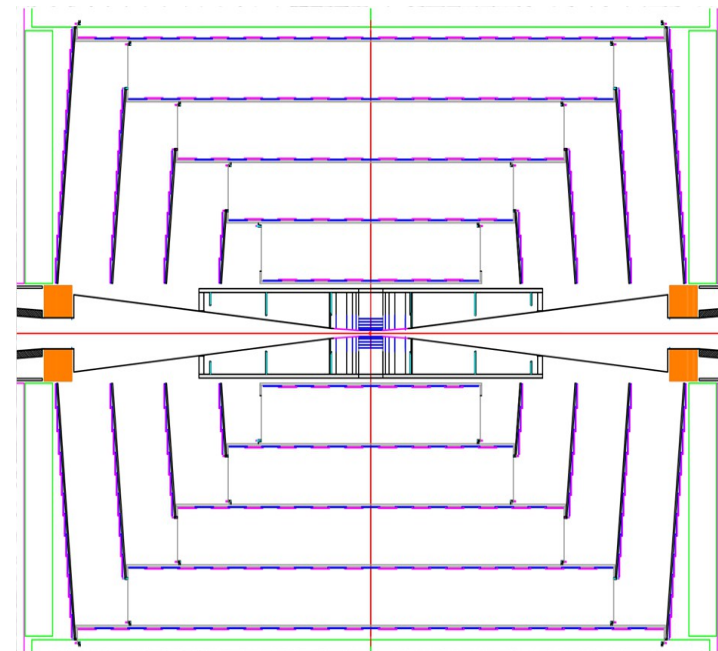
ILD Silicon Strip Tracking

- Si strip tracking around TPC and in forward region:

  - 3 barrel + 5 fwd false double layers + 1 forward single layer

  - Silicon micro-strip sensors 10x10cm, AC-coupled p-on-n, 50 um pitch

- Air cool ~6-9 mW/cm^2 power dissipation

- Readout:

 - SiTR ASIC in 130 nm technology

  - Analog pipeline, low-noise OpAmp, 8-bit ADC

  - Prototype exists and 65nm technology foreseen for next gen.
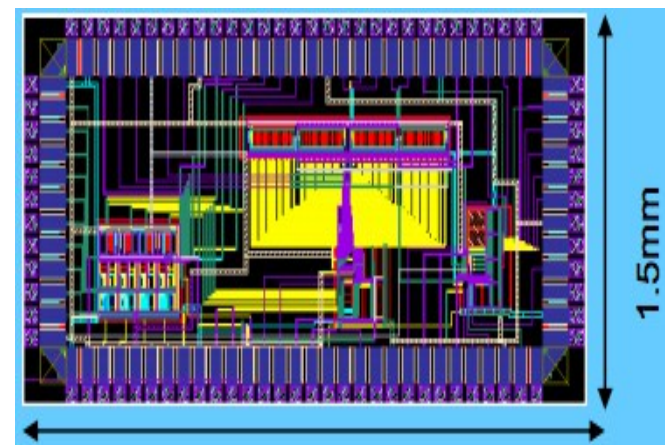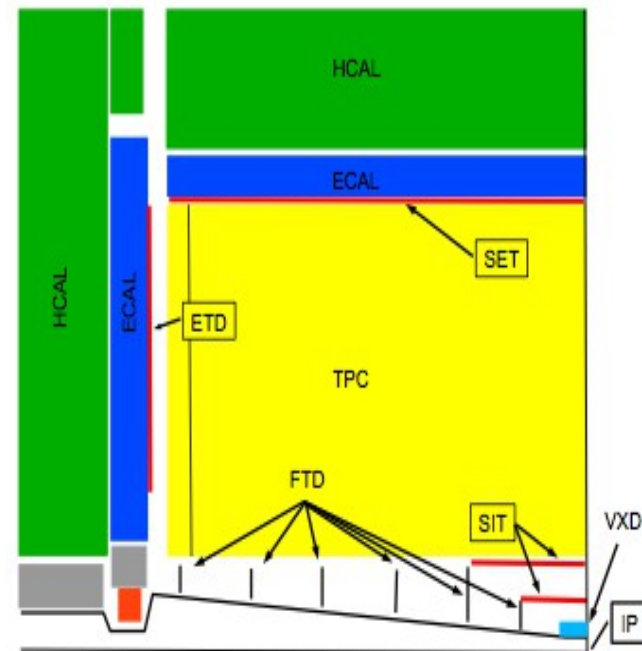
Radiation Damage

•Incident particle interacts with nucleus to cause displacement damage of silicon atoms from their lattice position, creating middle-gap energy states.

•Increased leakage current due to shot noise, power, and heat.

•Bulk material acts more "p type" as defects act as acceptors than as donors.

•Damage is partially reversible (temperature dependant annealing occurs)

•Bulk damage is used in terms of damage caused by a flux of 1 MeV neutrons.

•Reduction in charge collection efficiency: Ratio of collection & charge trapping
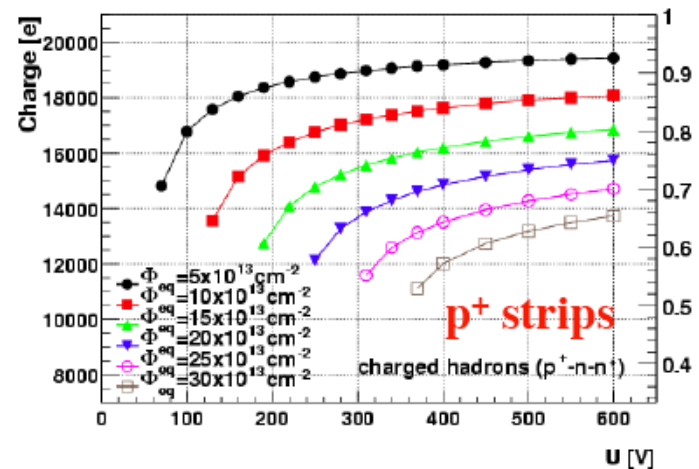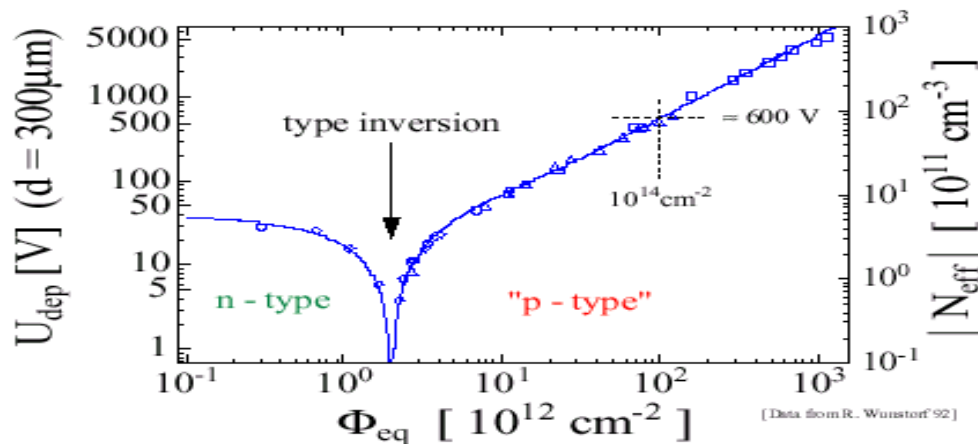
Improving Radiation Tolerance

- Reducing size
  - Smaller volumes generates less leakage current
  - Thinner detectors deplete at lower voltage

- Temperature
  - Lower temperature(-10C) operation can "stabilize" reverse annealing.
  - Reduce leakage current effects

- Integration time: noise is reduced for short shaping times at the expense of increased pre-amp noise.

- Biasing schemes: reduce parallel biasing resistor to reduce votage drop

- HV operation: higher voltage operation, depletion voltage, partial depletion.

- Low noise electronics: tolerate reduced signal due to charge collection efficiency (CCE) and partial depletion

- Configuration: p in n substrate(simple); n in n (could work); n in p (no invert)

Conclusion

- There are significant progress made in the last 30 years to build silicon detectors using a broad suite of advanced technologies.

- The technology is mature and the detectors are getting large, more precise, and approaching billion channels.

- These devices have played a major role in precision tracking and vertexing in high energy physics experiments.

- There are still significant technical challenges for next generation experiments, but there are plenty of ideas to jump start for CEPC.