Status report of VTX sub-group

— Towards pre-CDR

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Representing VTX sub-group

The 4th international workshop on future high energy circular colliders

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Outline

- Requirements
- Baseline design
- Simulation and performance optimization studies
- Sensor options
- Critical R&D

Organization & Manpower

- IHEP
  - OUYANG Qun, co-convener
  - Faculty:
    LU Yunpeng, DONG Mingyi, QIN Zhonghua, ZHU Hongbo,
    LOU Xinchou — detector

    LIU Beijiang, WU Linghui — simulation
  - Post-Doc: XIU Qinglei — simulation
  - Graduate students: JU Xudong — detector
- SDU
  - WANG Meng , co-convener
  - Faculty: ZHANG Liang – sensor technology
  - Graduate students: LIU Qingyuan – simulation
- HKU
  - Faculty: TU Yanjun – simulation

TOC for pre-CDR (main editors)

4.1 Vertex

4.1.1 Introduction (OUYANG Qun)
4.1.2 Physics motivation (WANG Meng)
4.1.3 Detector challenges and performance requirements (WANG Meng)
4.1.4 Baseline design (OUYANG Qun)
4.1.5 Sensor options (LU Yunpeng)
4.1.6 Simulation and performance optimization studies (LIU Beijing)
4.1.7 Mechanics and integration (DONG Mingyi)
4.1.8 Critical R&D (WANG Meng)
4.1.9 Cost estimation (OUYANG Qun)
4.1.10 (Summary)
Bibliography

4.2 Si-strips (ZHU Hongbo, TU Yanjun)

4.2.1 Introduction requirements
4.2.2 Baseline design
4.2.3 Simulation study
4.2.4 Critical R&D
4.2.5 Integration
4.2.6 Cost
Bibliography

Pre-CDR Status

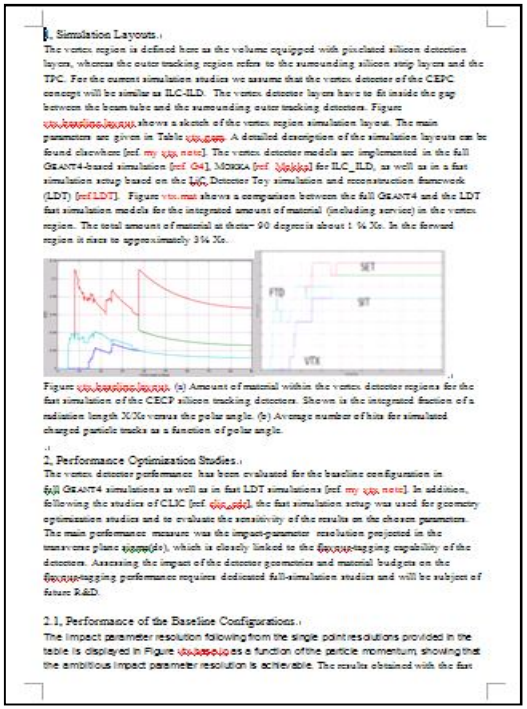
- Vertex:

- 4 pages of simulation and optimization

- 2 pages of sensor option

- 1 page of mechanics and integration

- Si tracker: 3 pages covering the baseline design, performance, critical R&D items, integration and cost estimation.



2. Simulation Layouts.

The vertex region is defined here as the volume equipped with pixelated silicon detection layers, whereas the outer tracking region refers to the surrounding silicon strip layers and the TPC. For the current simulation studies we assume that the vertex detector of the CEPC concept will be similar as ILC-ILD. The vertex detector layers have to fit inside the gap between the beam tube and the surrounding outer tracking detectors. Figure shows a sketch of the vertex region simulation layout. The main parameters are given in Table . A detailed description of the simulation layouts can be found elsewhere [ref.]. The vertex detector models are implemented in the full GEANT4-based simulation [ref. G4], MOKKA [ref.] for ILC_ILD, as well as in a fast simulation setup based on the Marlin Detector Toy simulation and reconstruction framework (LDT) [ref LDT]. Figure shows a comparison between the full GEANT4 and the LDT fast simulation models for the integrated amount of material (including service) in the vertex region. The total amount of material at theta= 90 degrees is about 1 % X0. In the forward region it rises to approximately 3% X0.

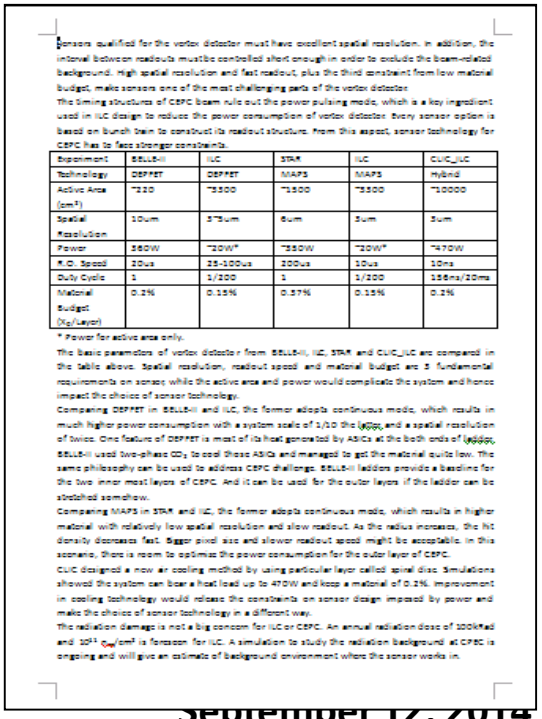
Figure (a) Amount of material within the vertex detector regions for the fast simulation of the CEPC silicon tracking detectors. Shown is the integrated fraction of a radiation length X/X0 versus the polar angle. (b) Average number of hits for simulated charged particle tracks as a function of polar angle.

2. Performance Optimization Studies.

The vertex detector performance has been evaluated for the baseline configuration in full GEANT4 simulations as well as in fast LDT simulations [ref]. In addition, following the studies of CLIC [ref], the fast simulation setup was used for geometry optimization studies and to evaluate the sensitivity of the results on the chosen parameters. The main performance measure was the impact-parameter resolution projected in the transverse plane (d0), which is closely linked to the -tagging capability of the detectors. Assessing the impact of the detector geometries and material budgets on the -tagging performance requires dedicated full-simulation studies and will be subject of future R&D.

2.1. Performance of the Baseline Configurations.

The impact parameter resolution following from the single point resolutions provided in the table is displayed in Figure as a function of the particle momentum, showing that the ambitious impact parameter resolution is achievable. The results obtained with the fast



Sensors qualified for the vertex detector must have excellent spatial resolution. In addition, the interval between readouts must be controlled short enough in order to exclude the beam-related background. High spatial resolution and fast readout, plus the third constraint from low material budget, make sensors one of the most challenging parts of the vertex detector.

The timing structure of CEPC beam rule out the power pulsing mode, which is a key ingredient used in ILC design to reduce the power consumption of vertex detector. Every sensor option is based on bunch train to construct its readout structure, from this aspect, sensor technology for CEPC has to face stronger constraints.

Experiment	BELLE-II	ILC	STAR	ILC	CLIC_ILC
Technology	DEPFET	DEPFET	MAPS	MAPS	Hybrid
Active Area (cm^2)	~220	~3500	~1500	~3500	~10000
Spatial Resolution	10um	5~7um	6um	3um	3um
Power	360W	~20W*	~350W	~20W*	~470W
R.O. Speed	20us	25-100us	200us	10us	10ns
Duty Cycle	1	1/200	1	1/200	156ns/20ms
Material Budget (X0/Layer)	0.2%	0.15%	0.37%	0.15%	0.2%

* Power for active area only.

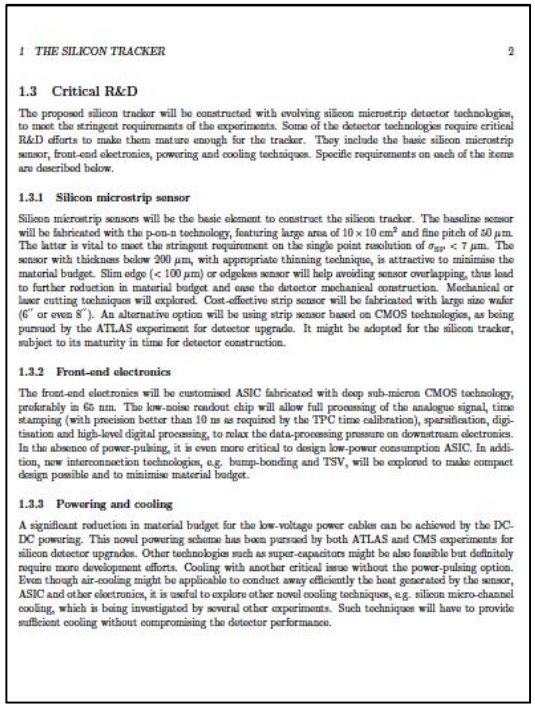
The basic parameters of vertex detector from BELLE-II, ILC, STAR and CLIC_ILC are compared in the table above. Spatial resolution, readout speed and material budget are 3 fundamental requirements on sensor, while the active area and power would complicate the system and hence impact the choice of sensor technology.

Comparing DEPFET in BELLE-II and ILC, the former adopts continuous mode, which results in much higher power consumption with a system scale of 1/10 the , and a spatial resolution of twice. One feature of DEPFET is most of its heat generated by ASICs at the both ends of . BELLE-II used two-phase CO_2 to cool those ASICs and managed to get the material quite low. The same philosophy can be used to address CEPC challenge. BELLE-II ladders provide a baseline for the two inner most layers of CEPC. And it can be used for the outer layers if the ladder can be stretched somehow.

Comparing MAPS in STAR and ILC, the former adopts continuous mode, which results in higher material with relatively low spatial resolution and slow readout. As the radius increases, the hit density decreases fast. Bigger pixel size and slower readout speed might be acceptable. In this scenario, there is room to optimize the power consumption for the outer layer of CEPC.

CLIC designed a new air cooling method by using particular layer called spiral disc. Simulations showed the system can bear a heat load up to 470W and keep a material of 0.2%. Improvement in cooling technology would release the constraints on sensor design imposed by power and make the choice of sensor technology in a different way.

The radiation damage is not a big concern for ILC or CEPC. An annual radiation dose of 100krad and 10^{11} n_{eq}/cm^2 is foreseen for ILC. A simulation to study the radiation background at CPEC is ongoing and will give an estimate of background environment where the sensor works in.



1 THE SILICON TRACKER 2

1.3 Critical R&D

The proposed silicon tracker will be constructed with evolving silicon microstrip detector technologies, to meet the stringent requirements of the experiments. Some of the detector technologies require critical R&D efforts to make them mature enough for the tracker. They include the basic silicon microstrip sensor, front-end electronics, powering and cooling techniques. Specific requirements on each of the items are described below.

1.3.1 Silicon microstrip sensor

Silicon microstrip sensors will be the basic element to construct the silicon tracker. The baseline sensor will be fabricated with the p-on-n technology, featuring large area of 10×10 cm^2 and fine pitch of 50 μm. The latter is vital to meet the stringent requirement on the single point resolution of $\sigma_{sp} < 7$ μm. The sensor with thickness below 200 μm, with appropriate thinning technique, is attractive to minimise the material budget. Slim edge (< 100 μm) or edgeless sensor will help avoiding sensor overlapping, thus lead to further reduction in material budget and ease the detector mechanical construction. Mechanical or laser cutting techniques will explored. Cost-effective strip sensor will be fabricated with large size wafer (6″ or even 8″). An alternative option will be using strip sensor based on CMOS technologies, as being pursued by the ATLAS experiment for detector upgrade. It might be adopted for the silicon tracker, subject to its maturity in time for detector construction.

1.3.2 Front-end electronics

The front-end electronics will be customised ASIC fabricated with deep sub-micron CMOS technology, preferably in 65 nm. The low-noise readout chip will allow full processing of the analogue signal, time stamping (with precision better than 10 ns as required by the TPC time calibration), sparsification, digitisation and high-level digital processing, to relax the data-processing pressure on downstream electronics. In the absence of power-pulsing, it is even more critical to design low-power consumption ASIC. In addition, new interconnection technologies, e.g. bump-bonding and TSV, will be explored to make compact design possible and to minimise material budget.

1.3.3 Powering and cooling

A significant reduction in material budget for the low-voltage power cables can be achieved by the DC-DC powering. This novel powering scheme has been pursued by both ATLAS and CMS experiments for silicon detector upgrades. Other technologies such as super-capacitors might be also feasible but definitely require more development efforts. Cooling with another critical issue without the power-pulsing option. Even though air-cooling might be applicable to conduct away efficiently the heat generated by the sensor, ASIC and other electronics, it is useful to explore other novel cooling techniques, e.g. silicon micro-channel cooling, which is being investigated by several other experiments. Such techniques will have to provide sufficient cooling without compromising the detector performance.

Detector challenges and performance requirements

ILD:*B=3.5T*

CEPC detector will keep the same vertexing and tracking performance

- momentum resolution $\sigma_{1/p_T} = 2\times10^{-5} \oplus 1\times10^{-3}/(p_T \sin\theta)$
- impact parameter resolution $\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$

Vertex detector specifications:

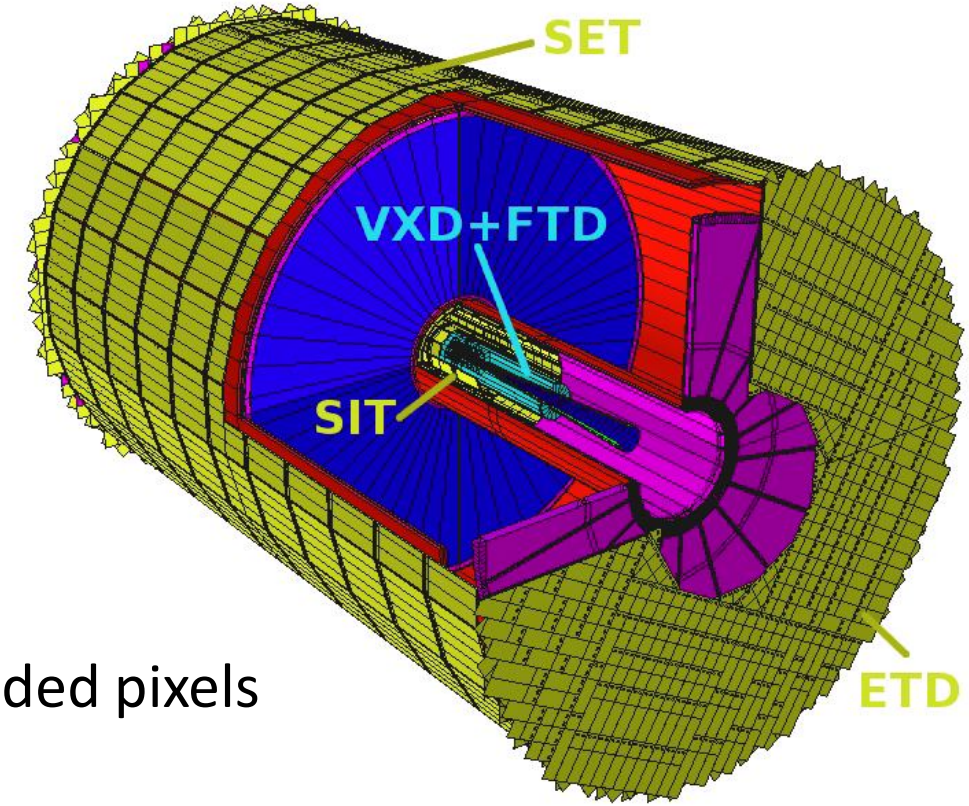
- spatial resolution near the IP: *≤3 μm*
- material budget*: ≤ 0.15%X $_0$/layer*
- pixel occupancy: *≤ a few %*
- radiation tolerance: Ionising dose: *100 krad/ year*
  Non-ionising fluences : *≤10^{11} n_{eq}/ (cm^2 year)*
- first layer located at a radius: *~1.6 cm*

Silicon tracker specifications:

- σ_{SP} : *≤ 7 μm* → small pitch (50 μm)
- material budget: *≤ 0.65%X $_0$/layer*

Baseline design

ILD-like design



- VXD： 3 layers double-sided pixels
- Si-tracker：

  FTD — 7 disks (2 disks with pixels and 5 disks with Si strip sensor) on each side

  SIT — 2 inner layers Si strip detectors

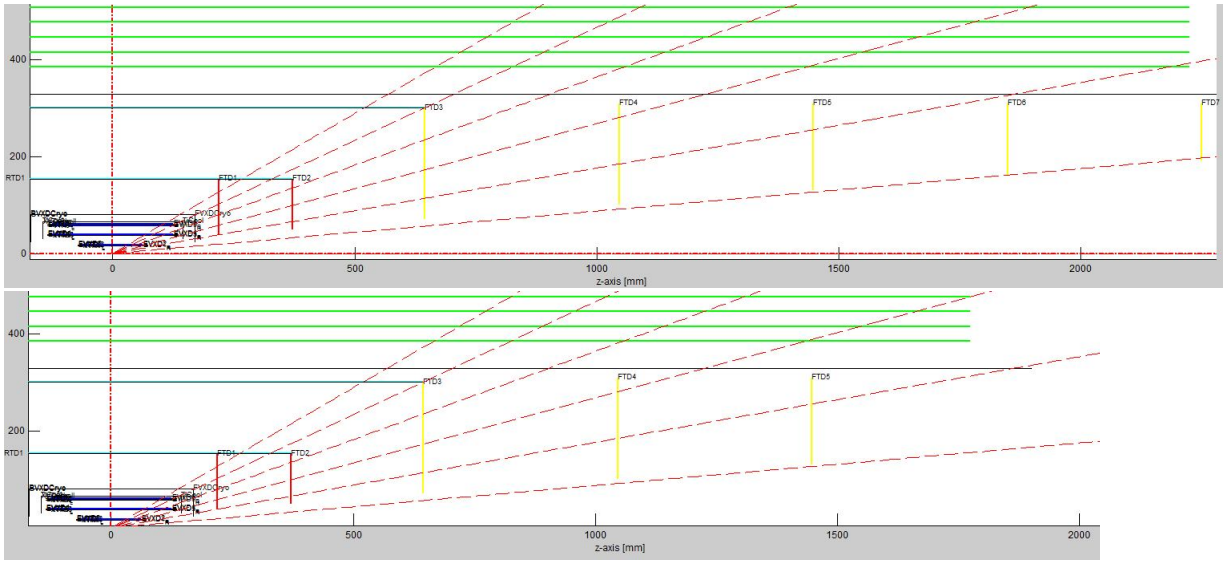
  SET — 1 outer layer Si strip detector

  ETD — 1 end-cap Si strip on each side

Baseline design: forward region

L*=1.5m

An alternative layout is being investigated for the constraints induced by the QD0 at 1.5m



ILC_ILD

Smaller TPC
without FTD6, 7

- Remove FTD6 and FTD7 will ruin the IP resolution for tracks <10 degrees (and if smaller TPC, worse momentum resolution)
- One more pixel measurement can save the IP resolution
- further optimization studies needed based on IP design and background

Simulation and performance optimization studies

- LDT simulation setup

  LDT: Fast simulation using **Kalman filter**

  – A helix track model inclusion **multiple scattering**

  – Simplified **simulation** + track **reconstruction**

  – **"Validated" by CLIC CDR**

- Studies

  – Dependence on material budget

  – Dependence on single point resolution

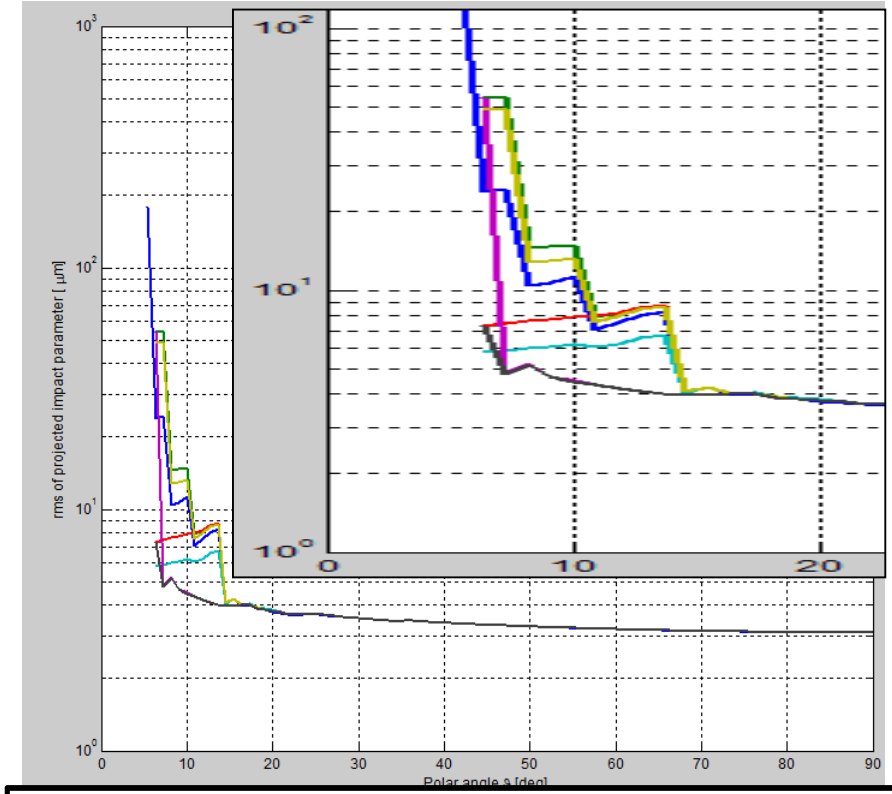
  – Dependence on arrangement of layers

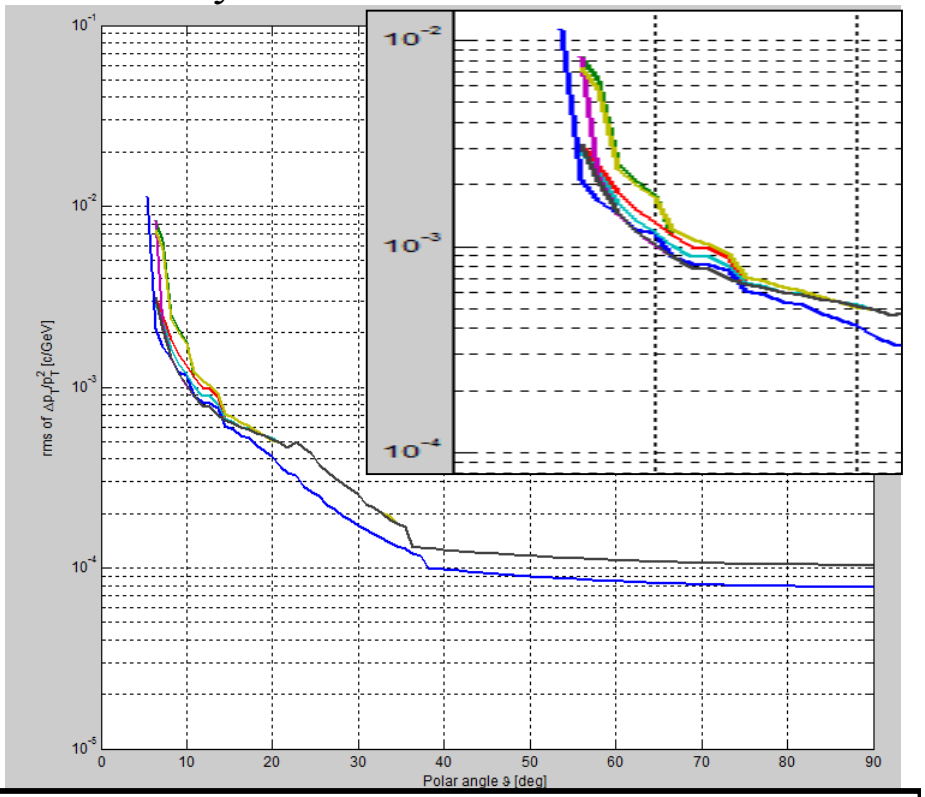
    - R_beampipe=10 mm
    - L*~=1.5m

• If single point resolution worse by 50%, ip.resol worse by 30%/10% for high/low pt tracks
• If material budget increase by a factor of 2, ip.resol worse by 20% for 90 degrees tracks
• Reduce the radius of beam pipe will gain a little

Forward impact parameter resolution and momentum resolution can be cured by 1 additional pixel measurement

Barrel momentum resolution is dominated by the smaller TPC





1，ILC

2，L*=1.5 remove FTD6/7

~~3，2 and insert FTD6/7~~

4，2 and Extend VTX1/2

5，2 and Reduce FTD1 inner radius

6，2 and Add FTD0

7，with both 4 and 5. only slightly better than 4

constrained by IP region, background

Sensor options

Identification of b/c quarks and τ lepton requires:

- Spatial resolution
  - 3um
- Material Budget
  - 0.15% X0/Layer
- Inner-most Layer Radius
  - ~1.6cm
- Occupancy
  - Less than a few %
- Radiation tolerance
  - 1KGy&$10^{11}n_{eq}/cm^2$ per year

→

- Pixel Pitch
  - 20um
- Sensor thinning
  - 50um thick
- Power consumption
  - Less than 50 mW/cm^2 required by air cooling
- Time window
  - 20us (depends on beam induced background)
- Radiation tolerance
  - 1KGy&$10^{11}n_{eq}/cm^2$ per year

- ILC/CLIC Vertex
- DEPFET for BELLEII
- ALPIDE for ALICE upgrade

The same physics, but pulsed colliding mode

Continuous colliding mode

DEPFET for BELLEII

Possible application for CEPC inner most layer:

- 0.15% material budget (0.21% currently)
- 2.5W/ladder in sensitive area
- Time window of 50μs

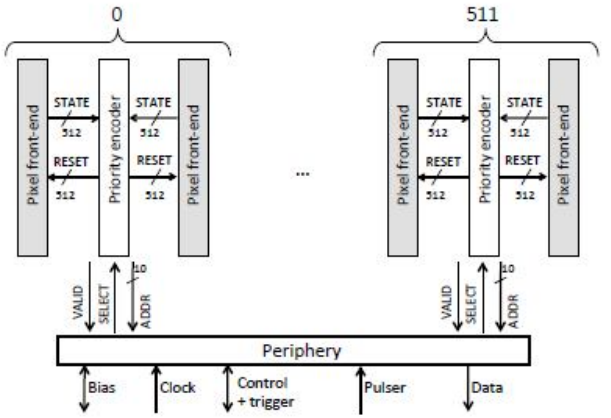
ALPIDE for ALICE Upgrade

- HR-CMOS Sensor with a novel readout structure
  - In-pixel discriminator and digital memory based on a current comparator,
  - In-column address encoder,
  - End-of-column read-out,
  - 22μm*22μm,
  - <50mW/cm^2 expected,
  - Capable of readout every ~4μs.
- The same principle can be applied to SOI
  - Mature process available, 0.2μm KEK-SOI process,
  - Full CMOS circuit,
  - Fully depleted HR substrate,
  - Thinning to 50μm demonstrated.

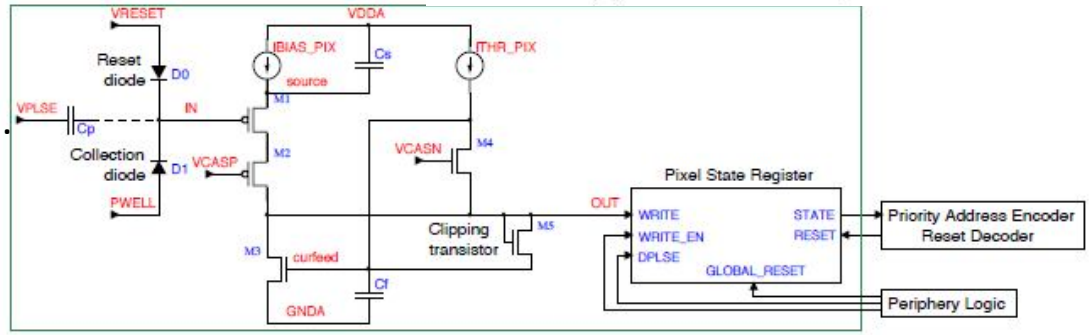
Low power

Read hit pixel only

Data compression



(a) Functional block diagram



(b) In-pixel front-end circuitry of ALPIDE (simplified)

Critical R&D: pixel

- Cooling
  - Air cooling 50mW/cm2 with acceptable vibration due to air flow.
  - CO_2 cooling at the end of ladder.
- Light weight mechanics
  - 0.05%(0.1%) material budget without(with) cabling.
- Sensor thinning to 50μm
- Novel readout structure and low power circuit
  - In-pixel discriminator
  - In-matrix sparsification
- Systematic study on radiation tolerance
  - Mild compared to LHC but careful characterization needed.

Critical R&D: Silicon tracker

- Silicon microstrip sensor
  - Slim edge or edgeless (< 100 um) to avoid material excess from overlapping sensors → mechanical/laser/etching ?
  - Cost-effective sensors with large wafer size (6'' or even 8''); possible different sensor designs for barrel and disks
  - HV-CMOS applicable? (being pursued by ATLAS)
- Front-end electronics
  - Low noise, low power consumption
  - Deep sub-micron CMOS technology, preferably in 65 nm
  - Unified application with other detector readout → to be pursued
- Powering and cooling
  - DC-DC powering to reduce cable material → more results from the detector upgrades of the LHC experiments
  - Air-flow cooling sufficient? Or more aggressive CO2 cooling or even silicon micro-channel cooling?

Summary

- Lots of effort towards pre-CDR
- ILD-like vertex and Si-tracker layout, with some changes on forward region
- simulation
- R&D on HR-CPS and SOI technology possible to start
- Detailed costing methodology needed
- Very tight schedule for pre-CDR documentation

Thank you!

Backup

探测器物理性能和指标要求

b and c Tagging vs. Extrapolation Resolution

Study change in efficiency of b & c tagging in Z0-like flavor composition

R Hawking, LC-PHSM-2000-021

Geometry	$\sigma_{IP}(\mu m)$		
ILC	$5 \oplus 10/p_t$	b purity=0.9	ε_b=0.75
"LHC"	$12 \oplus 70/p_t$	b purity=0.9	ε_b=0.25
R_{in} 1.2cm	$4 \oplus 7/p_t$	c purity=0.7	ε_b=0.49
↓ 2.1cm	$5.5 \oplus 14/p_t$		ε_b=0.40

Total efficiency = ε^N， with N = number of jets to be tagged

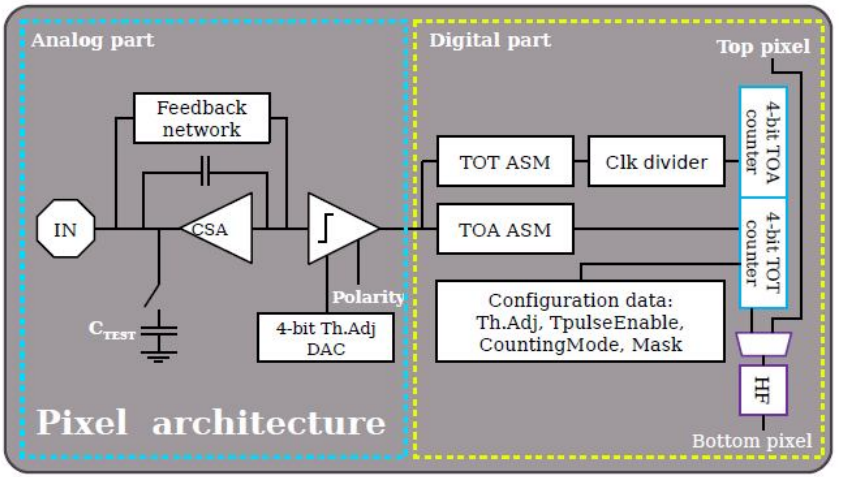
Experiment	BELLE-II	ILC	STAR	ILC	CLIC_ILC
Technology	DEPFET	DEPFET	MAPS	MAPS	Hybrid
Active Area (cm^2)	~220	~3300	~1500	~3300	~10000
Spatial Resolution	10um	3~5um	6um	3um	3um
Power	360W	~20W*	~350W	~20W*	~470W
R.O. Speed	20us	25-100us	200us	10us	10ns
Duty Cycle	1	1/200	1	1/200	156ns/20ms
Material Budget (X_0/Layer)	0.2%	0.15%	0.37%	0.15%	0.2%

Upgrade of the ALICE Inner Tracking System

Based on high resistivity epi layer MAPS
3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)
Radial coverage: 21-400 mm
~ 10 m^2
$|\eta|<1.22$ over 90% of the luminous region
0.3% X0/layer (IB)
0.8 % X0/layer (OB)
Radiation level (L0): 700 krad/10^{13} n_{eq} cm^{-2}

Expt-System	σ_t	σ_{sp}	TID	Fluence	T_{op}
STAR-PXL	≤ 200µs	~5µm	150kRad	$3 \cdot 10^{12} n_{eq}/cm^2$	30°C
ALICE-ITS	***10~30µs***	~5µm	***700kRad***	***$10^{13} n_{eq}/cm^2$***	30°C

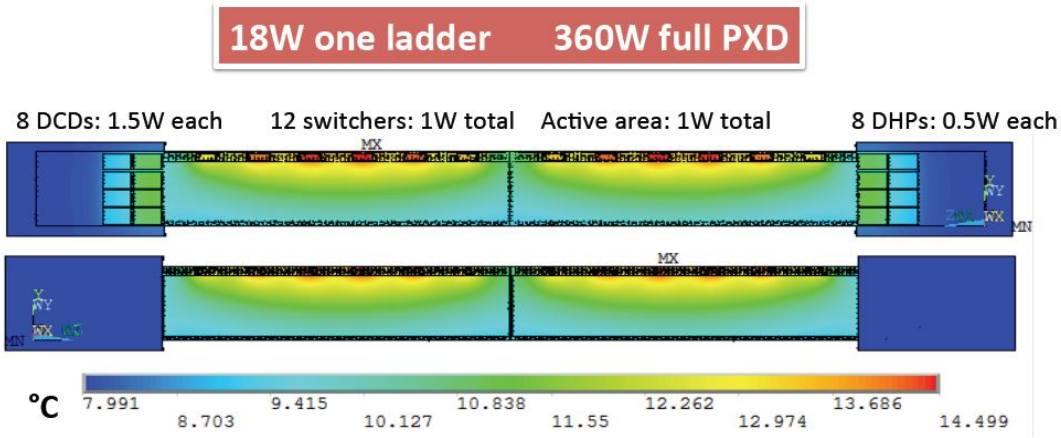
CLIC Vertex



- Much shorter time window(10ns)
  - imposes higher power consumption
  - and thus higher cooling capability.
  - 20us for ILC (possibly longer for CEPC).
- Hybrid Pixel with 65nm-based readout chip
  - In-pixel measurement and fine time stamping (10ns)
  - **470W in total(50mW/cm^2)** with power pulsing applied(reduction to 1/20).
- Air cooling (50mW/cm^2)
  - 150-190g/s mass flow for CDR layout,
  - **20g/s mass flow for the improved layout named "Spiral Discs".**
  - Also 20g/s mass flow for ILC layout but with a smaller heat load(~10mW/cm^2).

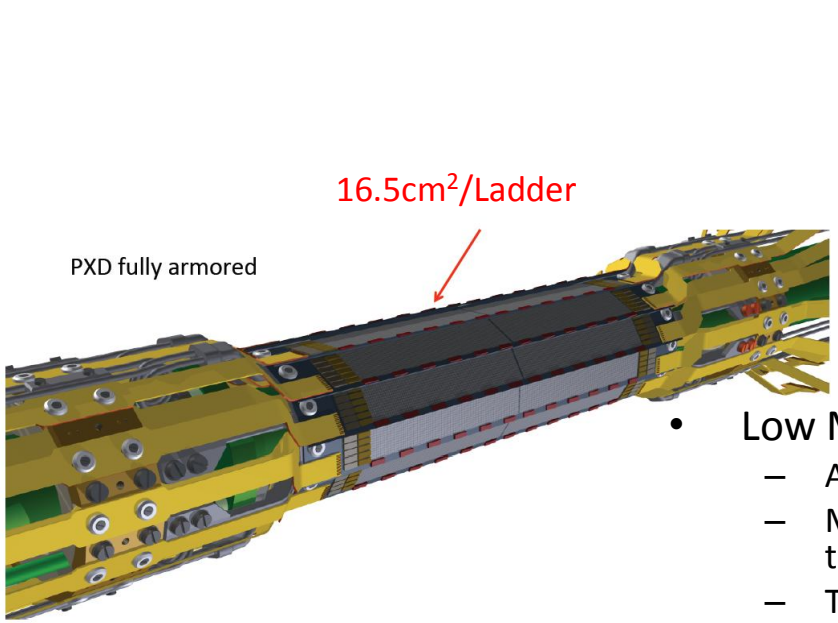
Power Pulsing is the key ingredient leading to a low power solution!

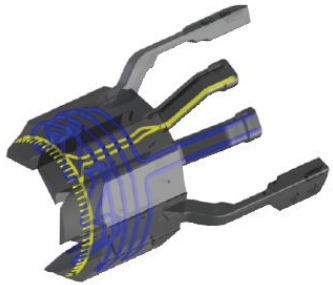
DEPFET for BELLEII



- Short time window of 20us
- Continuous readout:
  - 16W cooled by CO_2
  - 2W cooled by air flow
- Possible application for CEPC inner most layer:
  - 0.15% material budget (0.21% currently)
  - 2.5W/ladder in sensitive area
  - Time window of 50us

Pixel Array:
- 500(column)*1050(row)
- 25um*25um within |z|<1cm
- 50um*25um within 1<|z|<2cm
- 100um*25um within |z|>2cm



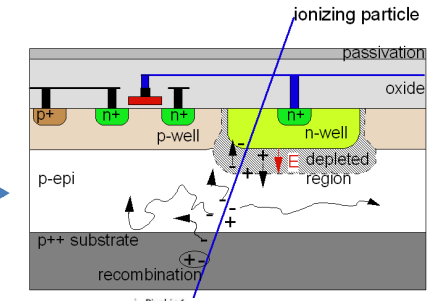


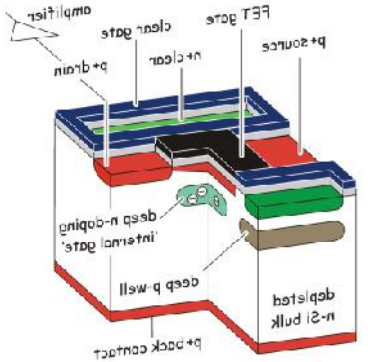
- Low Material Budget Cooling
  - All-silicon module
  - Massive structures outside the acceptance to cool down the readout chips(CO_2)
  - The sensor in the center relys on cold air

高密度、低功耗Si sensor及读出ASIC

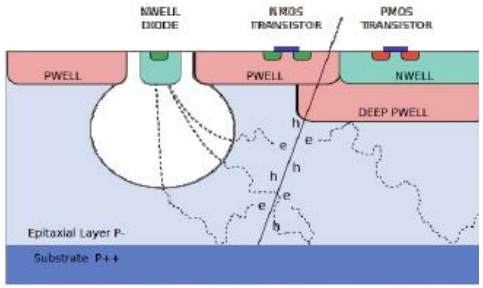
MONOLITHIC PIXEL DETECTORS

较成熟技术

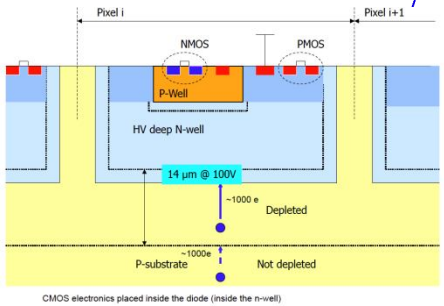




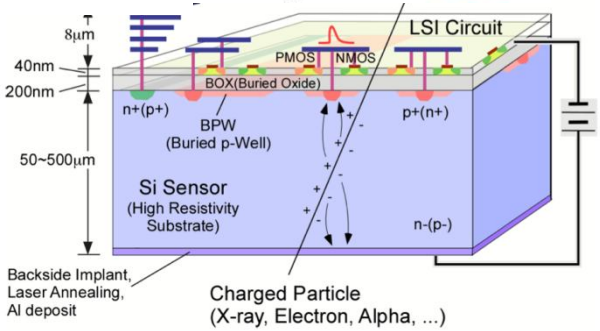
新发展技术



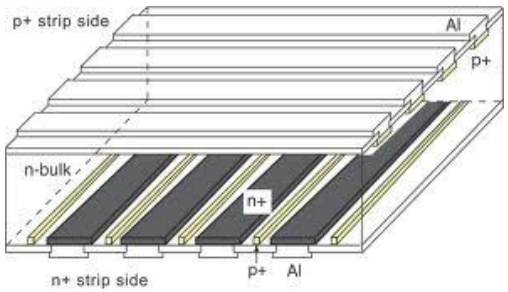
Schematic cross-section of CMOS pixel sensor (ALICE ITS Upgrade TDR)



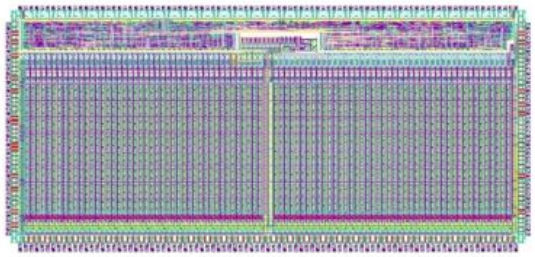
CMOS electronics placed inside the diode (inside the n-well)



CEPC探测器与ILC的区别：不是power plusing的工作模式，ILC的Sensor Option全是基于bunch train的时间结构来构建读出架构的。

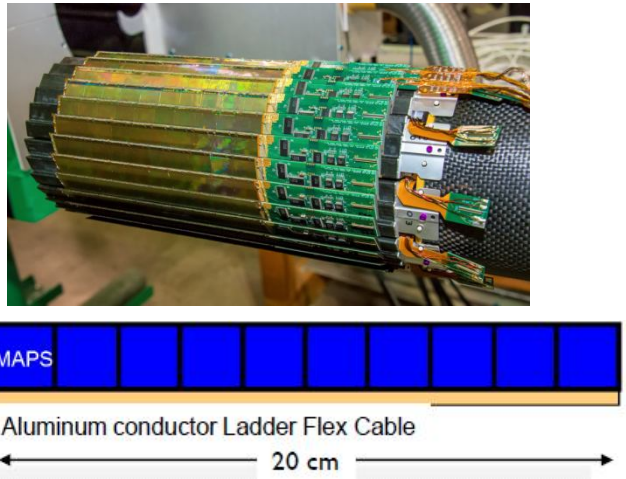


thinner, edgeless or 3D active edge, lower voltage biased strip sensors



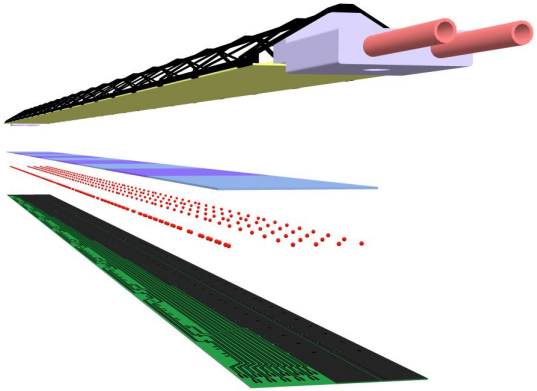
deep submicro CMOS technology (130 nm → 65 nm)

Mechanics and integration

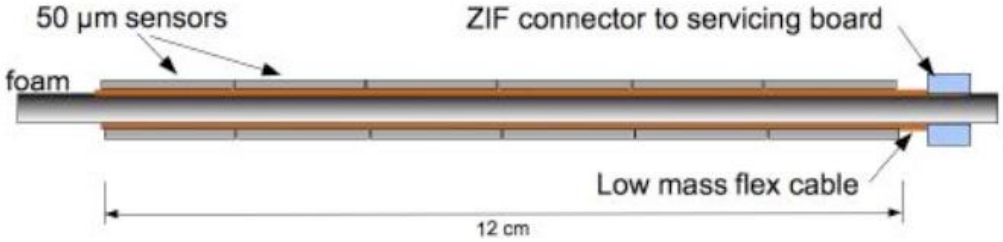


0.37 % X0 per layer

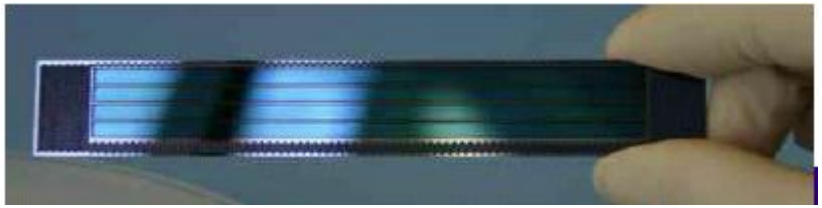
0.21 % X0 per layer



0.3% X0/layer



PLUME:0.2-0.3% X0



DEPFET with self-supporting handle wafer 0.11% X0