

# Silicon-Tungsten ECAL R&D

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**Jiao Tong University, Shanghai**  
**12 / 09 / 2014**

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# Si-W ECAL for ILD

Work of many groups:

LLR (Palaiseau), LAL (Orsay), LPNHE (Paris), LPC (Clermont), LPSC (Grenoble),  
Tokyo, Kyushu

## Adaptation for CEPC

“Small ILD” model: simulation & mechanical model

1<sup>st</sup> Cooling Studies

# an ECAL optimised for the PFA

## Requiments:

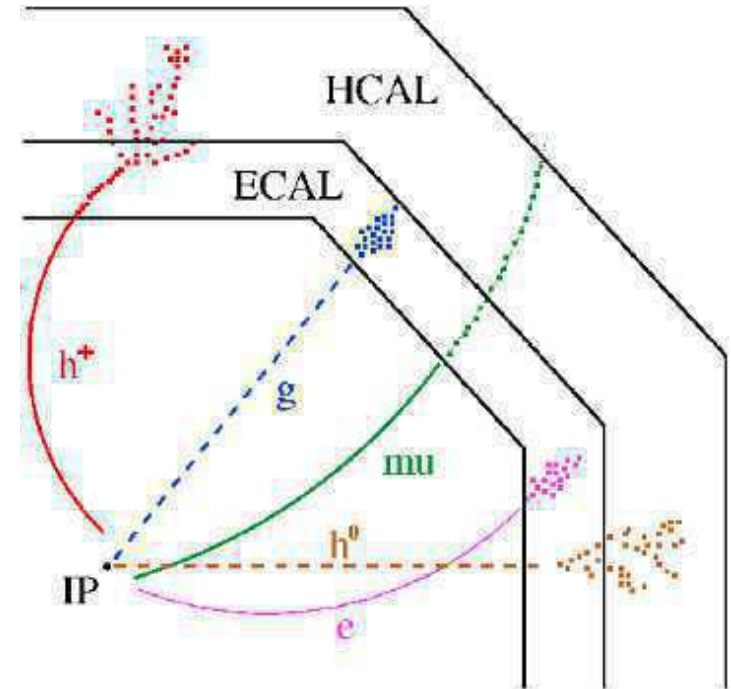
- Measure the photons
- Identify the electrons deposits (to be removed)  
↔ tracks
- Follow the tracks
  - to a eventual hadronic interaction
- measure the non-charged hadrons  
(1/3 interact in the ECAL)

## IN HIGH E JETS

⇒ Excellent Imaging capacities, separation

- Compact showers: Si-W ECAL

⇒ Good resolution for  $\gamma$ ,  $h^0$

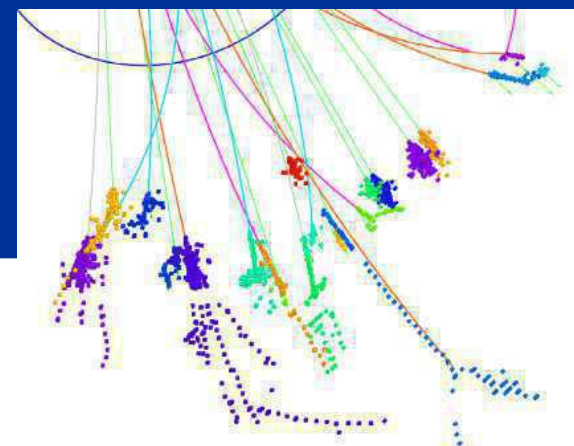


## Particle Flow Algorithms :

- Jets = 65% charged + 25%  $\gamma$  + 10%  $h^0$   
Tracks ECAL CALO's
- TPC  $\delta p/p \sim 5 \cdot 10^{-5}$ ; VTX  $\sigma_{x,y,z} \sim 10 \mu\text{m}$

H. Videau and J. C. Brient, "Calorimetry optimised for jets," in Proc. 10th International Conference on Calorimetry in High Energy Physics (CALOR 2002), Pasadena, California. March, 2002.

# Imaging Calorimetry



Imaging Calorimeters 1000× current granularity

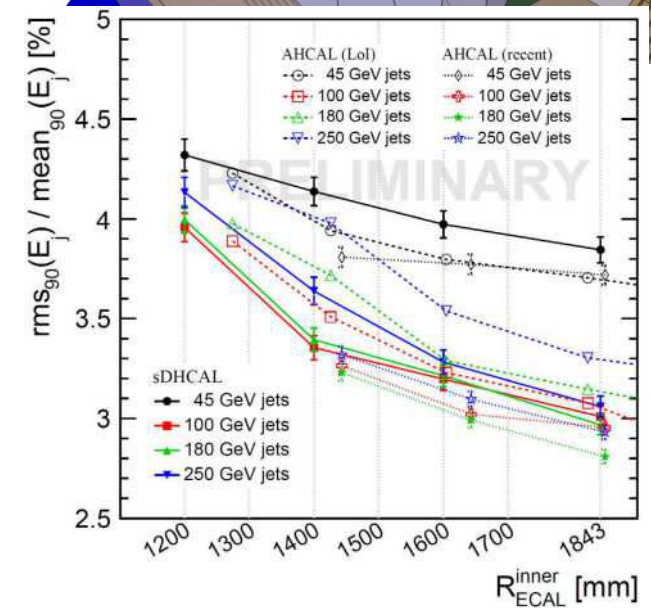
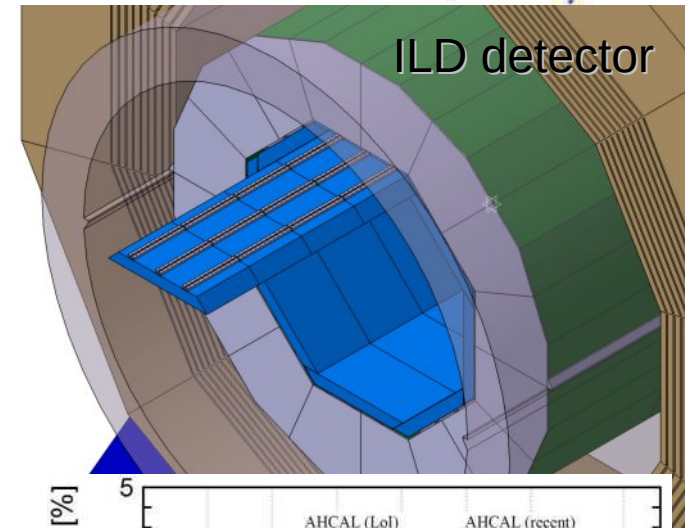
- wrt LHC: data rate ↘↘ but embedded electronics
- Pattern recognition

Needed R&D:

- Dimensioning, Mechanics (uniformity), Sensors, Electronics, VFE, Power Consumption, Thermal dissipation & uniformity
- Iterative construction & test of Prototypes
- Detector & Integration
  - Optimisation : Physics vs cost, services (PP, cooling)

Dedicated SW tools for PFA:

**Difficulty : perf in JER = HW ⊗ SW**



# SiW ECAL: Physics & Technological prototype

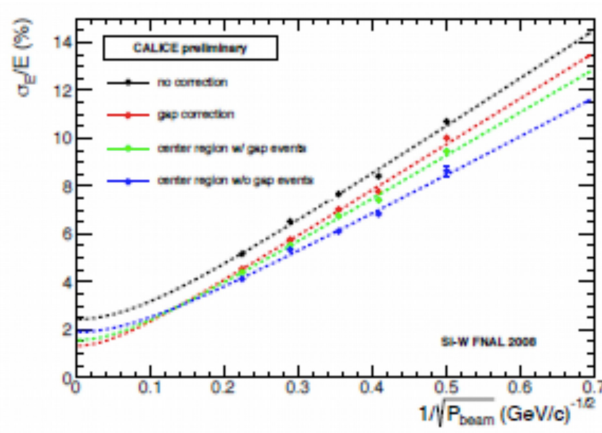
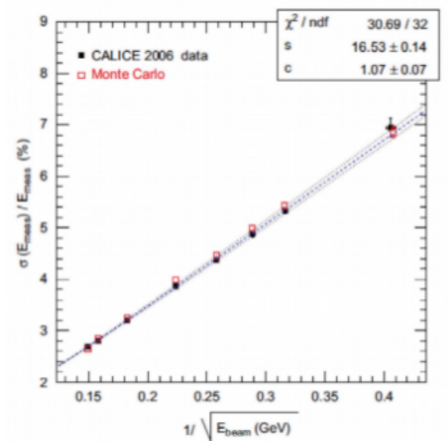
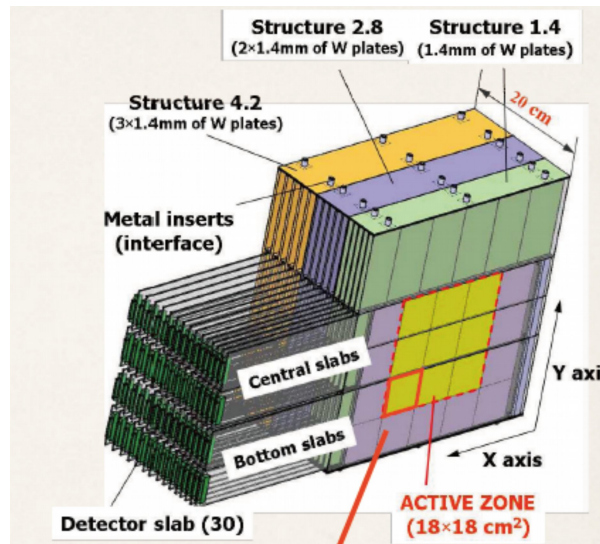
## Physics prototype: 2005-2011

PFA proof of concept with comparison to MC (PandoraPFA etc.)

Electronics outside

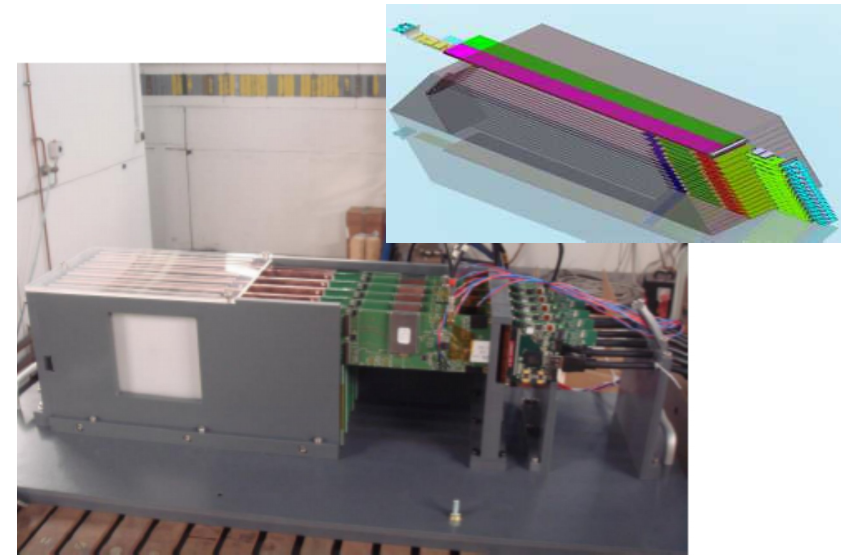
- 1cm x 1cm pixels
- full 30 layers

(used for PAMELA sat.)



16.5%(stochastic) 1–2% (constant) obtained with 1–45 GeV e-/e+ at 2006/2008 BT

## Technological prototype



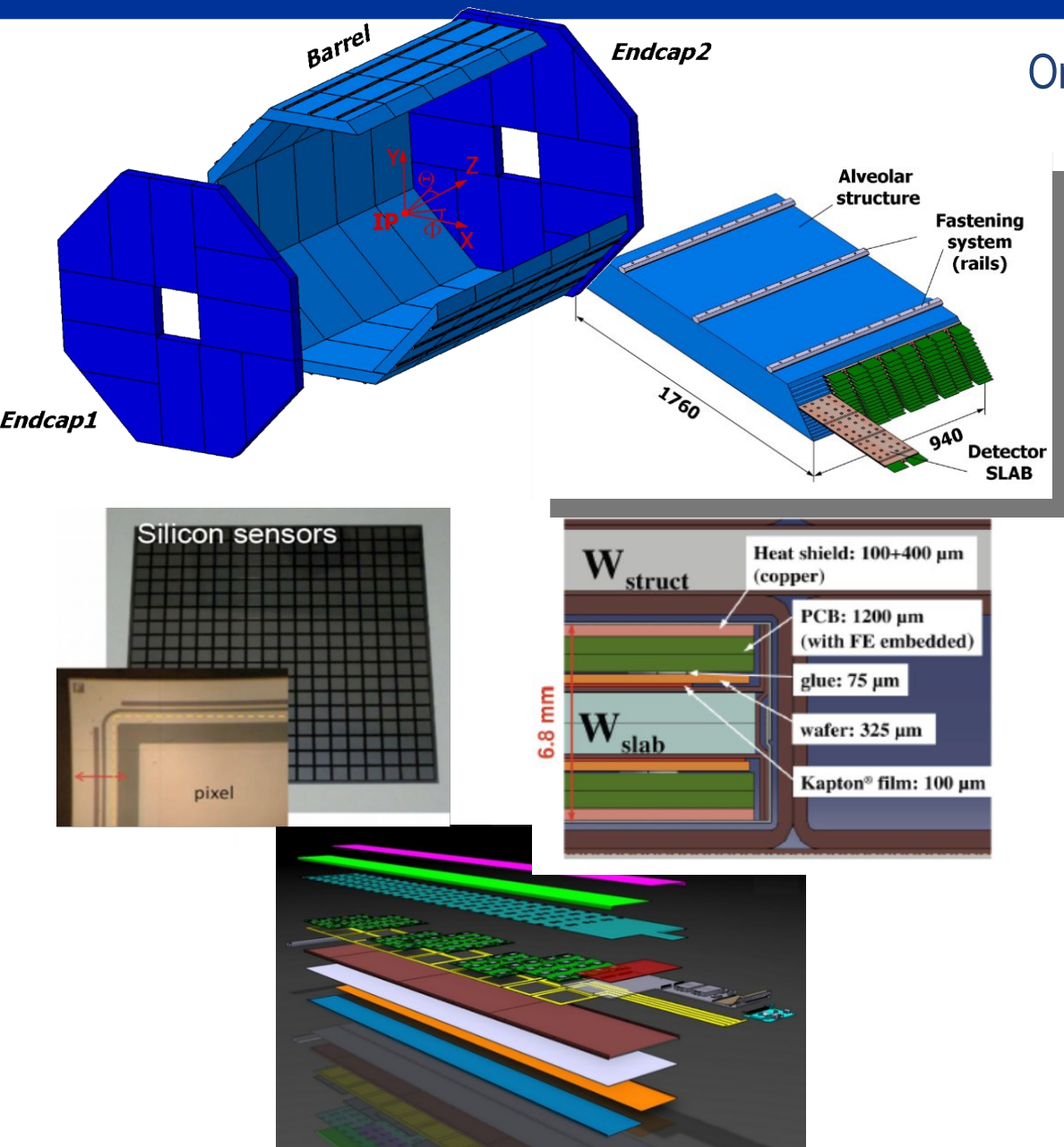
Embedded electronics

- SKIROC2 analog/digital ASICs
  - auto-triggered, zero suppr., PP
- pixels 5x5mm<sup>2</sup>

Assess the feasibility

Establish procedures and develop test benches for mass production

# The SiW-ECAL of ILD



## On going R&D

- **Thermic & Mechanical studies**
  - Production, Characterisation & Monitoring
  - Thermic simulation & cooling
    - Also for the CMS-HGCAL
- **Assembly: Quality tests & preparation of large production for ILD**
  - VFE, PCB's, ASU's
  - TB, Cosmics, Charge injection
- **Wafers:**
  - Guard Ring Studies
  - Characterisation
    - Charge injection by Laser
- **Optimisation: Cost → reduction of radius**
  - for ILD, CEPC (Dan Yu).

# ECAL structure

Barrel: 5 octagonal wheels

- $R_{\min} = 1808 \text{ mm}$ ;  $R_{\max} = 2020$
- Width = 940mm

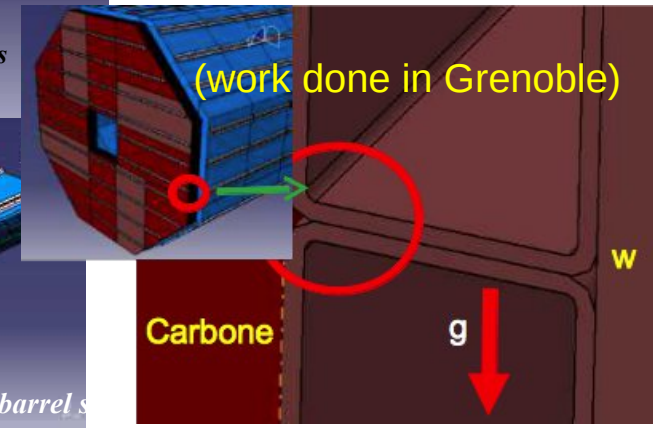
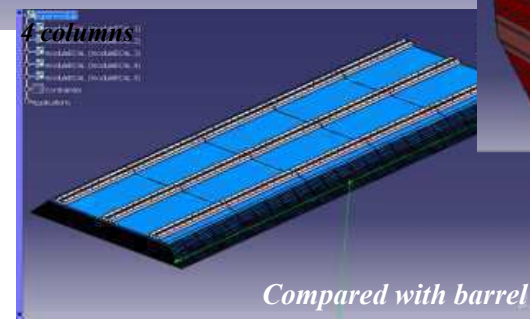
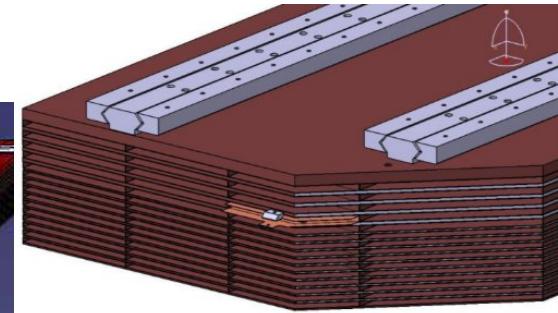
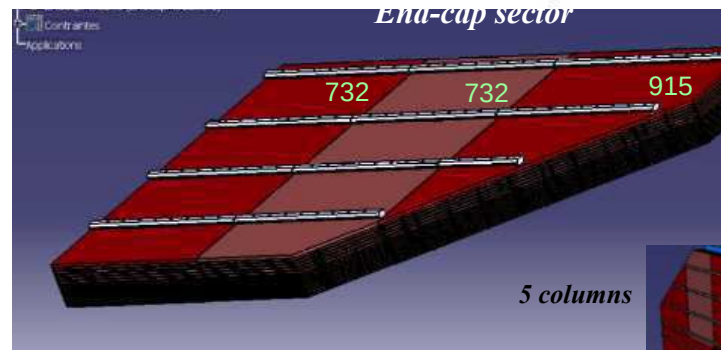
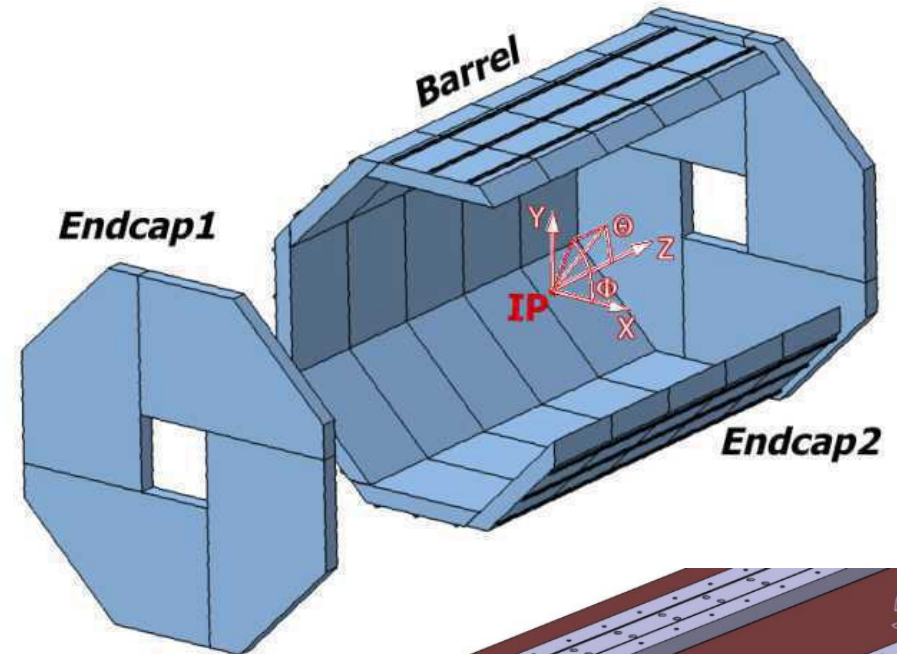
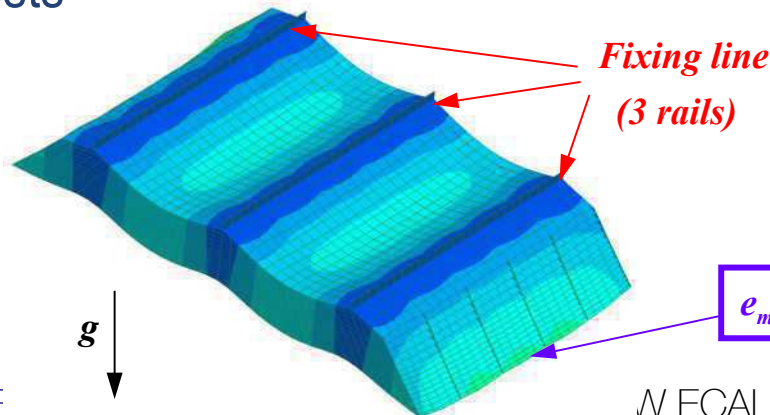
End-caps: 4 quarters

- $\varnothing_{\min} = 800 \text{ mm}$

Carbone / Tungsten structure

- filled with Si or scintillators (option MAPS/DECAL)

Extensive mechanical simulation & tests



$e_{\max} = 0.07 \text{ mm}$

# ECAL : Composite Structure (barrel)

Carbon Fiber + Tungsten

- Prod : dec 2011 (5 yrs of R&D)
- 600kg, 15 layers

15 alveoli produced, 1 faulty

1 equipped with Fiber Bragg-Grated (FBG)

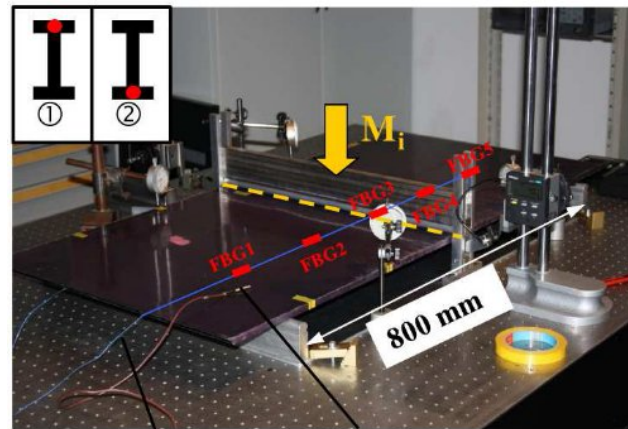
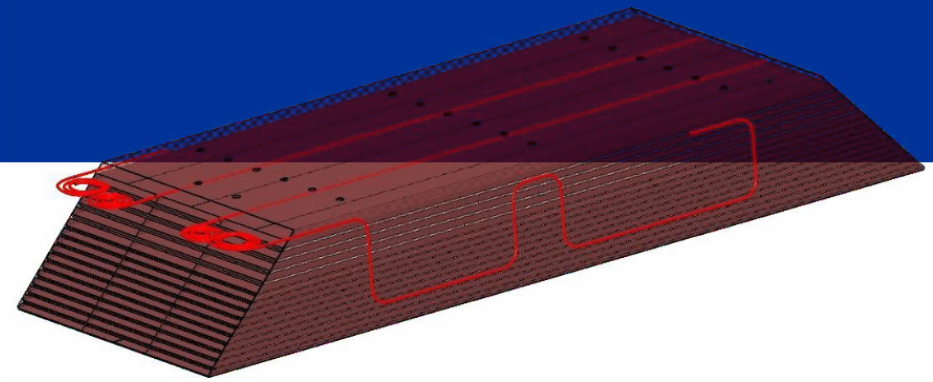
⇒ Comparison calculation and measurement

Assembling mould

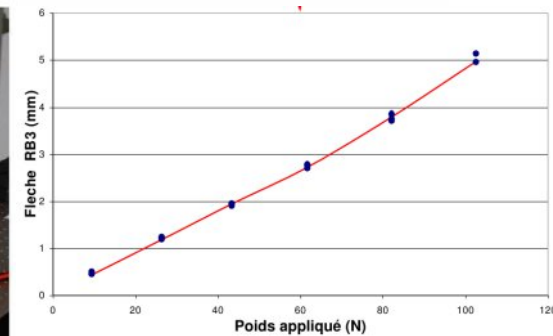
- Cooking in autoclave

Metrology

- Minor on-side deformation



Optical fiber Thermal sensor



Vérification des paramètres du modèle en comparant la flèche FBG3 mesurée et simulée



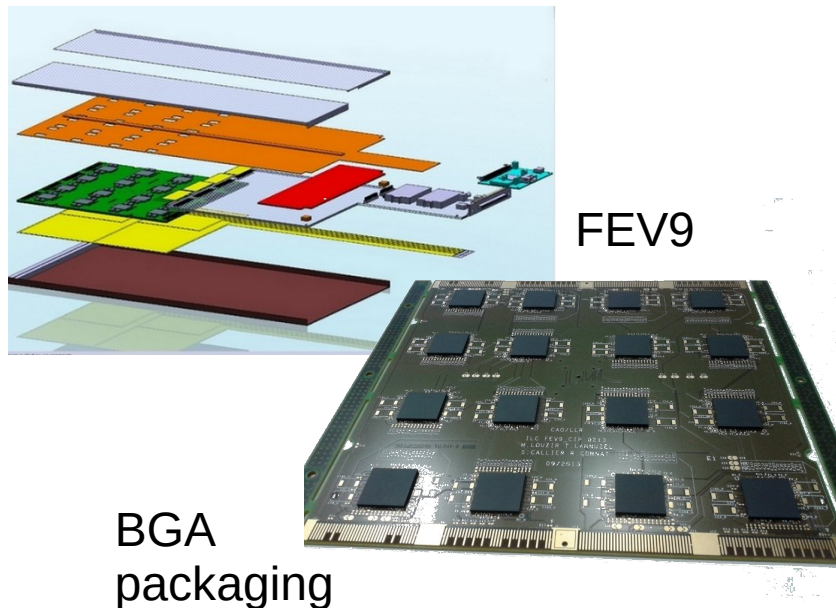
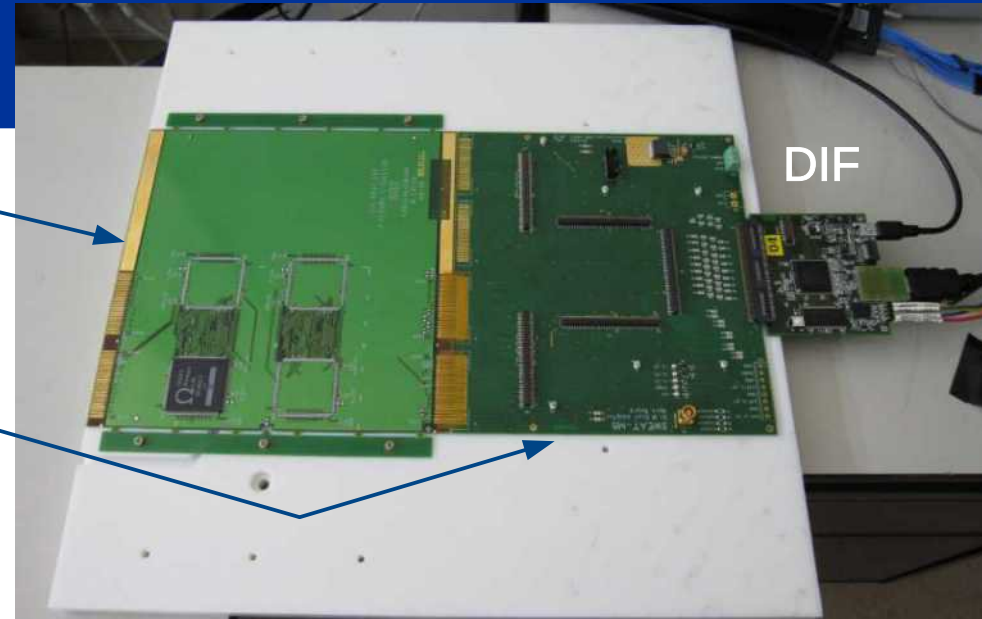


# ECAL : FE Boards

Tests of (early) FEV7 CIP et COB PCB  
(now FEV11 in production)

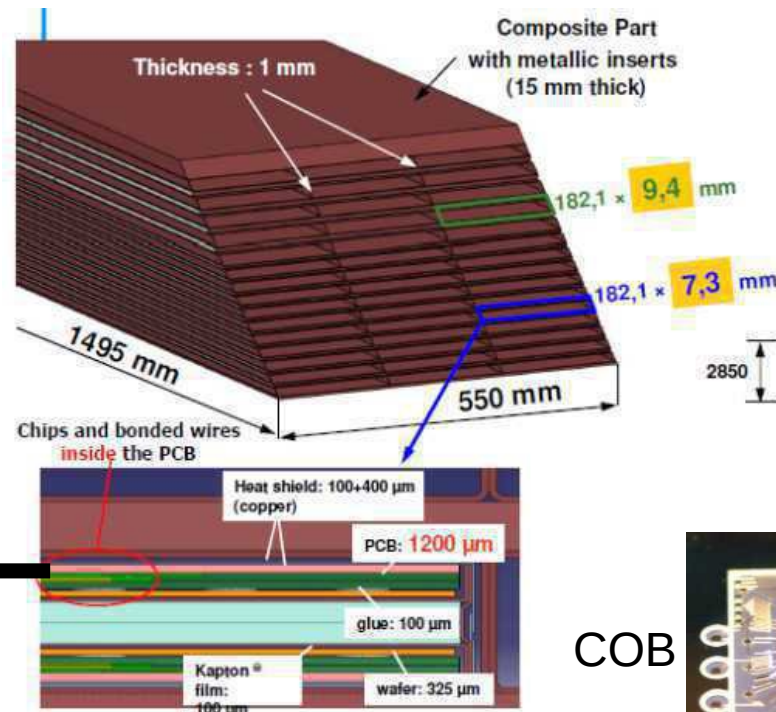
“Adaptator” board

- Interface to cooling
- Buffer for power pulsing
  - with super-capacitors (super-C)
- Connexions tested in strong B field  
→ DESY (02/2013): no effect

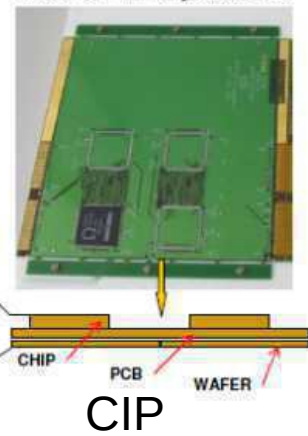


FEV9

BGA packaging



FEV7 CIP at the present time



CIP



COB

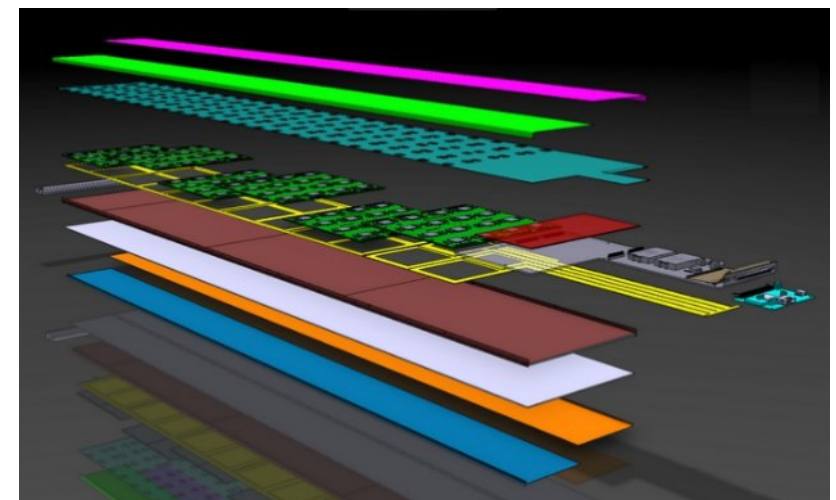
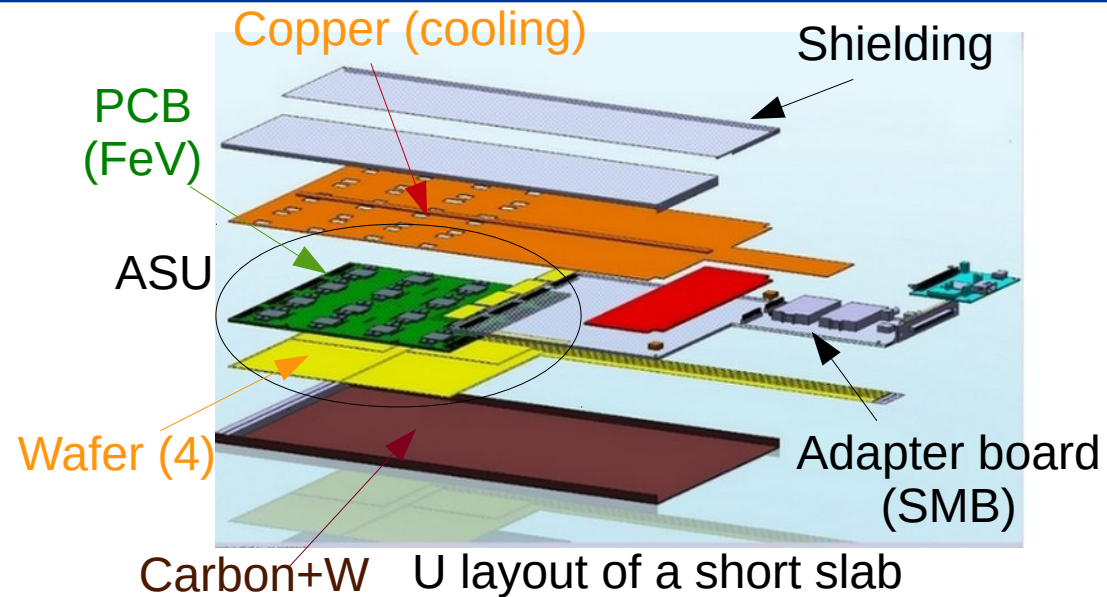
# SLAB Assembly: full chain

R&D for “mass production” and QA

- Quality tests & preparation of large production
- Modularity → ASU & SLABs
  - Choice of square wafers (≠ from hex: SiD, CMS HGICAL)

Numbers ( $R_{ECAL} = 1,8 \text{ m}$ ,  $|Z_{Endcaps}| = 2,35\text{m}$ )  
(likely to be reduced by 30–40%)

- Barrel modules: 40 (as of today all identical)
- Endcap Modules: 24 (3 types)
- Slabs = 6000 (B) + 3600 (EC) = 9600
  - many ≠ lengths
- ASUs = ~75,000
  - Wafers ~ 300,000 (2500 m<sup>2</sup>)
  - VFE chips ~ 1,200,000
  - Channels: 77Mch



# Wafers:

## Key elements of detector

- Basic unit for the size of the detector
- (Most expensive part too)

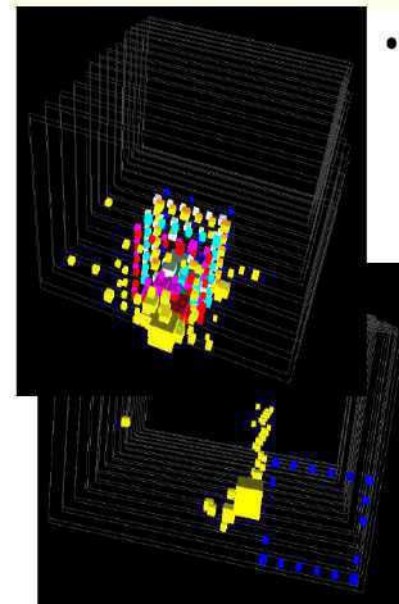
## Guard Rings

- Alternative designs
  - segmented, “edgeless”
- Complete characterisation of sensors  
⇒ link to & test variety of producers
- Work in CALIIMAX-HEP French ANR  
in relation with Kyushu/Hamamatsu

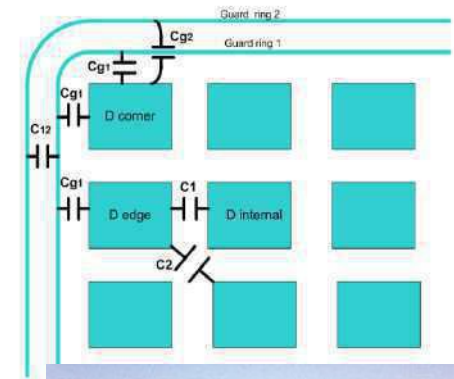
## Test of Silicon sensors

- Test different HPK designs: C-V, I-V.
- Laser tests: xtalk via GR.

## From physics prototype test beams



- “Square events”
  - cross talk between guard rings and pixels



## Plans:

- Irradiation tests ( $\gamma, n$ )
- Validation of GR design in HE electron beam.

# Si-W ECAL for the CEPC

Same mechanical structure as ILD but...

- Rates of machine  $\neq$   $\Rightarrow$  worst case: ~continuous
- no power-pulsing  $\Rightarrow$  VFE power  $\nearrow \nearrow \nearrow$ 
  - 27  $\mu$ W/ch  $\rightarrow$  ~5mW/ch (for 25 ns BX)
    - $\mu$ -power pulsing for slower modes ?

Adaptations:

- Reduced number of layers
  - 30  $\rightarrow$  20 ?
- Less electronics channels
  - 0.5 x 0.5 cm<sup>2</sup>  $\rightarrow$  1x1 cm<sup>2</sup> ?

Radiations ?  $\rightarrow$  leakage current  $\nearrow$

- cooling at -20°C for CMS-HGCAL ?

Performances to be evaluated

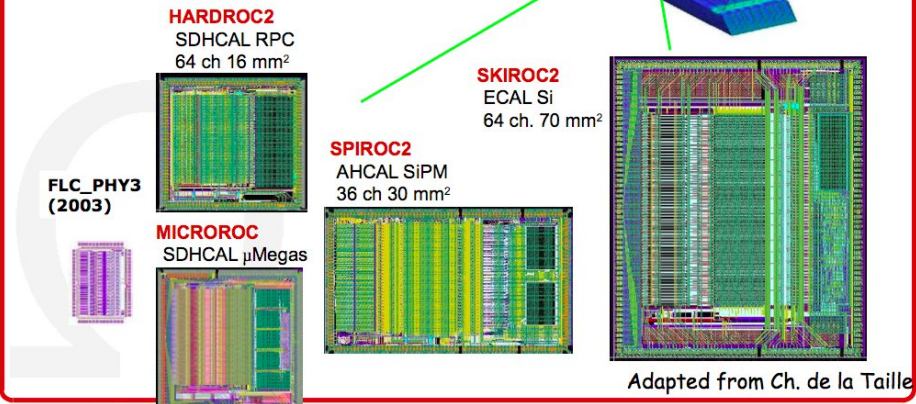
- Occupancy!!!  $\rightarrow$  power consumption
- (Simulation on Small ILD version).

## ROC family 2nd Generation ASICs

FE electronics adapted for the ILC:

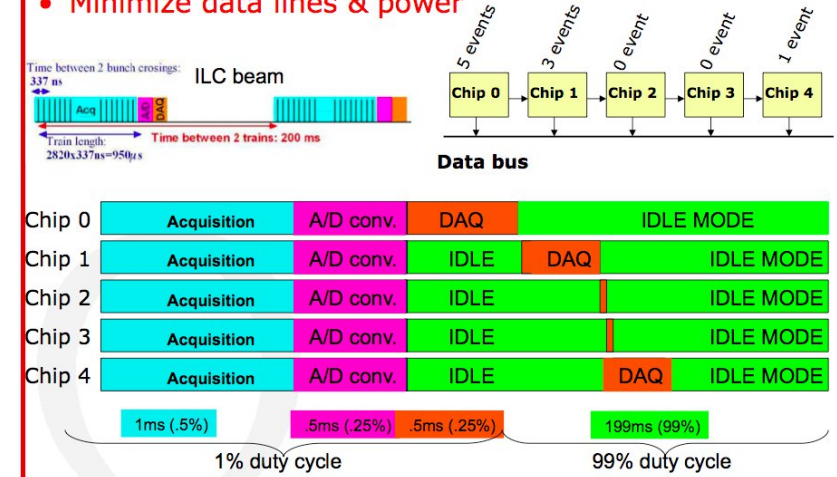
- Add **auto-trigger**, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ...)

Technological prototypes



## Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power



Slide from Ch. de la Taille

# Exemple of design with cooling

## Passive cooling

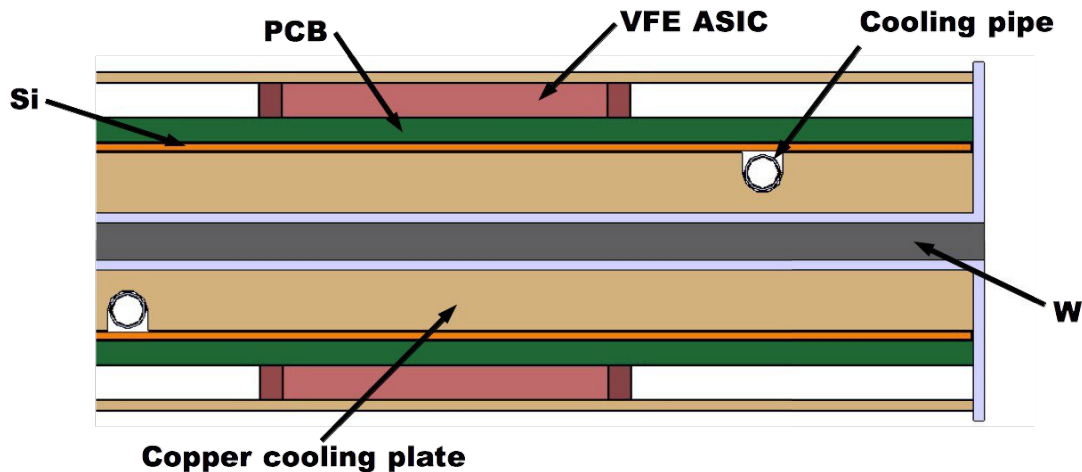
- too much gradient in Si...

## Active cooling

- Evaporative CO<sub>2</sub> cooling in thin pipes embedded in Copper exchange plate

- for CMS-HGCAL : 33mW/cm<sup>2</sup>
  - down to 0.6×0.6cm<sup>2</sup> OK (safety margin of 2)

→ To be modelled for Mokka simulation



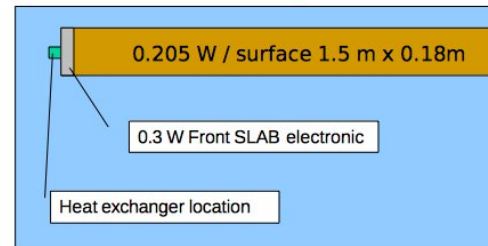
## Thermic Studies & Cooling for ILD

**Power dissipation** : Final goal with power pulsing 1/100 s

For 1/2 SLAB from barrel  
 Wafers consumption : 0.205 W  
 Front SLAB electronic : 0.3 W

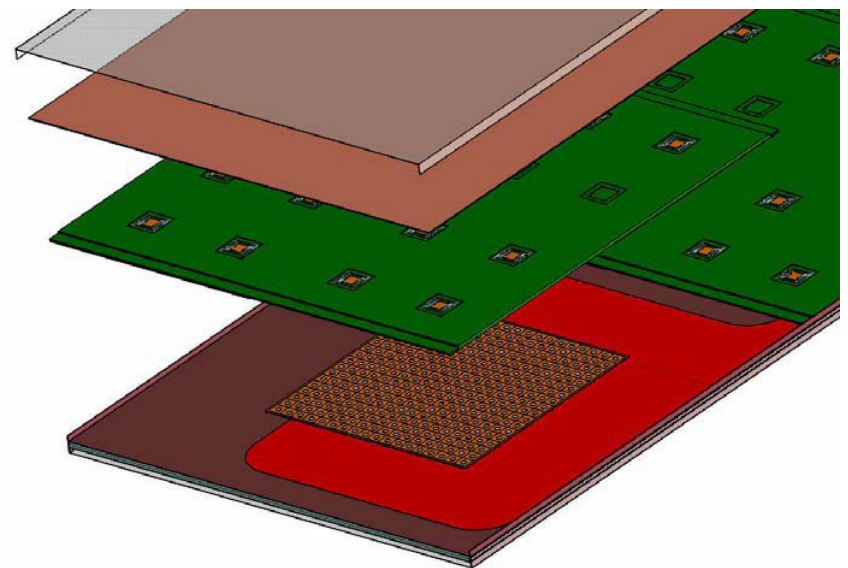
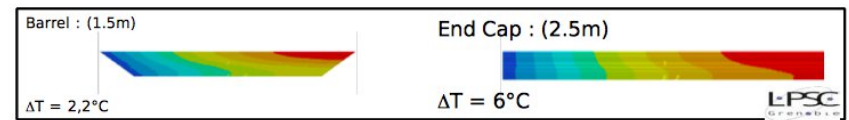


Ecal detector : 4.5 kW



Passive cooling : OK

... support up to 10x bigger heat load (for details see backup)



# Simulation studies

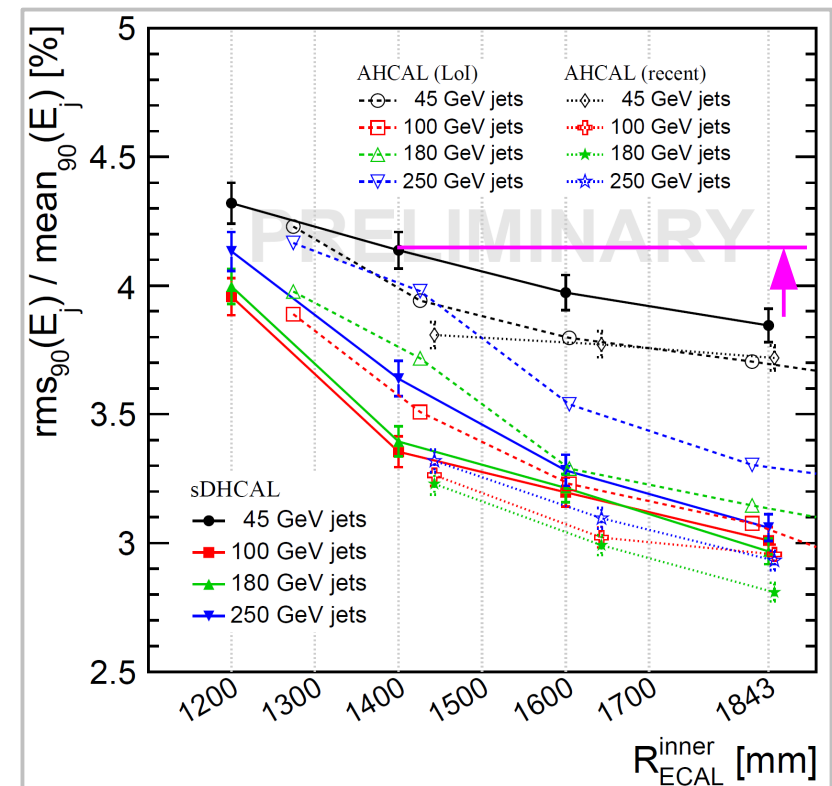
Shown @ LCWS'13 (work by Trong Hieu Tran)

<https://agenda.linearcollider.org/getFile.py/access?contribId=67&sessionId=35&resId=0&materialId=slides&confId=6000>

- Evaluation of the JER vs  $R_{INNER}$  ( $\leftrightarrow R_{TPC}$ , @ fixed R/L ratio).
- Using PandoraPFAnew v0.12 and full calibration procedure
  - $\mu$ ,  $\gamma$ ,  $K^0_L$  samples  $\Rightarrow$  ECAL/HCAL intercalib + E2H/H2H + angular corr.
- ILD\_o1/2\_v05(SEcal04, AHCAL/SDHCAL)
  - SiW ECAL:  $5 \times 5$  mm<sup>2</sup>,  
AHCAL:  $3 \times 3$  cm<sup>2</sup>, sDHCAL:  $1 \times 1$  cm<sup>2</sup>

## Results

- $\leq 10\%$  for  $RI_{INNER} = 1800 \rightarrow 1400$ mm



# Variation of $N_{\text{Layers}}$

PhD student in co-tutelle LLR / IHEP  
on ILC / CEPC ECAL

Shown @ 6<sup>th</sup> ILD Optim meeting (16/07/2014) [Internship work of **Dan Yu (LLR)**]

<https://agenda.linearcollider.org/getFile.py/access?contribId=2&resId=0&materialId=slides&confId=6435>

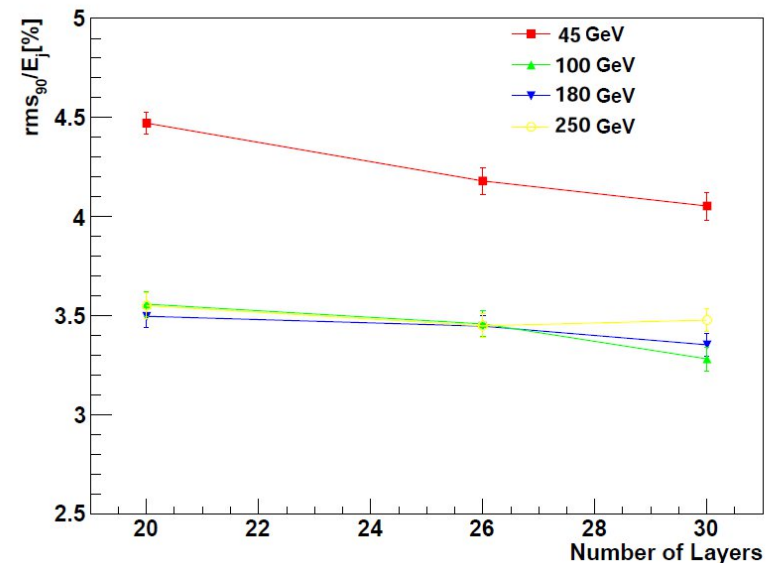
- Variation of ECAL's  $N_{\text{Layers}}$  for  $R=1450\text{mm}$ ,  $HZ_{\text{Barrel}}=1848\text{mm}$  on ILD\_o2\_v05
- Exact Same procedure as previous study
  - Non-Linearity  $\leq 1\%$
- For  $|\cos\theta| \leq 0.7$

number of Si layers	W layers (1st section)	Thickness (mm)	W layers (2nd section)	Thickness (mm)
20	13	3.15	6	6.3
26	17	2.4	8	4.8
30	20	2.1	9	4.2

## Results

- JER +  $\leq 6\%$  @45 GeV

Simulation to be improved in endcaps



# Realistic parameters for small ILD

From preliminary mechanical model  $\Rightarrow$  in simulation & cost

Reduced radius  $R_{\text{INNER}}=1400\text{mm}$ .

Base unit = Wafer size

- Larger Wafers: 6"  $\rightarrow$  8" (OK from HPK, LFoundry); smaller wafers (4") in 2<sup>nd</sup> part ?
- Wafer side:  $\sim 90 \rightarrow 126$  mm; Alveola  $\sim 200\text{mm} \rightarrow 253,8$  mm;

Barrel: **5 modules of 3 alveola**

- $L_{\text{Barrel}} = 3829\text{mm}$  ( $Z_{\text{endcap}} = 3929\text{mm}$ ).

Endcaps: **Quadrants of 2 modules of 2 and 3 alveola**

- with  $R(\text{ECAL Ring}) = 40\text{cm} + \text{Integer number of Wafers} + \frac{1}{2} \text{ Wafers}$   
 $\Rightarrow R_{\text{Endcap}} = 1676\text{mm}$

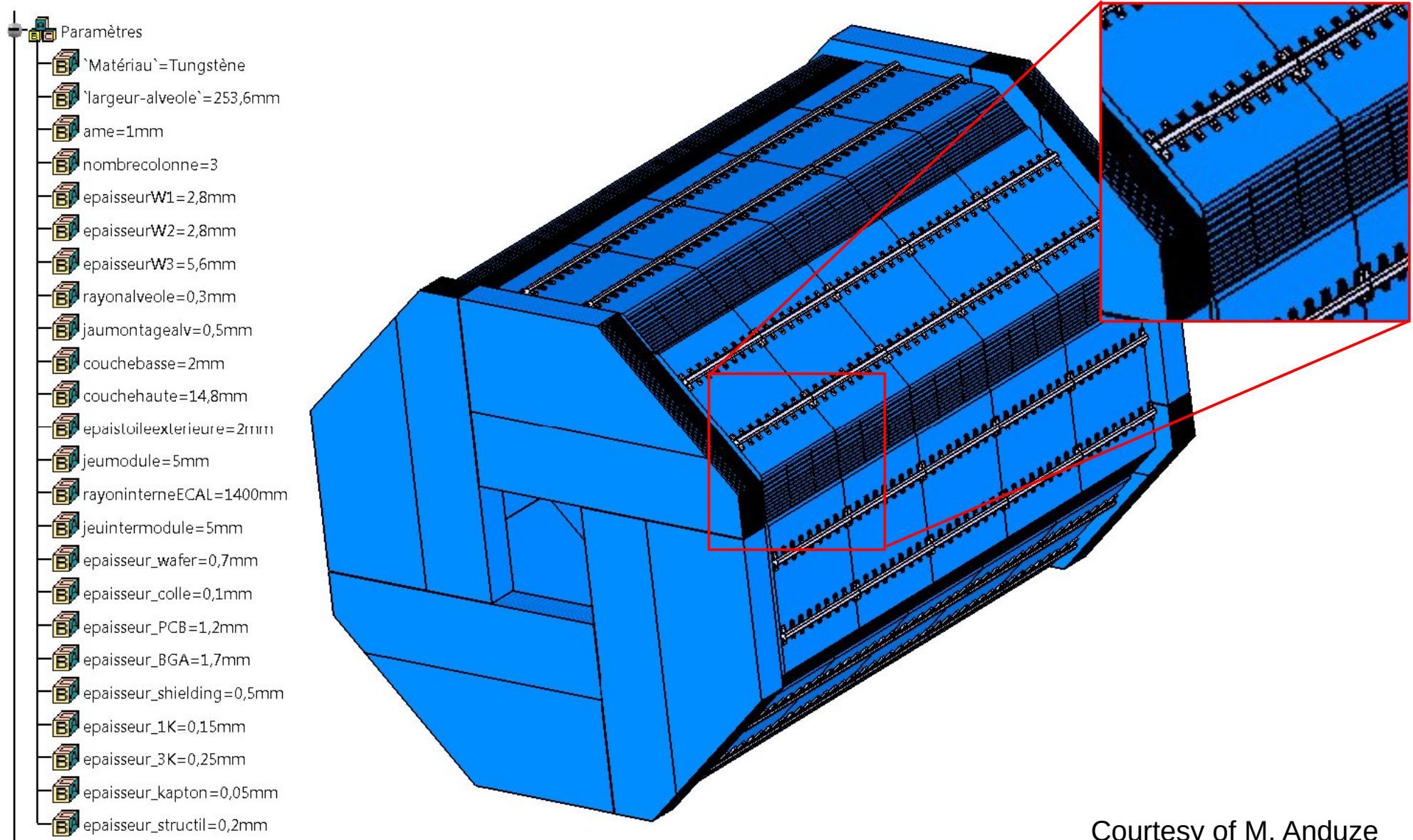
$N_{\text{layers}} = 22 = 14 + 8$  (single and double W thickness)

Wafer thickness 500  $\rightarrow$   **$\sim 725\mu\text{m}$**

- Improved  $\sigma(E\gamma) \propto \sqrt[5]{t} \Rightarrow \sim$ recovery of  $N_{\text{layers}}$  effect.  $\Rightarrow$  compensation of  $N_{\text{Layer}}$  loss.
- ECAL thickness = 223,85 mm



# Mechanical model



Courtesy of M. Anduze

# Small ILD ECAL Cost

Complete re-evaluation for the ressource survey in July (PRELIMINARY)

- **Number of elements**
  - Wafers, ASICs, PCB's, SLABs, structures,
  - moulds, processes, test benches
  - transportation boxes
- **Man•Years**
  - Reception, Tests, Mounting, Installation

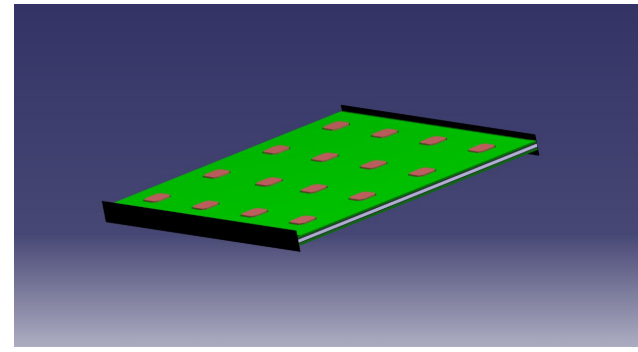
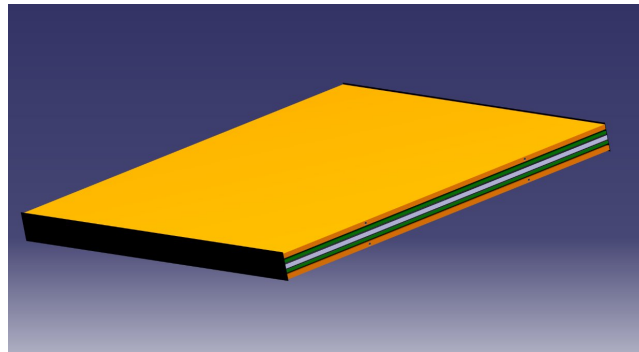
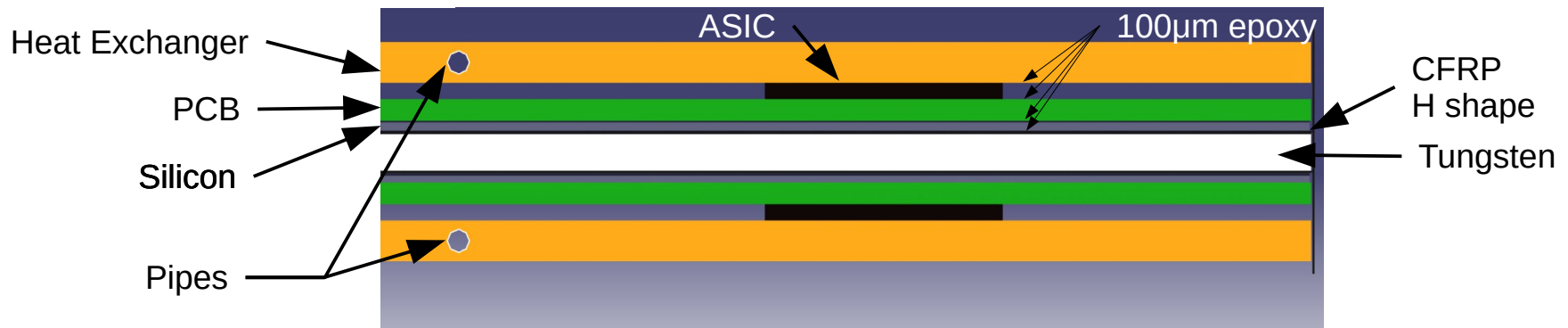
Outcome:

- **Cost ratio 1.4m/1.8m of 47,5%**

# Cooling studies (preliminary)

Based on CALICE and CMS-HGCAL schemes

- cooling with di-phasic CO<sub>2</sub> pipes with extra Copper for heat transfert:



- 3 mm of Cu, 2.8mm of W, Silicon Wafers of 725 µm, pipes of  $\varnothing_{int/ext} = 1.6/1.8\text{mm}$
- Working point of CO<sub>2</sub> : 20°C, Chips power of 10mW/ch × 64 = 0.64W

# ANSYS thermal simulation

Fully transversally isolated system,  
with ASICs a sole heat source, and pipes @ 20°C as heat sink

- purely diffusive model (no convection), at equilibrium,
- ideal heat interfaces, chips packaging, cooling pipes
- 2 side longitudinal modules simulated

Heat conductivity are “best guess” only:

- Epoxy ~ 0.795 W/m.K
- Composite highly anisotropic (high along fibres)
- PCB are laminated of 3% of Cu (385W/m.K) + 97% of FR4 (0.3W/m.K)
- ASICs package choosen as 1 W/m.K

First results, to be re-evaluated...

# Results (very preliminary)

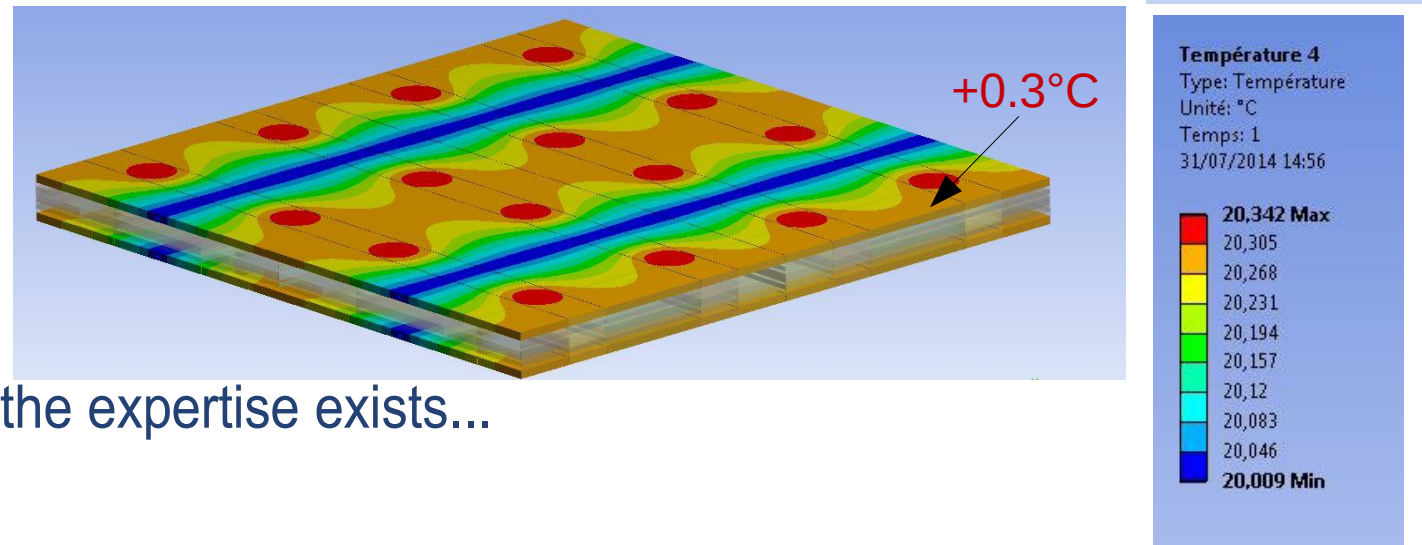
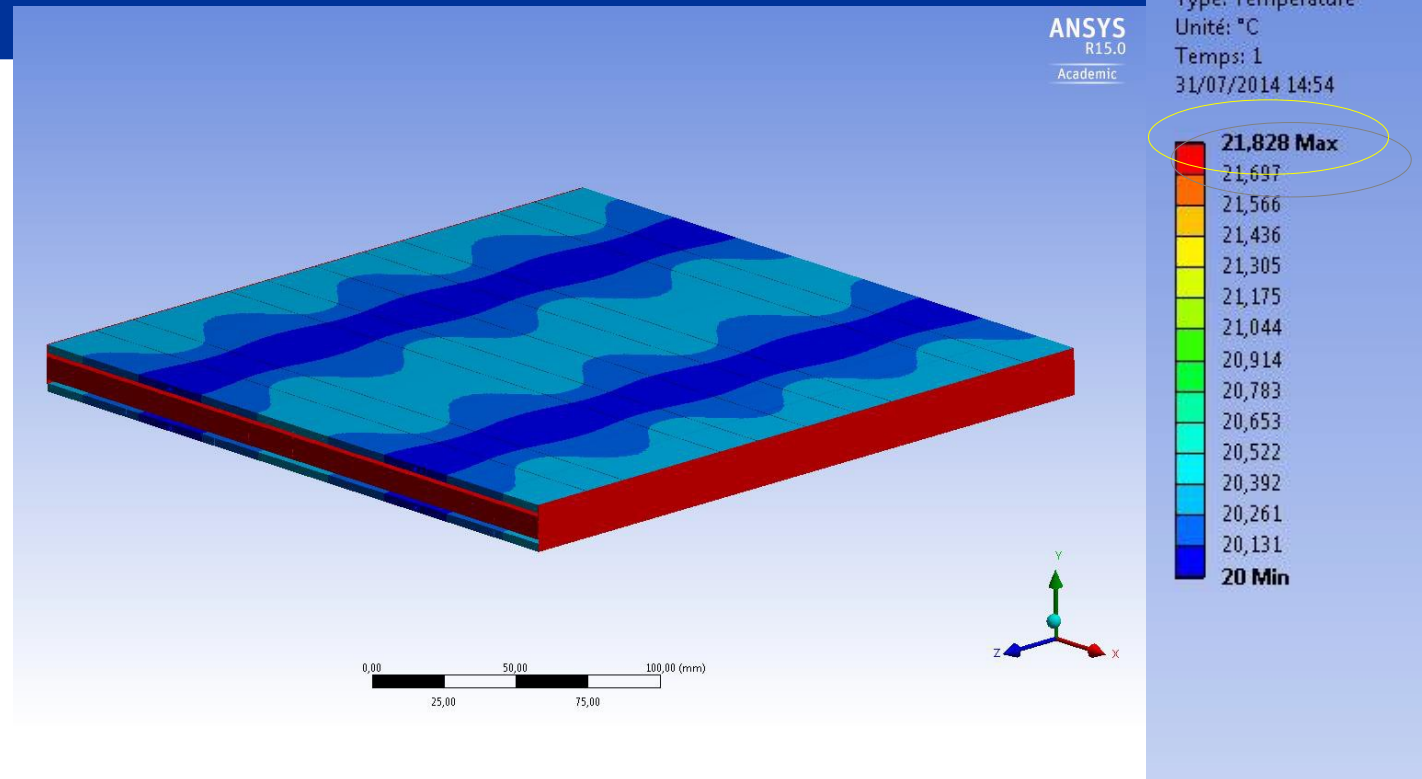
Over complete module:

- $\Delta T \leq \sim 2^\circ\text{C}$
- Mostly in ASICs
- PCB, CFRP & W harmonize the temp.
- Max temp at the center

Over the exchanger:

- $\Delta T \sim 0.3^\circ\text{C}$

Conclusion: the tool and the expertise exists...  
... results will arrive.



# Perspectives

Many years of R&D on ECAL (esp. at LLR) for ILC “easily” adaptable to CEPC case

Work on design model has started

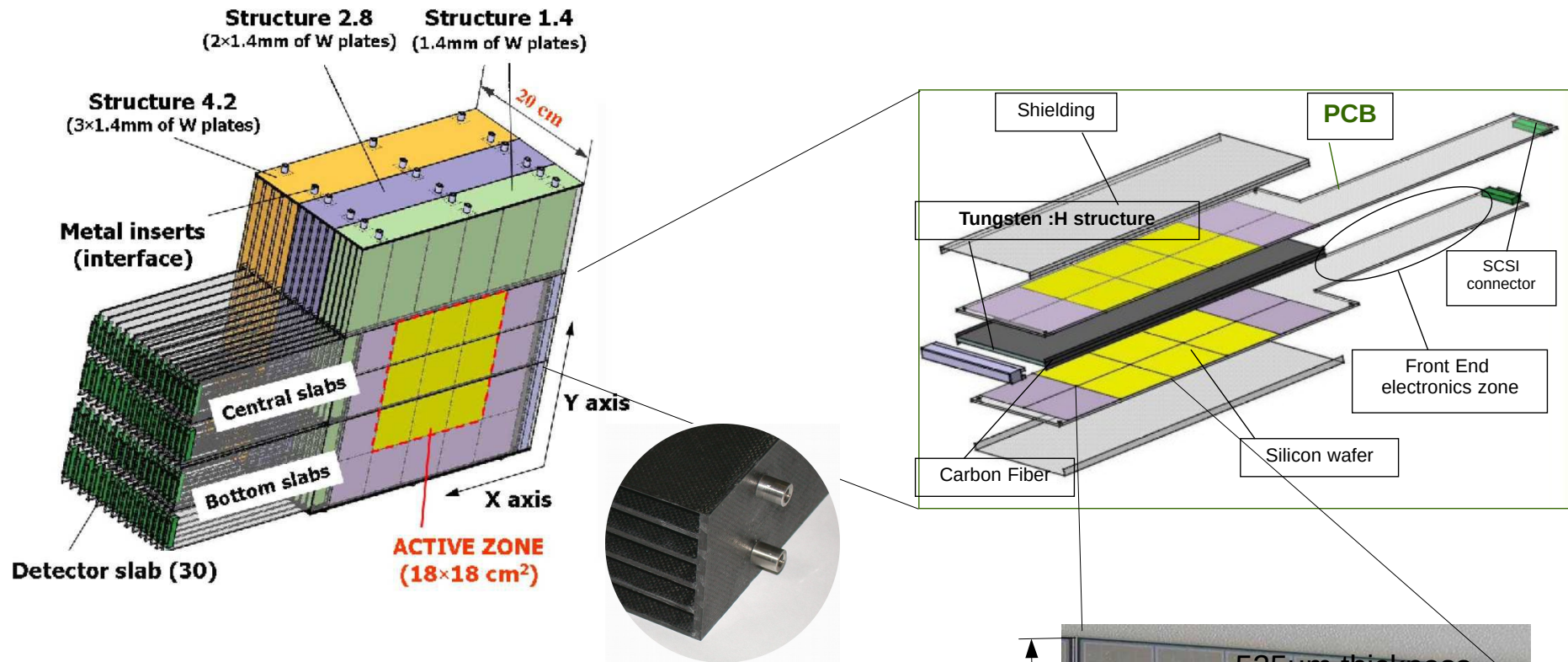
- benefit from CMS-HGCAL studies
- expertise on cooling and thermal simulation building-up

Most urgent to assess the performances and the needed granularity:

- Bunch structure of the machine will determine the granularity and performance of the ECAL
  - ⇒ Occupancy studies mandatory to fine tune the electric consumption
    - Specific R&D needed on VFE ASICs
- Updated GEANT4/Mokka models needed (support from LLR)
- 1 PhD student (Dan Yu) will work both on ILD and CEPC performances

# Extras

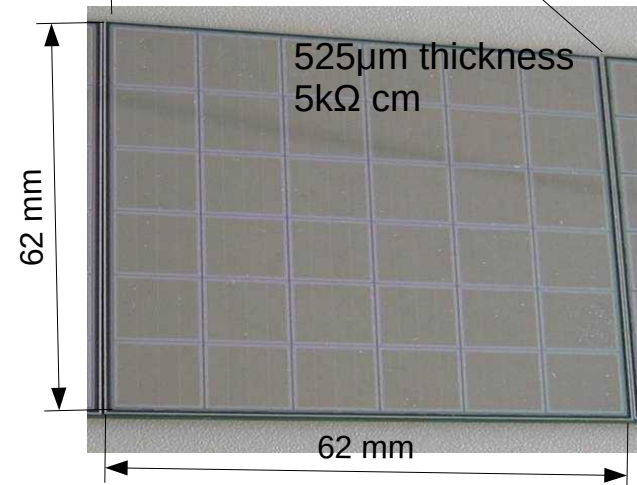
# Physical prototype



## Structure

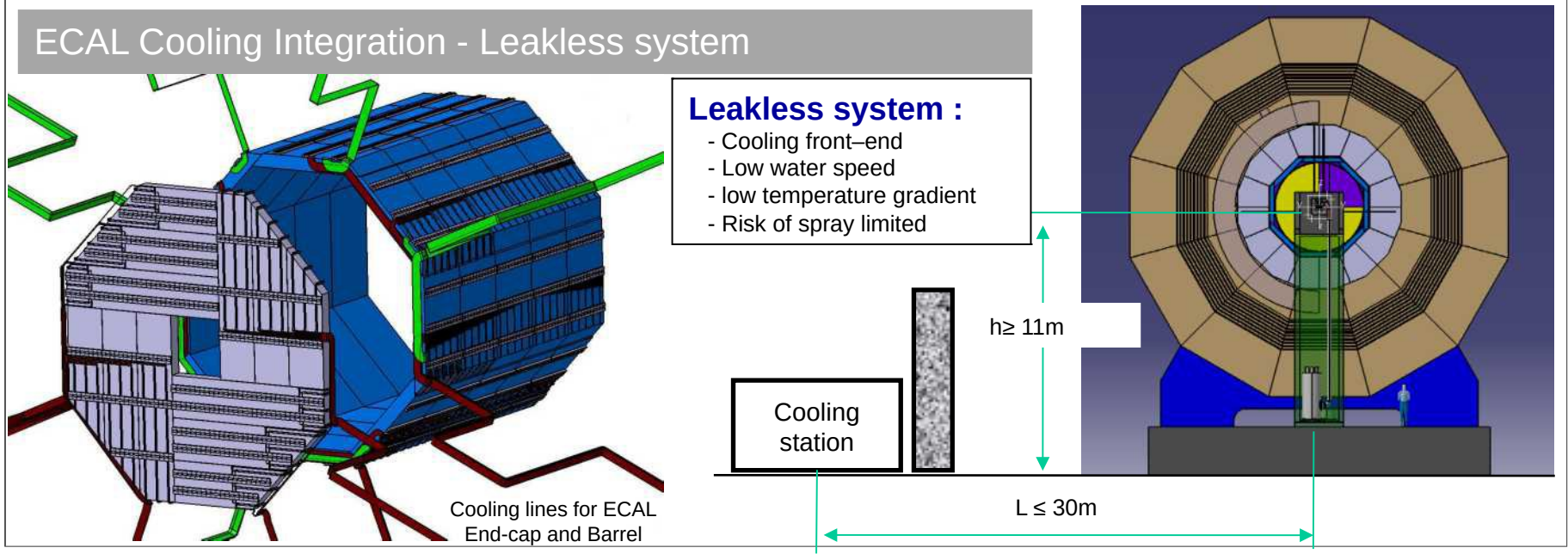
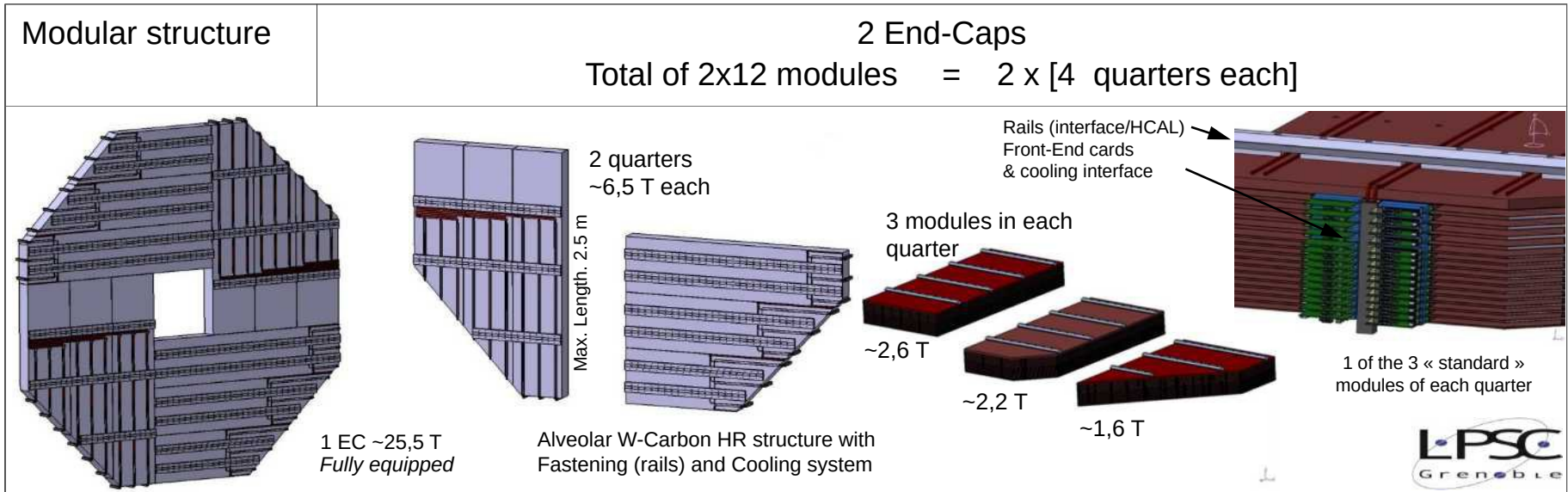
- 30 layers of Carbon Fiber /Tungsten  
 $10 \times 0.4 X_0 + 10 \times 0.8 X_0 + 10 \times 1.2 X_0 = 24 X_0$
- Self supporting Structure
- Sensor Units with external analog readout chips

High resistivity Si PIN Diode divided in  $10 \times 10 \text{ mm}^2$  cells





# Current structure of end caps



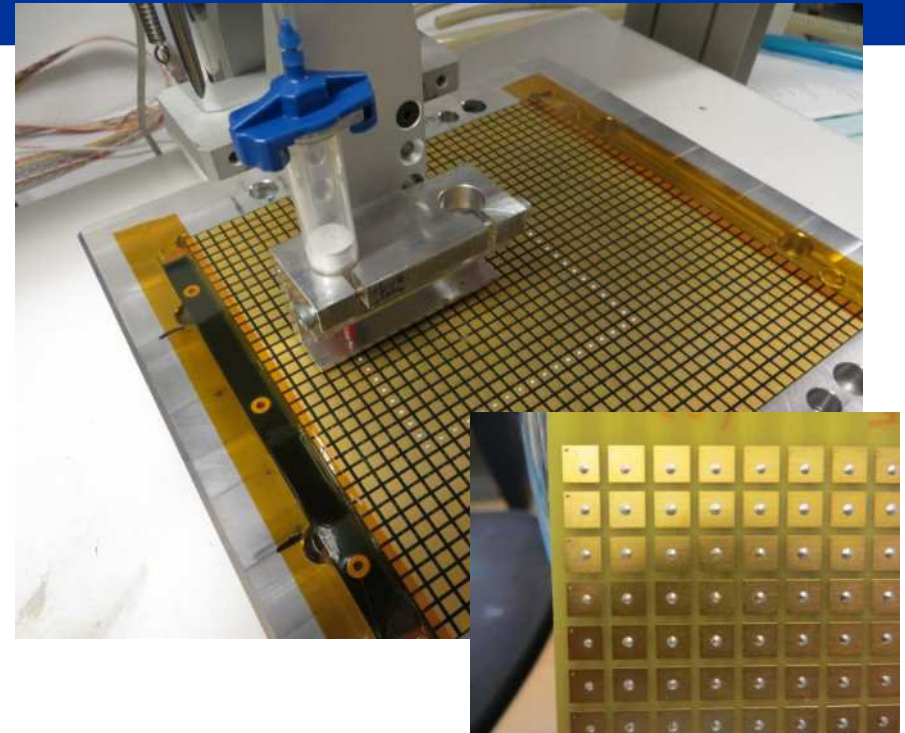
# Assembly 1: Gluing

Toward semi-automatic gluing of 4 wafers on every PCB:

- Constraints on the PCB geometry have been identified:
  - Flatness
  - Parallelism of the edges
  - Uniform height of the ASIC soldered on the board

9 sensors has been glued with the robot:  
used at 2012–13 beam tests

The leakage currents measured before  
and after the gluing process are similar.



Recent improvements

- Use of specific pumps for dry and clean vacuum
- Careful cleaning of PCB
- New positioning of the glue dots for the external pads, to avoid short-circuits.