

# CMOS Pixel Sensor for CEPC Vertex Detector

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# Outline

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- ▶ Introduction
- ▶ CMOS Pixel Sensor (CPS)
- ▶ CPS for the CEPC vertex detector
- ▶ Summary and outlook

# Introduction

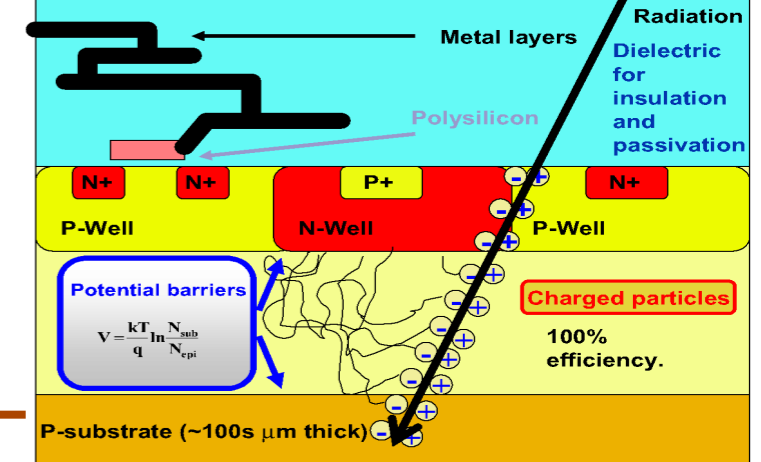
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- ▶ Impact parameter resolution required for the identification of heavy quarks and  $\tau$ -leptons (essential for CEPC physics):

$$\sigma_{\text{IP}} = 5 \oplus 10/p \cdot \sin^{3/2} \theta \text{ } \mu\text{m}$$

- ▶ Translating to requirements on the CEPC vertex detector:
  - Single point resolution  $\sigma_{\text{SP}} \sim 3 \text{ } \mu\text{m}$  → high granularity
  - Material budget  $\leq 0.15\% X_0$  per layer
    - Sensor+ASIC thickness  $\sim 50 \text{ } \mu\text{m}$  → monolithic sensors
    - **Air cooling** → low power consumption (extremely challenging without power-pulsing)
  - Radiation tolerance  $\sim 100 \text{ kRad/y}$  &  $10^{11} n_{\text{eq}}/\text{cm}^2$
  - Low detector occupancy  $\sim 0.5\%$  → fast readout

# CMOS Pixel Sensor



- ▶ Front-end electronics and sensor (utilising the epitaxial-layer) integrated on the same silicon bulk, featuring:
  - High granularity → **high spatial resolution**
  - Sensor thinned down to 50 μm → **low material budget**
  - Standard CMOS fabrication technology → **cost effective**
  - Signal processing on-chip → **relaxing down-stream data processing**
  - Radiation tolerance (moderate) → **usable for electron machines**
- ▶ **Example CPS sensors designed by IPHC**
  - Mimosas26 (EUDET beam telescope), Mimosas28 (STAR PXL)
  - MISTRAL/ASTRAL (ALICE ITS Upgrade, CBM-MVD)
  - Adaption to the ILD VTX

# CPS for CEPC

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- ▶ CEPC CPS project supported by the **State Key Laboratory of Particle Detection and Electronics**
  - “Semiconductor detectors for CPEC”, 2014- 2015, 400k CNY
- ▶ Project kick-off meeting on 21 July 2014; defined the following tasks for this one-year project:
  - To form a strong development team with sufficient expertise and identify the most critical R&D items
  - To complete the prototype design with the selected CMOS process and prepare for MPW submission (request for additional funding )
  - MPW submission and preparation for sensor characterisation, including DAQ development, beam telescope construction etc.
  - To define the roadmap for future development



# Building up the Team

- ▶ Collaborative team members with great enthusiasm

	Affiliation	Responsibilities	
Hongbo Zhu	IHEP	Project leader & beam telescope	
Min Fu	OUC	TCAD simulation	} <i>PhDs from IPHC</i>
Ying Zhang	IHEP	Front-end electronics	
Liang Zhang	SDU	Front-end electronics	
Ke Wang	IHEP	Readout electronics	
Pelian Liu	IHEP	DAQ and detector simulation	
Qinglei Xiu	IHEP	DAQ and background simulation	

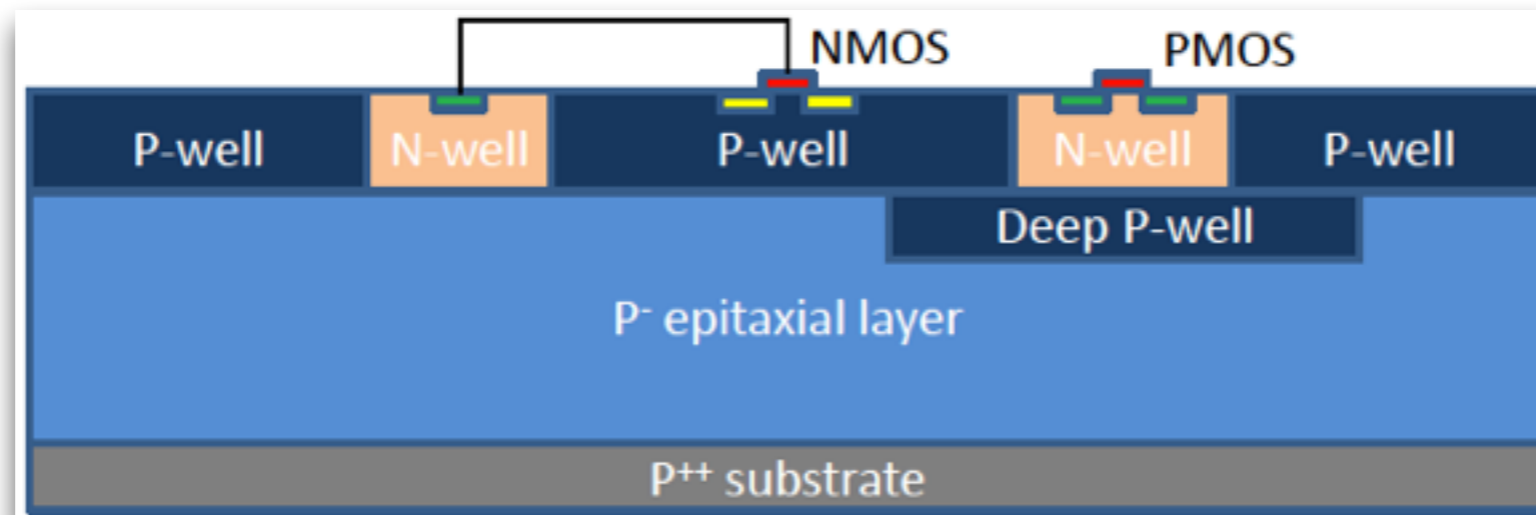
Yet more electronics/detector experts and students (!) are welcome to join the adventure.

## CMOS Processes

- Basic requirements: **EPI-layer** ( $\geq 10 \mu\text{m}$ , high resistivity), **Deep N/P-well** (to implemented in-pixel circuit)

	Feature size ( $\mu\text{m}$ )	EPI thickness	EPI resistivity	MPW availability	Cost
TowerJazz	0.18 CIS	5-18 $\mu\text{m}$	1 $\text{k}\Omega \cdot \text{cm}$	TBC	600k CNY
	0.18 BCD	TBC	10 $\Omega \cdot \text{cm}$	YES	
XFAB	XH035	P-5/15 $\mu\text{m}$	8 $\Omega \cdot \text{cm}$	YES	
	XO035	P-14 $\mu\text{m}$	0.55 - 2 $\text{k}\Omega \cdot \text{cm}$	YES	TBC
	XH018	P-10 $\mu\text{m}$	15 $\Omega \cdot \text{cm}$	YES	125k CNY/10 mm
SMIC	0.13/0.18 CIS	P-7 $\mu\text{m}$	0.55 - 2 $\text{k}\Omega \cdot \text{cm}$	UNLIKELY	
GF	0.18 BCDlite	7 $\mu\text{m}$	1 $\Omega \cdot \text{cm}$	YES	30k CNY/9 mm
CSMC	0.25 BCD	7 $\mu\text{m}$	TBC	TBC	
TSMC	CMOS	7-8 $\mu\text{m}$	8.5 -11.5 $\Omega \cdot \text{cm}$	UNLIKELY	
	CIS	TBC	TBC	UNLIKELY	

# TowerJazz® CMOS Process



- ▶ Feature size: 0.18  $\mu\text{m}$
- ▶ Thick epitaxial layer: 5-18  $\mu\text{m}$ ,  $1 < \rho < 6 \text{ k}\Omega \cdot \text{cm}$
- ▶ Six metal layers
- ▶ Deep P-well option (P-layer underneath N-well protecting from parasitic charge collection) allows usage of PMOS transistors
- ▶ Stitching option → to make large area detector

**Ideal for the fabrication of CPS, but rather expensive!**



# Power Consumption

- ▶ **Air-cooling** desirable for the CECP vertex detector to minimise material budget but **power-pulsing not optional** → imposing stringent requirement on power consumption: **50 mW/cm<sup>2</sup>**

Table 2.2: Chip design options.

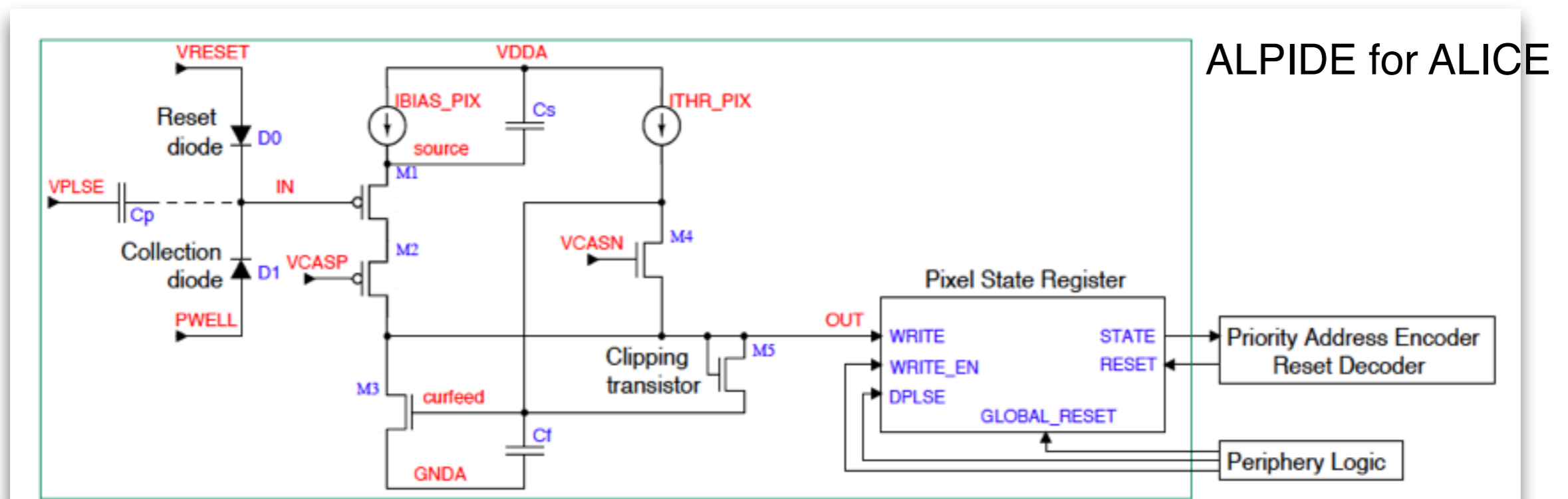
Architecture (discriminator, read-out)	Pitch ( $r\phi \times z$ ) ( $\mu\text{m}^2$ )	Integration time ( $\mu\text{s}$ )	Power consumption ( $\text{mW cm}^{-2}$ )
MISTRAL (end-of-column, rolling-shutter)	$22 \times 33.3$	30	200
ASTRAL (in-pixel, rolling-shutter)	$24 \times 31$ $36 \times 31$	20	85 60
CHERWELL (in-stixel <sup>a</sup> , rolling-shutter)	$20 \times 20$	30	90
ALPIDE (in-pixel, in-matrix sparsification)	$28 \times 28$	4	< 50

<sup>a</sup> A stixel is a 128-pixel column over which the electronics are distributed.

Can we learn more from the fast developing CMOS image sensor readout designs?

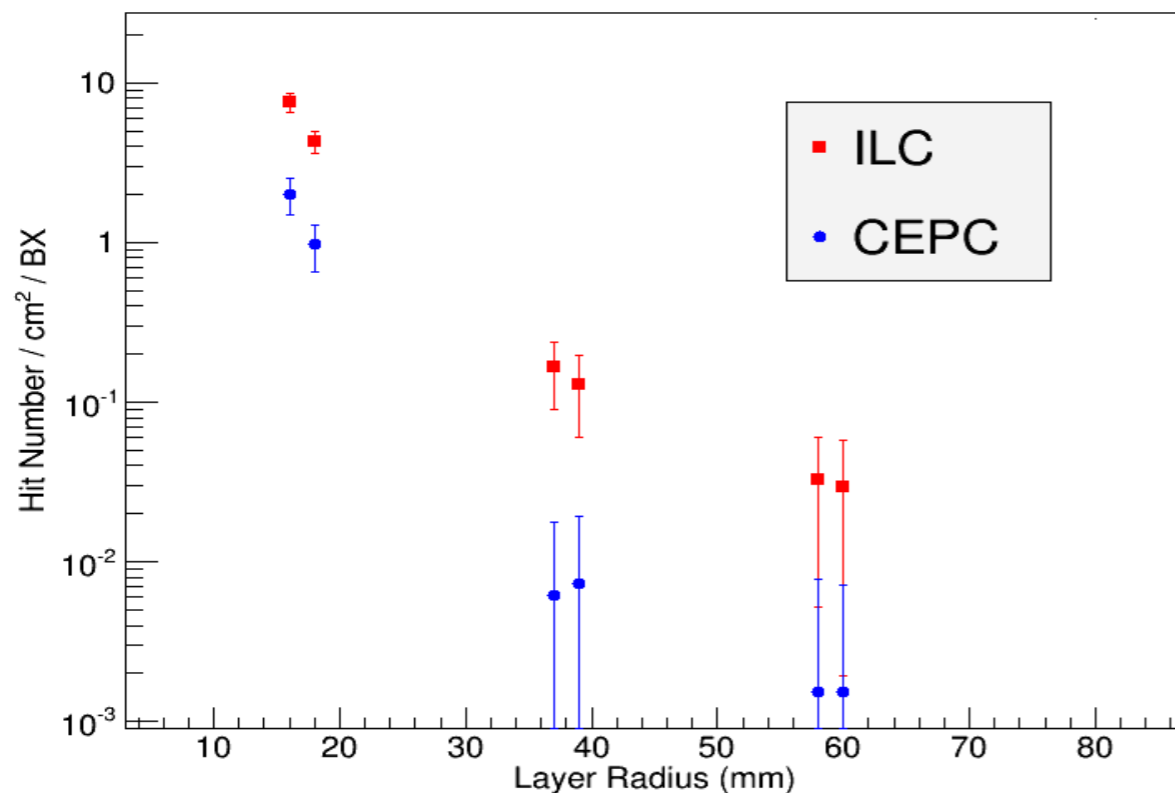
## Readout Architecture

- ▶ The classical rolling shutter with end-of-column discriminators yields a long integration time ( $\sim 200 \mu\text{s}$ ) and high power consumption ( $\sim 200 \text{ mW/cm}^2$ ). Moving discriminators to in-pixel improves the performance. → optional for CEPC
- ▶ New readout architectures, e.g. in-matrix sparsification, make possible shorter integration time and lower power dissipation.

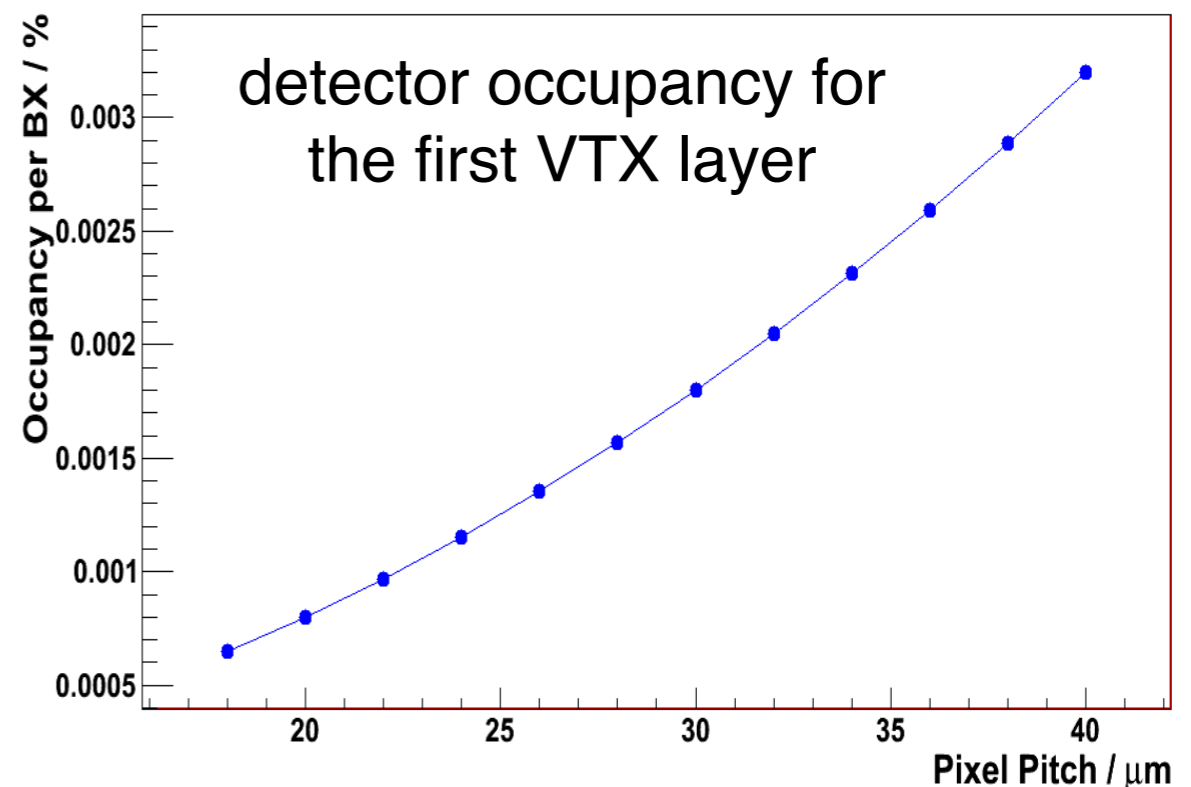


# Radiation Background

- ▶ Estimated the hit density and detector occupancy of the CEPC vertex detector → to provide reference for sensor design



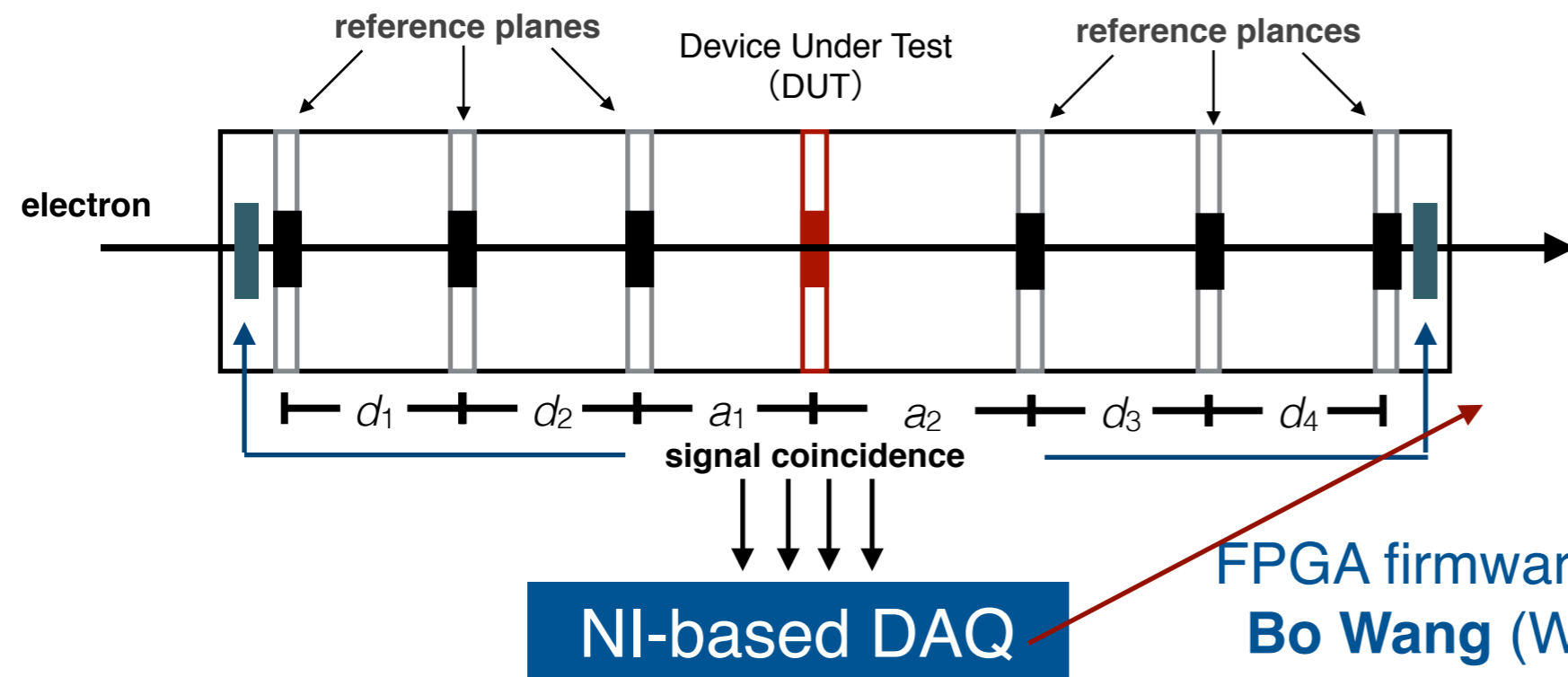
Radiation background conditions better for CEPC than ILC



No constraint for CEPC (empirical requirement of 0.5%)

# Preparation for Sensor Tests

- ▶ Semiconductor Lab@IHEP maintains a class-10000 clean room (150 m<sup>2</sup>) equipped with probe station, wire-bonder, etc.
  - I-V/C-V curves, laser/radioactive source responses
- ▶ High resolution beam telescope in preparation
  - Similar design to the EUDET telescope but with larger pixel sensors (MIMOSA28) and improved DAQ



FPGA firmware developed by summer student **Bo Wang** (Washington Univ.), ready for test

# Summary and Outlook

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- ▶ CMOS pixel sensor, a promising candidate for the CEPC vertex detector, relies on an appropriate CMOS process and may achieve fast readout with low power consumption.
- ▶ We have formed a team, aiming to address a few critical R&D items for the application of CPS to CEPC. Design efforts have started but experts/students are always welcome to join us.
- ▶ We have defined the expected achievements of the one-year project and shall request for additional funding for MPW submission and follow-up sensor tests.

ultimate design goal:

- Spatial resolution:  $\leq 3 \mu\text{m}$
- Detection efficiency:  $\geq 99\%$  (fake rate  $< 10^{-5}$ )
- Readout time:  $< 20 \mu\text{s}$
- Power consumption:  $< 50 \text{ mW/cm}^2$
- Radiation tolerance: close to ILC requirement