Pico-Second Timing with Micro-Channel Plate Devices and Waveform Sampling Readout Electronics

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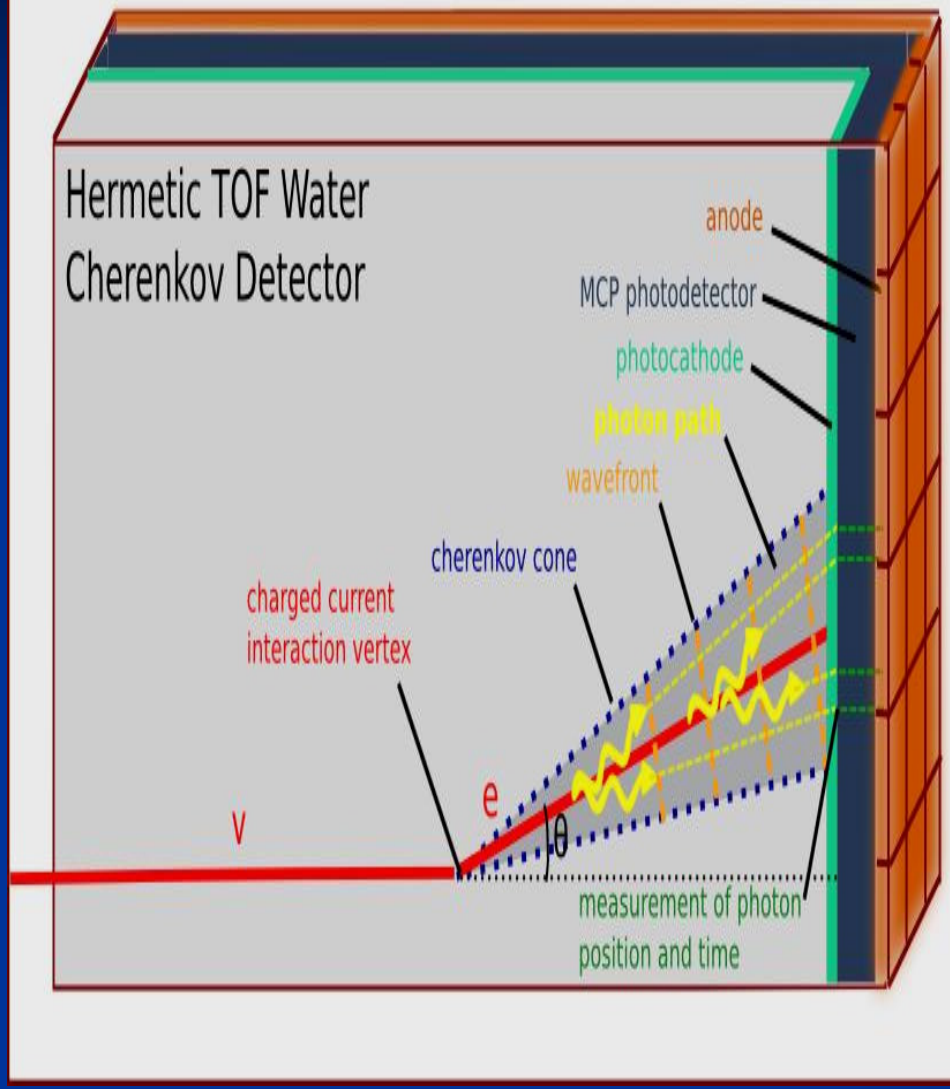
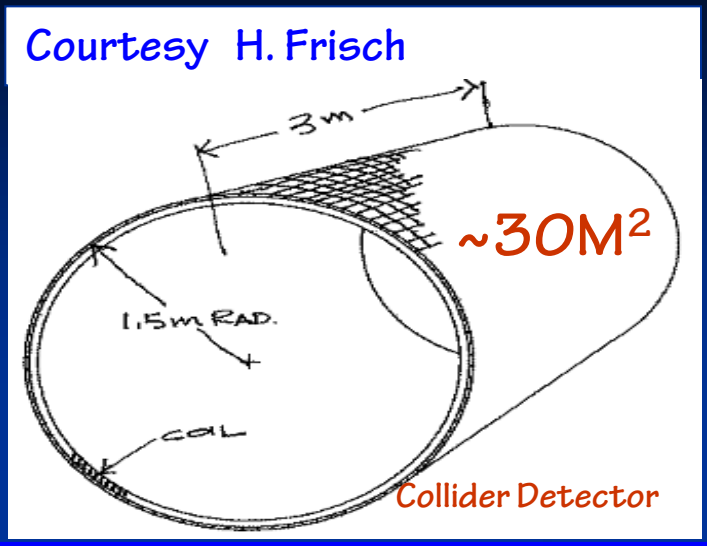
- Introduction
- Characteristics of MCP-PMT output signals
- Transmission-line readout and simulations
- Readout techniques for picoseconds timing measurements
- 40Gsps fast sampling chip design
- Summary & plan

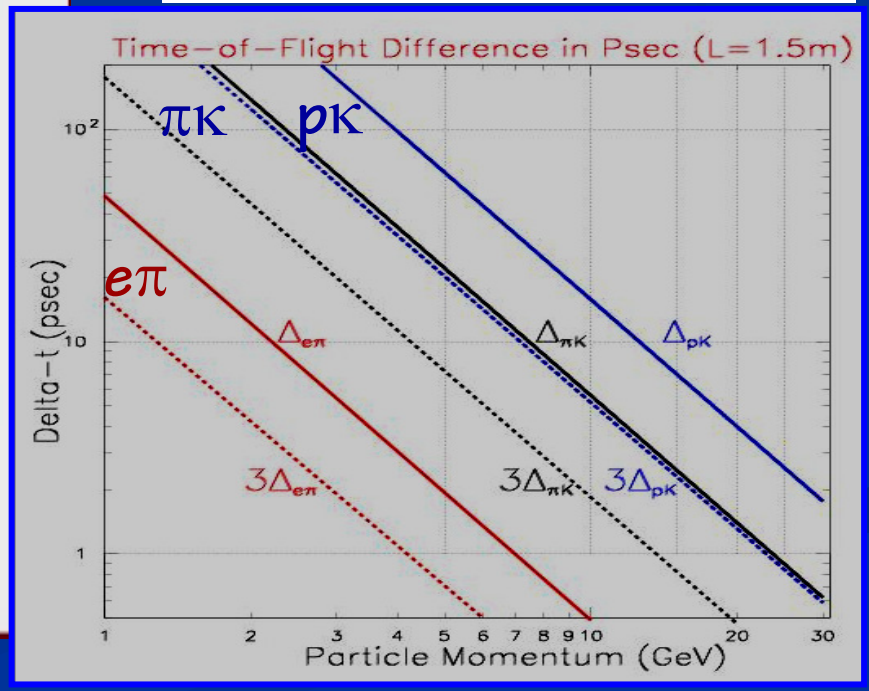
Introduction: Applications of Time-of-Flight for HEP

Courtesy H. Nicholson/DOE



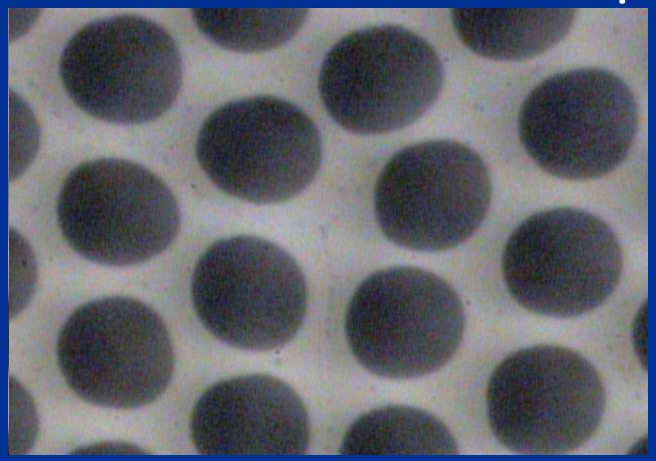
Courtesy H. Frisch

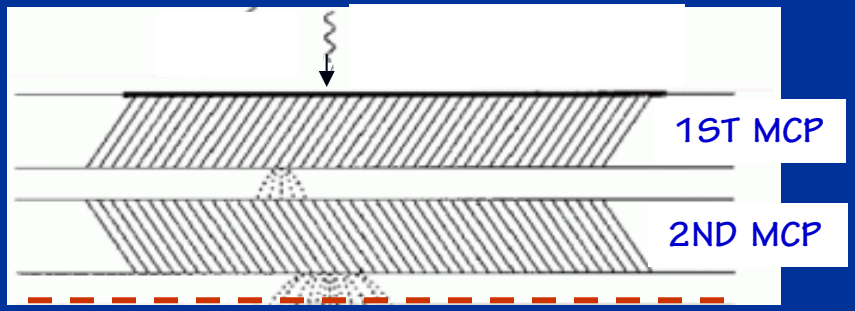


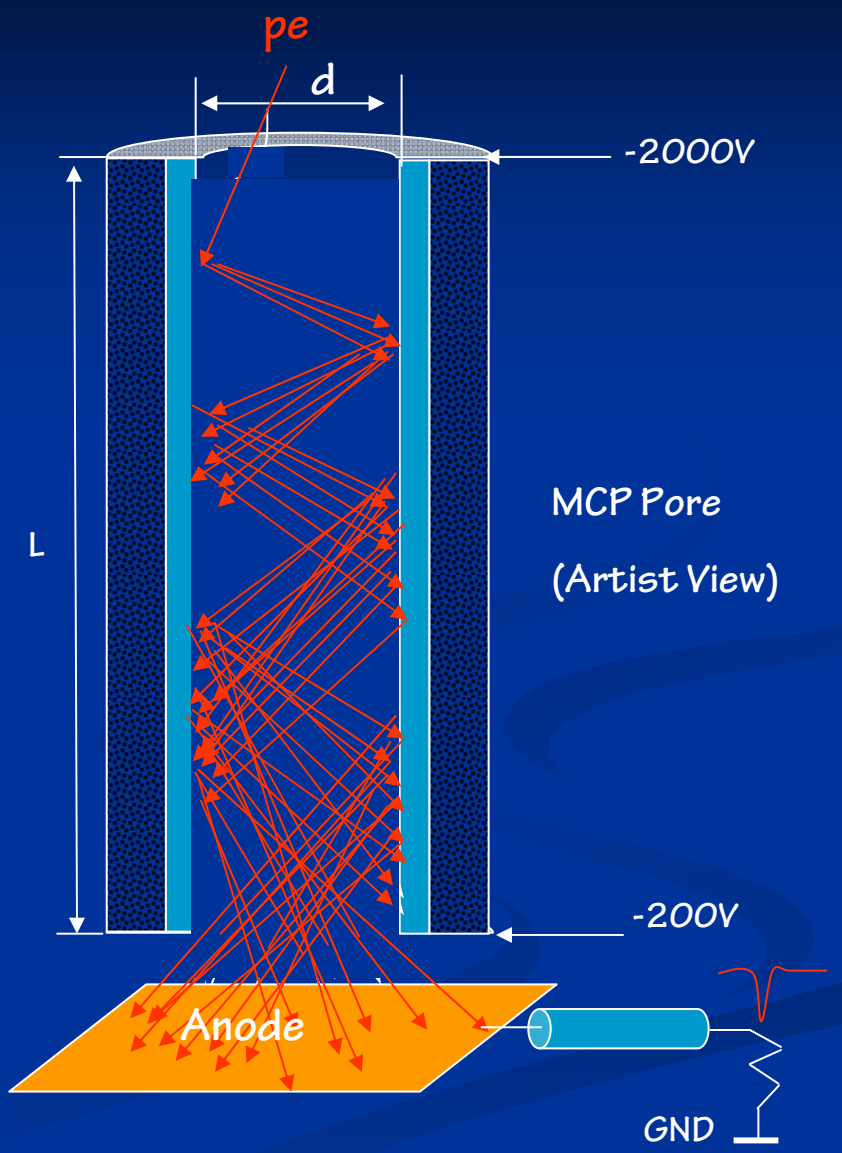


Why MCP Can Achieve Fast Timing?

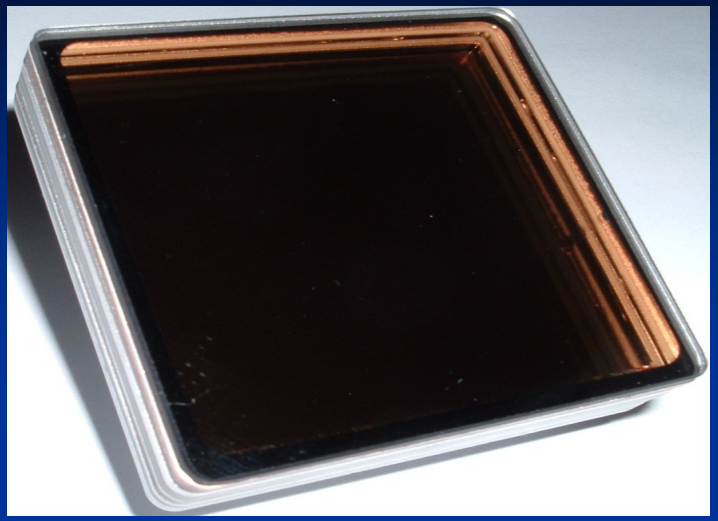
Commercial MCP tubes with pore diameters from 2um to 25um available, MCP with pore size of 100nm or smaller are developing with AAO and ALD techniques. Gain range is in 1E5 to 1E6. TTS is down to ~15ps

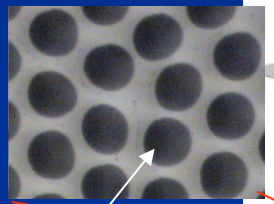




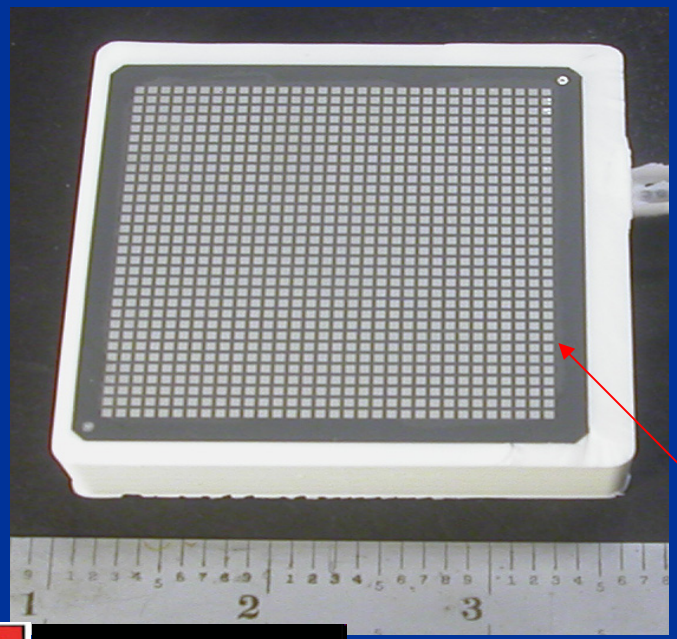


Introduction: Planacon MCP-PMT Tube & Anode Array

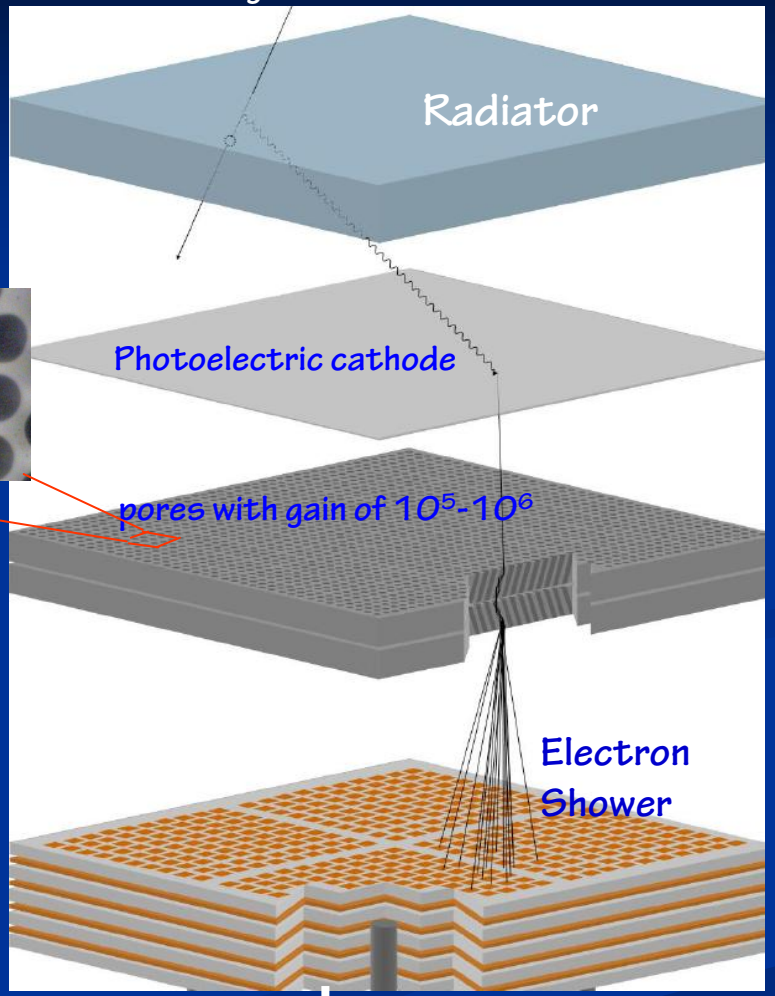




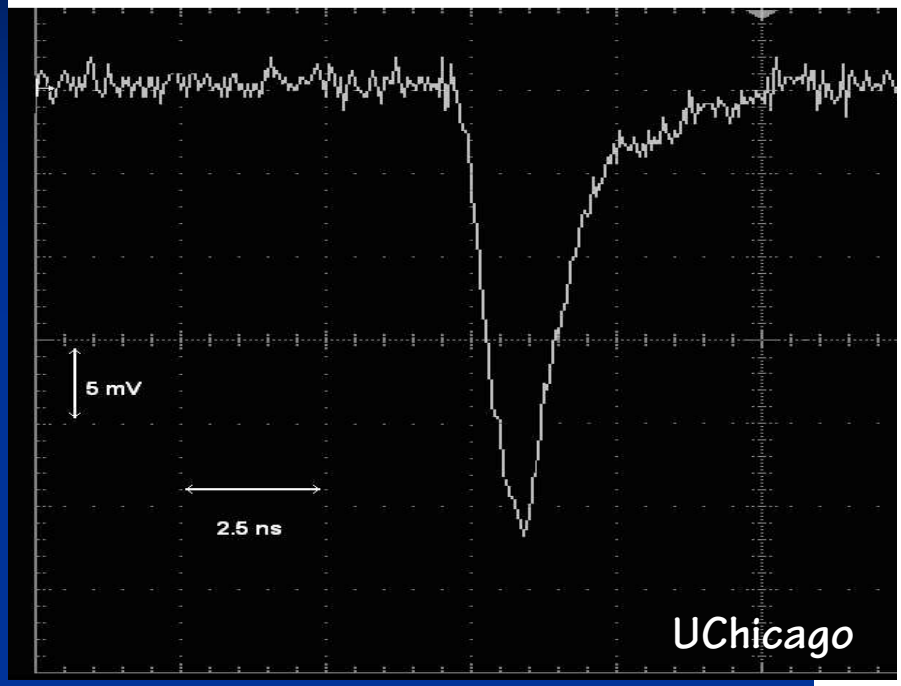
Pore size:
10um/25um

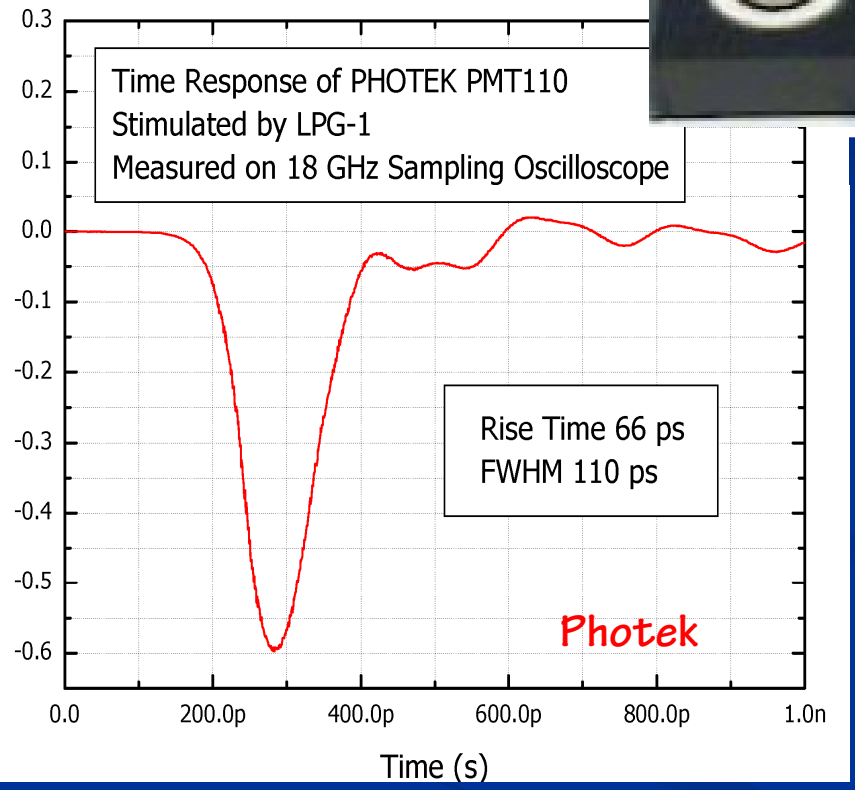


Photonis Planacon 2x2"
tube with 1024 anodes



Typical MCP Output Signals





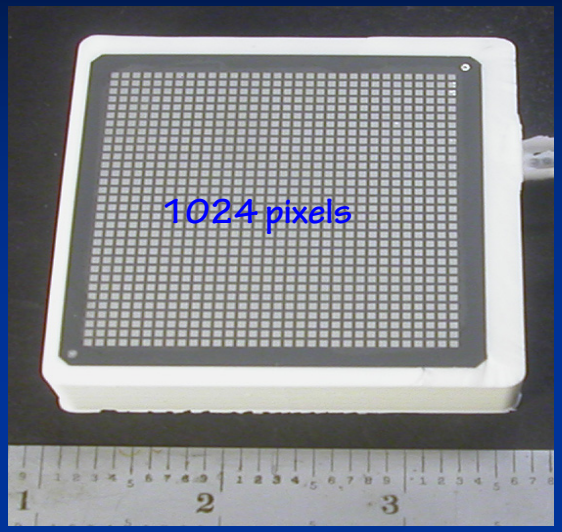
UChicago/FNAL/ANL/SLAC beam test

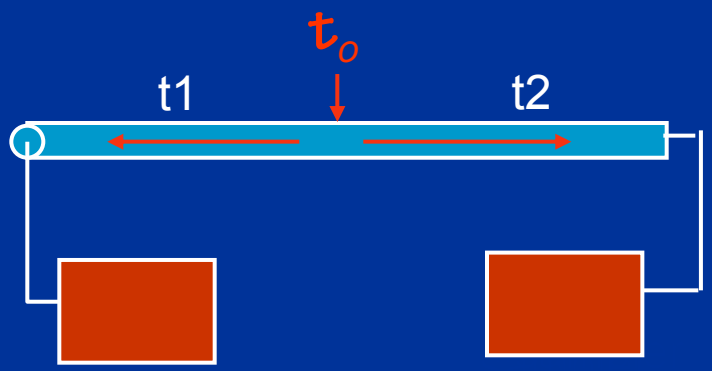
- Measured (beam-test):
- Pore size: 25um
- Rise-time: 380ps
-- Active Area: 2x2 inch

- Measured (laser-test):
- Pore size: 3.2um
- Rise-time: 66ps
- Active Area: 25mm in Diameter.

Transmission-line with Fast Sampling Readout for Planicon MCP-PMT

- Reduce readout channels (from 1024 down to 64 channels)
- Readout of timing, position and energy information
- Good transmission-line bandwidth (up to 3.5GHz)





40Gsps Pulse Sampling

Timing: $$t_0 = \frac{t_1 + t_2}{2}$$

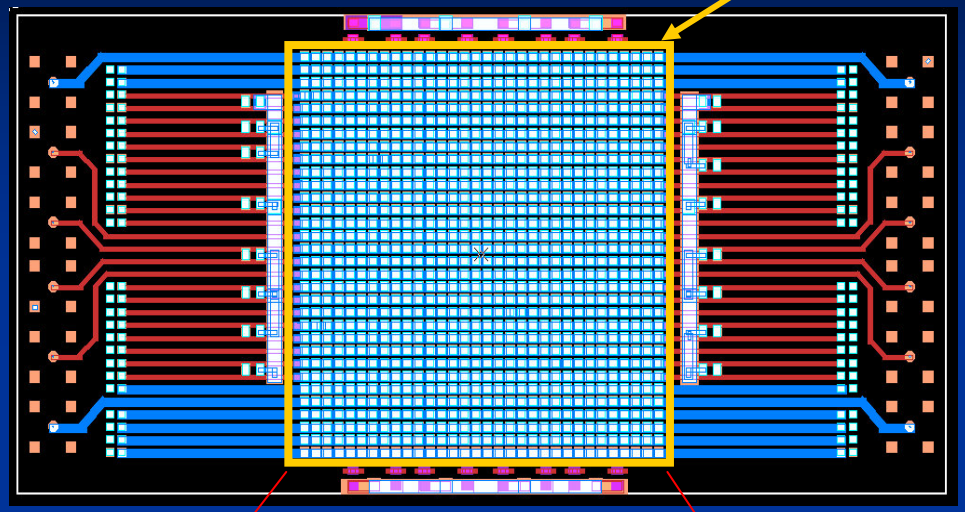
Position: $$x_i = \frac{t_1 - t_2}{t_1 + t_2}$$

Energy: $$E_i = q_1 + q_2$$

Prototype Transmission-line Readout Board

Board Size: 130x60mm

Tube Outline 58x58mm



When TL readout board Is mounted on MCP, the TL can be modeled as 32 equally distributed C(~100f) along 2-in line, It actually reduces impedance and bandwidth in middle area of the line.

$$Zo' = \sqrt{\frac{L}{C + \alpha C_L}}$$

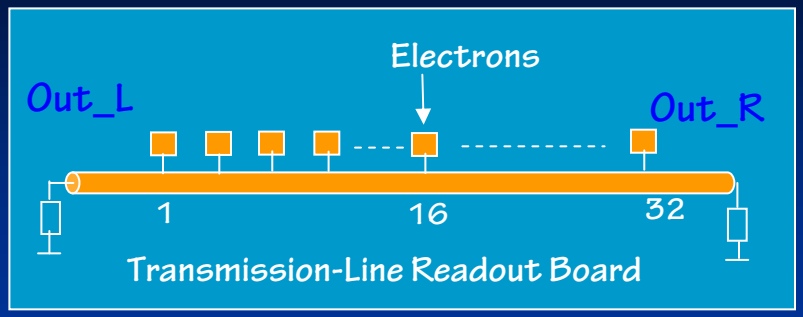
$$\alpha = \frac{nC_L}{Length}$$

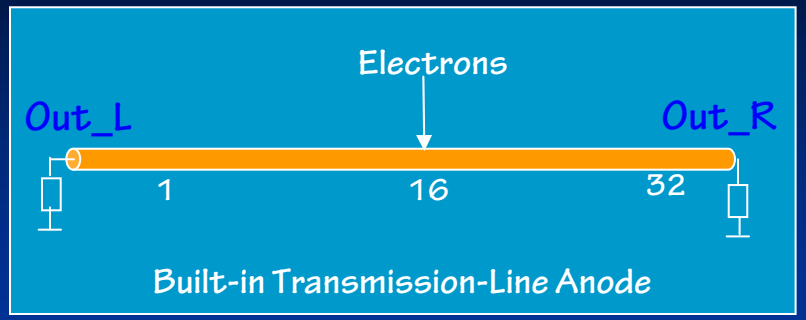
$$\alpha C_L = 1.6p$$

$$Tr = 2.2\tau = 2.2\frac{Z_0}{2}\alpha C_L \approx 100\,ps$$

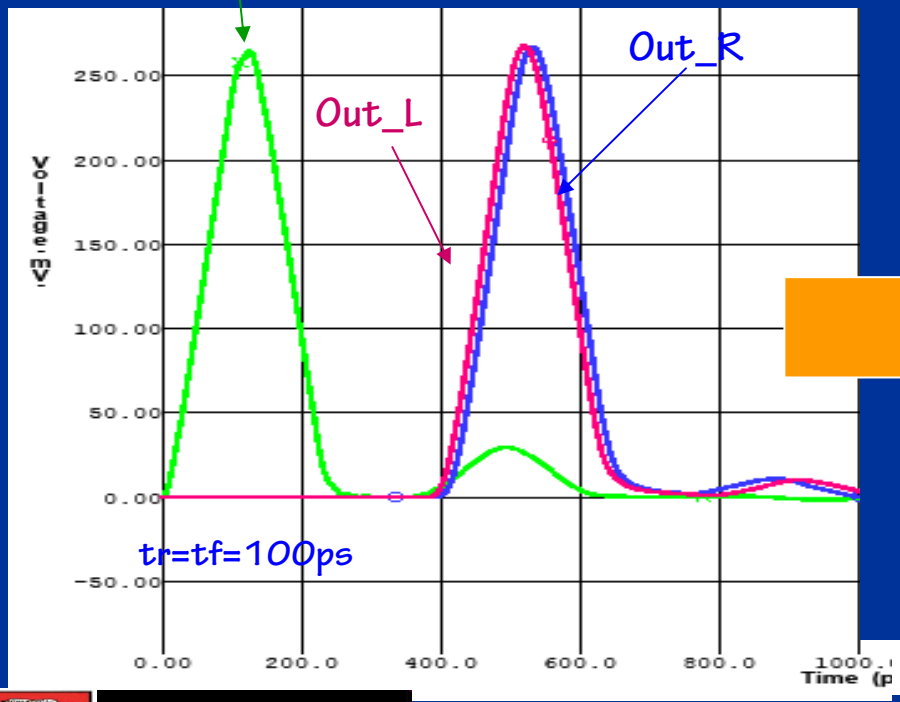
$$BW \approx 3.5GHz$$

Simulations of TL Readout Board and Built-in TL Anode

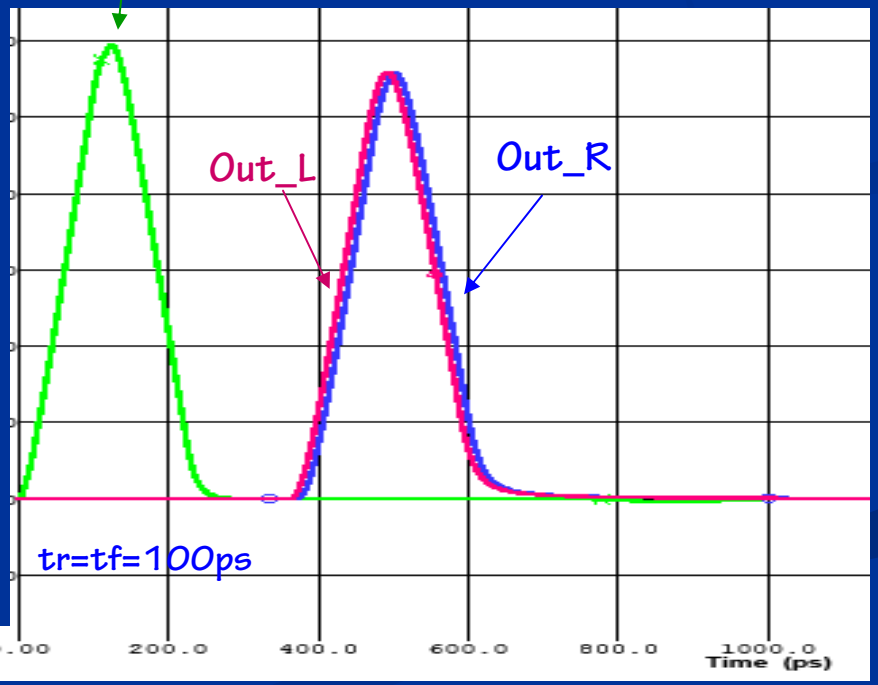




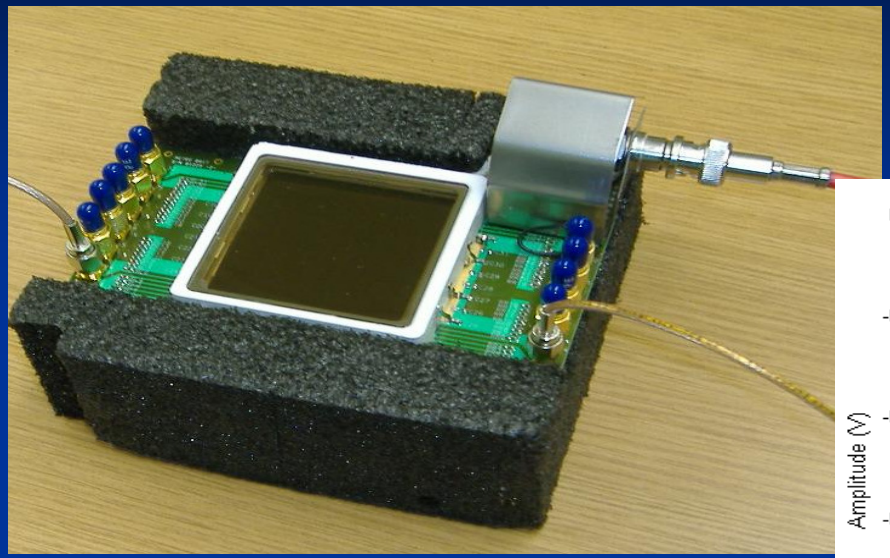
Input on Pad-16



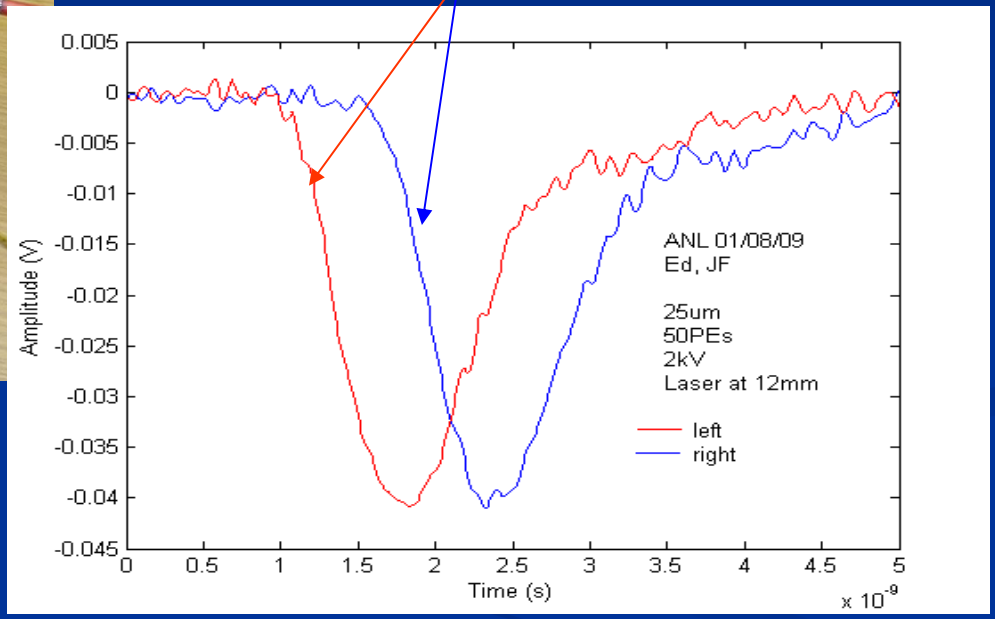
Input on pad-16



Transmission-Line Readout with 25um MCP (Laser Test)



Signals obtained from two-ends with laser test.



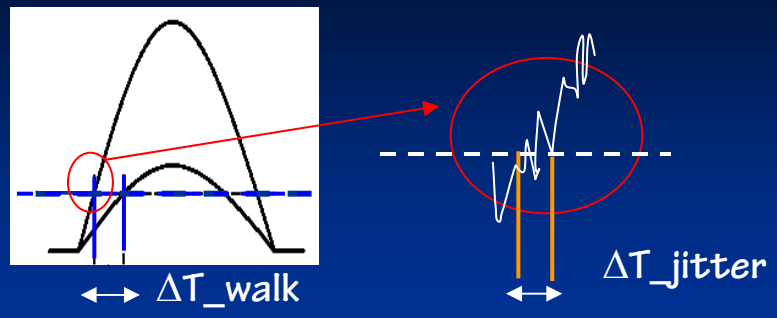
Transmission-line readout board is built with Rogers 4000B PCB, the line impedance is 50Ω. Laser wavelength is 408nm, No amplifiers applied.

Limitation of Conventional TDC Techniques

(1) Leading edge discriminator + TDC/ADC

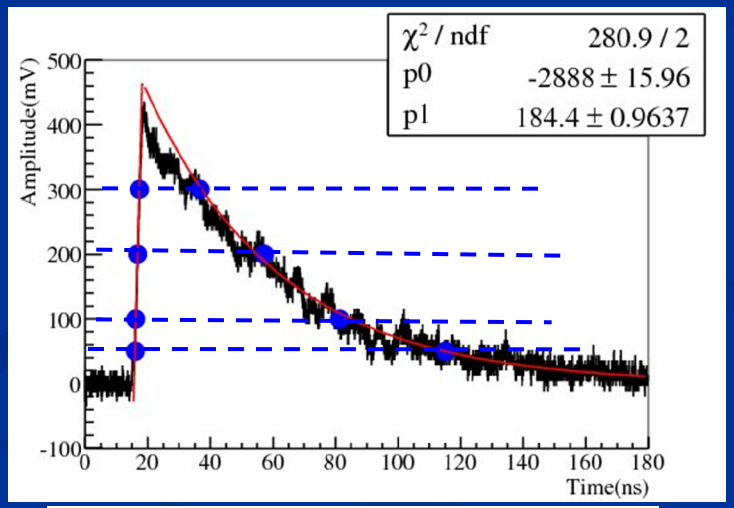
Timing jitter can not be avoid.

The amplitude dependent time walk can be compensate with an extra ADC.



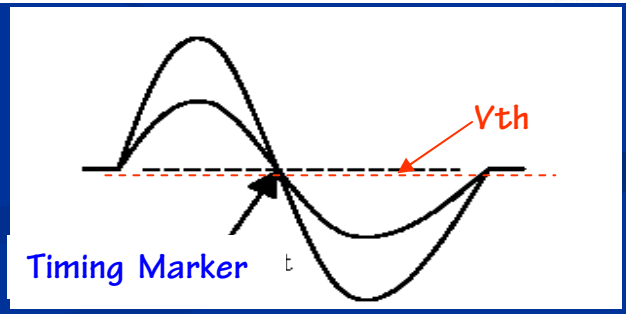
(2) Multi-threshold discriminators (Horizontal Sampling) + TDCs

Multi-threshold discriminators work like a horizontal sampling, leading edge or full waveform can be obtained by waveform fitting. In principle, It can achieve better timing than single leading edge discriminator. The disadvantage is multiple channel of electronics is required.



(3) Constant fraction discr. (CFD) + TDC/ADC

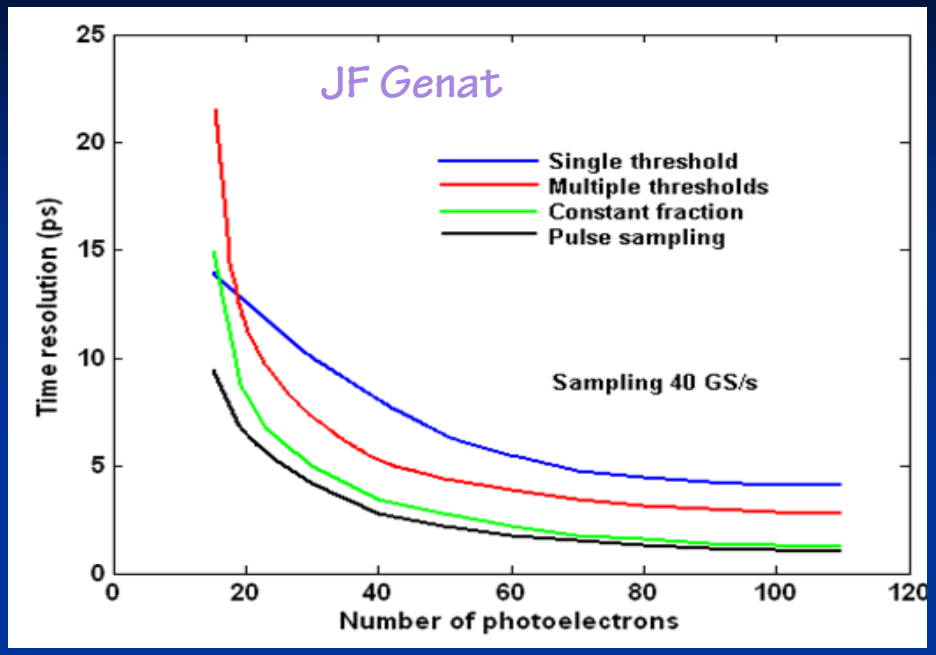
Best timing. But it is very hard to build into picoseconds timing ASIC since it requires wideband delay components, high speed zero-crossing discriminator and feasible attenuation ratio tuning circuitry for best SNR. Slight time walk can not be avoid.

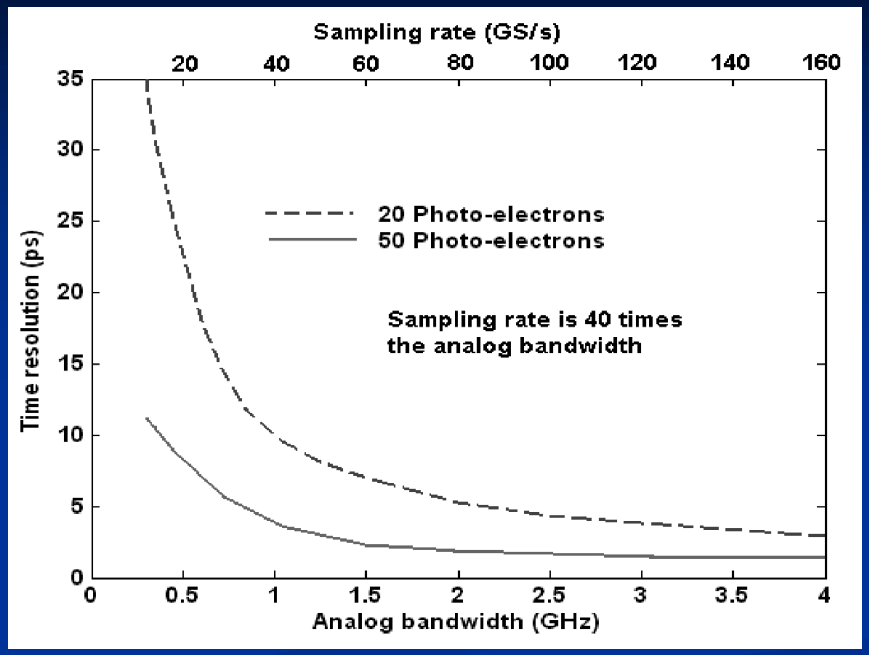


Electronics Requirements

- Picoseconds timing resolution(1~3ps).
- Capable of using for large scale detectors which may cover tens square meters (tens of thousands channels or more).
- Capable of measuring timing, position and energy.
- Fully digital interface to the system.
- Self/external trigger.
- Adequate dynamic range.
- Low power implementation.
- Stability and reliability.
- Others.

Simulation Comparison of Fast Timing Techniques





Pulse sampling

Simulation setup:

Assume 1.5 GHz analog bandwidth, 100 samples taken at 10-40 Gsps.

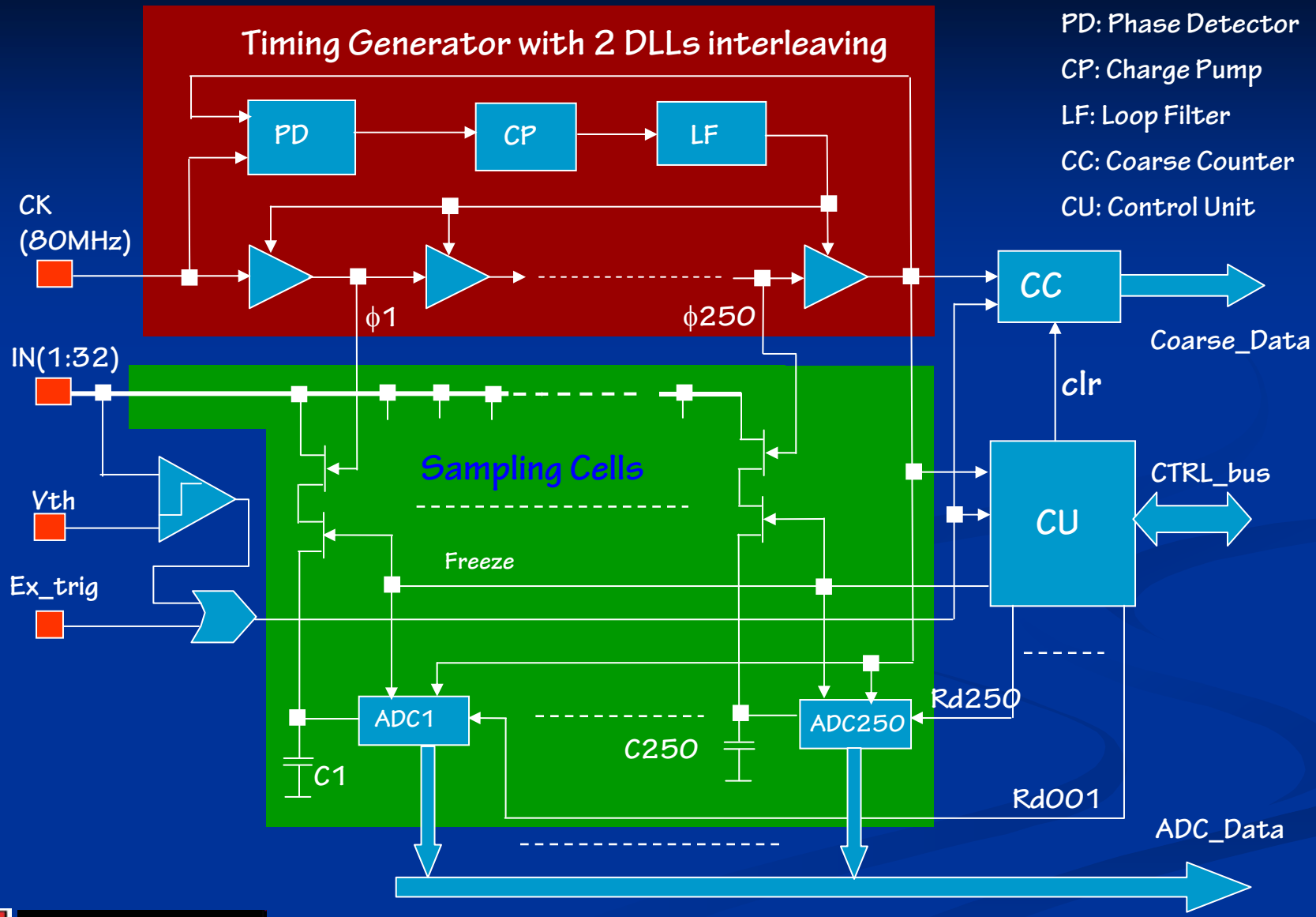
- Better timing resolution than CFD particularly at low PEs.
- Record the full pulse waveform which allows energy measurement.

Design Specification of UChicago 40Gs/s Sampling Chip

This work is in collaboration with UHawaii, Orsay/Saclay France

Sampling Rate	40Gs/s
Analog Bandwidth	1-2GHz
Input Signal Range	-100mV to -800mV
Storage Cell	250
Input Channel	4 (prototype) 16-32 (Production)
ADC Dynamic Range	10-bit (on-Chip)
Effective Resolution	8-bit
Self/External Trigger	Yes
Expected Timing Resolution	~2-3ps
Technology	IBM CMOS 8RF 0.13uM

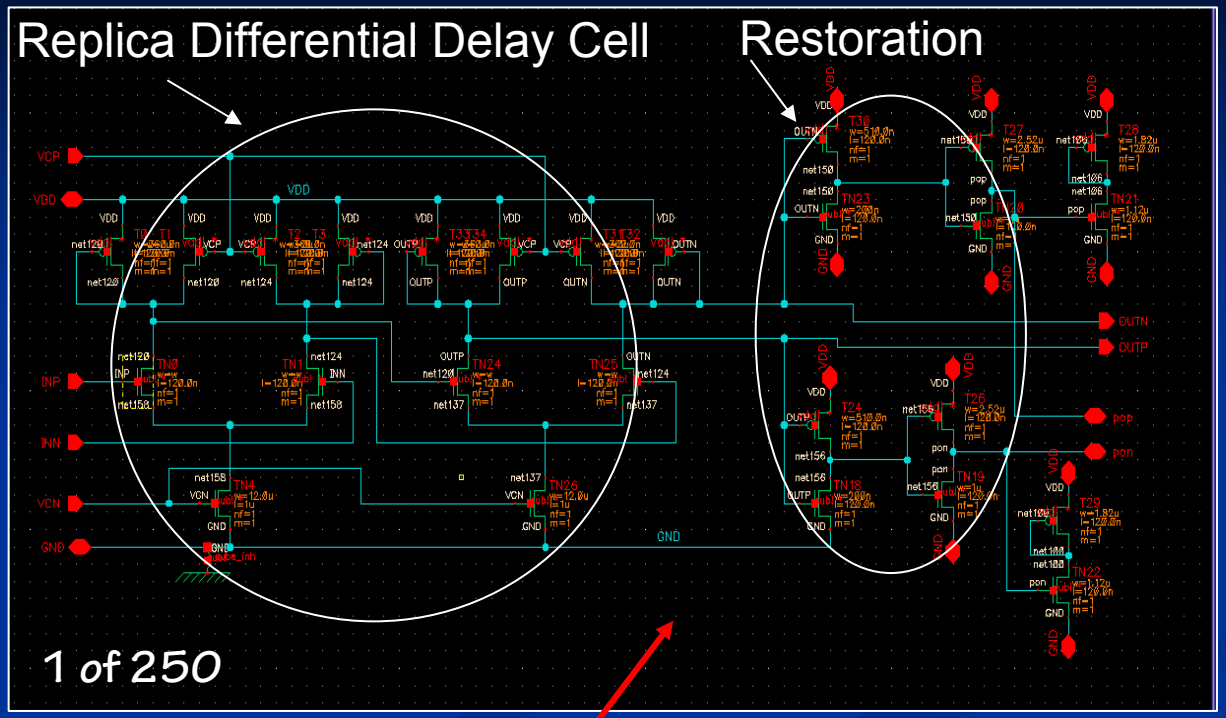
Diagram of 40Gs/s Sampling Chip

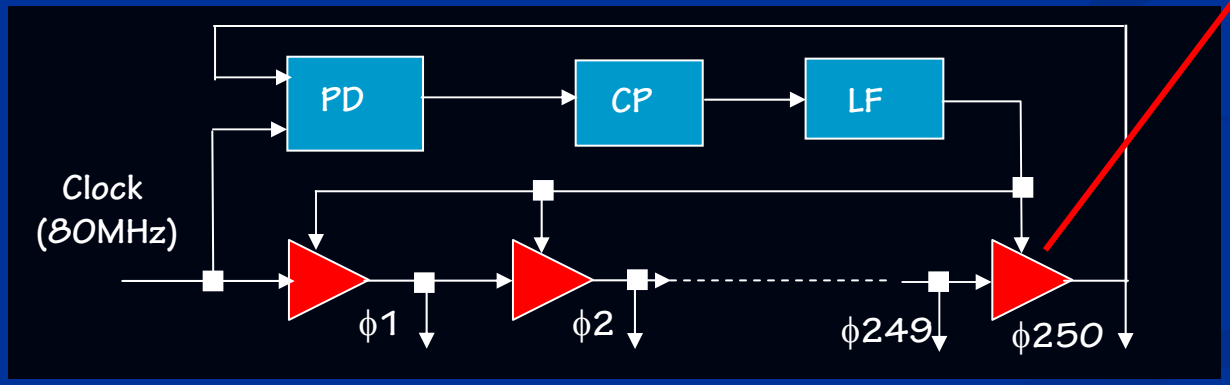


Schematic of Replica Differential Delay Cell

Features:

1. 80MHz input clock.
2. Delay 50ps per cell.
3. Tuning range of delay >20%.
4. 50% duty-cycle
5. True differential
6. 1.2V Voltage





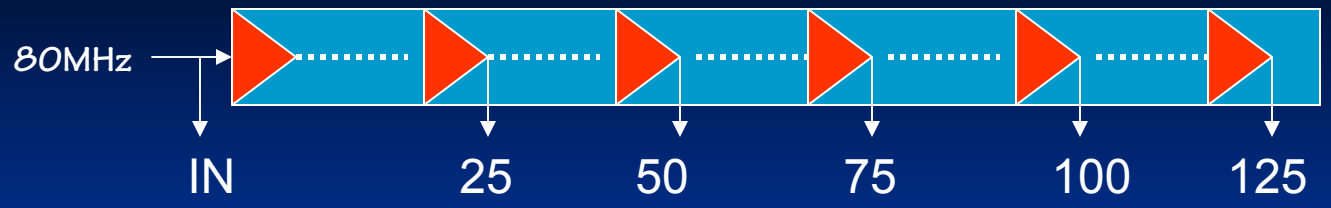
Delay Locked Loop

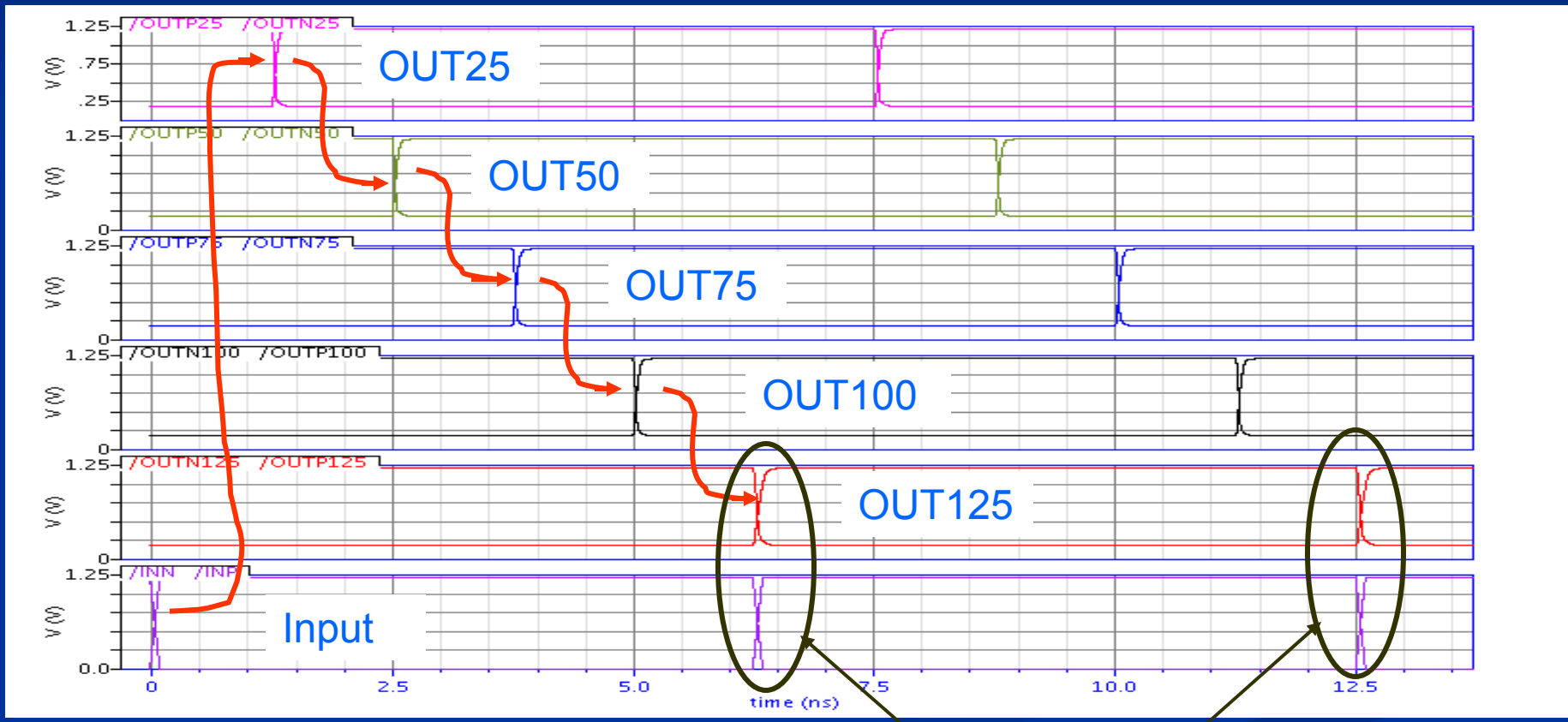
Track (6.25ns)

50%

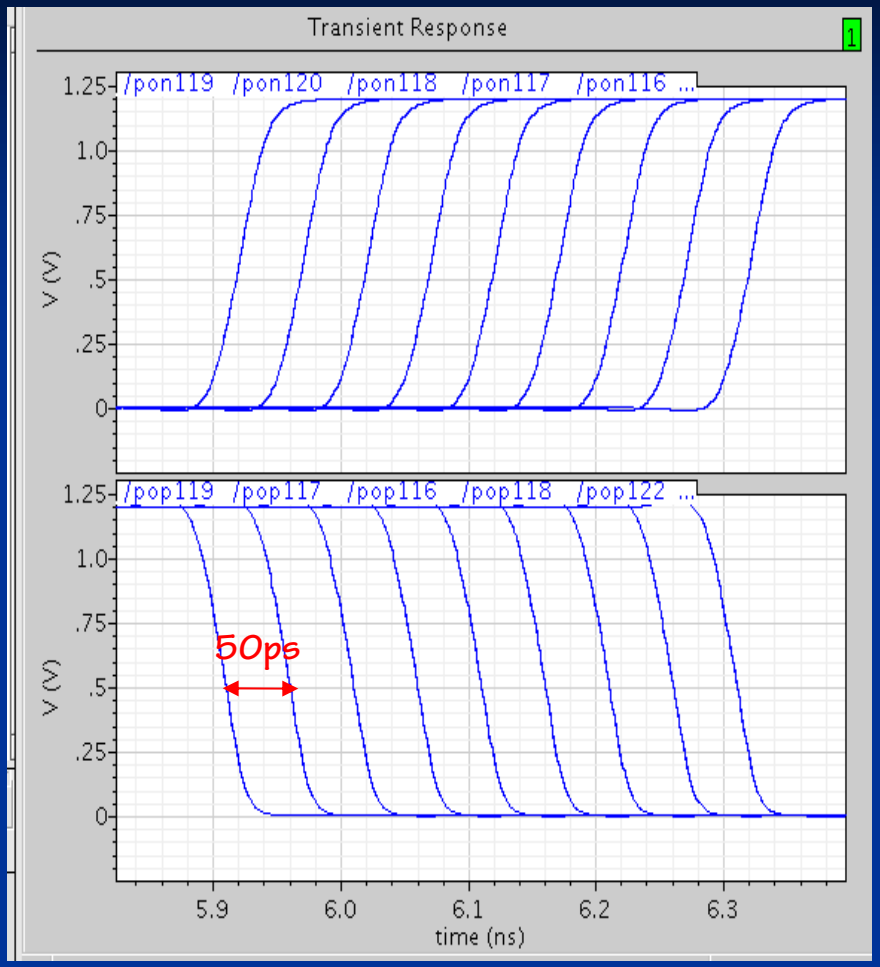
Hold (6.25ns)

Open Loop Simulation of 40Gsps Timing Generator

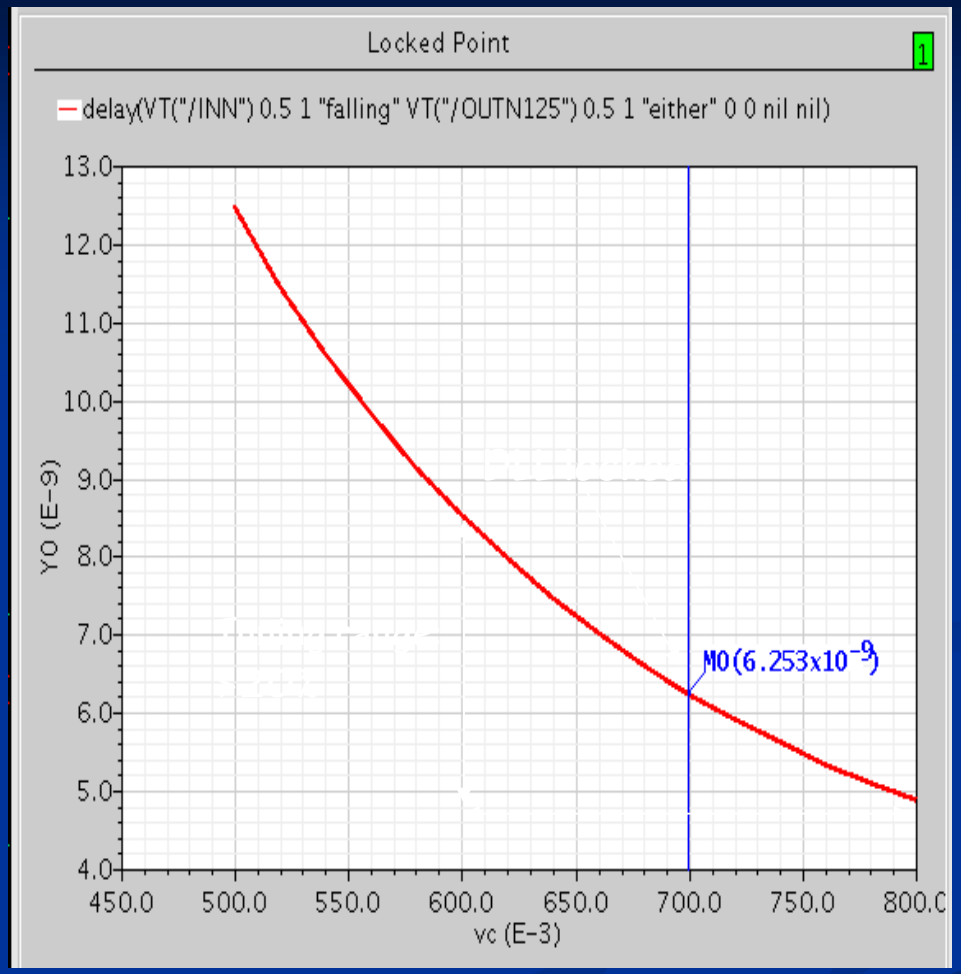




Track-and-hold timing and V-D Transfer Function



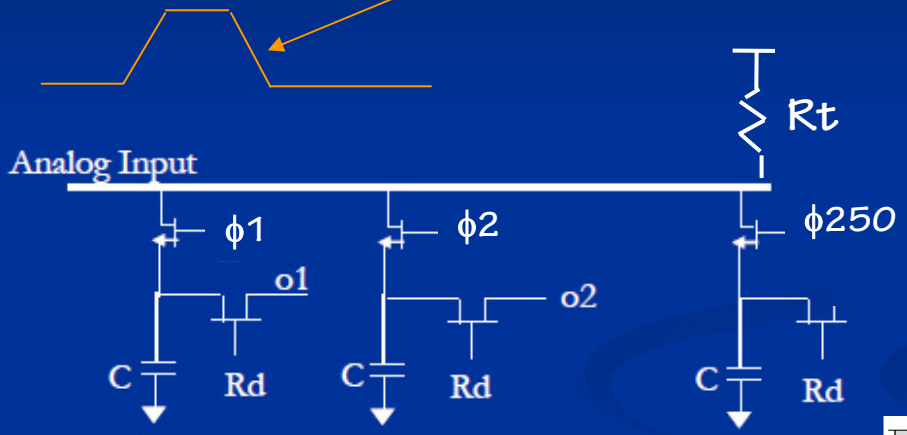
Sampling pulse phases
(Cell 116 - 124)



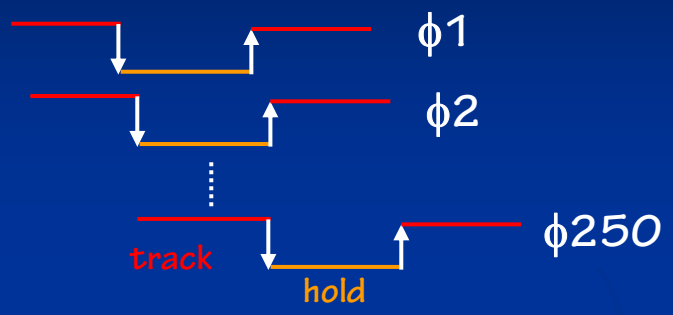
125-cell V-D Transfer Function Chart

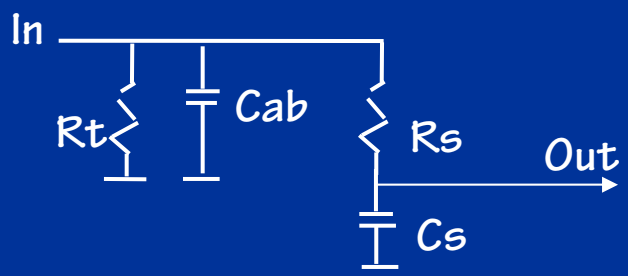
Analog Input Bandwidth

Analog input pulse: Tr=Tf=Tw=100ps



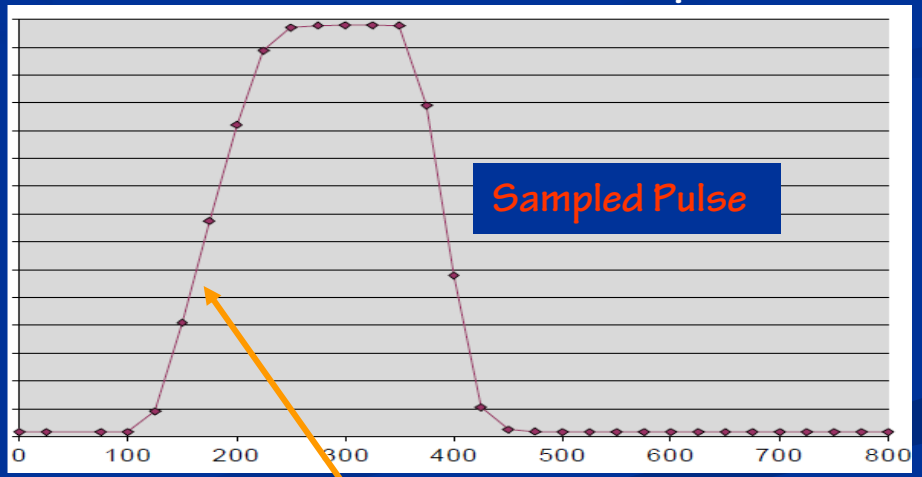
125 switches are sequentially on for tracking, the other 125 switches are sequentially off for holding.





Analog bandwidth is determined by a simplified 2-pole system

Simulation Results with 32 Sampling Cells



Analog bandwidth is ~2GHz

Measured Performance with TL Readout

Tested at Argonne by *Jean-Francois Genat and Ed May etc.*

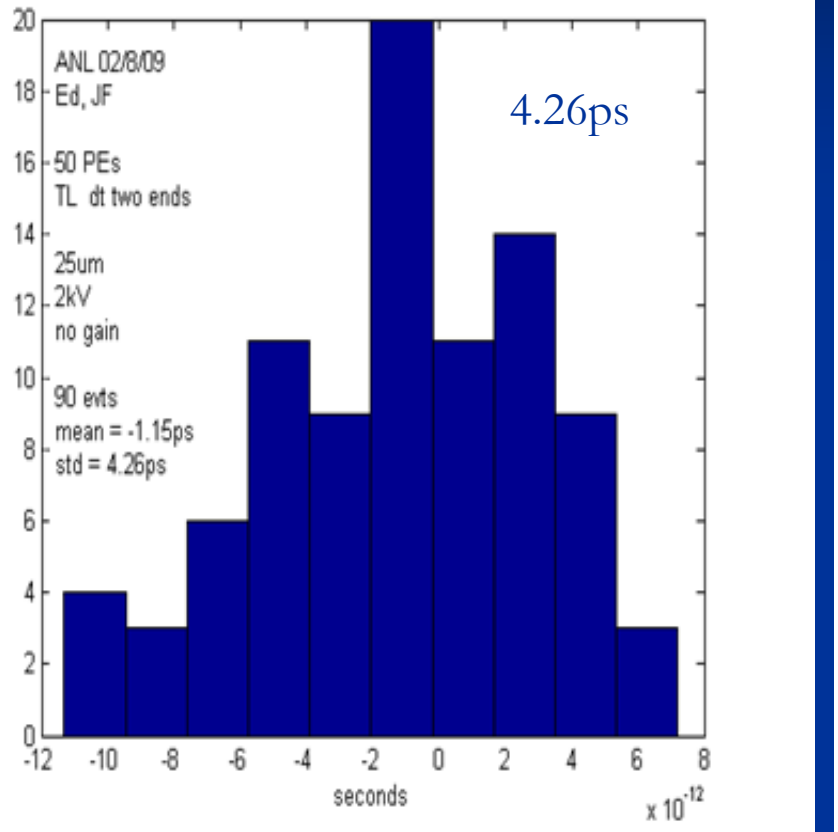
Test setup:

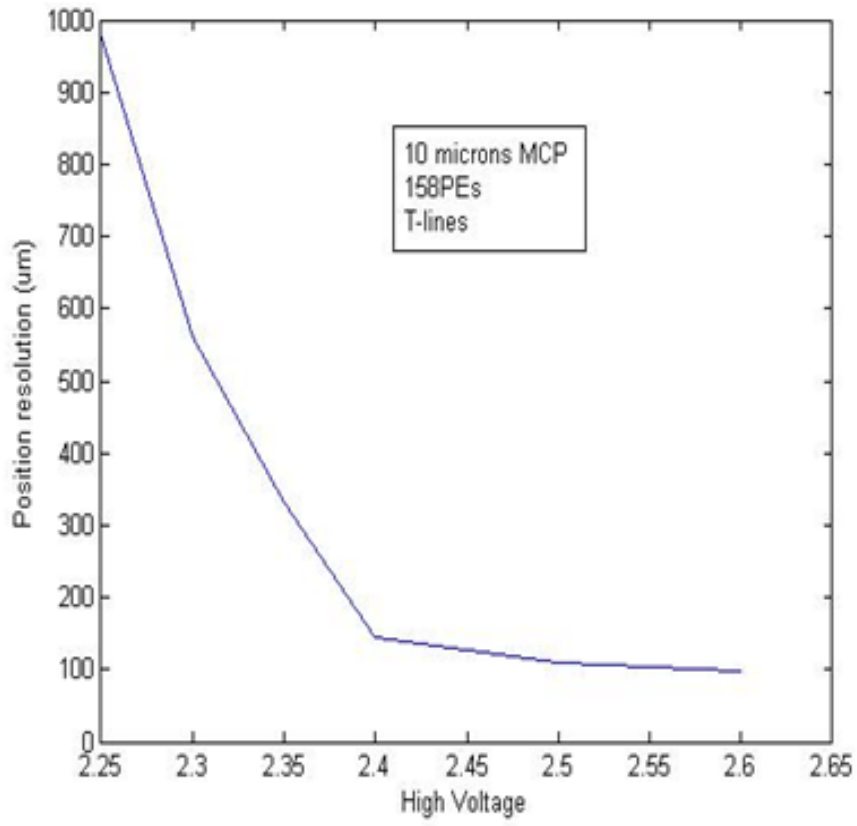
- Laser pulse with wavelength of 408nm, width of 70ps rms, Intensity of 50PEs
- 10um MCP at 2.5kV, read at two ends on 50 Ω line.
- 20 GHz sampling scope (Tek 6254C) + signal processing

Timing resolution for t1-t2 is 3.9ps rms

Results are almost same compared to previously measured with Ortec's constant fraction discriminator and TAC modules.

Timing & Spatial Resolution





Summary & Plan

- CMOS implementation allows us to design chip for large scale high resolution TOF system.
- Transmission line readout makes readout electronics channels be manageable .
- With 40Gs/s sampling chip, 2-3ps timing resolution can be achievable.
- Readout of timing, position and energy with a single chip without adding extra electronics.

3 Years Milestones:

Year 1: Submit a first prototype of psASIC chip (4-Channel) with timing control, sampling capacitor array and ADC blocks and test.

Year 2: Submit second fully functional psASIC chip (4-channel) and test.

Year 3: Submit 16(32)- channel psASIC chip and test.

Backup Slides