A Serial Link Transmitter in Monolithic Active Pixel Sensors

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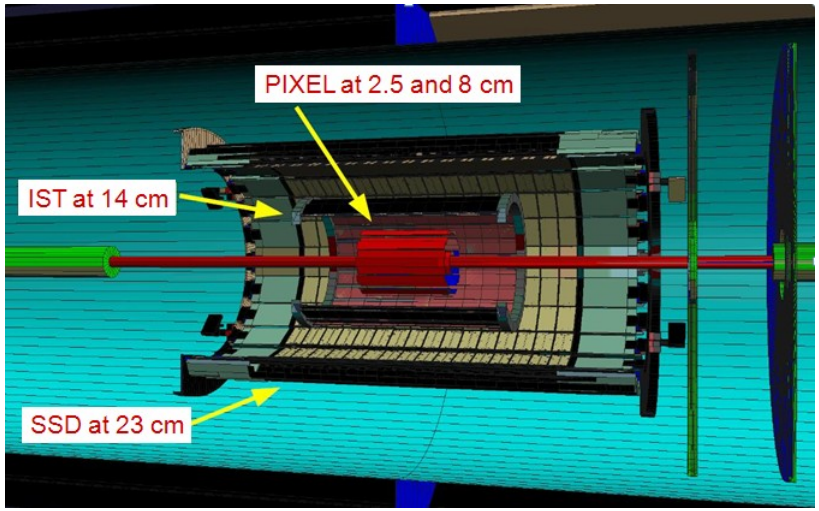
Outline

Propose a serial link transmitter prototype which is integrated in Monolithic Active Pixel Sensors (MAPS)

- **Motivation**
- **Architecture of Transmitter Prototype**
- **Implementation of Building Blocks**
  - ✓ **8B/10B Encoder**
  - ✓ **Serializer**
  - ✓ **Line Driver**
  - ✓ **Clock Generator**
- **Experiments Results**
- **Conclusion and Prospect**

Motivation(1): MAPS for Vertex Detector

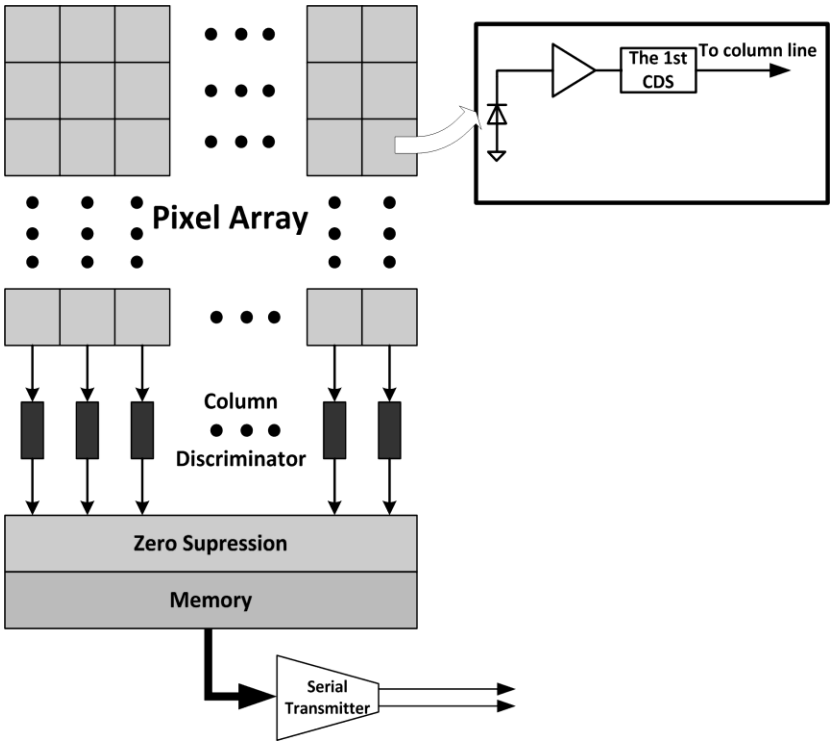
- **CMOS MAPS provide an attractive trade-off among granularity, material budget, readout speed, radiation tolerance and power consumption**
- **MAPS have been foreseen to equip several vertex detectors, such as in the upgrade of the Solenoidal Tracker at RHIC (STAR).**
- **Photodiode and front-end electronics are integrated on the same chip, providing small material budget to satisfy requirement of subatomic physics experiments.**



Heavy Flavor Tracker of the Solenoidal Tracker at RHIC (STAR) detector upgrade. At the STAR experiment, in order to achieve a vertex pointing resolution of about, or better than, 30 μm, two nearly cylindrical MAPS layers with averaged radii of about 2.5 cm and 8 cm, will be inserted in the existing detector.

Motivation(2): Tx In MAPS

MAPS data path:
- carriers collection by photodiodes
- preamplifier
- discriminator: several Gbits/s
- zero suppression
- memory
- data transmission at 160 Mbits/s

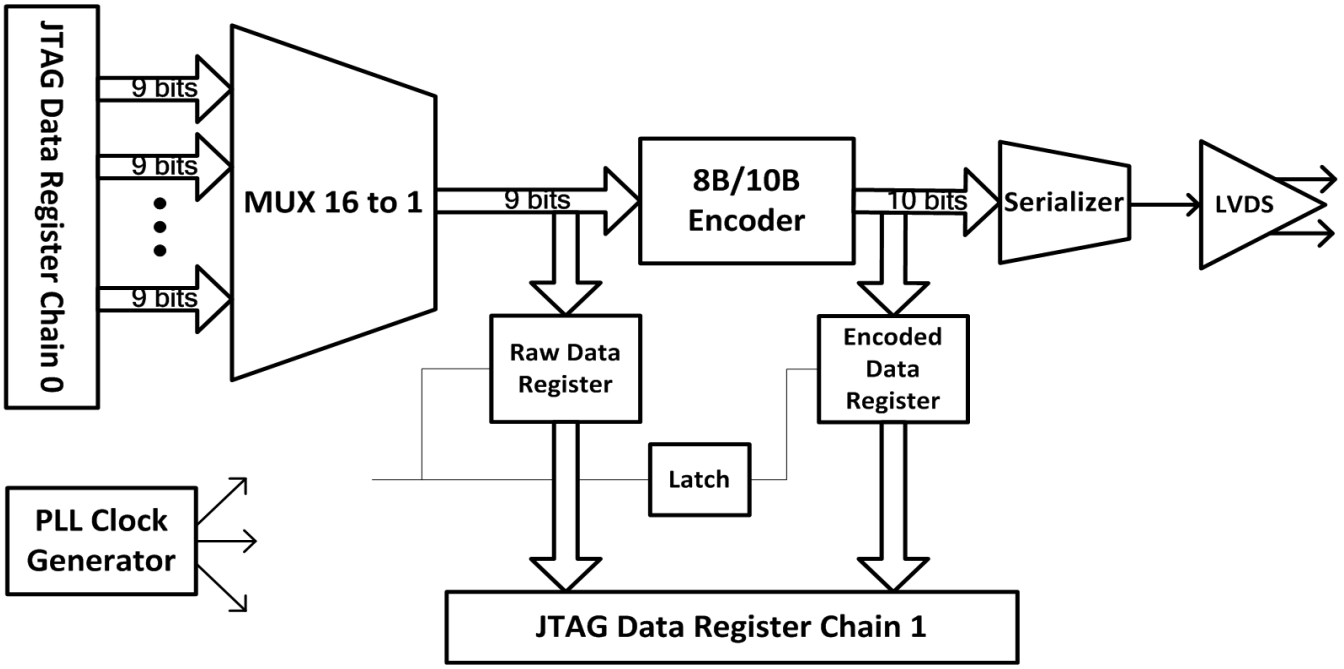


Architecture of MAPS

- **Small dead zone: Tx must be integrated on MAPS.**
- **Low Material budget: Cables used for data transmission are as less as possible.**

Serial transmitter in MAPS offers a fast link with only a differential cable.

Architecture of Transmitter Prototype



Architecture of serial transmitter

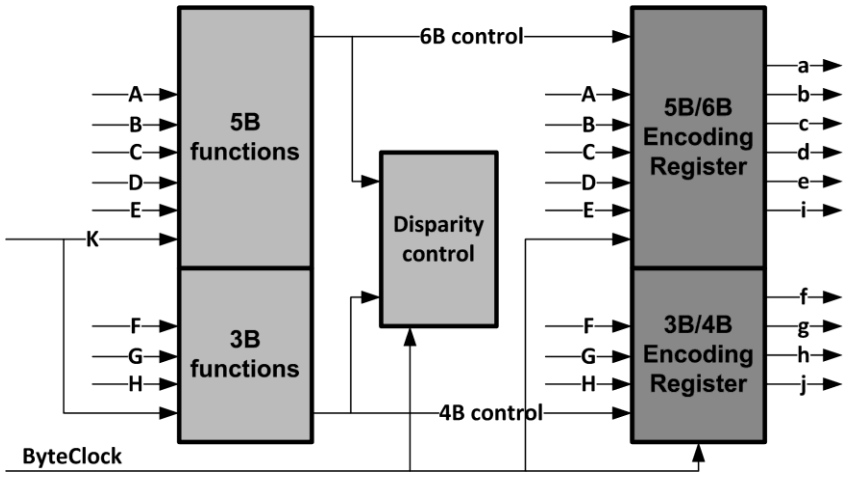
The design of the transmitter is organised according to five issues:

- Encoding parallel raw data to a suitable line code: 8b/10b encoding have enough edges to allow clock recovery
- Serializing encoded data
- Transmitting data sequence by a line driver
- Clock generation: low jitter, power supply noise insensitive
- Data for test is written and read by JTAG.

Building Blocks: 8B/10B Encoder

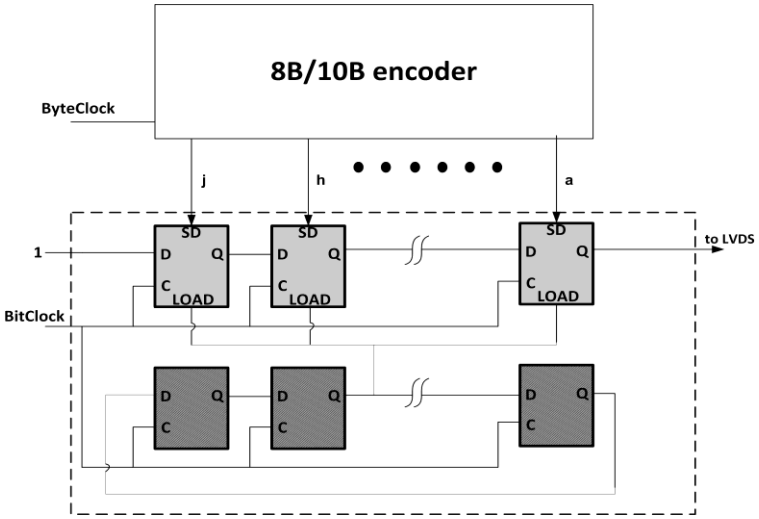
IBM proposed 8B/10B in 1983. Since the patent has expired, the scheme has become even more popular and is used in many standards.

- 8 bits symbols → 10 bits symbols: 20% of the bandwidth is overhead
- 256 data characters + 12 special characters: An additional input K is used to indicate special characters.
- DC balanced code: encoded data have enough edges to allow clock recovery.

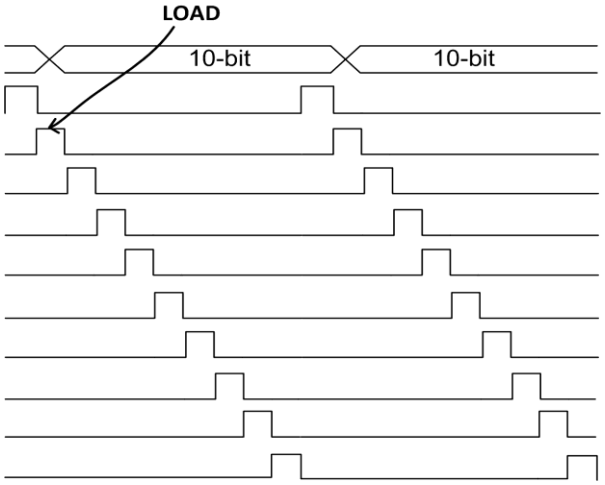


Block diagram of the 8B/10B encoder

Building Blocks: Serializer



Architecture of serializer



Timing sequences of loading signal

shift register based serializer

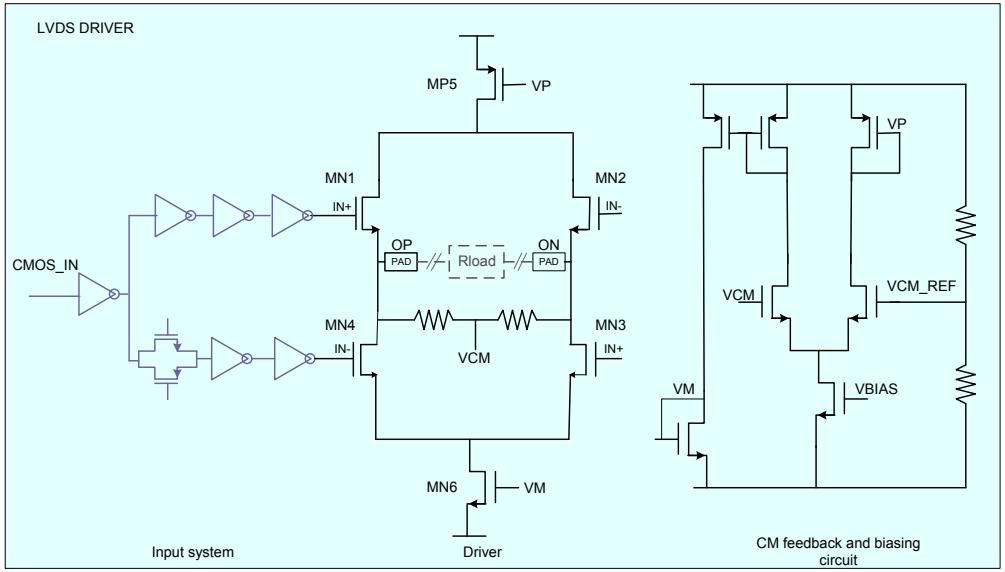
- clocked at bit rate frequency of 160 MHz
- periodically load parallel data at byte clock of 16 MHz
- highest operation frequency is limited by delay of scanning FF and proper loading signal

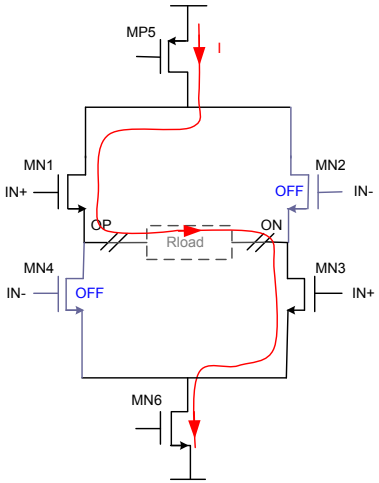
Typical FF delay:1ns ----- ok with our bit rate

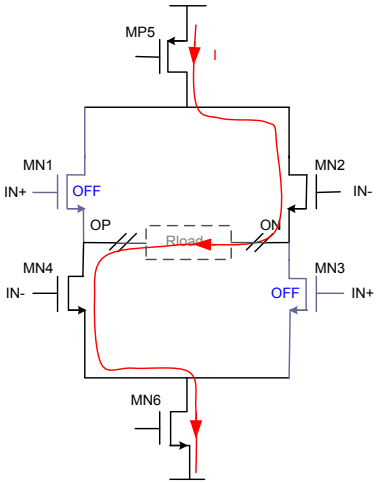
Loading signal generation is critical.

- A normal frequency divider doesn't work: combinational logic should be avoided
- Ring counter avoids using combinational logic

Building Blocks: LVDS driver







The low voltage differential signaling (LVDS) uses balanced signals to provide a high speed interconnection using a low voltage swing.

- ➢100Ω termination resistor
- ➢Maximum 400 mV differential swing
- ➢1.2V common mode voltage

driver works in current mode configuration:

✓ A adjustable bias current flows between two single ended outputs

✓ Four switches control polarity of transmission

✓ Common voltage is set by common mode feedback (CMFB) amplifier

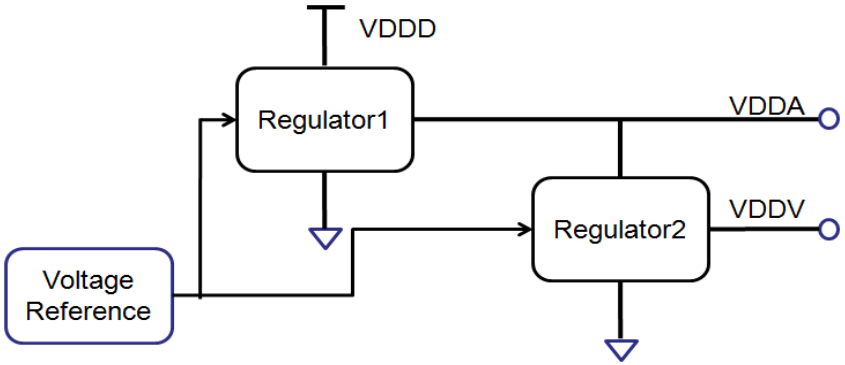
Typical current consumption: 5.6 mA

- ➢4 mA for driver
- ➢1.5 mA for common mode feedback

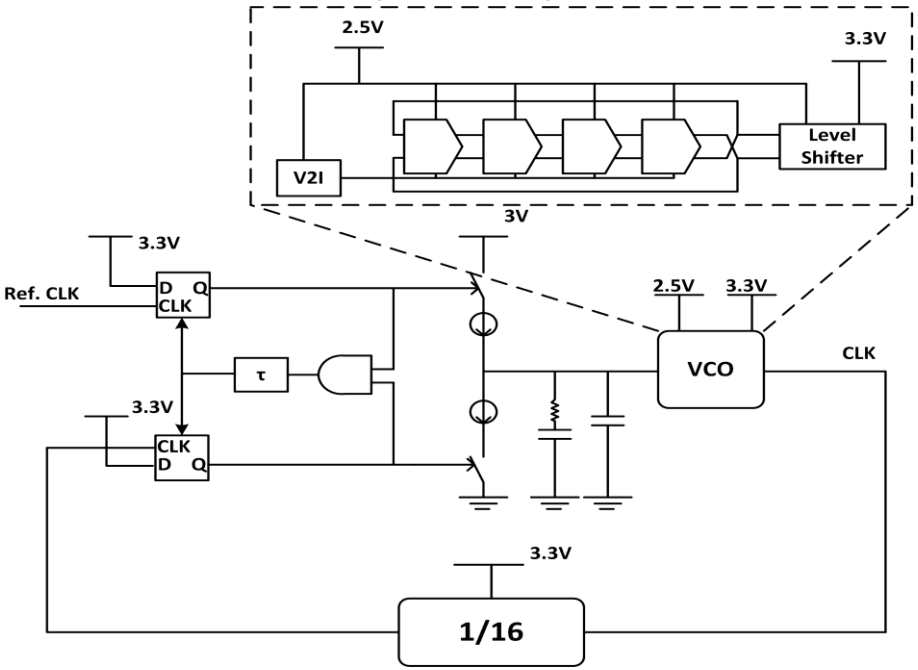
Building Blocks: Clock Generator

To minimize power supply noise from pixels and digital circuitry, a power supply noise insensitive PLL is required.

- Generating a 160 MHz 'bit-clock' for serializer from a 10 MHz reference clock.
- A on-chip voltage regulator with -40dB power supply noise rejection.
- A multi-power domain phase locked loop (PLL):
  - ✓VCO is very sensitive to power noise.
  - ✓Charge pump requires stable and large power

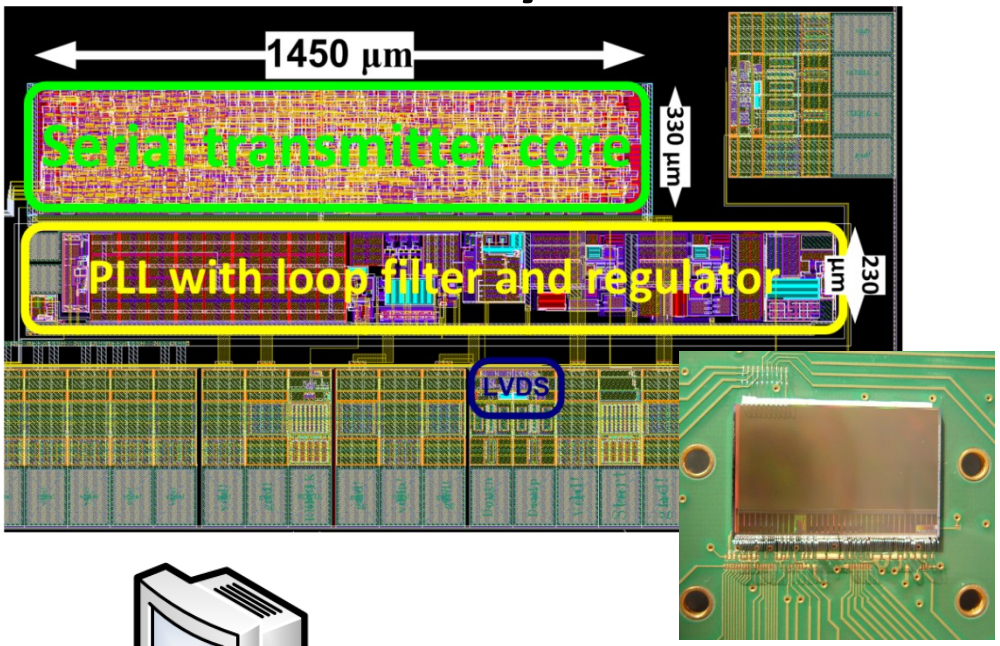


Block diagram of regulator



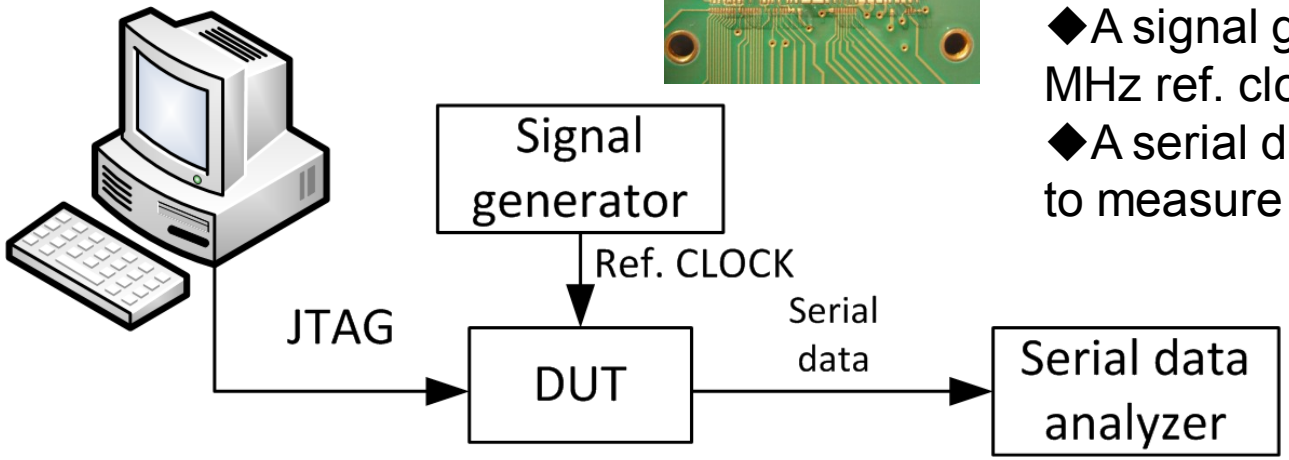
Multi-power domain PLL used in the transmitter

Implementation and Measurement (1): layout and test setup

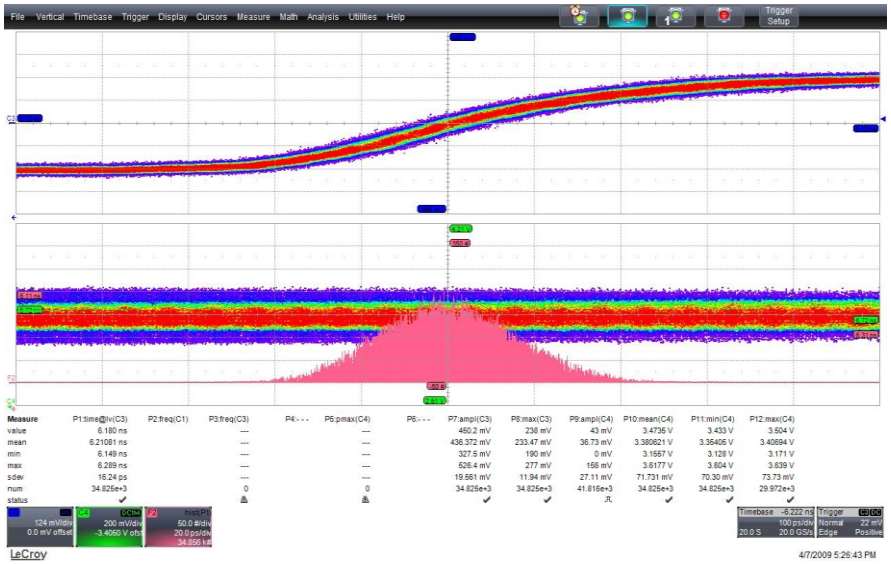


- AMS CMOS 0.35 µm tech.
- 0.92 mm^2
- Directly bond to PCB

◆Test data is sent to chip and read out by a PC through JTAG
◆A signal generator provides 10 MHz ref. clock
◆A serial data analyzer is used to measure clock and serial data



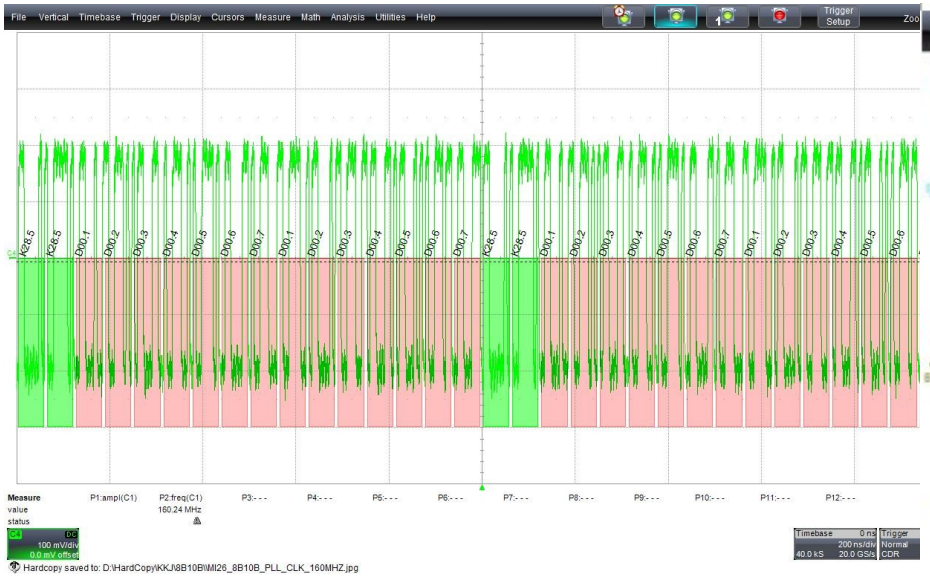
Implementation and Measurement (2): PLL Performance Summary



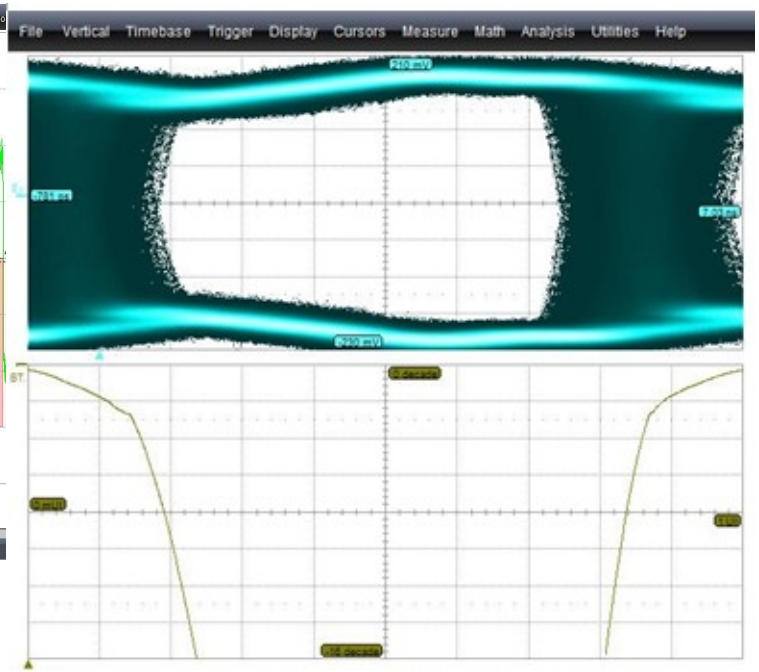
Jitter histogram of the PLL

PLL die area	0.42 mm^2 (with loop filter and on-chip regulator)
Multiplication Factor	16
Locking Range	138 MHz~300 MHz
Power Supply Requirement	3 V~3.6 V
Power Consumption	7 mW at 160 MHz
Period jitter (With voltage regulator)	13.64 ps at 160 MHz (clean power supply)
Period jitter (With voltage regulator)	16.24 ps at 160 MHz (supply modulated with 400 mV 10 kHz square wave)
Locking Time	60 μs

Implementation and Measurement (2): Measurement of The Transmitter



Decoded data on the serial data analyzer



Eye and bathtub of serial data

- Serial data can be decoded correctly
- Data eye is 60% opening at BER of 10^{-12} (160 MHz)
- bit rate could reach to 300 Mbit/s

The transmitter prototype is fully functional.

Conclusion and Prospect

- A serial link transmitter prototype for Monolithic Active Pixel Sensors is presented
- By using JTAG, This first prototype demonstrates line encoder, serializer, LVDS driver and clock generator with limited number of pads.
- The transmitter prototype works at 160 Mbit/s and could be extended to 300 Mbit/s.
- The clock generator in the transmitter provides good power supply noise immunity.

➢8B/10B encoder, serializer and LVDS driver can be reused in future work

➢Clock generator can be further improved: loop bandwidth, VCO

➢We may investigate optical fiber link for MAPS in next chip

Thank you for your attention!