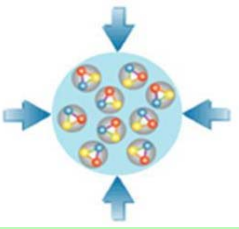


Active Buffer in CBM Experiment

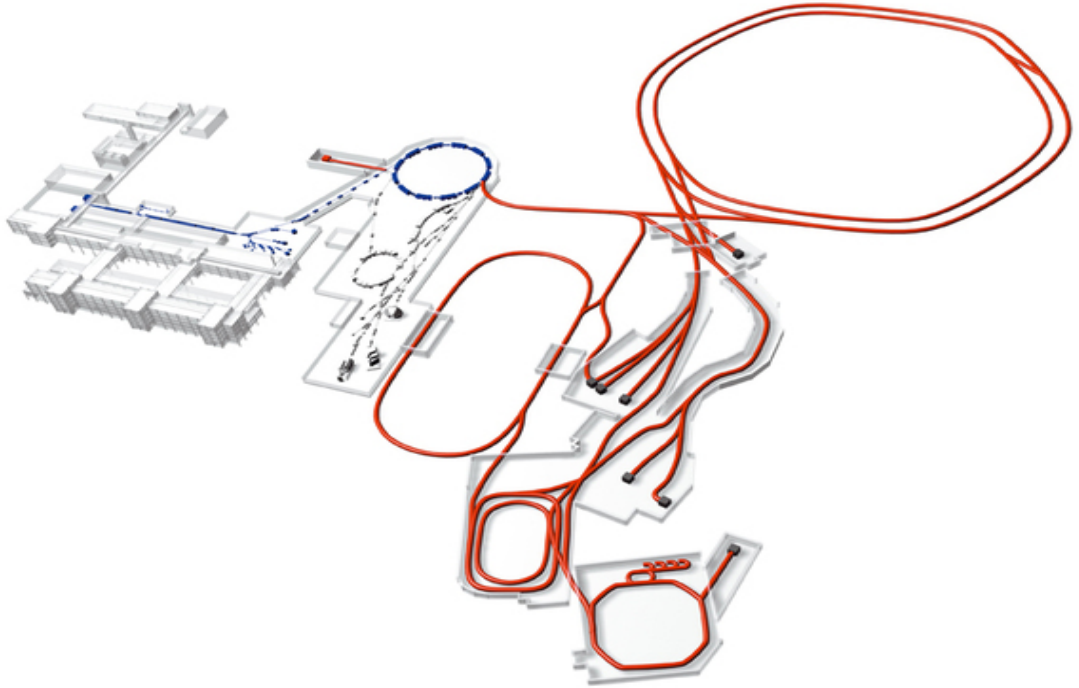
Wenxue Gao, Andreas Kugel,
Andreas Wurz, Guillermo Marcus, Reinhard Männer

ziti, University Heidelberg, Germany

15 May 2009

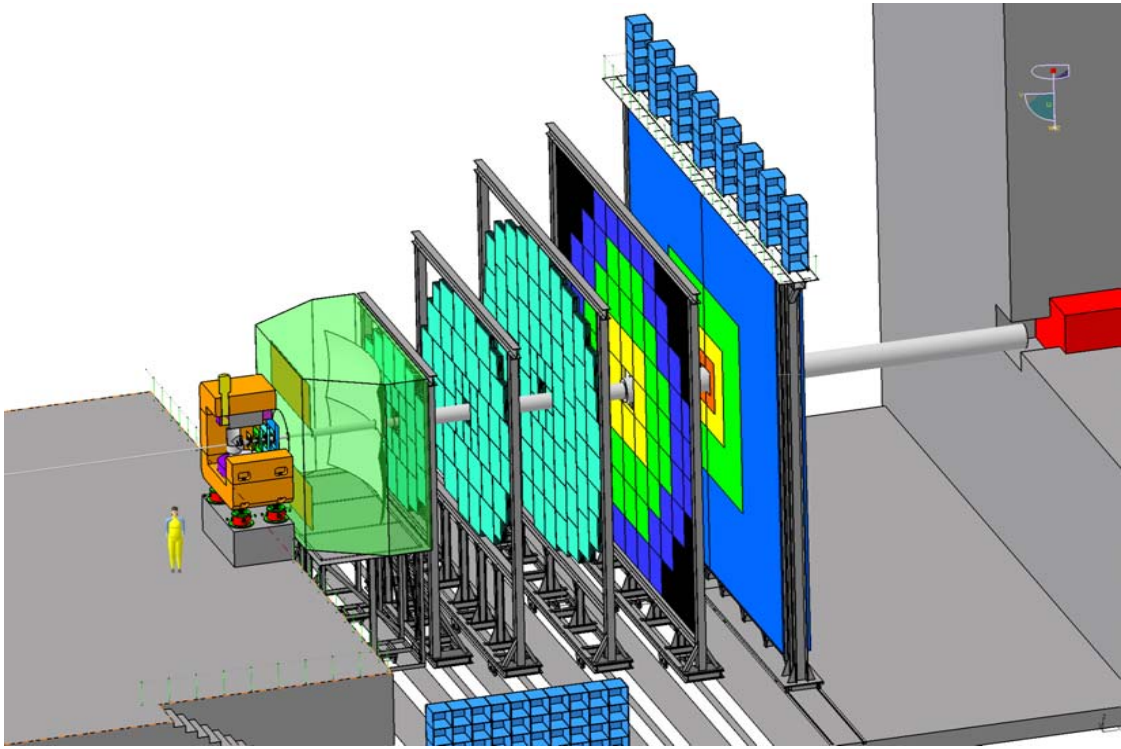
Agenda

- CBM
- Active Buffer
- PCI Express DMA
- Performance Tests



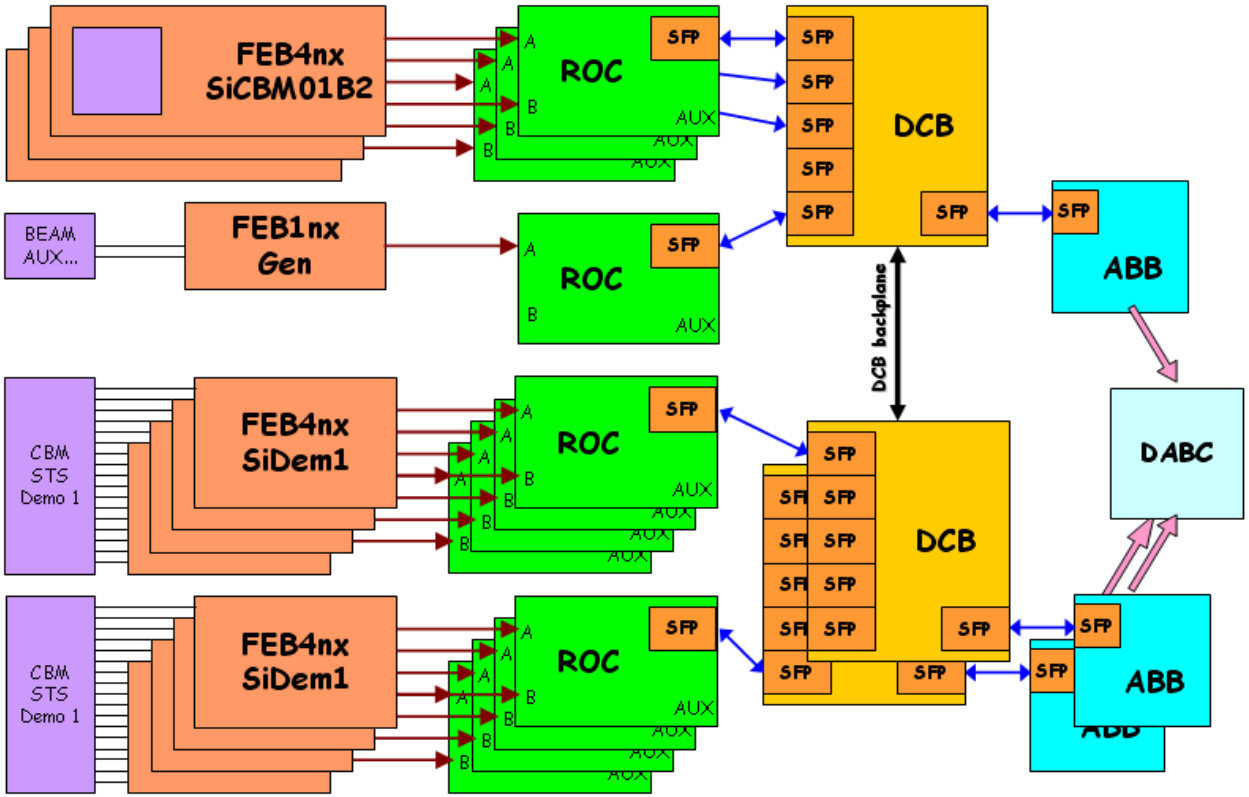
CBM Experiment

- Compressed Baryonic Matter
- FAIR@GSI, Darmstadt, Germany
- QCD phase
  - High Temperature
  - High baryon density
- ms after the big-bang
- Centre of neutron stars



DAQ of CBM

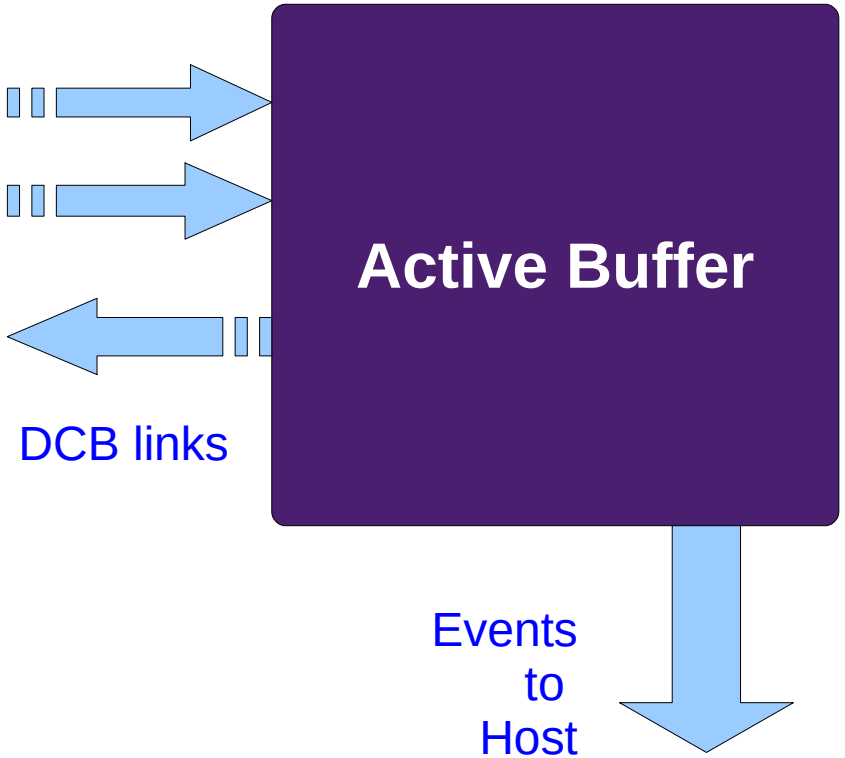
- – FEE – ROC – DCB – **Active Buffer** – DABC
- ~ 1TB/s data flow
  - 5Gbps / fibre
  - 3000x scale
- Small packets
- Trigger challenge
  - Non-trigger fashion



W.F.J. Müller, 06 Nov 2008

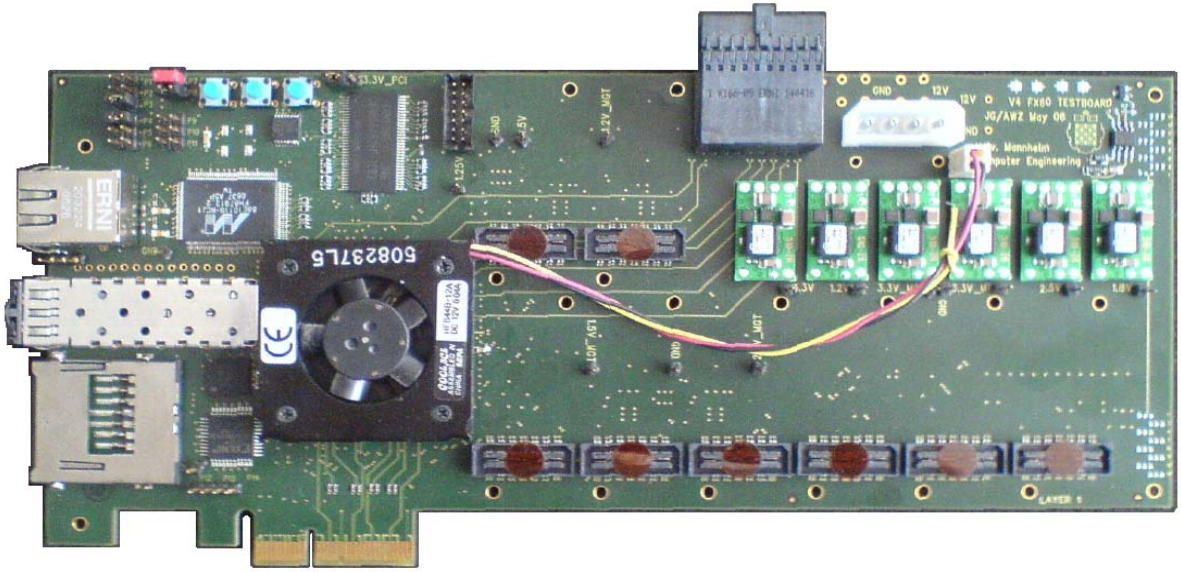
Active Buffer

- Powerful buffering system for hit packets
-
- Event building
  - Epoch marker
  - ROC ID
  - ...
- Traffic classes
- Dual-port memory emulation
- Fast channels to the host: PCI Express



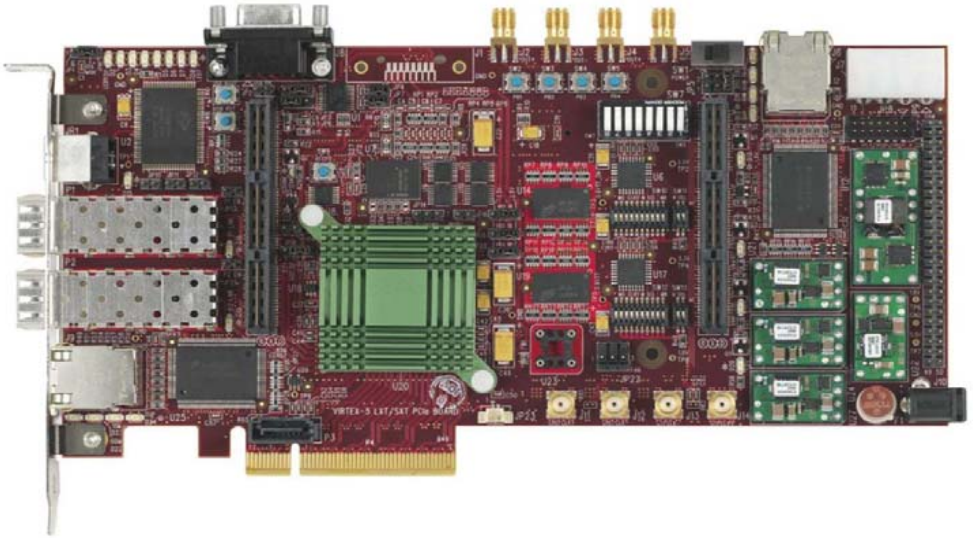
Prototype Board #1 - Virtex4

- FPGA - FX60
- Self-developed
  - 4-lane PCIe
  - DDR 32MB +
  - 1 fibre channel
- “Soft” PCIe core
- 32-bit interface
- 790 MB/s DMA write
- 480 MB/s DMA read
- Dynamical Partial Reconfiguration → *Norbert Abel, TDA4-4*



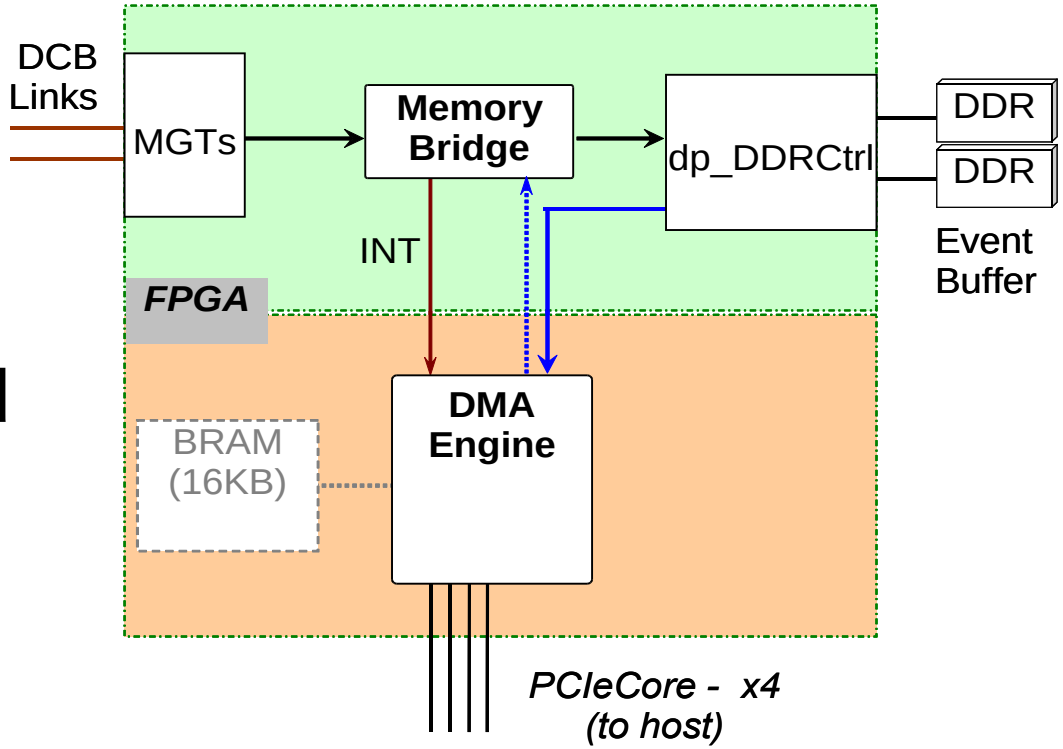
Prototype Board #2 - Virtex5

- AVNET AES-XLX-V5LXT-PCIE110-G
  - 8-lane PCIe
  - DDR2 SODIMM 256MB +
  - 2 fibre channels
- FPGA - LX110T
- “Hard” PCIe core
- 64-bit interface
- PLDA 8-lane reference design
  - 1013 MB/s DMA write
  - 960 MB/s DMA read



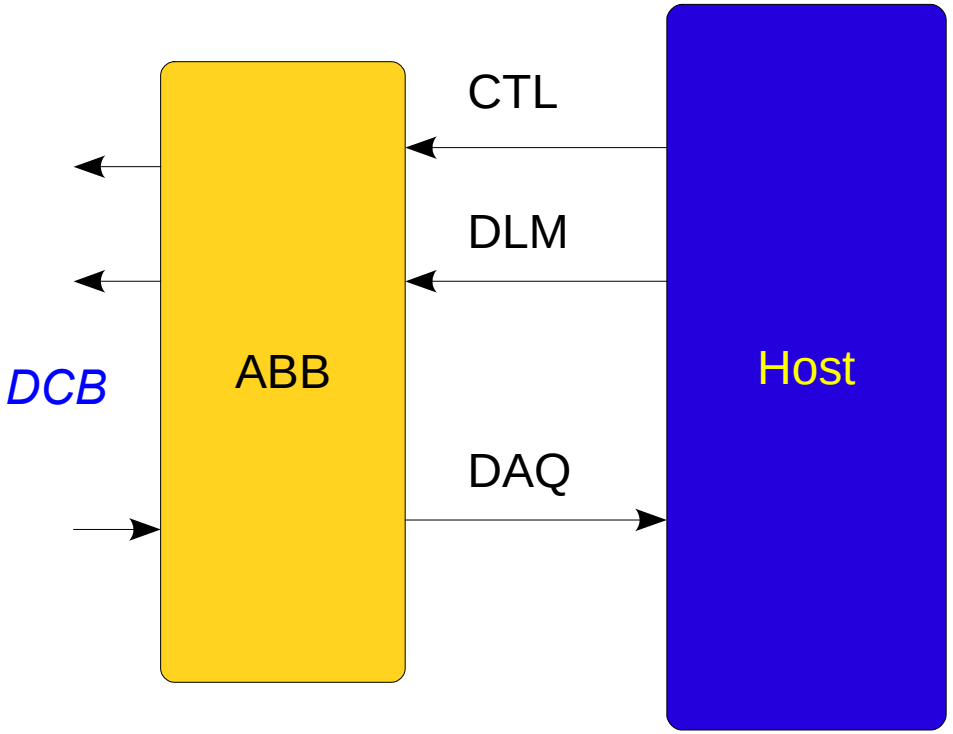
PCIe DMA Engine

- Transaction layer of PCIe
- Independent channels
  - Upstream
  - Downstream
- Concurrent DMA supported
- DONE status
  - INT
  - Polling
- PIO supported

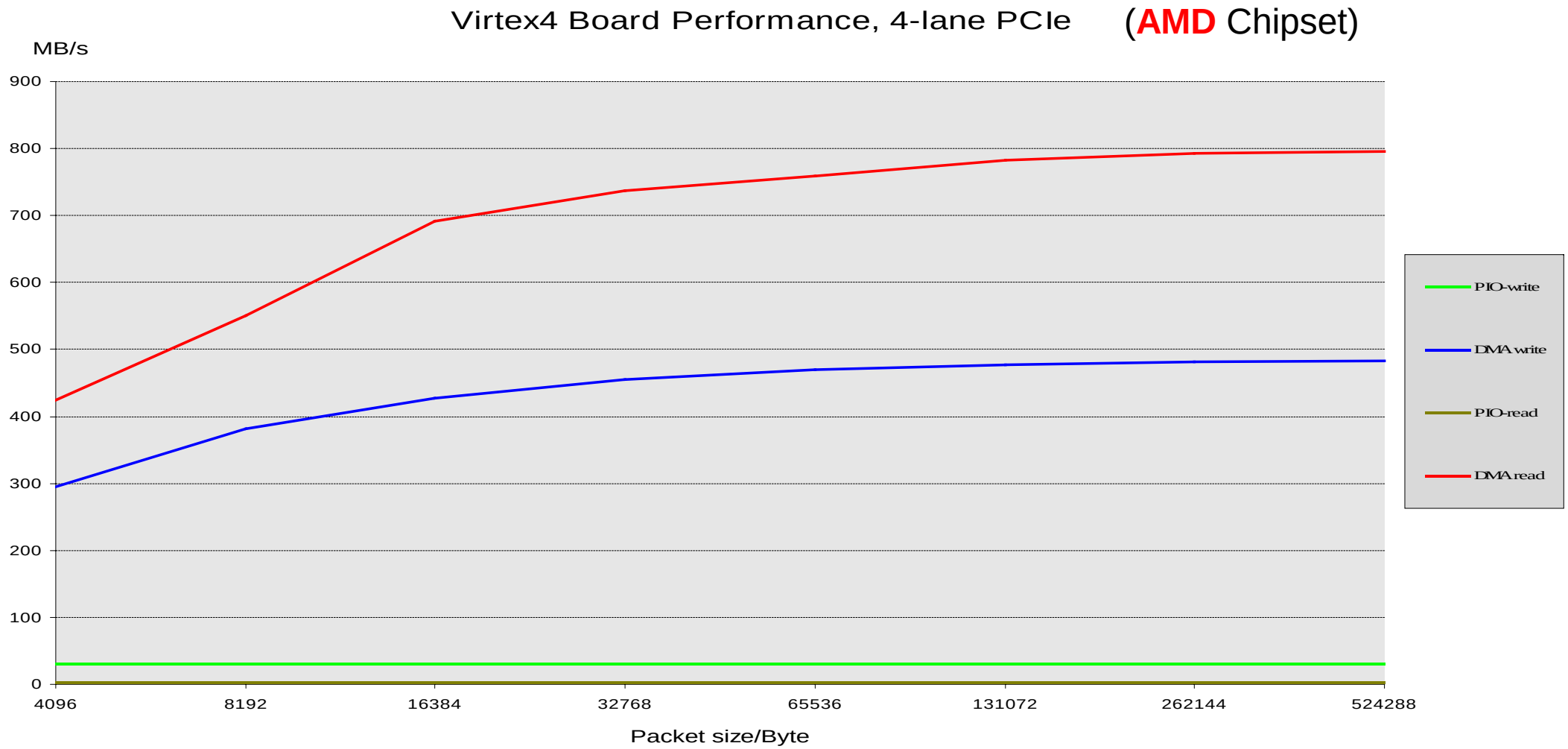


Driver & Library

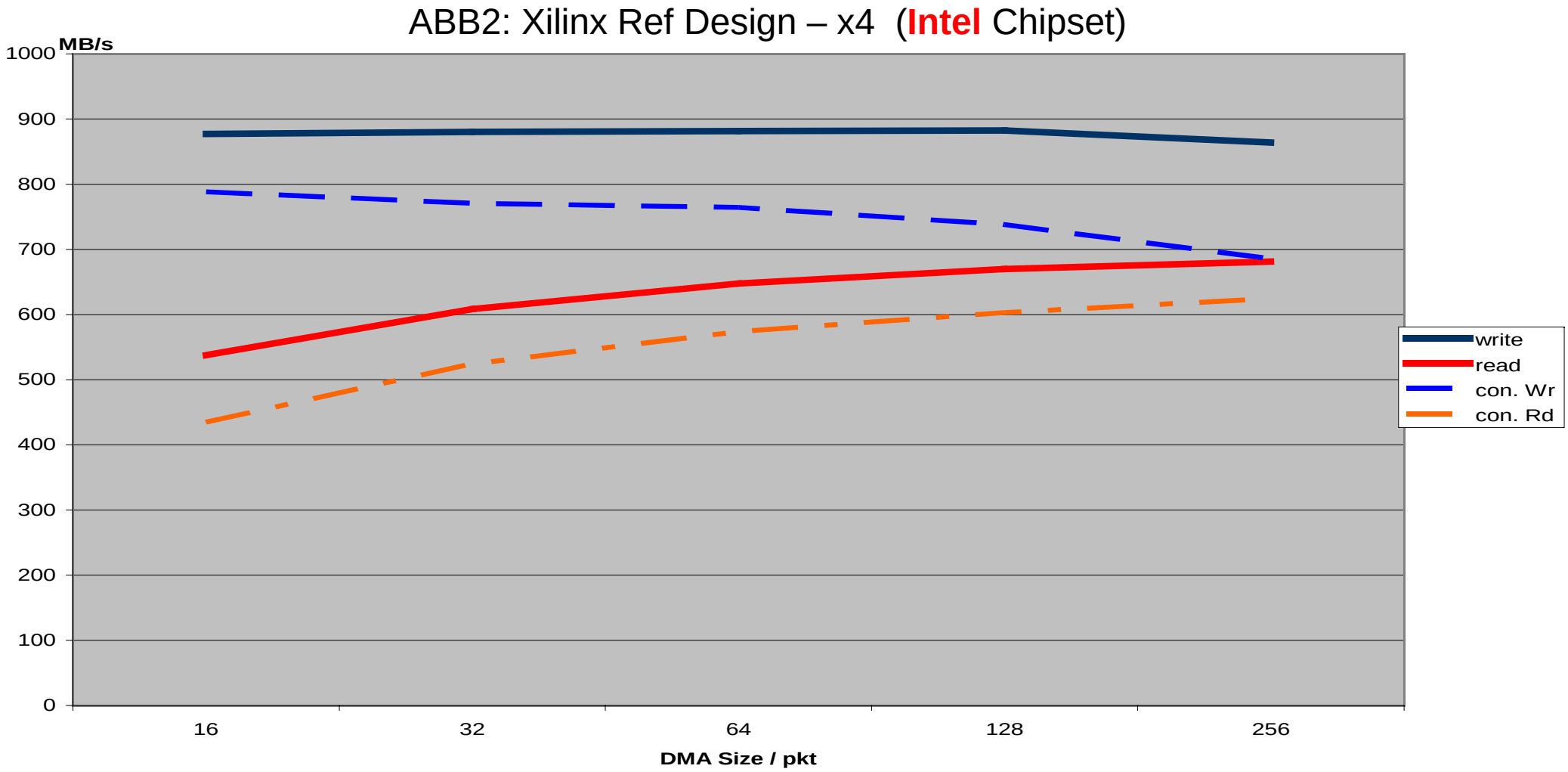
- Peer structure
- KERNEL & USER spaces
- Peek & poke
- Multiple-BAR support
  - Registers
  - RAM
  - FIFO/SDRAM
- Traffic classes
- Driver under Linux 2.6



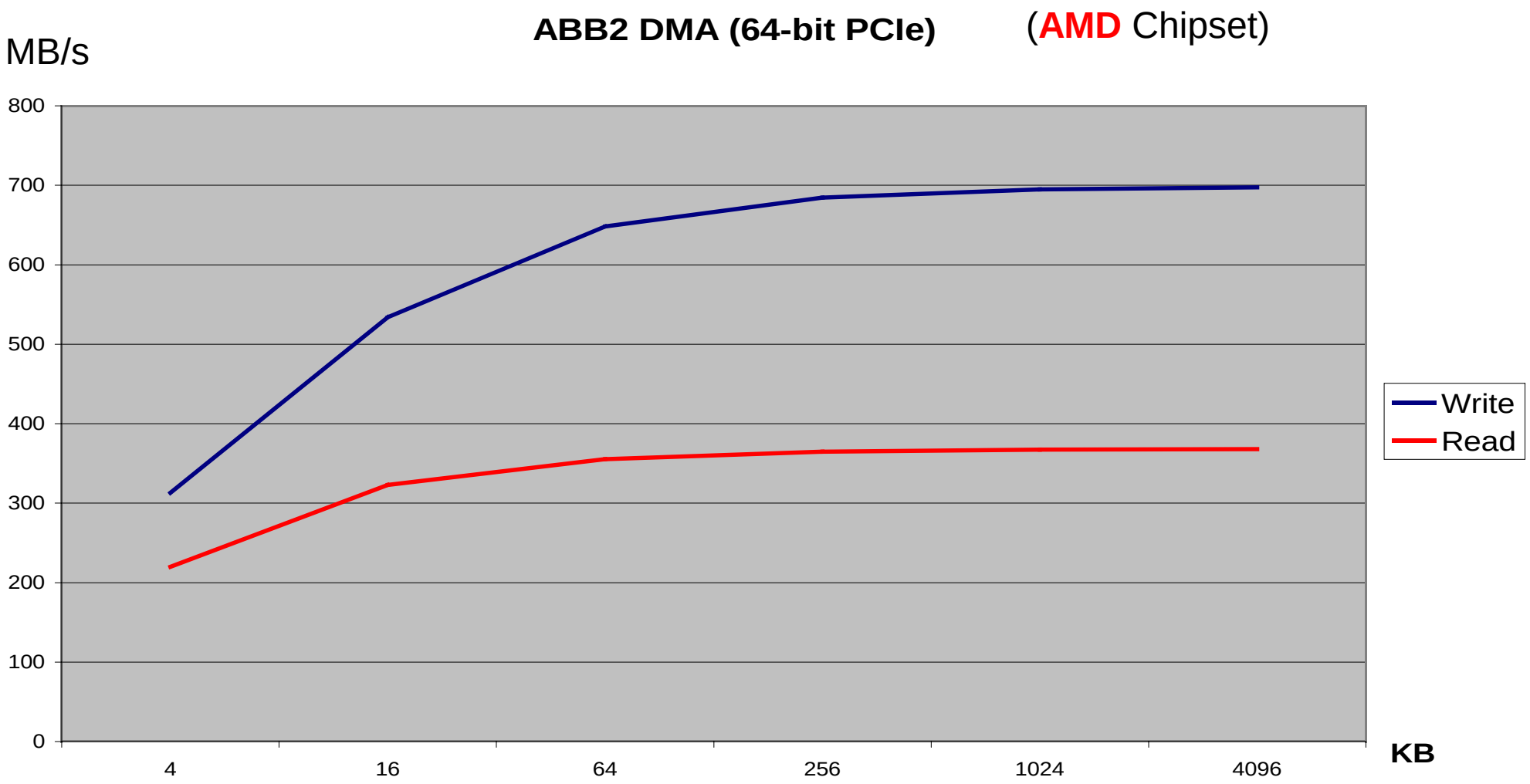
Performance Tests - 1



Performance Tests - 2a



Performance Tests - 2b



Notes on Tests

- Correctness guaranteed
- Performance strongly dependent upon the host chip-set
- DMA write is not going to target on the Event Buffer
  - the concurrent test on ABB2 not made
  - DMA write might be intended for CTL traffic
- Averaged from endurable running

Work being undertaken

-
- Debug Virtex5 basic DMA: DDR2 module calibration
- Adding more traffic classes support
- DMA read performance improvement

Summary

- HEP application
- Good bandwidth
- FPGA application
- PCI Express implementation
- Up-to-date memory modules
- Software framework