## Advances in Developing Next-Generation Electronics Standards for Physics

IEEE Real Time Conference & xTCA Workshop

Institute of High Energy Physics, IHEP

Beijing China

May 10-15, 2009 Ray S. Larsen

SLAC National Accelerator Laboratory
Chair, PICMG xTCA for Physics Coordinating
Committee





#### **Outline**

- Physics Interest in ATCA & MicroTCA (xTCA)
- Achieving Interoperability
  - Hardware Software Firmware
  - The Important Role of IPMI
  - Interoperability Testing within PICMG
- PICMG xTCA for Physics Coordinating Committee
  - Defining Physics Requirements
  - Progress to Date
  - Future Plans
  - How to Participate
- Acknowledgment





## Physics Interest in xTCA

- PICMG ATCA, AMC standard specifications released June 2004
  - "The most ambitious development ever undertaken by the PICMG Consortium."
  - Unique for Telecom industry to adopt common modular platform:
    - Up front R&D cost savings, shorter time-to-market for new technology products
  - First attracted Physics due to (A) High Performance (BW, throughput), (B) High Availability design critical to next-generation very large machines
    - 1. PICMG press release, April 2009





## **Physics Developments In Progress**

- Growing evaluation projects at major labs
  - DESY, SLAC, IHEP, FNAL, ANL, BNL, KEK, CERN, FZJ, IN2P3, IPFN, JET, ...
- Direct interest by funded and future projects
  - XFEL, ILC, ITER, JET, ATLAS Upgrade, Project X, FAIR, AGATA, ...
- xTCA interest both accelerators and experiments
- Interest in options: ATCA+RTM,
   ATCA+AMC+RTM, AMC-μTCA (MTCA) + μRTM¹
  - New, under discussion by Physics Coordinating Committee





### Other Developments of Interest

- Interest by medical physics company for new video rate imaging platform
- µTCA generating strong interest among companies serving non-telecom industrial control, instrumentation markets
- Industry developing analog products, AMC Mezzanine adapters for existing standards such as Industry Pack (IP)
- PICMG announces new committee to explore nontelecom applications esp. high BW computing – Apr 2009





## **xTCA** Components for Evaluation



5-Slot Shelf w/Dual Processors & Hub Switcher



14-Slot Shelf



SLAC DAQ 2Gb/s DAQ



AMC 105 MS/s 8ChADC



μTCA 6 Slot 1U Shelf



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**AMC Module** 

#### xTCA Evaluations 2 DESY (Kay Rehlich)



- Development of an 'universal' AMC module
  - Hardware design with Virtex5 and 256MB DDR2 SRAM (1GB/s)
  - FPGA code development with PCIe interface and DMA
    - 370 MB/s into user space (128byte payload size)
  - DOOCS server and OS driver with hot-swap
  - → IPMI code for 'Module Management Controller' (Atmega-128)
  - Piggyback with 2 ADC and 2 DAC channels, 100MHz





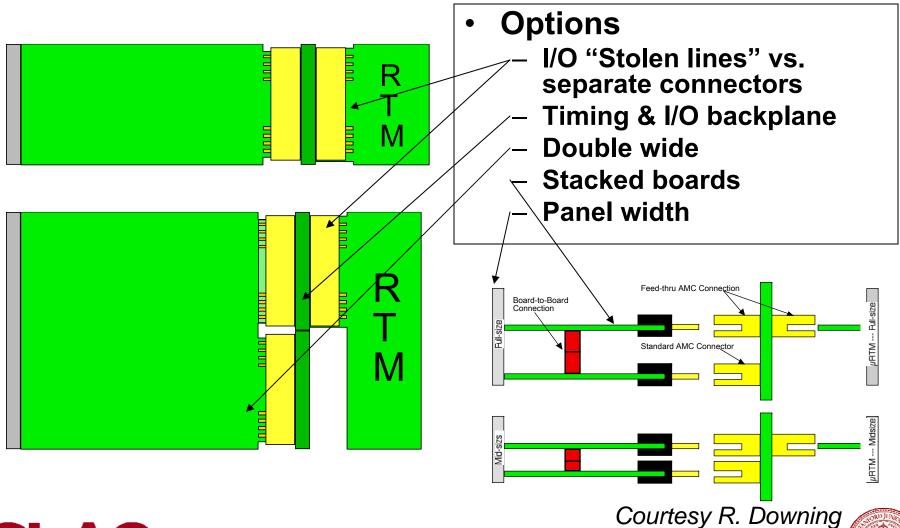
# PICMG xTCA for Physics Coordinating Committee Technical Subcommittee

- Why a Physics Subcommittee of PICMG?
- Major Goals of a formal specifications, guidelines effort
  - Maximize commonality of infrastructure choices for interoperability of products, whether designed in labs or industry or a partnership
  - Collaborate to get best possible system architecture, designs for future major lab systems
  - Save engineering development effort for new designs, both hardware and software; concentrate on unique problems within stable platform
  - Share infrastructure designs, drivers, firmware, system software before embarking on major new system designs
  - Make products available through industry by developing large enough markets to be interesting for industry
  - Avoid destructive fragmentation of the relatively small physics market!





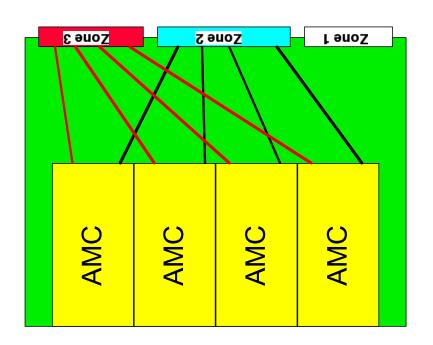
# Technical Challenges 1 Single & Double Wide on µTCA

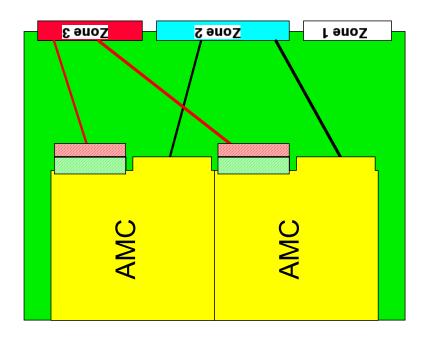




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#### Single & Double Wide on ATCA Carrier





- All I/O, special timing connections via Zone 3
- All serial data connections via Zone 2
- All Power Zone 1



Courtesy R. Downing



#### "Stolen Lines" Initial Concept for µRTM

Pin #	Signal	Driven By	Mating	Pin Function on the AMC	Pin#	Signal	Driven By	Mating	Pin Function on the AMC
85	GND	Carrier	First	Ground	86	GND	Carrier	First	Ground
84	PWR	Carrier	First	Power, 12V	87	Rx8-	AMC or	Third	Port 8 Rcvr -
83	PS0#	Carrier	Last	Presence 0	88	Rx8+	Carrier	Third	Port 8 Rcvr +
82	GND	Carrier	First	Ground	89	GND	Carrier	First	Ground
81	FOLKA-	FCLKA	Third	Fabric Clock A -	90	Tx8-	AMC or	Third	Port 8 Xmitter -
80	FCLKA+	driver	Third	Fabric Clock A -	91	Tx8+	Carrier	Third	Port 8 Xmitter +
79	GND	Carrier	First	Ground	92	GND	Carrier	First	Ground
78	TCLKB-	FCLKB	Third	Telco Clock B -	93	Rx9-	Carrier	Third	Port 9 Rcvr -
77	TCLKB+	driver	Third	Telco Clock B +	94	Rx9+		Third	Port 9 Rcvr+
76	GND	Carrier	First	Ground	95	GND	Carrier	First	Ground
75	TCLKA-	FCLKC	Third	Telco Clock A -	96	Tx9-	AMC	Third	Port 9 Xmitter -
74	TCLKA+	driver	Third	Telco Clock A +	97	Tx9+		Third	Port 9 Xmitter +
73	GND	Carrier	First	Ground	98	GND	Carrier	First	Ground
72	PWR	Carrier	First	Power, 12V	99	Rx10-	Carrier	Third	Port 10 Rcvr -
71	SDA_L	IPMI Agent	Second	IPMB-L Data	100	Rx10+		Third	Port 10 Rcvr+
70	GND	Carrier	First	Ground	101	GND	Carrier	First	Ground
69	Rx7-	Carrier	Third	Port 7 Rcvr -	102	Tx10-	AMC	Third	Port 10 Xmitter -
68	Rx7+	Carrior	Third	Port 7 Rcvr+	103	Tx10+	74110	Third	Port 10 Xmitter +
67	GND	Carrier	First	Ground	104	GND	Carrier	First	Ground
66	Tx7-	AMC	Third	Port 7 Xmitter -	105	Rx11-	Carrier	Third	Port 11 Rcvr -
65	Tx7+	AIVIC	Third	Port 7 Xmitter +	106	Rx11+	Carner	Third	Port 11 Rcvr+
64	GND	Carrier	First	Ground	107	GND	Carrier	First	Ground
63	Rx6-		Third	Port 6 Rcvr -	108	Tx11-	AMC	Third	Port 11 Xmitter -
62	Rx6+	Carrier	Third	Port 6 Rcvr +	109	Tx11+		Third	Port 11 Xmitter +
61	GND	Carrier	First	Ground	110	GND	Carrier	First	Ground
60	Tx6-		Third	Port 6 Xmitter -	111	I/O 15-	AMCor	Third	Port 15 I/O -
59	Tx6+	AMC	Third	Port 6 Xmitter +	112	I/O 15+	Carrier	Third	Port 15 I/O+
58	GND	Carrier	First	Ground	113	GND	Carrier	First	Ground
57	PWR	AMC	First	Power, 12V	114	I/O 14-	AMCor	Third	Port 14 I/O -
56	SCL L	IPMI Agent	Second	IPMB-L Clock	115	I/O 14+	Carrier	Third	Port 14 I/O+
55	GND	Carrier	First	Ground	116	GND	Carrier	First	Ground
54	Rx5-		Third	Port 5 Rcvr -	117	I/O 13-	AMC or	Third	Port 13 I/O -
53	Rx5+	Carrier	Third	Port 5 Rcvr +	118	I/O 13+	Carrier	Third	Port 13 I/O+
52	GND	Carrier	First	Ground	119	GND	Carrier	First	Ground
51	Tx5-		Third	Port 5 Xmitter -	120	I/O 12-	AMCor	Third	Port 12 I/O -
50	Tx5+	AMC	Third	Port 5 Xmitter +	121	I/O 12+	Carrier	Third	Port 12 I/O+
49	GND	Carrier	First	Ground	122	GND	Carrier	First	Ground
48	Rx4-		Third	Port 4 Rcvr -	123	I/O 11-	AMC or	Third	Port 11 I/O -
47	Rx4+	Carrier	Third	Port 4 Rcvr +	124	I/O 11+	Carrier	Third	Port 11 I/O+
46	GND	Carrier	First	Ground	125	GND	Carrier	First	Ground
45	Tx4-		Third	Port 4 Xmitter -	126	I/O 10-	AMCor	Third	Port 10 I/O -
44	Tx4+	AMC	Third	Port 4 Xmitter +	127	I/O 10+	Carrier	Third	Port 10 I/O+
43	GND	Carrier	First	Ground	128	GND	Carrier	First	Ground
42	PWR	Carrier	First	Power, 12V	129	I/O9-	AMC or	Third	Port 9 I/O -
41	ENABLE#	Carrier	Second	AMC Enable	130	I/O9+	Carrier	Third	Port 9 I/O+
40	GND	Carrier	First	Ground	131	GND	Carrier	First	Ground
39	Rx3-		Third	Port 3 Rcvr -	132	I/O8-	AMC or	Third	Port 8 I/O -
38	Rx3+	Carrier	Third	Port 3 Rcvr +	133	I/O8+	Carrier	Third	Port 8 I/O+
37	GND	Carrier	First	Ground	134	GND	Carrier	First	Ground
36	Tx3-		Third	Port 3 Xmitter -	135	TOLKC	FCI KC	Third	Telco Clock C-
35	Tx3+	AMC	Third	Port 3 Xmitter +	136	TCLKC+	driver	Third	Telco Clock C+
34	GND	Carrier	First	Ground	137	GND	Carrier	First	Ground
	SIL	Cullici			138	TOLKO-	FCLKD	Third	Telco Clock D -
	R <sub>2</sub> -	_							
33 32	Rx2- Rx2+	Carrier	Third Third	Port 2 Rcvr - Port 2 Rcvr +	139	TO KD+	driver	Third	Telco Clock D +

30	Tx2-	AMC	Third	Port 2 I/O -	141	1/07-	AMC or	Third	Port 7 I/O -
29	Tx2+	AWC	Third	Port 2 I/O +	142	1/07+	Carrier	Third	Port 7 I/O+
28	GND	Carrier	First	Ground	143	GND	Carrier	First	Ground
27	PWR	Carrier	First	Power, 12V	144	1/06-	AMC or	Third	Port 6 I/O-
26	GA2	Carrier	Second	Geog. Addr. 2	145	1/06+	Carrier	Third	Port 6 I/O+
25	GND	Carrier	First	Ground	146	GND	Carrier	First	Ground
24	Rx1-	Carrier	Third	Port 1 I/O -	147	1/05-	AMC or	Third	Port 5 I/O-
23	Rx1+	Camer	Third	Port 1 I/O +	148	I/O5+	Carrier	Third	Port 5 I/O+
22	GND	Carrier	First	Ground	149	GND	Carrier	First	Ground
21	Tx1-	AMC	Third	Port 1 I/O -	150	1/04-	AMC or	Third	Port 4 I/O-
20	Tx1+	7	Third	Port 1 I/O +	151	1/04+	Carrier	Third	Port 4 I/O+
19	GND	Carrier	First	Ground	152	GND	Carrier	First	Ground
18	PWR	Carrier	First	Power, 12V	153	1/03-	AMC or	Third	Port 3 I/O-
17	GA1	Carrier	Second	Geog. Addr. 1	154	I/O3+	Carrier	Third	Port 3 I/O+
16	GND	Carrier	First	Ground	155	GND	Carrier	First	Ground
15	Rx0-	Carrier	Third	Port 0 I/O -	156	I/O2-	AMC or	Third	Port 2 I/O-
14	Rx0+	Carrier	Third	Port 0 I/O +	157	1/02+	Carrier	Third	Port 2 I/O+
13	GND	Carrier	First	Ground	158	GND	Carrier	First	Ground
12	Tx0-	AMC	Third	Port 0 I/O -	159	I/O1-	AMC or	Third	Port 1 I/O-
11	Tx0+	AVIC	Third	Port 0 I/O +	160	I/O1+	Carrier	Third	Port 1 I/O+
10	GND	Carrier	First	Ground	161	GND	Carrier	First	Ground
9	PWR	Carrier	First	Power, 12V	162	I/O.0-	AMCor	Third	Port 0 I/O -
8	RSRVD8		Second	Reserved	163	I/O 0+	Carrier	Third	Port 0 I/O +
7	GND	Carrier	First	Ground	164	GND	Carrier	First	Ground
6	RSRVD6		Second	Reserved	165	TOK	Carrier	Second	JTAG Clk In
5	GA0	Carrier	Second	Geog. Addr. 0	166	TMS	Carrier	Second	JTAG Mode Sel In
4	MP	Carrier	First	Power, 3.3V	167	TRST#	Carrier	Second	JTAG Rst In
3	PS1#	AMC	Last	Presence 1	168	TDO	AMC	Second	JTAG Data Out
2	PWR	Carrier	First	Power, 12V	169	TDI	Carrier	Second	JTAG Data In
1	GND	Carrier	First	Ground	170	GND	Carrier	First	Ground
KEY									
	Color	Function			# Pins		Notes		
		Ground			56				
		Power +1	2 V		8		limited to 80	W for AM	Cmodule
		Power +3			1		power for ma		
		System Management Interface			13		Mant 5. GA - 3. JTAG - 5		
		Common Options Fabrics			16		reserve 4 channels for fabric connec		
		Clocks			10		telco spec'd. useful?		
		RTM signals			64		16 channels converted to 32 diff. R		d to 32 diff_RTM I/ 0
		Reserved			2		do not use!		
					-		GO 1 NOT 1000:		
				total	170				

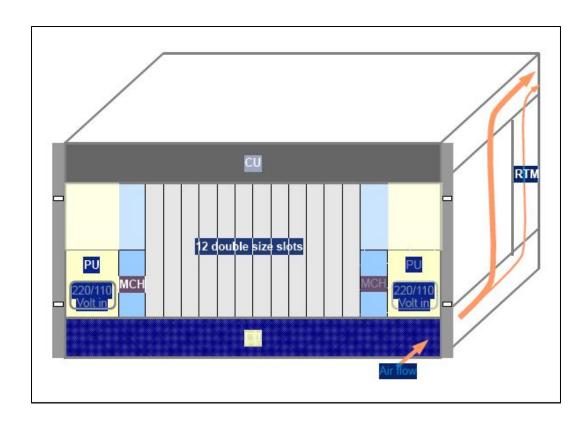
- •Appropriated unused Telco Lines for Physics I/O, clocks-sync-triggers
- •Note: Precision clocks best on star configuration, not bussed
- •Could use extraneous 10GbE lanes

Pin #	Signal	Driven By	Mating	Pin Function on AMC	Physics definition of Function on AMC
81	FCLKA-	FCLKA	Third	Fabric Clock A-	Used for PCIe in Physics
82	FCLKA-	driver	Third	Fabric Clock A+	Used for PCIe in Physics
78	TCLKB-	TCLKB	Third	Telco Clock B-	Physics Clock B-
77	TCLKB+	driver	Third	Telco Clock B+	Physics Clock B+
75	TCLKA-	TCLKA	Third	Telco Clock A-	Physics Clock A-
74	TCLKA-	driver	Third	Telco Clock A+	Physics Clock A+
135	TCLKC-	TCLKC	Third	Telco Clock C-	Physics Clock C-
136	TCLKC+	driver	Third	Telco Clock C+	Physics Clock C+
138	TCLKD-	TCLKD	Third	Telco Clock D-	Physics Clock D-
139	TCLKD+	driver	Third	Telco Clock D+	Physics Clock D+



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#### MicroTCA Shelf Concept (Kay Rehlich, DESY)



#### Features

- 12-Double high payload slots
- RTM powered
- Dual bulk power
- Dual MCH-Shelf Manager
- Accommodates standard AMC's in half height
- Scalable number of payloads
- Scalable redundancy





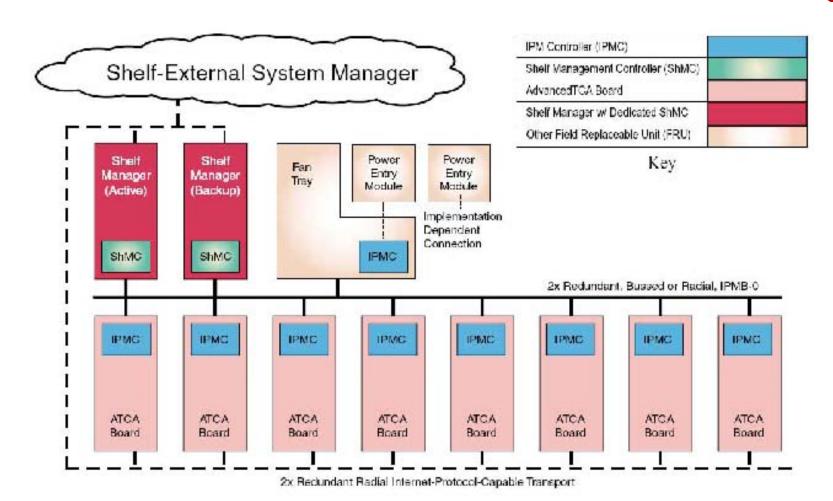
# **Technical Challenges 2**

- Auto-failover software for HA
- Low latency software & firmware protocols for fast feedback systems
- IPMI subsystem
  - Out-Of-Band vs. In-Band systems, HA implications of choices
  - Extension of IPMI to "non-managed-platform" chassis as currently found throughout accelerator systems





#### IPMI in ATCA (Chris Engels, 2008 Tutorial)



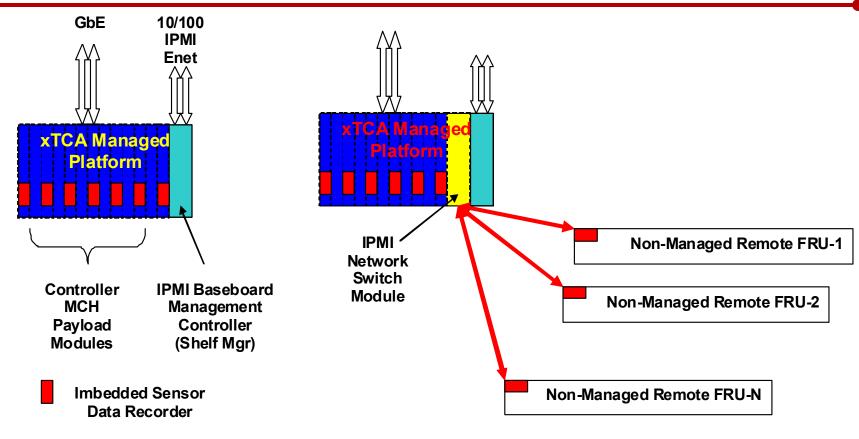
IPMI is the main Protocol of System Management

NATIONAL ACCELERATOR LABORATORS





# IPMI Concepts for Managed, Non-Managed Platform Extensions



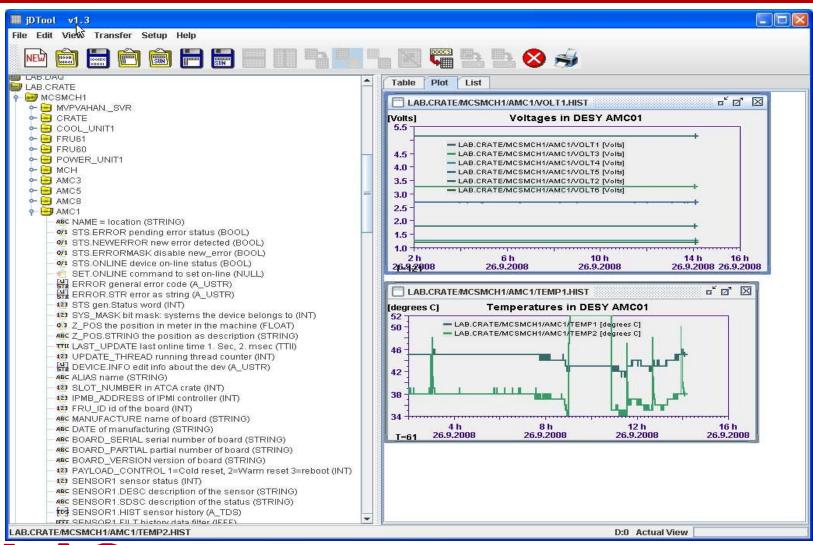
A. Managed System with Shelf IPMI

B. Managed System with Shelf IPMI Extended to Remote FRUs





### IPMI Example – DESY (Kay Rehlich)







#### IPMI Developments – DESY (Kay Rehlich)

#### IMPI code on Atmel-128

- Implements version 1.5 functions
- FPGA code loading in preparation
- IPMI control system integration
  - → Control System server for ATCA, µTCA and computers
  - IPMI communication via Ethernet to the crates
  - Extracts from IPMI the available information
  - Creates a dynamic list of AMC modules
  - Creates a dynamic list of sensors
  - Archives values and provides reset/boot commands to FPGAs or CPUs
  - Required configuration: one entry per crate (IP name)





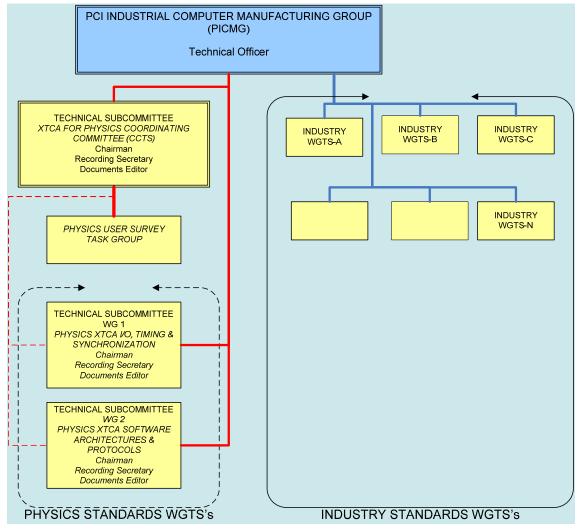
# PICMG xTCA for Physics Coordinating Committee Technical Subcommittee

- PICMG TC for Physics (CCTS)
  - Proposed at 2008 Nuclear Science Symposium,
     Dresden, in conjunction with 2-day xTCA Workshop
  - Organization of Coordinating Committee subsequently sponsored by PICMG Executive Members SLAC, DESY, IHEP and FNAL plus two Executive Member companies, Cypress Point Research & Performance Technologies
  - Approved by PICMG ExCom, organized March 10, 2009
  - CCTS acts as steering committee to spawn Working Group TSs, initiate Preliminary SOWs, review TS work products before submittal to PICMG-wide vote of approval
    - Holds weekly web meetings
    - Current membership 44 companies, 5 labs, 65 individual members





# Organization xTCA for Physics Technical Subcommittee





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#### **New Working Groups**

 Two major Working Groups approved, about to be formalized with election of officers

 WG1: Physics xTCA I/O, Timing and Synchronization Working Group

 WG2: Physics xTCA Software Architectures and Protocols Working Group





### WG1 Preliminary SOW Tasks

- Specify AMC's with Rear I/O (AMC-IO) and an associated µRTM
- Consider potential needs for Mezzanine Cards.
- Specify ATCA carrier for the AMC-IO.
- Specify ATCA RTM module to accommodate AMC-IO along with support features such as power, management, JTAG, etc.





#### WG1 SOW Tasks -2

- Specify e-keying code extensions to the Shelf Management Section to accommodate the additions to the AMC, RTM, μRTM and the μTCA shelf specifications.
- Specify lines, both bussed and radial, that are in both ATCA and μTCA backplanes that could be used for Physics clocks, gates and triggers. If necessary, specify lines that are not in the ATCA and μTCA backplanes but could be added to the RTM and/or μRTM for such use.





### WG2 Preliminary SOW Tasks

- Define protocols and APIs for management and control of real-time data acquisition and machine-control components, to include calibration, synchronization, and triggering mechanisms.
- Define protocols and APIs for high-rate and lowlatency distribution of data among the various data acquisition, machine-control, data processing, data storage, and data transmission components, including use of the backplane fabrics within shelves and use of external links between shelves.
- Define the mechanisms and techniques within the ATCA/μTCA infrastructure to manage component-, shelf-, subsystem-, experiment-, and facility-level redundancy and automated failover.





#### WG2 SOW Tasks -2

- Define protocols and APIs for management of resources within an xTCA network, including identification and allocation of common functional modules among subsystems and experiments, management of active module disposition and status, and auditing of component usage and maintenance.
- Define a common set of APIs and functional blocks at the software and FPGA firmware levels to be provided as a standard development library for xTCA application development, including standard operating system and thread management functions, module identification and data routing functions, standard I/O management functions, and standard data processing blocks.





#### **Future Plans**

- Conduct survey of requirements among labs actively engaged or planning on using xTCA
  - Find contact person in labs to help distribute survey
  - Small CCTS team correlates results, distributes report
  - Survey team led by Stefan Simrock, DESY,
     CCTS Assistant Chair





#### **Future Plans 2**

- Establish public web page for Physics on PICMG site
  - Background, goals of group
  - Reports, papers of current interest
  - xTCA Workshop presentations (FNAL '07, Dresden '08, IHEP '09, ...)
  - Current organization, information contacts, how to join CCTS and/or WG's
- Operational before end 05/09





#### **Future Plans 3**

- Review WG Work Products
  - Some WG tasks urgent, driven by project needs at DESY, SLAC, etc.
  - Aiming for initial design, MTCA with µRTM by end 09 with prototype efforts underway
  - Down-select preferred first draft protocols on same timeframe.
- Further Information
  - www.picmg.com ("coming soon")





### **Acknowledgments**

- The ongoing work described is a collaboration of several labs and industry partners.
- Thanks to the PICMG organization, members and officers for encouragement and generous help, and to the key people at the founding labs.
- Special thanks to PICMG Physics Committee officers Augustus Lowell and Zhen-An Liu; to Assistant Officers Stefan Simrock and Robert Downing; to Kay Rehlich and Stefan Simrock and their teams for generous sharing of xTCA R&D for the new XFEL accelerator control systems; and again to Robert Downing for leading the Profile for Physics concepts development and documentation and many fruitful discussions.



