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Compact SiPM based Detector Module for Time-of-Flight PET/MR

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Project Overview

- Project funded by the European Union in FP7.
- Develop a compact PET detector module for use in a simultaneous ToF PET/MR detector, scalable to a whole-body scanner.
- Develop novel reconstruction algorithms to make good use of the available information (MR based attenuation and motion correction).

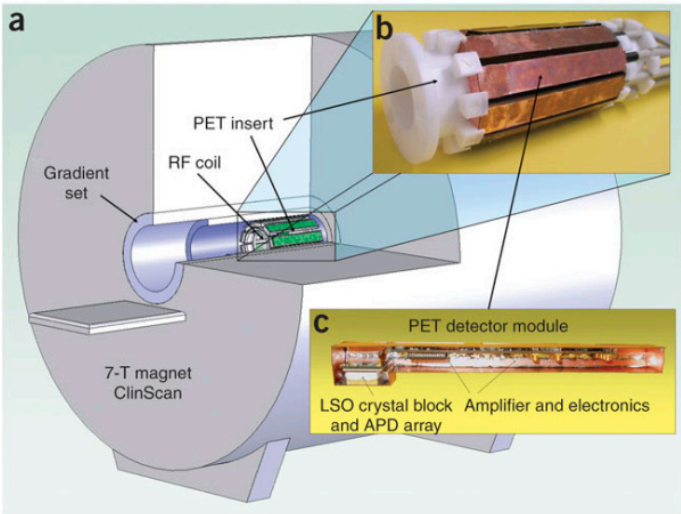
Requirements for the PET Detector

- MR compatible design, i.e. no magnetic components, especially no PMTs, inside the magnet, no wire loops.
- Fit inside the little available space inside the MR scanner.
  1. Develop a compact detector module.
  2. Require few wire and other connections through the MR scanner.
- No relevant performance degredation by MR gradients and HF signals from MR operation.
- Sub-nanosecond timing for ToF PET.
- Several thousand channels even in a “small” animal scanner.
- Rugged design to withstand the vibrations inside an MR scanner.

State of the Art in Simultaneous PET/MR

- Use a light guide to guide the scintillation light to PMT detectors outside the magnet.
  Drawback: Lots of optical fibres, bad light yield.
- APD detectors with first amplification stage inside the field, all other processing outside the B field.
  Drawback: Lots of connections required, potential of large noise pickup on long wires.

→ Not scalable.



M. Judenhofer et al., "Simultaneous PET-MRI: a new approach for functional and morphological imaging," *Nature Medicine* **14**, 459 - 465 (2008)

Our Approach

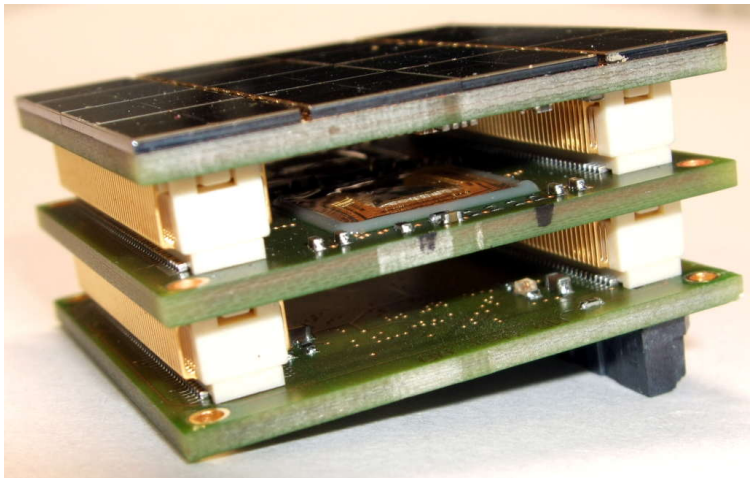
Put everything inside the tube:

- Light detection
- Amplification
- Digitization
- Timestamping
- Serialization

→ Only few data connections for a large number of channels.

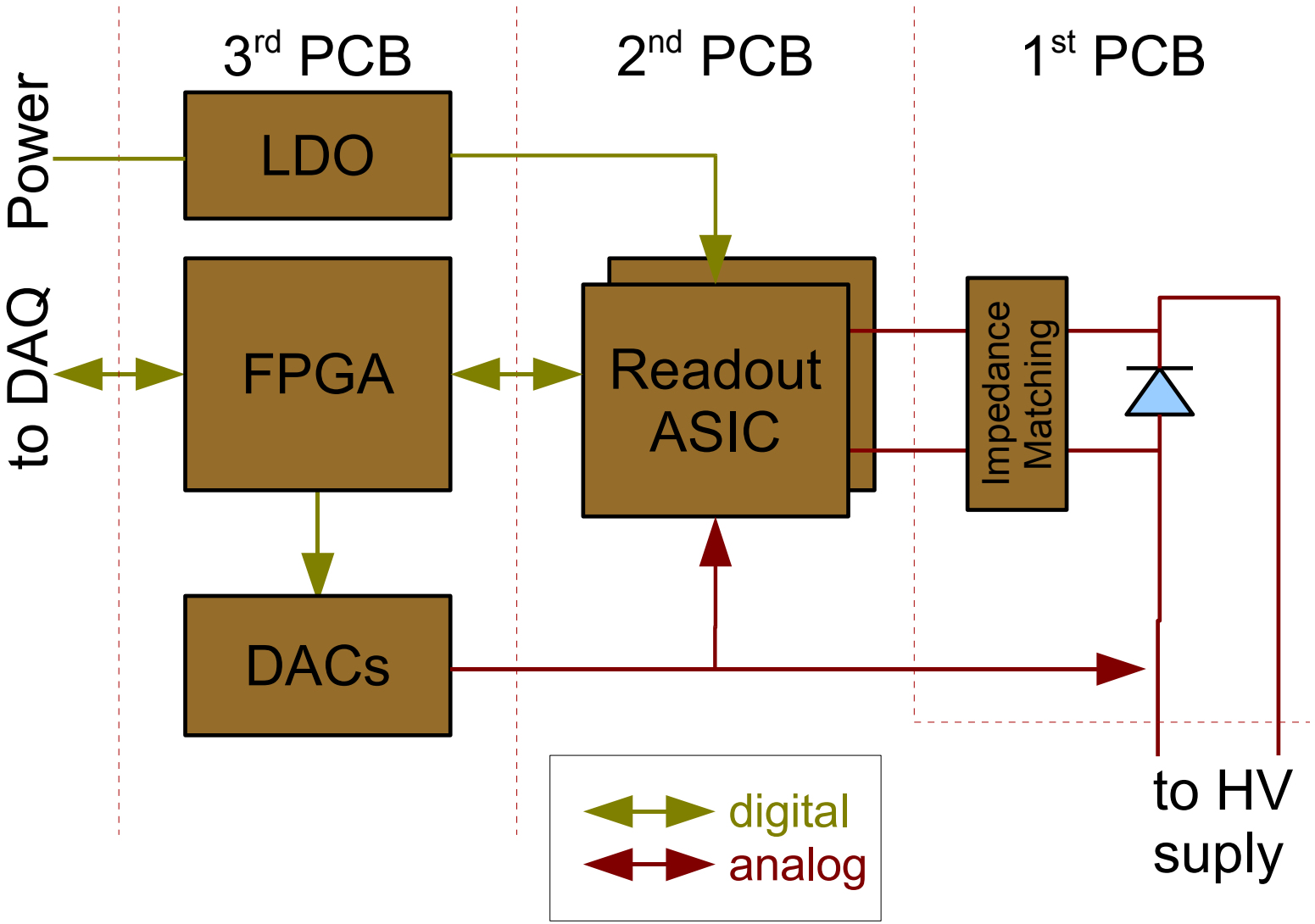
Methods

- Highly integrated electronics.
- Very compact module design.
- Large area SiPM detectors.
- Aggressive mechanics and cooling.
- Differential architecture for EMI robustness.
- Modular concept with defined interfaces on the connectors.



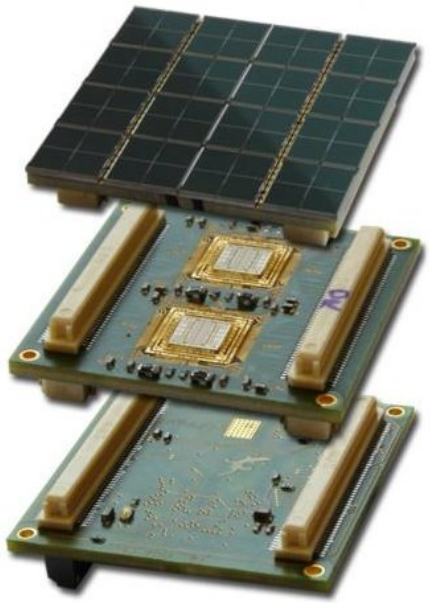
Actual size: 33×33 mm².

Block Diagram



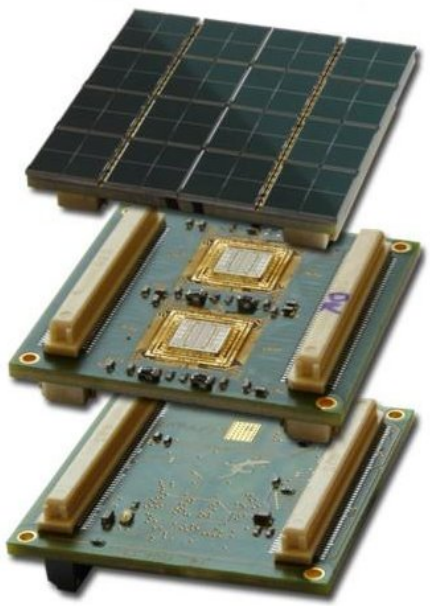
Top PCB: Detectors

- 64 channels.
- 4×4 mm² SiPMs.
- 4×4 monolithic arrays of 2×2 silicon photomultipliers.
  - → Entire surface covered by SiPMs
  - → High packing fraction.
- Passive components required to interface to the ASICs located on the bottom side of the PCB.



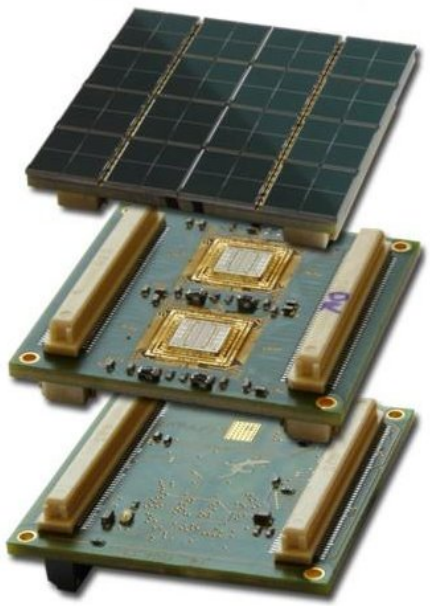
Middle PCB: Hit Digitizing

- Two readout ASICs, each handling 32 SiPM channels.
  - Self-triggering by leading-edge discriminator.
  - 100 ps FWHM coincidence timing resolution.
  - 20 bit timestamps.
  - 9 bit ADC for energy readout.
- Digitization of absolute arrival time and signal energy.
- All-digitial, differential output to the FPGA.



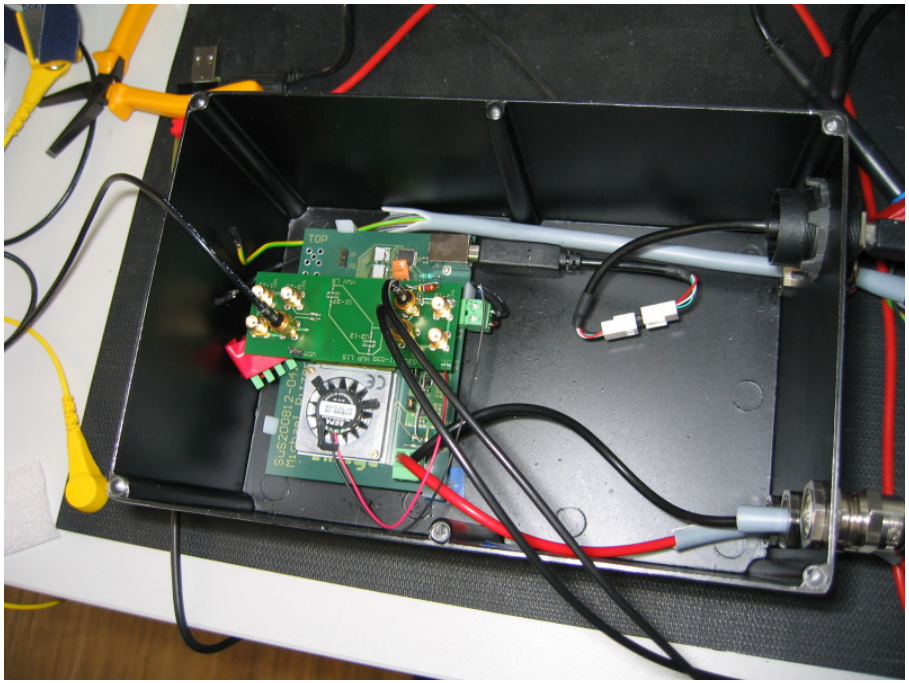
Bottom PCB: Control, Processing

- Xilinx Spartan FPGA for
  - Control of the ASICs.
  - Hit data preprocessing.
  - Interfacing between the ASICs and the system.
- DACs to generate bias voltages for the ASICs and SiPM devices.
- Interface to DAQ: Several LVDS connections.
- Local analog power regulation.



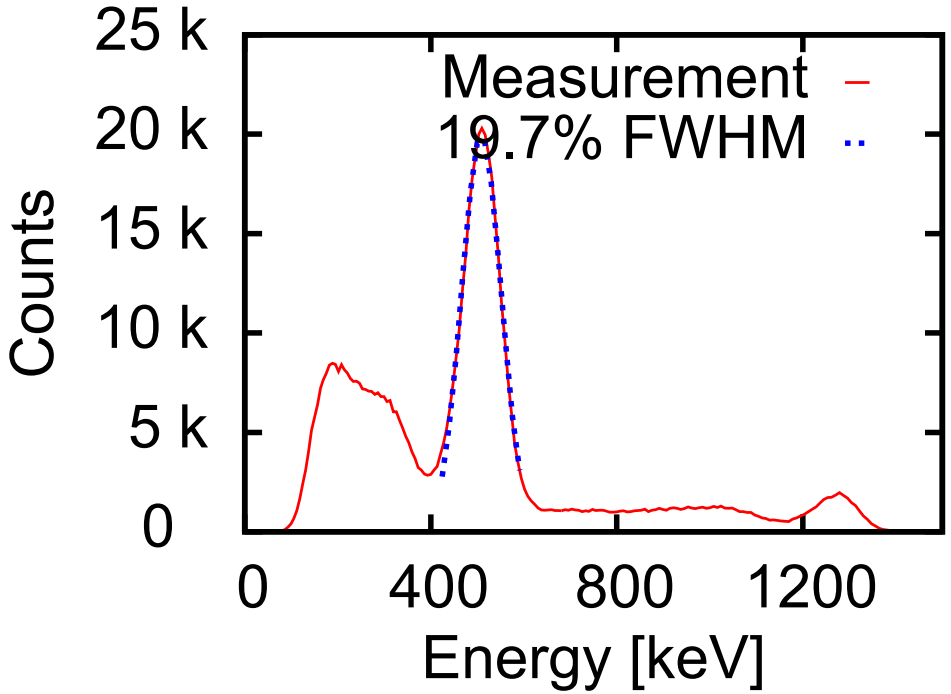
Test Setup

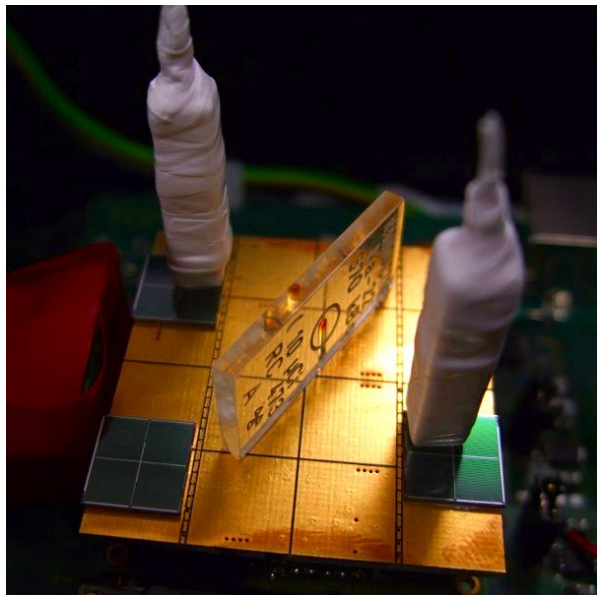
- Testboard containing a single PCB stack and interface to USB.
- Light-tight box for measurements with SiPMs.



- Detector board replaced with dummy board connecting pulse inputs to SMA connectors for ASIC characterization.
- Linux-based data acquisition and data analysis.

Results – Setup Verification

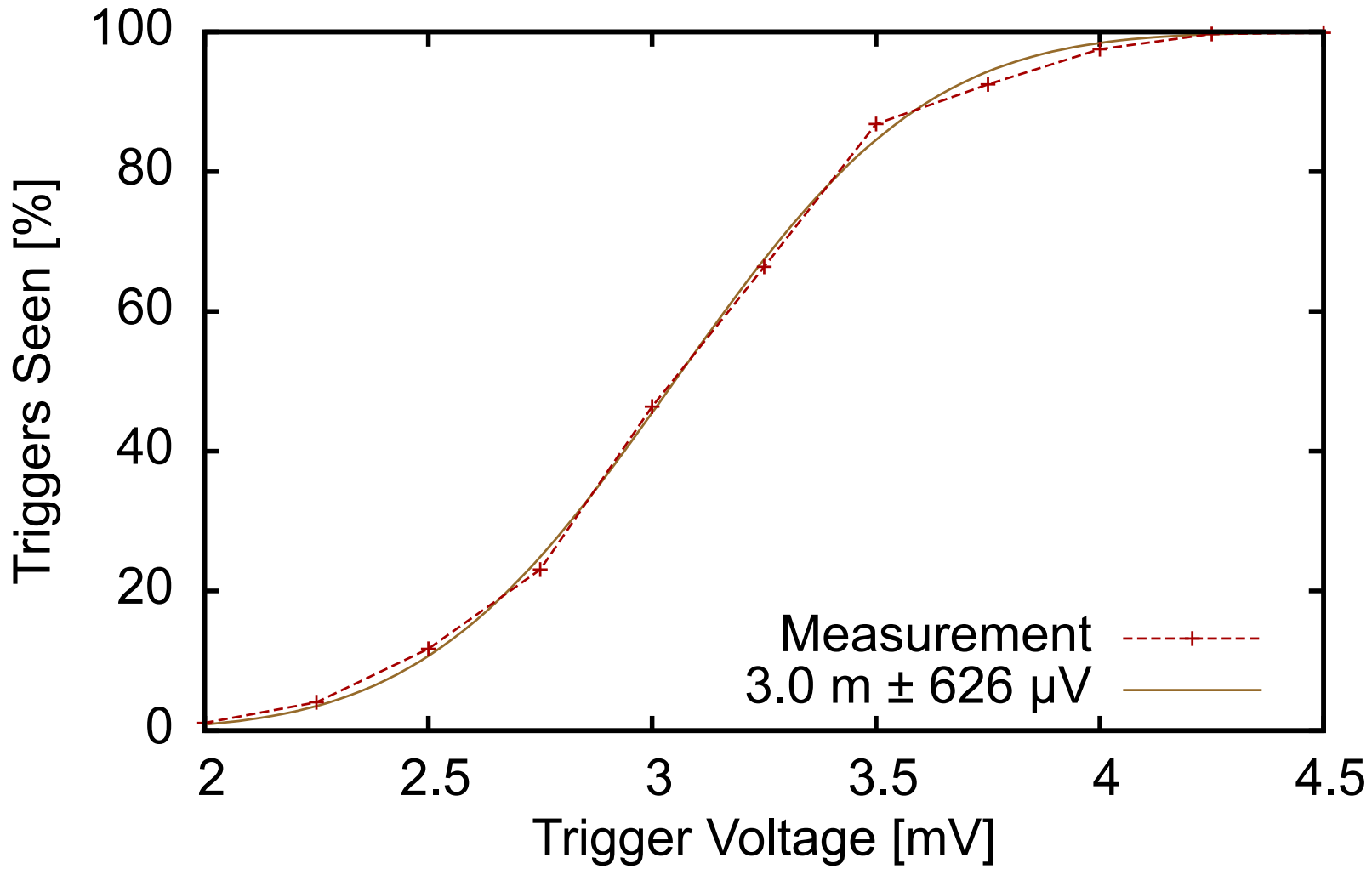




^{22}Na spectrum measured with a single LYSO crystal standing on one SiPM. Bad optical coupling! → Bad resolution.

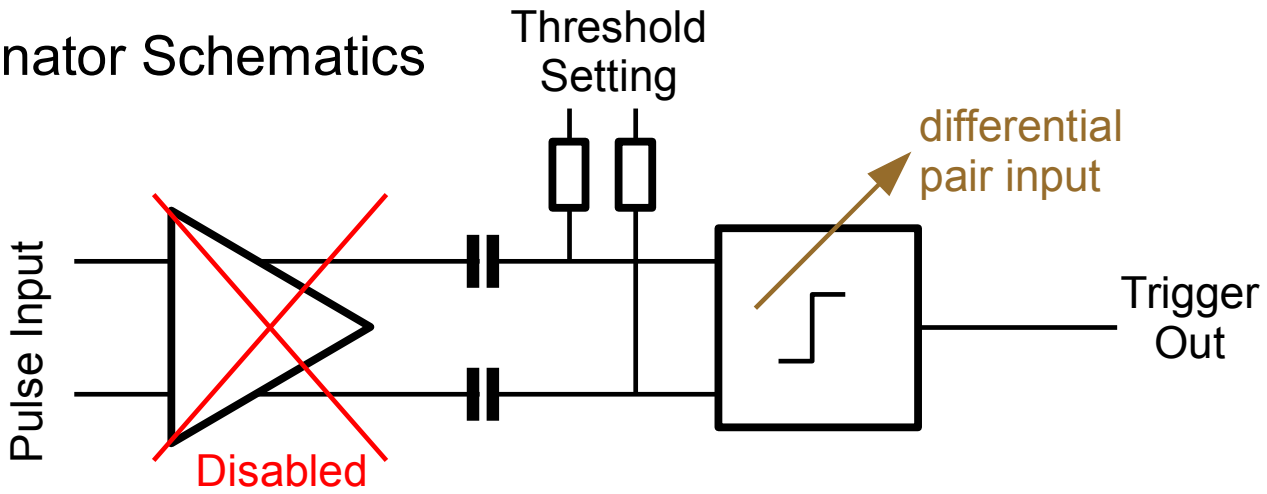
But: Proves that the entire stack works as expected!

Results – Discriminator Threshold

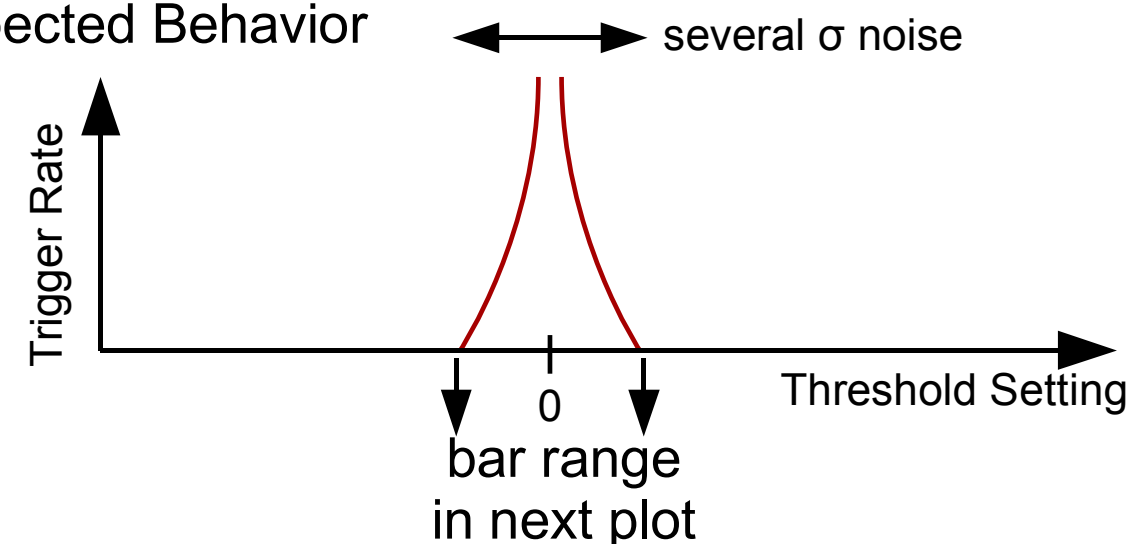


Results – Threshold Dispersion I

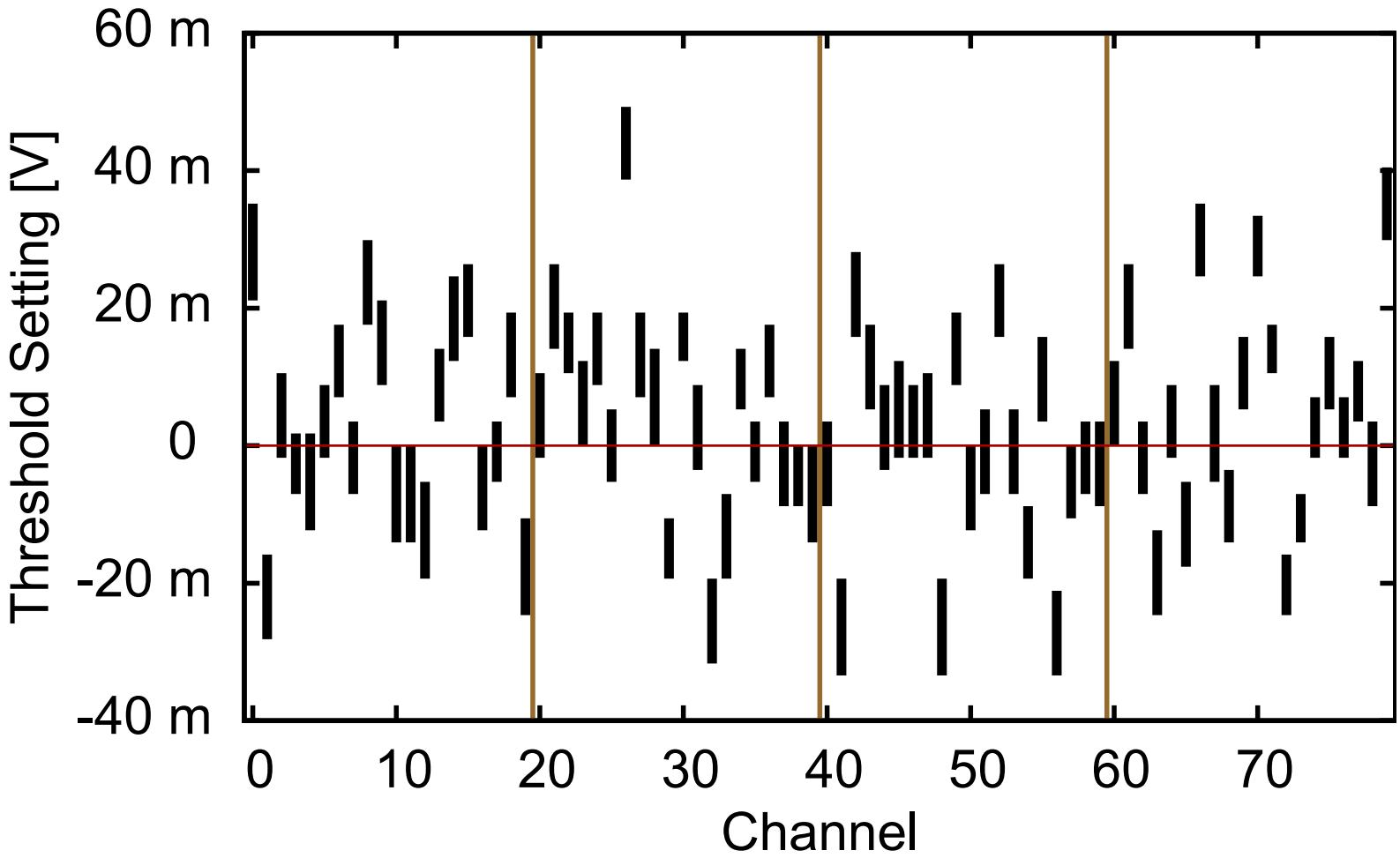
Discriminator Schematics



Expected Behavior



Results – Threshold Dispersion II

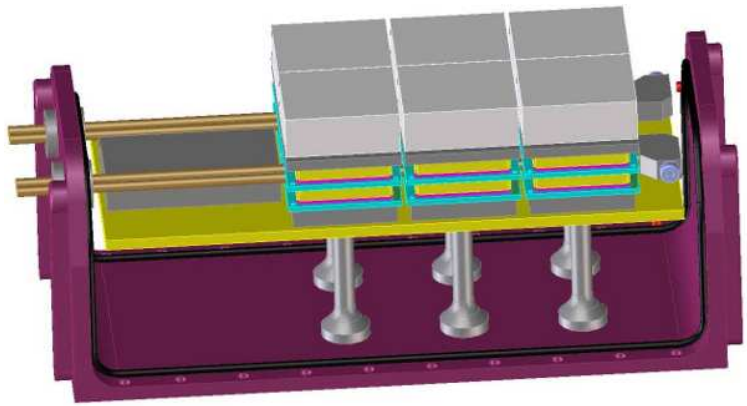


Results – Threshold Dispersion III

- Bar offset: Switching offset of a differential pair of NMOS transistors in close proximity.
- Effects: Large threshold dispersion between channels, limit on lowest possible threshold.
- Compensation circuit implemented in next generation ASIC.

Future System Integration

- Motherboard PCB with six (3×2) stacks with minimal spacing.
- Large FPGA to process the data and send it off via Gigabit Ethernet.
- Box to firmly hold the components and provide the infrastructure for cooling.



Outlook

- Improved ASIC
  - Decreased discriminator threshold dispersion.
  - Lower power consumption.
  - Should be back from fabrication just today.
- Operation with full crystal array.
- Measure performance in MR.

Acknowledgements

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