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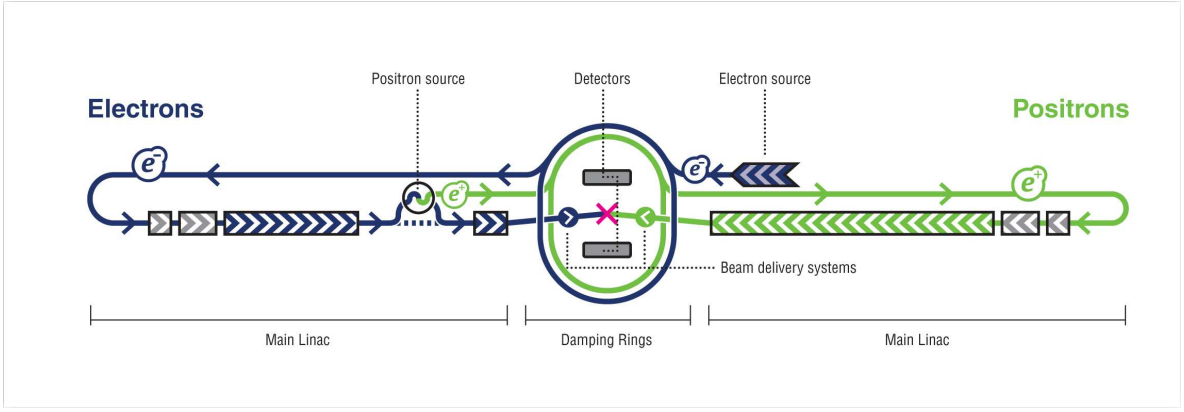
On behalf of the LC-TPC Collaboration

The Linear Collider Large Prototype Time Projection Chamber DAQ

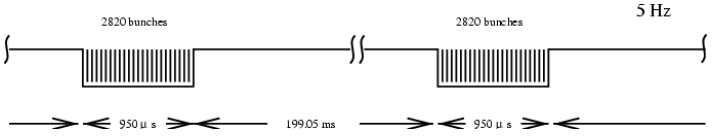
IEEE NPSS Real Time Conference, May 10-15, 2009, Beijing

e^+e^- Linear Collider Projects

The International Linear Collider: 0.5-1 TeV



Bunch train structure:



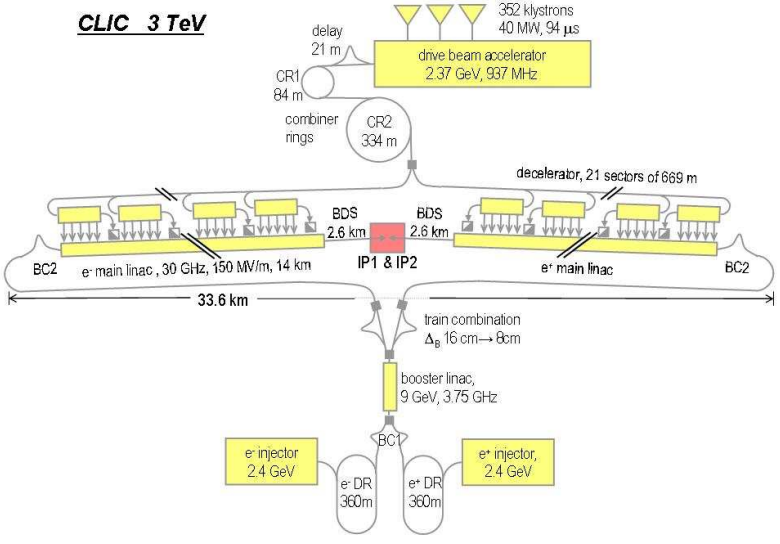
199 ms between trains to r/o:

⇒ Trigger free DAQ (if enough buffers)

⇒ Power cycling option for frontend to reduce needed cooling

⇒ Expect EDR phase ends by 2012, construction starts by >2015

The Compact Linear Collider: 3 TeV

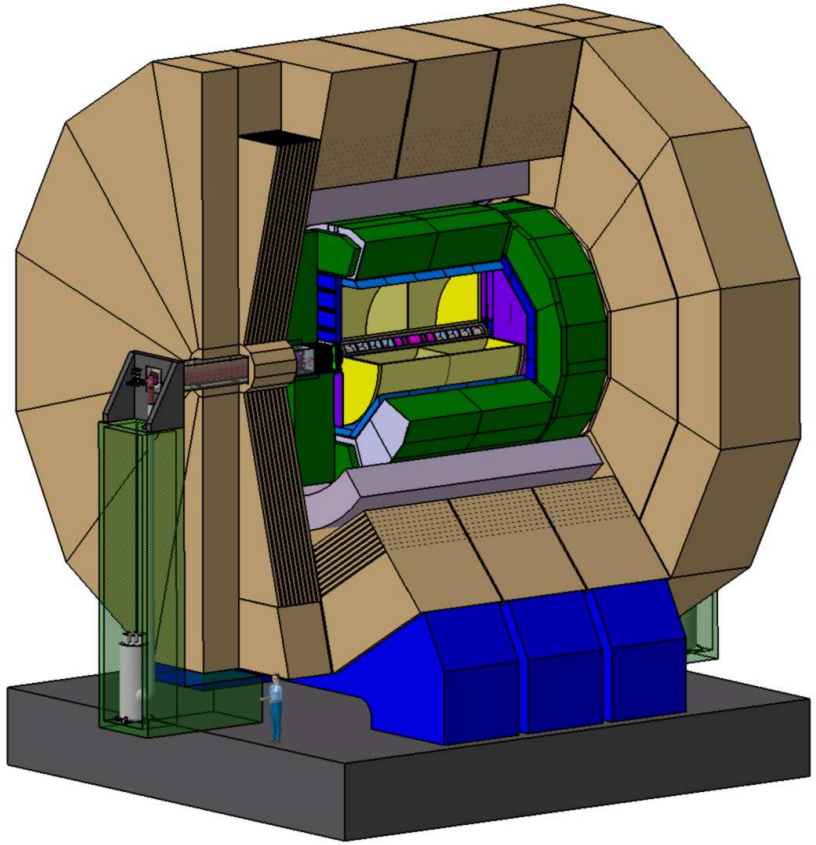


- Higher energy / compact design
- Technology not available before 2015

  ⇒ ILC remains base option

The ILD detector proposal

ILD= merging of LDC and GLD concepts for LOI (March 09)



Vertex detector:

Si detectors: precise vtx

central tracker detector:

Large TPC: $\sigma(1/P_t) < 5.10^{-5}\mathrm{Gev}^{-1}$
$\mathrm{dE/dx}$ measurements

Si Enveloppe: precise calo impact

Fine segmentation calo:

$$\sigma_{E_{\mathrm{em}}}/E_{\mathrm{em}} \simeq 15\%/\sqrt{E(\mathrm{GeV})} \oplus 1\%$$

$$\sigma_{E_{\mathrm{jet}}}/E_{\mathrm{jet}} \simeq 30\%/\sqrt{E(\mathrm{GeV})}$$

$\rightarrow$ Particle Flow Algorithm concept

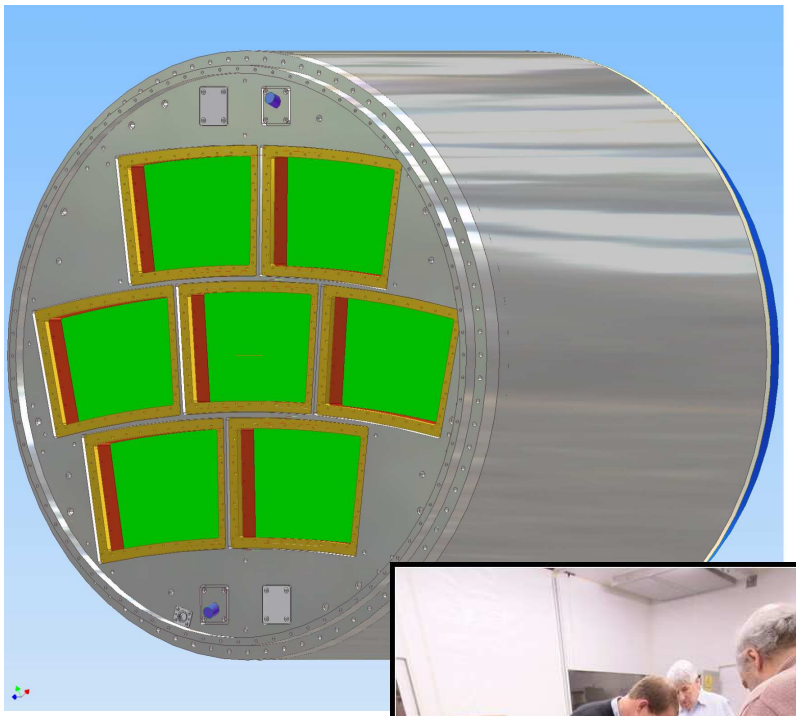
$\simeq$ Tracking inside calorimeters

$\Rightarrow$ Several collaborations studying technologies transversly to LOI's:
VtxDet and SiDet, TPC: LC-TPC, Calorimeters: CALICE, ...

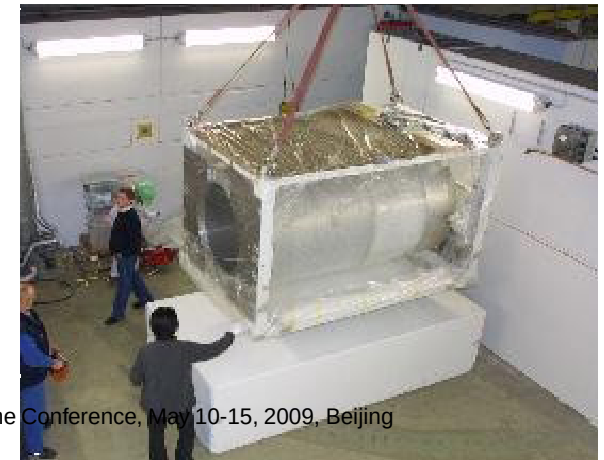
TPC Large prototype test beams at DESY

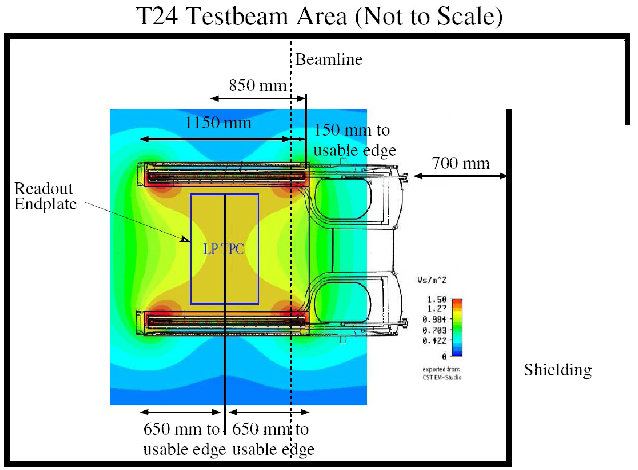
DESY test beams

- 1-6 GeV electron beam
- TPC: d=70 cm / L=1m
- Test several tecnologies:
  - Gaseous detectors:
    Micromegas, GEM
    - ⊗ ADC or TDC r/o
  - Si detectors
- Started End Nov. 2008



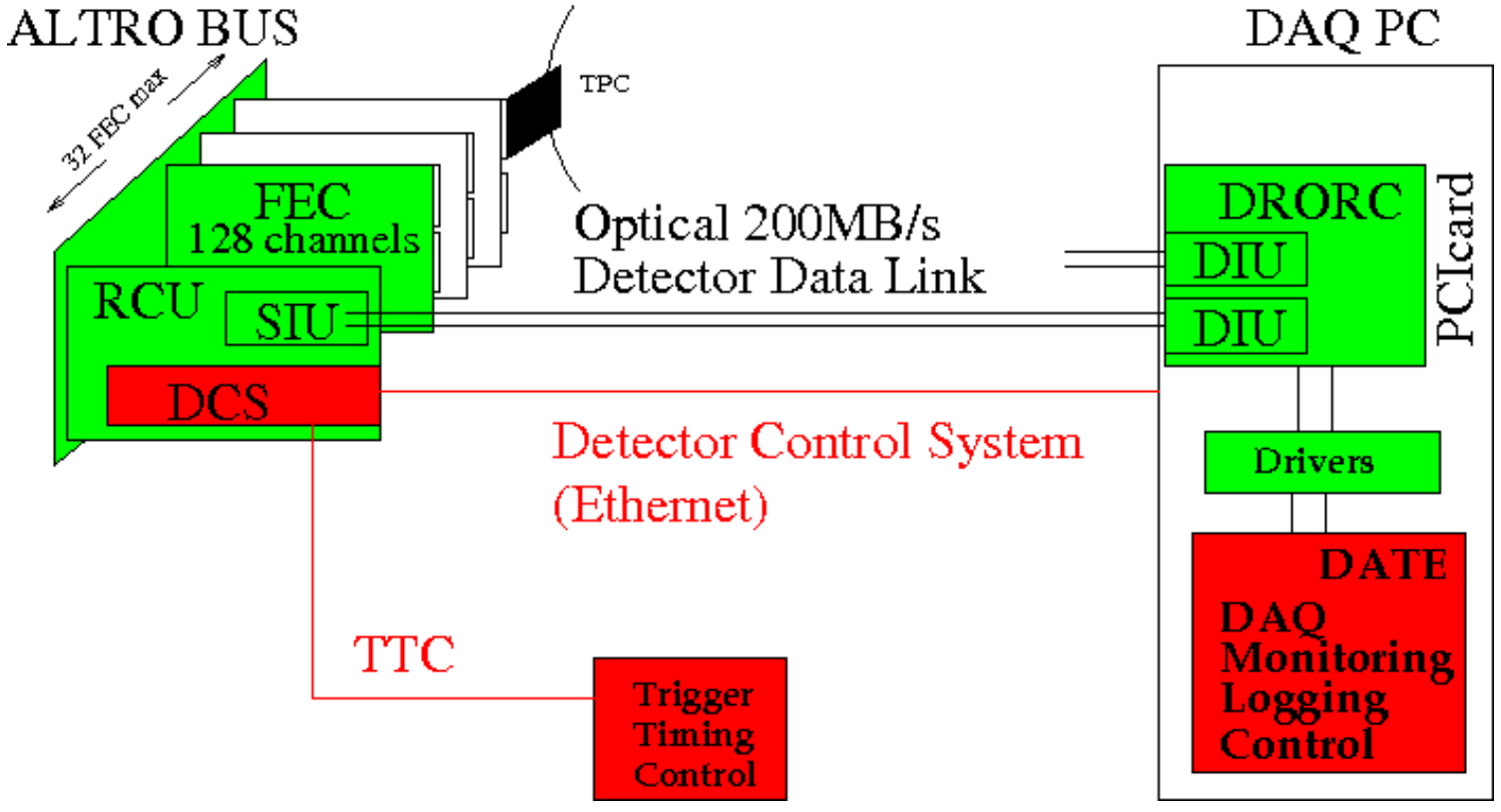
1 tesla KEK PCMAG magnet:





ALTRO r/o: ALICE TPC r/o overview

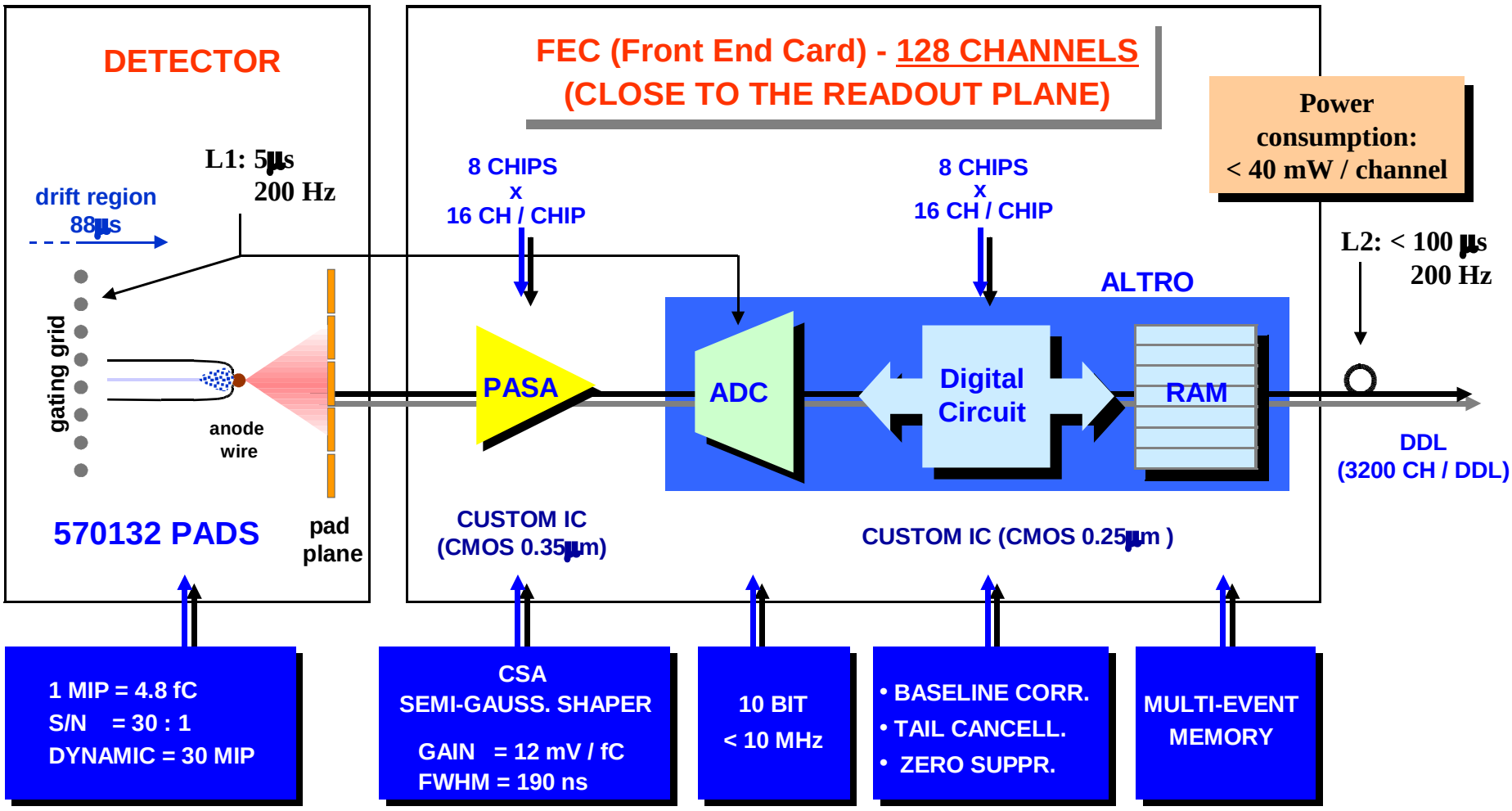
Original ALICE design:



Will not be used for LC-TPC:

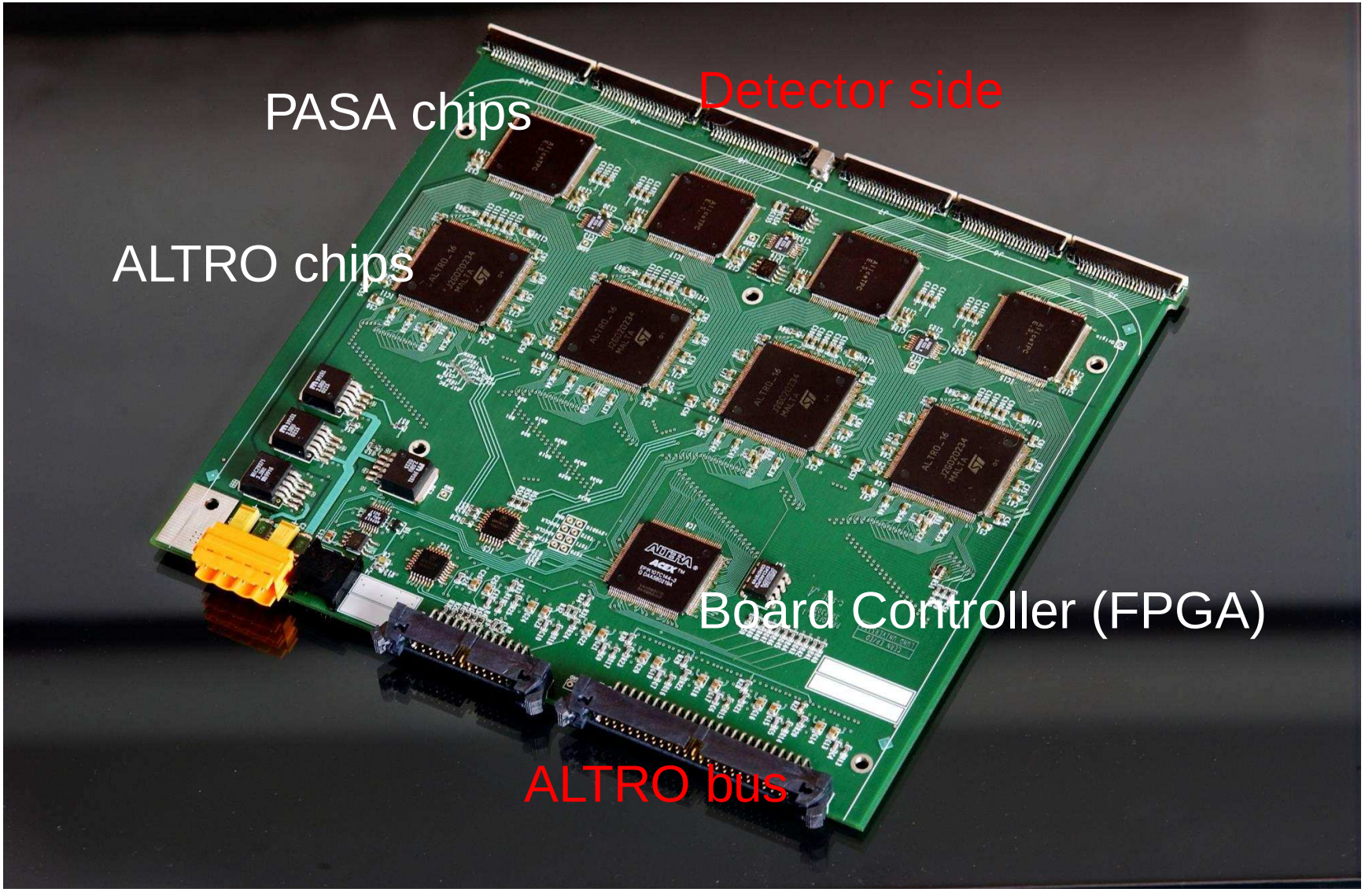
- TTC: LHC specific trigger electronics
- DATE r/o software (beyond drivers level)
- DCS

ALTRO r/o: ALICE Front End Card (1)



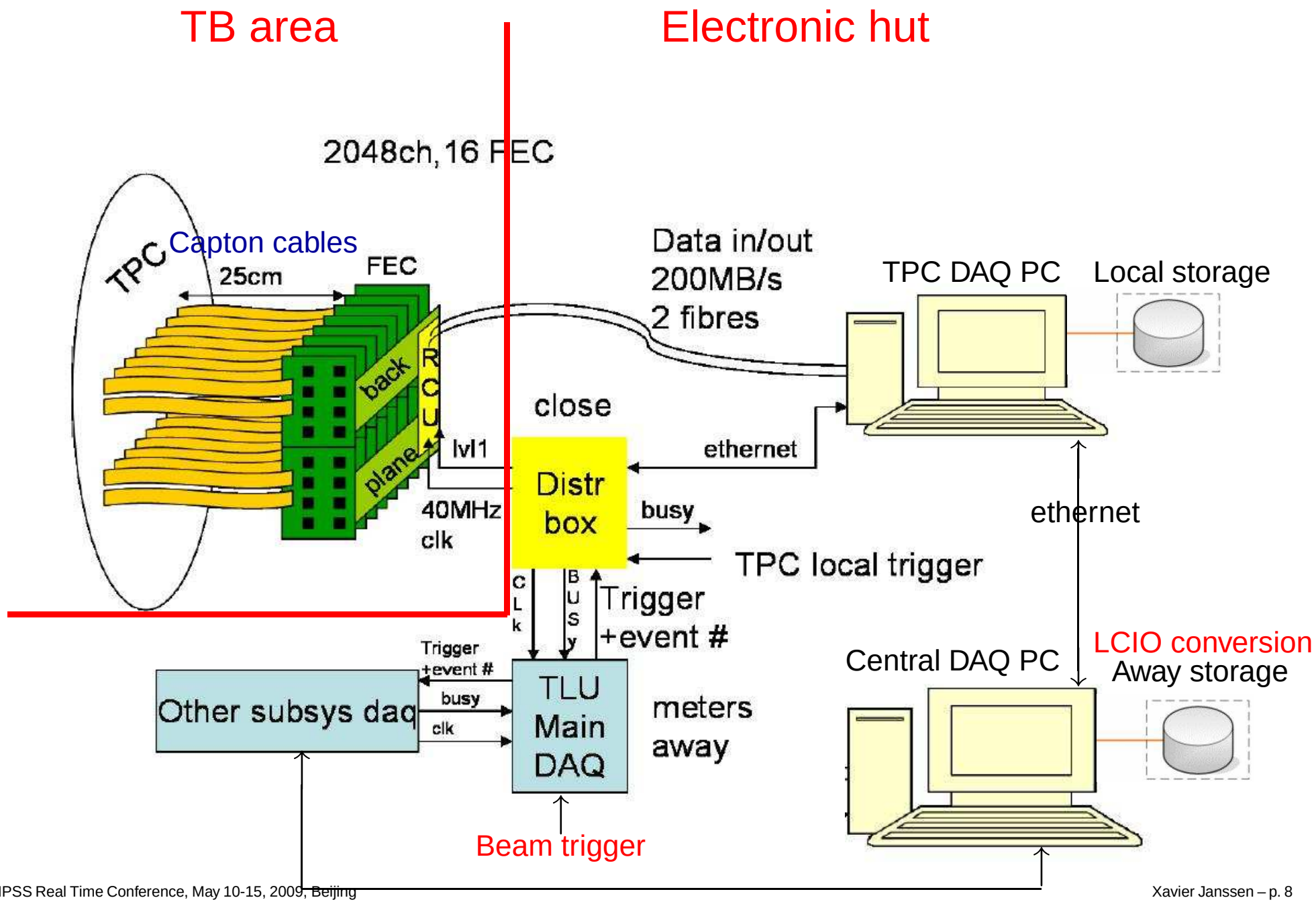
ALTRO r/o: ALICE Front End Card (2)

128 channels ALICE FEC:



+ 4 PASA chips on rear side

ALTRO r/o: LC-TPC DAQ overview



ALTRO r/o: New Amplifiers

16 channels Programmable Charge Amplifier - PCA16 (CERN)

- 1.5 V Supply, power consumption < 8 mW / channel
- programmable features:

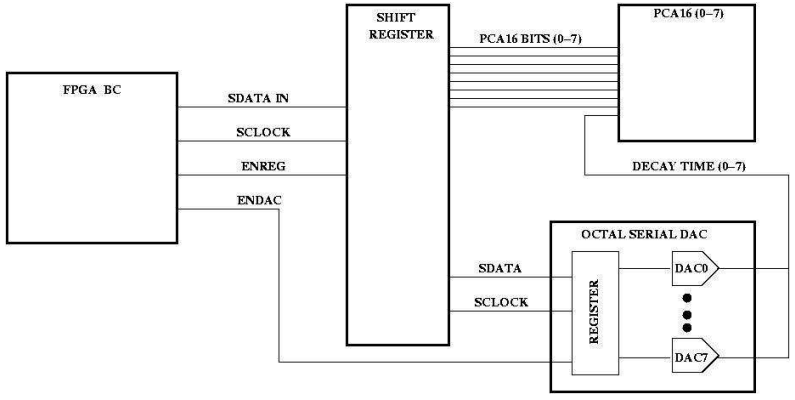
- Signal polarity
- Peaking time (30 ns - 120 ns)
- Decay time (continously programmable)
- Power down (wake-up = 1 ms)
- Gain in 4 steps (12 -27 mV/fC)

→ Final version was delivered at end of 2007

→ 1000 purchased for EUDET test beams

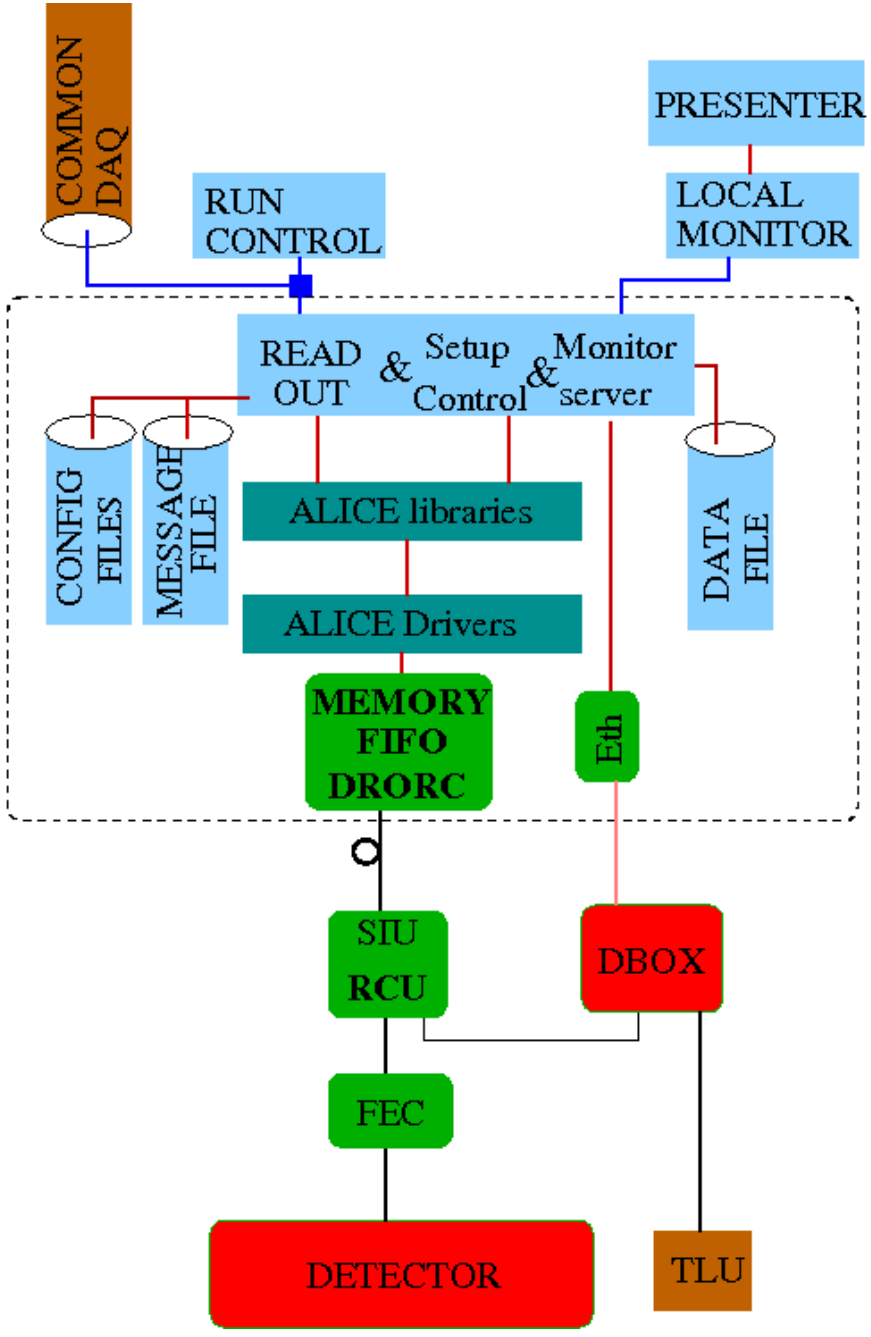
PCA16 control:

- FEC modified to add a DAC and a shift register (Lund)
- Reprogram FEC's FPGA to control them (Brussels)



→ Tested sucessfully with 1st prototype of modified FEC

ALTRO r/o: DAQ Software



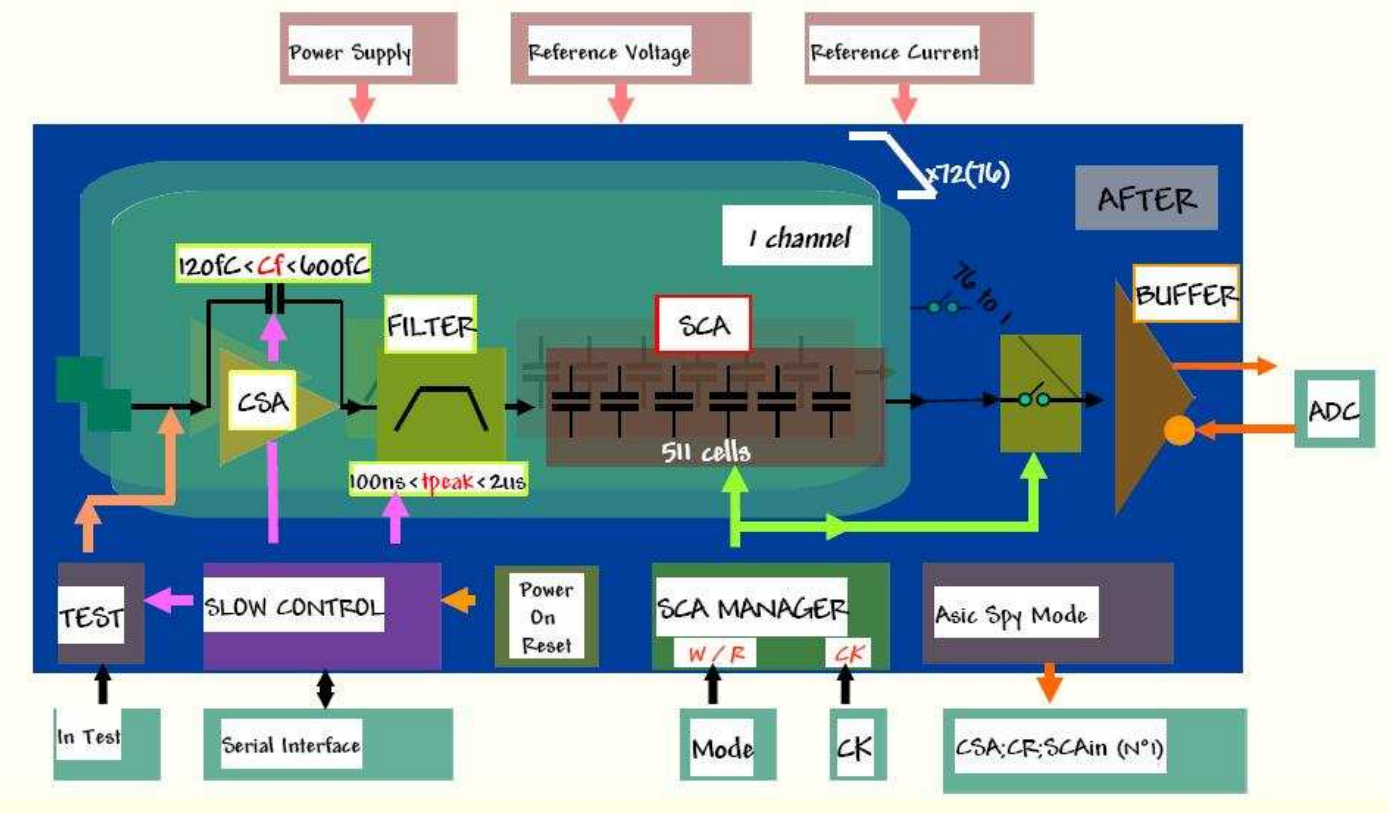
Local Readout Software (Lund)

- Use ALICE drivers and librairies
- Direct memory access for RCU
- Configuration: ASCII files
- Local data: binary files
- TCP/IP server for data transfer
- TCP/IP server for run control
- Local monitor (TCP/IP): Histos
- Message files: ASCII files
- DBOX interface: TCP/IP client

Common DAQ (Bonn)

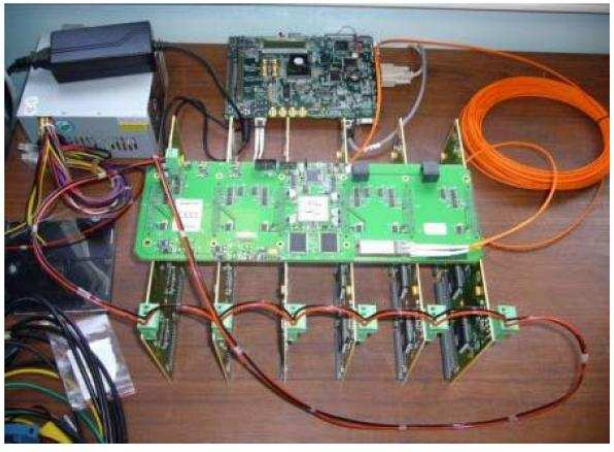
- TCP/IP connection to local DAQ
- Should ensure LCIO conversion

AFTER r/o: T2K TPC Electronic (CEA-Saclay)



AFTER ASICS:

- 72 Analog channels
- 2 input polarities
- 4 gains: 120, 240, 360 and 600 fC
- 16 peaking times: from 100 ns to 2 ps
- 511 analog memory cells / channel

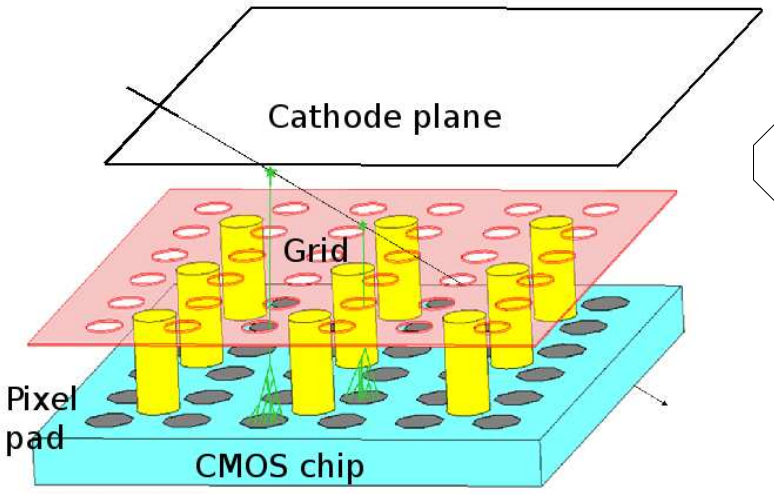


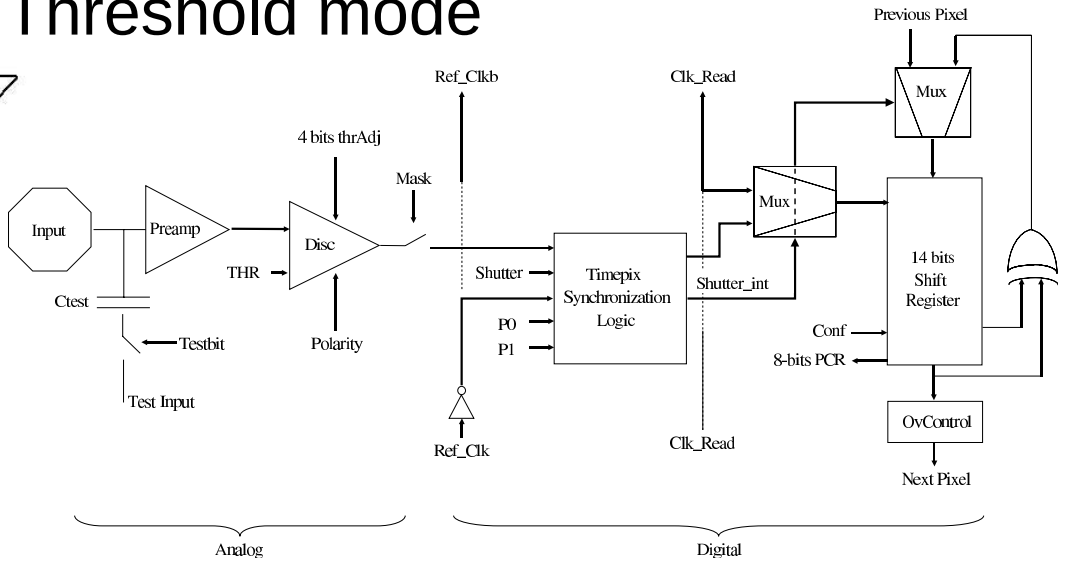
- Analog pipe-line + offline ADC/zero-suppress
- 1 crate for LCTPC TB (1738 channels)

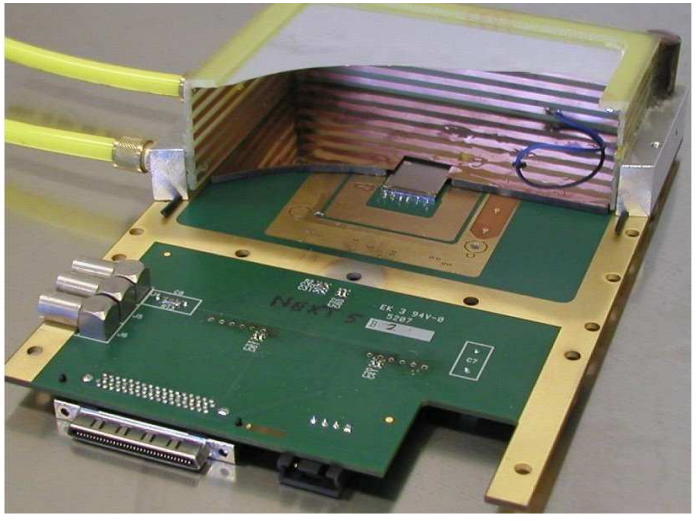
→ Used sucessfully for Micromegas panel in DESY test beam in november 08

Silicium TPC: Timepix chip (NIKHEF/Bonn/CEA)

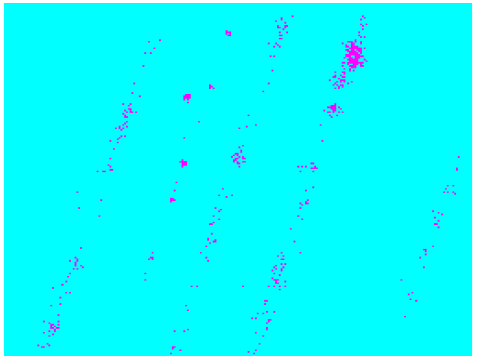
Timepix Chip: Evolution of the Medipix operating in Time of Arrival or Time over Threshold mode







- Sucessful tests with 1 chip (test beam)
- Next: Boards with 4 Timepix mounted



Future:

Developp chip with self triggering to limit power (needed cooling)

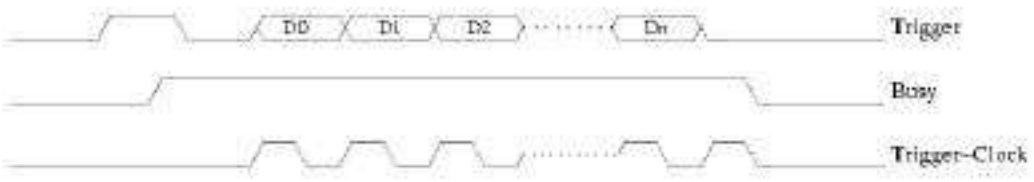
EUDET Trigger Logic Unit

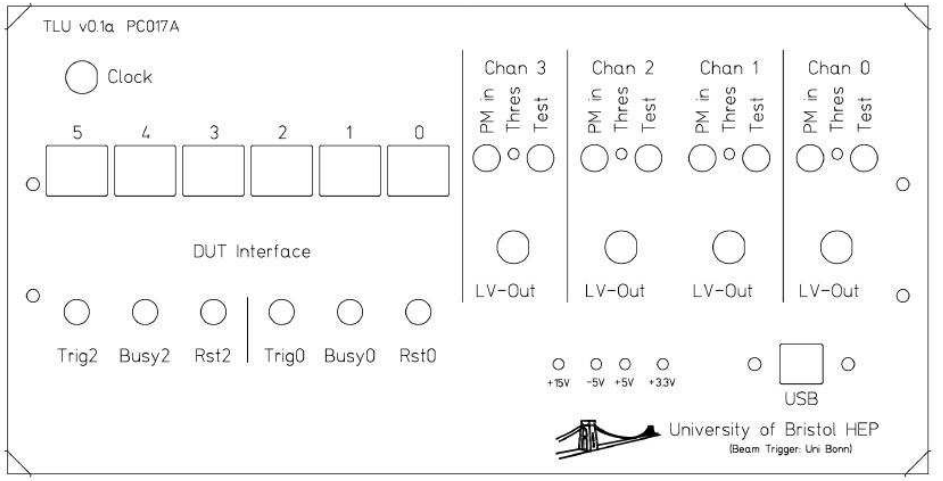
TLU inputs:

- 4 comparators with level between $\pm$800 mV (LEMO connectots)
  - $\rightarrow$ Cosmic trigger will send NIM signal to TLU
  - $\rightarrow$ beam trigger
- BUSY signal from TPC (+ other detectors: Si) in LVDS format
  - $\rightarrow$ None of r/o electronic provide such a signal

TLU outputs:

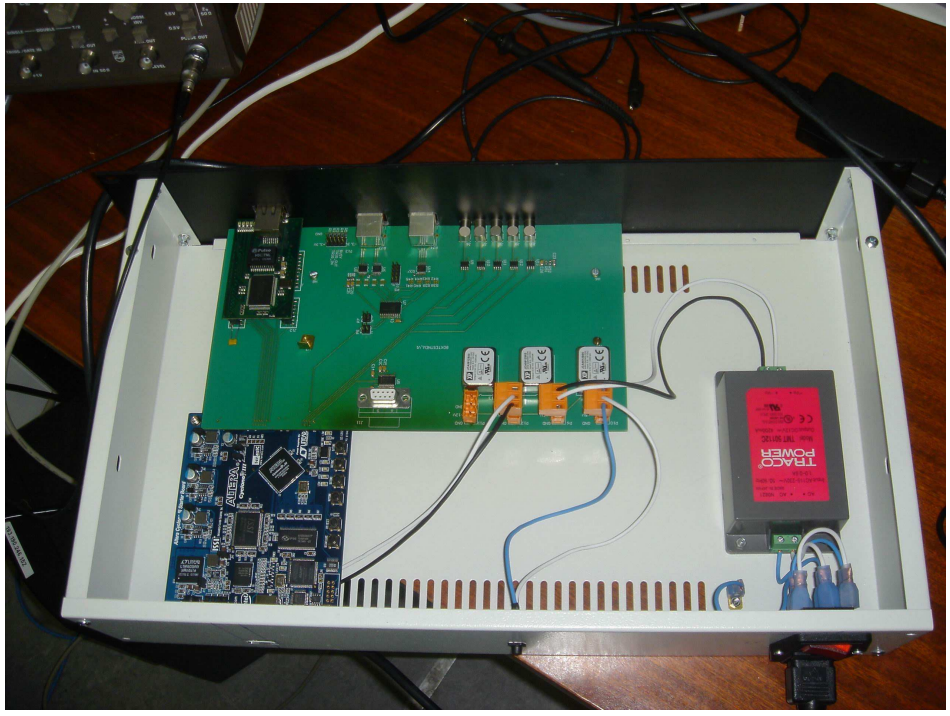
- Reset (LVDS)
- Trigger signal (LVDS)
- Event number (LVDS) pulled out by a data clock (LVDS)





Distributor Box *(Brussels)*

- ALTRO/AFTER needs a 3.3 V Trigger signal and a clock (ALTRO)
- ALTRO/AFTER do not provide BUSY $\longrightarrow$ Fixed timeout or ethernet
- Synchronisation (timestamp/event#) via special trigger count



Use commercial ALTERA Cyclone 3 board + few custom electronic board for LVDS (TLU) interface

Distributor box:

- Translate trigger level
- Get event# from TLU
- Tag event with time

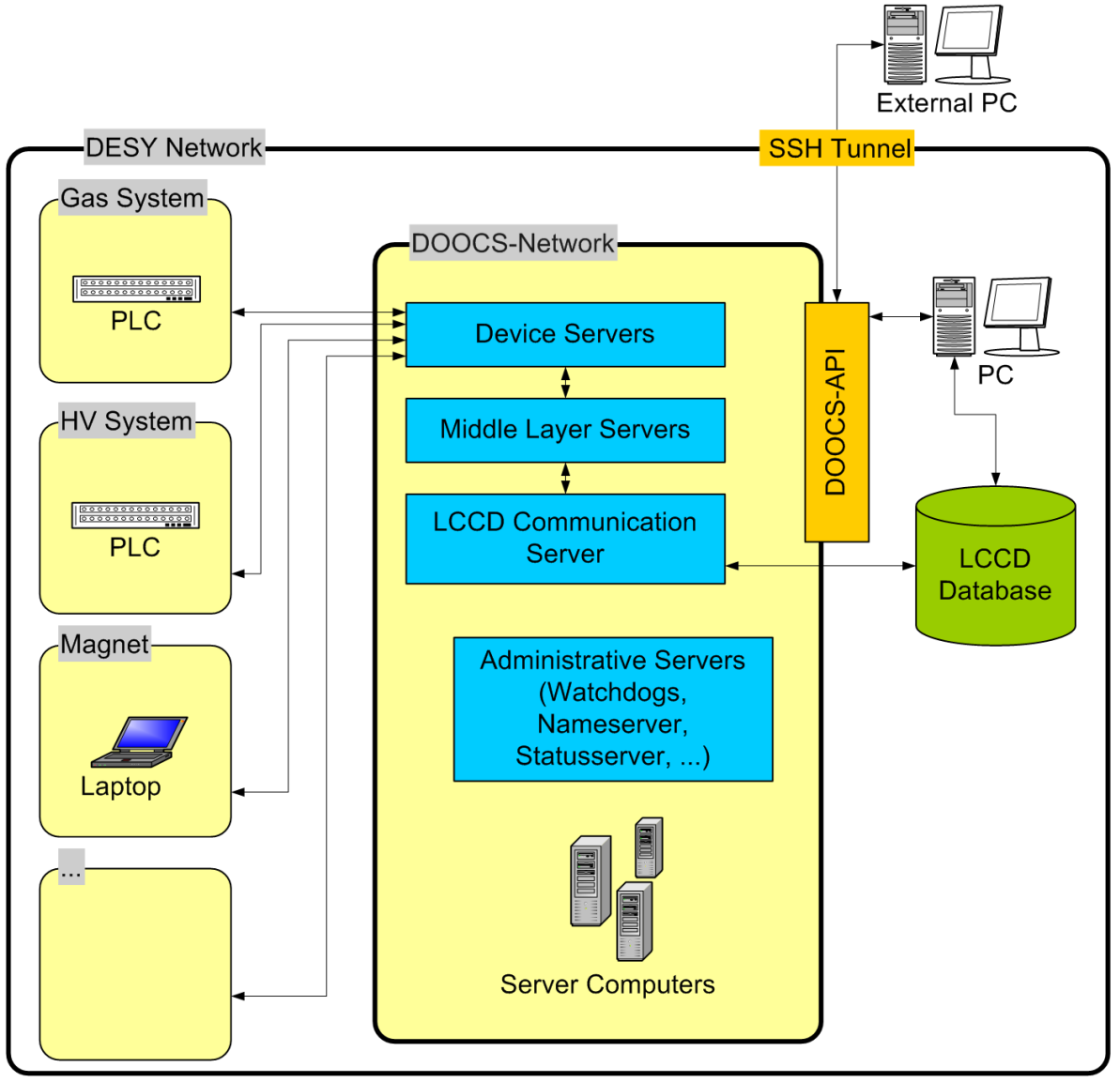
$\longrightarrow$ Send event # + time to DAQ computer (eth)

- Assert BUSY for a fixed time: waiting for DAQ pc end of r/o
- provide soft trig / reset
- provide common clock

LPTPC Slow Control General Layout *(DESY)*

- Based on Distributed Object Oriented Control System (dev. by DESY)
- Hardware communication by C++ server programs
- Internal communication via DOOCS address system
- API for access to this address system
- DOOCS provides broad set of tools for control tasks

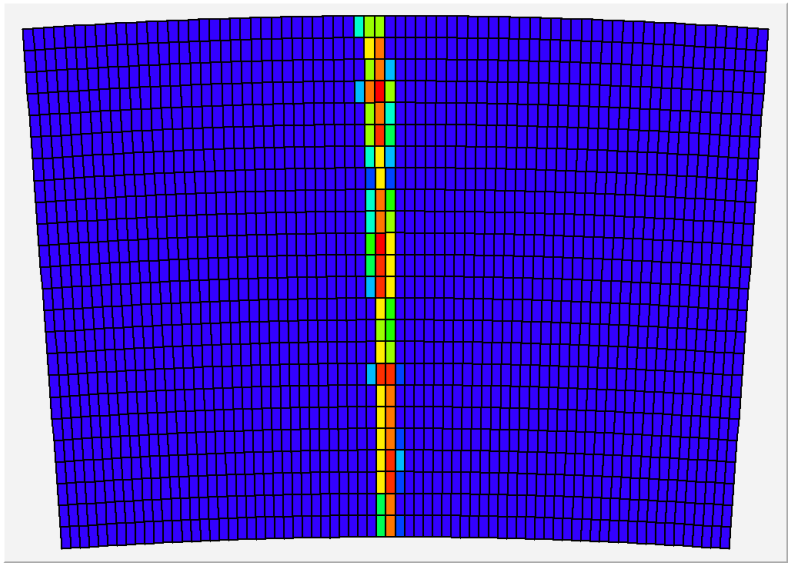
⇒ http://doocs.desy.de



TPC Test Beams: Status and plans

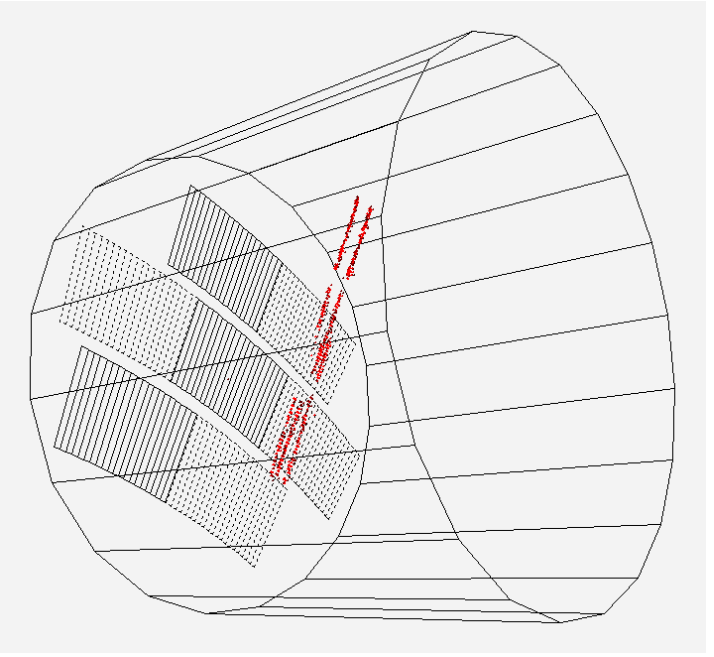
November 2008:

1 MicroMegas module with resistive anode



March 2009:

3 GEM modules



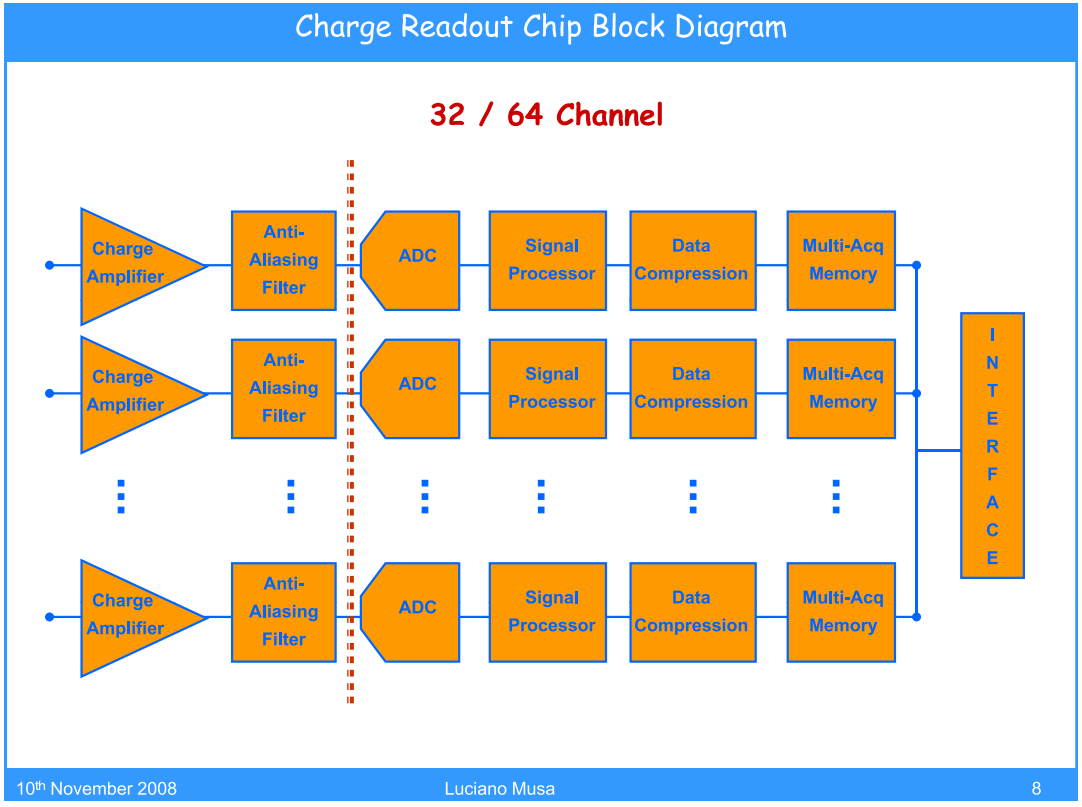
Future test beam plans:

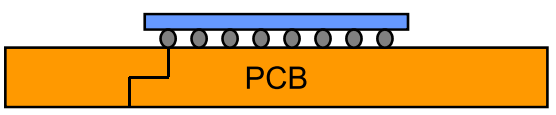
- Ongoing: test of TDC r/o electronic
- May 09: MicroMegas with new resistive anode
- June 09: Si TPC module
- July 09: GEM modules with ADC and TDC electronics

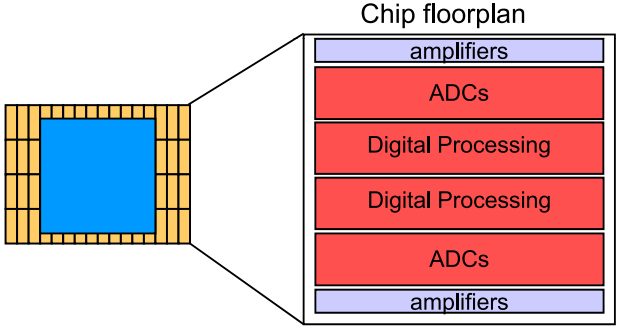
Future developments: Advanced End-plate

In ILD, limited space for TPC electronics (10 cm at each endplate)

- ⇒ Flip-mount r/o ASIC on the back of the detector PCB
- ⇒ Need to redesign front-end r/o and DAQ interface
- ⇒ 10 million channels: pad size 3-6 mm^2
- ⇒ CERN is developping an ASIC integrating the Ampli and the ADC







Power consumption:
167 W/m^2 for 3 mm^2 pads and
1% duty cycle (ILC bunch train)
⇒ Work needed on cooling

Advanced End-plate: Open DAQ issues

Other Front-end functionlities should fit close to (/on ?) the Endplate:

- Power cycling:
  - power regulators, large capacities, ...
  - synchronisation with bunch train
- Data transfert:
  - Data collector to replace RCU to be designed (Large FPGA ?)
  - Data link should intergrate redundancy (several paths)
- Other functionlities: clock distribution, slow control, ...

Local DAQ infrastructure:

- Replace actual data receiver (D-RORC) and PC farm
- Investigate xTCA technologies
- Insure modularity to integrate other front-ends candidates: TDC electronic, Si-TPC (Timepix, Medipix), ...
- Integration to future CDAQ of ILD: need common interface

SUMMARY

ALTRO r/o electronic DAQ for Linear Collider TPC test beams:

- New general purpose programmable amplifier: PCA16
- LHC TTC trigger system replaced by TLU + 1 FPGA distributor
- r/o software developped on top of ALICE API libraries
  - → Successfull test beams with GEM detectors in March 2009
  - → Further test beams this (and next ?) year at DESY

Other front-ends in tests:

- AFTER integrated ASIC: Ampli → Analog memory + external ADC
  - → Sucessfull test beams with MicroMegas detector in Nov. 2008
  - → Requires autotrigger and timestamping in SCA for ILC
- TDC electronic and Si-Chips (Timepix)

Furure: Advanced Endplate

- Integrate Ampli and ADC into a single ASIC
- ASIC's directly on the detector PCB + redesign the DAQ