CMOS Pixel Sensor for CEPC

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Outline

- Introduction
- CMOS pixel sensor
- Project progress
- Summary and outlook

Introduction

- Impact parameter resolution of required for the identification of heavy quarks and τ-leptons:

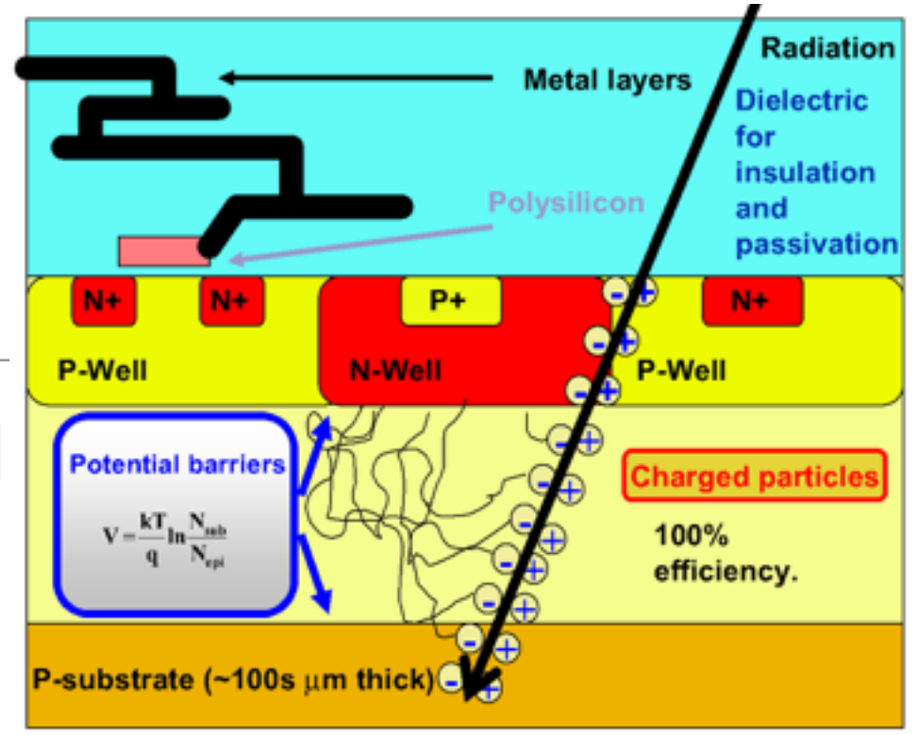
$$\sigma_{\mathrm{IP}} = 5 \oplus 10/p \cdot \sin^{3/2}\theta \ \mu\mathrm{m}$$

- Translating to the requirements on the CEPC vertex detector:
  - Single point resolution σ_{SP} ~ 3 μm → high granularity
  - Material budget ≤ 0.15% X_0 per layer
    - Sensor+ASIC thickness ~ 50 μm → monolithic sensors
    - Air cooling → low power consumption (extremely challenging without power-pulsing)~ 50 mW/cm^2
  - Anual radiation tolerance ~100 kRad & $10^{11} n_{eq}/cm^2$
  - Low detector occupancy ~0.5% → fast readout ~ 20 μs

Candidate Technologies

- ILC (and LHC) experiments have extensively investigated into several candidate technologies, which might meet the “requirements”.
  - High resolution, low material budget, low power consumption …
  - FPCCD, DEPFET, CMOS Pixel Sensor, SOI, 3D IC, etc.
- We have evaluated the availability and potential performance for those candidate technologies, and started to explore the CPS technology.
- But we shall always keep our eyes open on the fast developing sensor/electronics technologies and may have to revisit our R&D strategy later.

CMOS Pixel Sensor



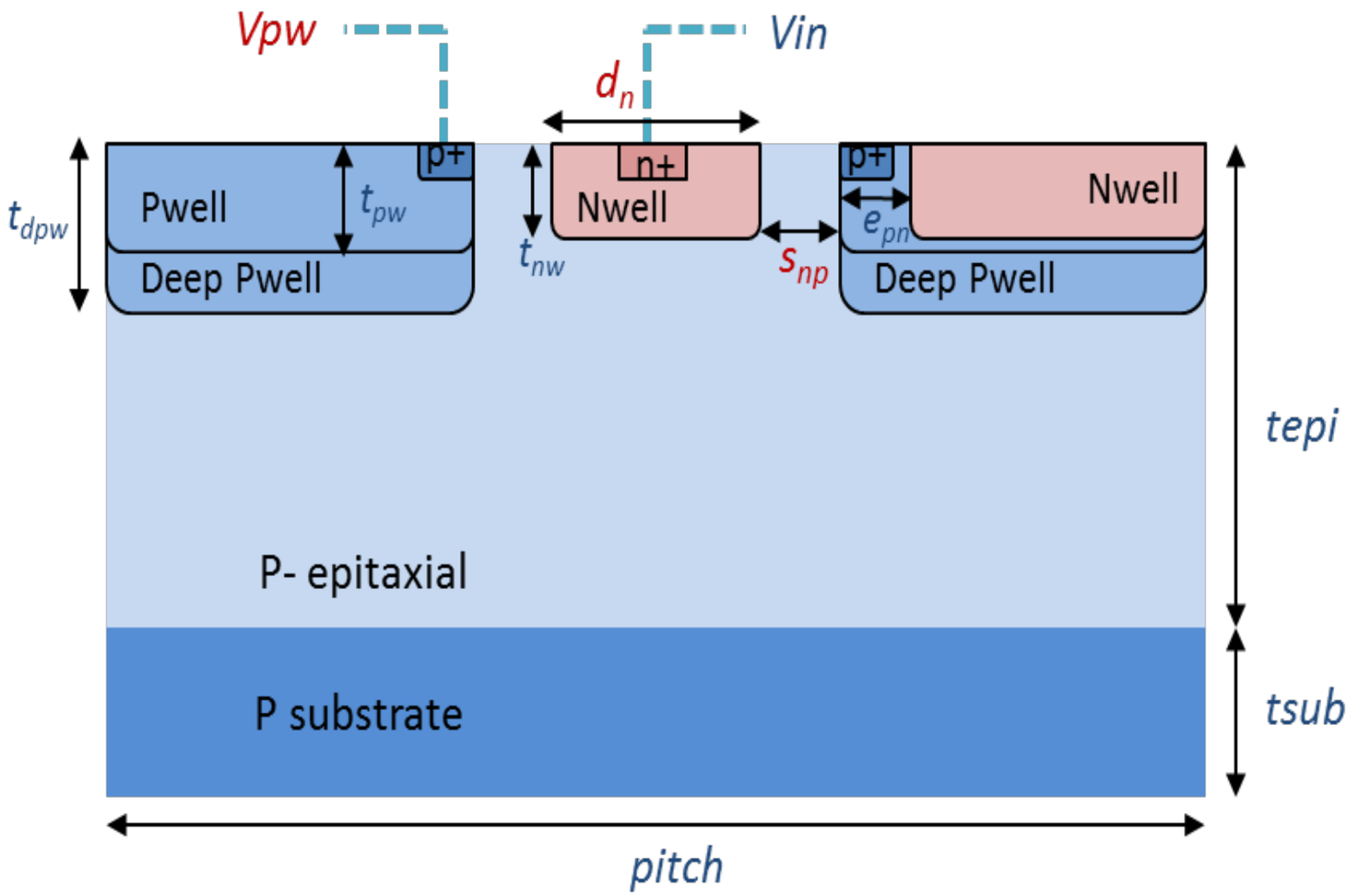
- Front-end electronics and sensor integrated on the same silicon bulk, featuring:
  - High granularity → high spatial resolution
  - Sensor thinned down to 50 μm → low material budget
  - Standard CMOS fabrication technology → cost effective
  - Signal processing on-chip → relaxing down-stream data processing
  - Radiation tolerance (moderate) → usable for electron machines
- Example CPS sensors designed by IPHC
  - Mimosa26 (EUDET beam telescope), Mimosa28 (STAR PXL)
  - MISTRAL/ASTRAL (ALICE ITS Upgrade, CBM-MVD)
  - Adaption to the ILD VTX

CMOS Process

- We have evaluated the accessibility of might-be suitable CMOS processes “provided” by the foundries
  - TSMC, SMIC, … a long list
- We “decided” to adopt the TowerJazz CIS 0.18 μm process for or R&D project and have started designing efforts.
  - Joint submission with IPHC around mid 2015
  - Searching for joint submissions with other projects (e.g. ATLAS)
  - Keep trying MPW submission via the EDA center
- Limited funding and submission opportunity → define properly the goal of each submission and more importantly the R&D roadmap

Pixel Structure

- Quadruple-well provided by the TJ CIS technology enable the possibility of implementing in-pixel digital circuit → design flexibility and reduction in power consumption



Team

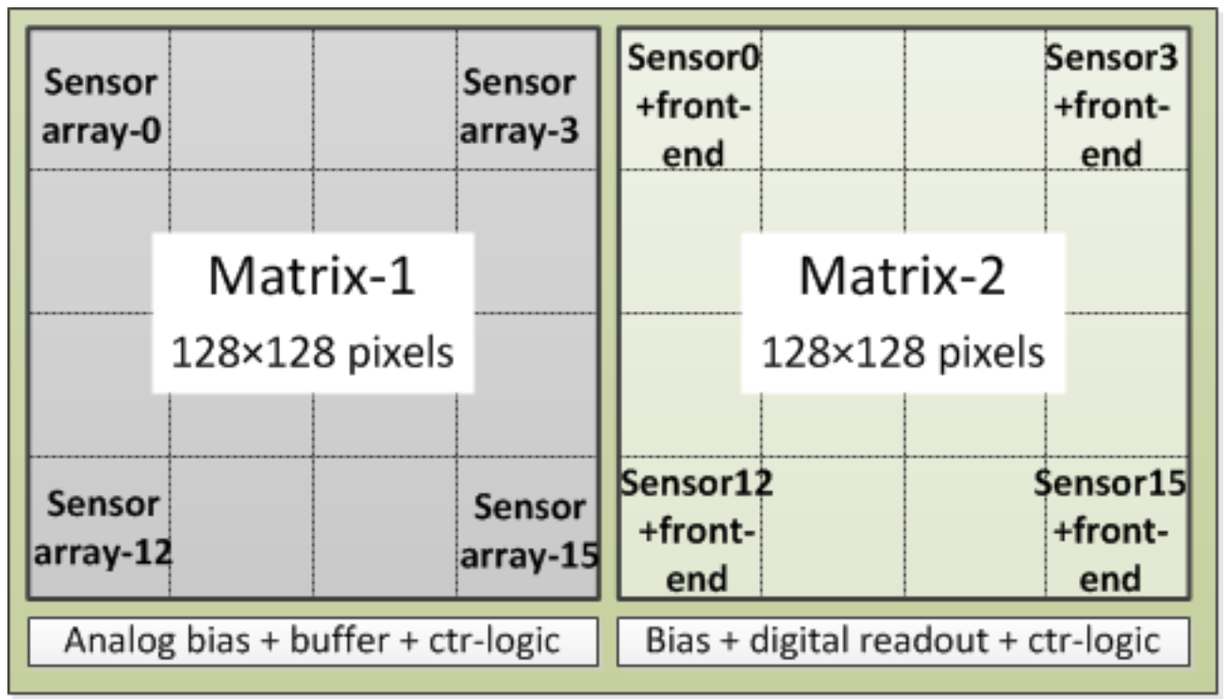
- We have managed to build up a team, consisting of detector and electronics experts, but also members with entry-level knowledge.

	Affiliation	Responsibilities
Hongbo Zhu	IHEP	Project leader & test beam
Min Fu	OUC	TCAD simulation (Sentaurus)
Mei Zhao	IHEP	TCAD simulation (Silvaco)
Ying Zhang	IHEP	Front-end electronics
Liang Zhang	SDU	Front-end electronics
Ke Wang	IHEP	Readout electronics and test system
Yu Penglu	IHEP	Readout electronics
Pelian Liu	IHEP	Detector simulation and sensor tests
Qinglei Xiu	IHEP	Background simulation and sensor tests

First Submission

- For the first submission, we hope to achieve:
  - Comprehensive understanding of the design rules
  - Optimisation of the diode design
  - Minimal analog circuit in the sensor
- 2 Matrices of 128×128 pixels, pitch size 30 μm (not fully defined)

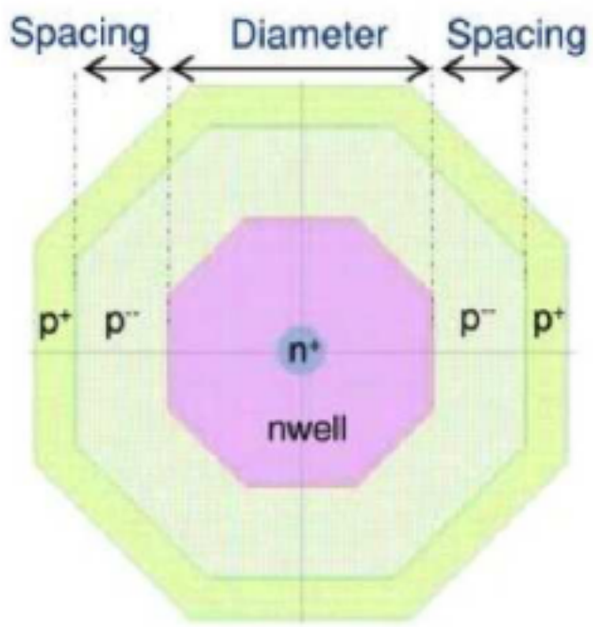
sensor with in-pixel traditional 2/3 T structure for analog readout

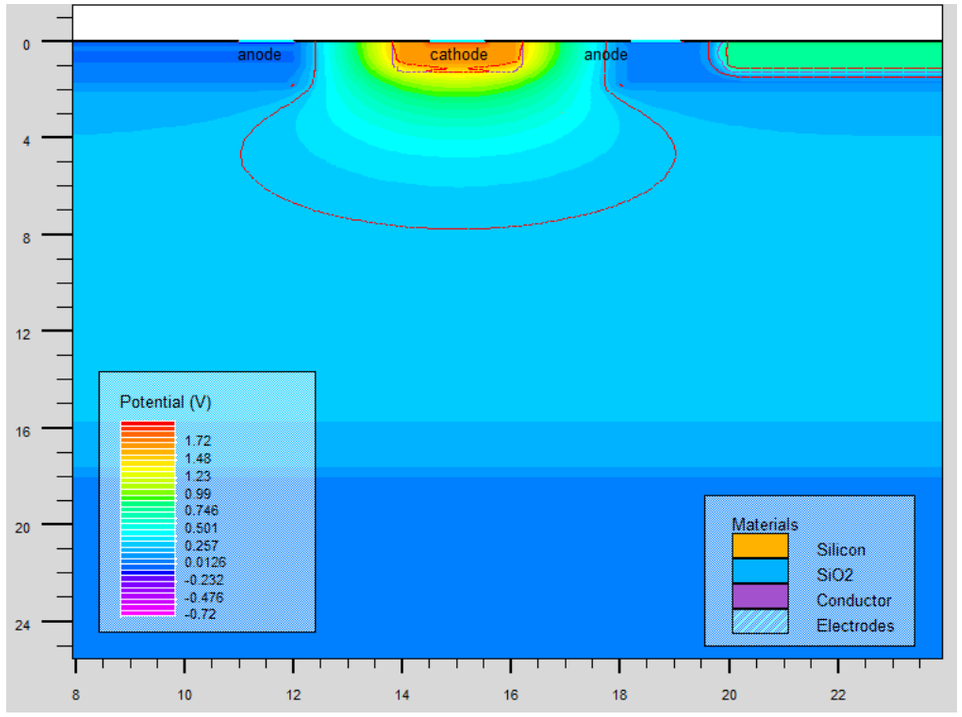


minimal in-pixel analog circuit

Diode Optimisation

- Taking advantage of the partially available results from the ALICE ITS upgrade project … we know roughly which parameters to optimise and to define 16 configurations for submission.



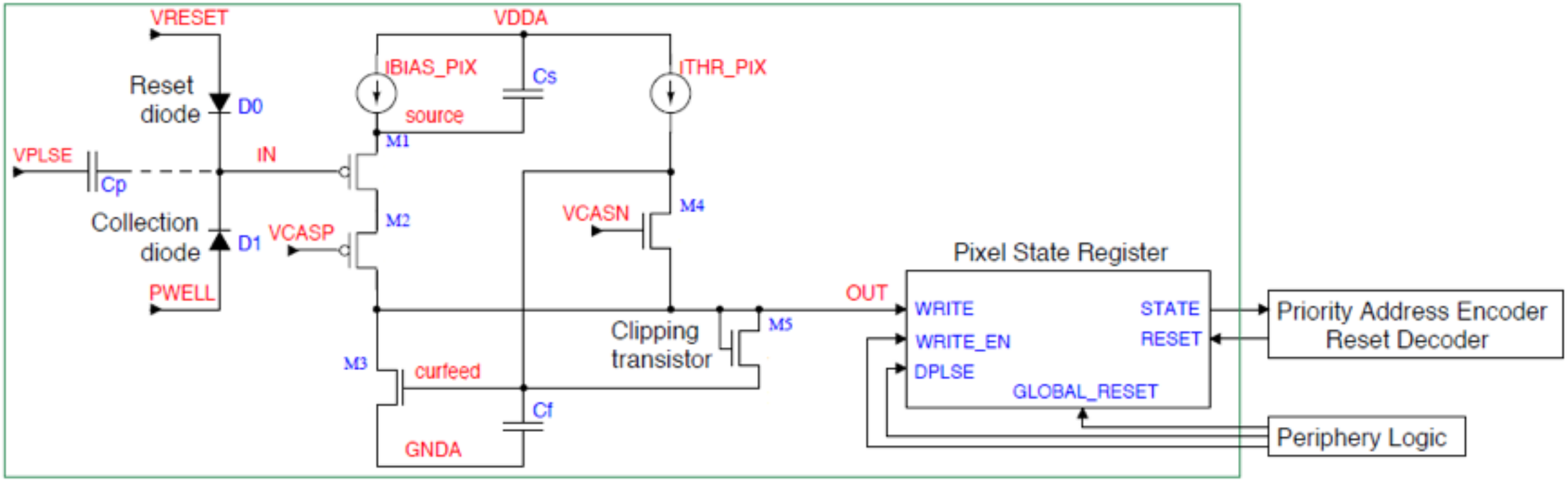


Field map from TCAD simulation

- Model implemented (optimising the conventional model)
- Charge collection time and efficiency to be evaluated

Readout Electronics

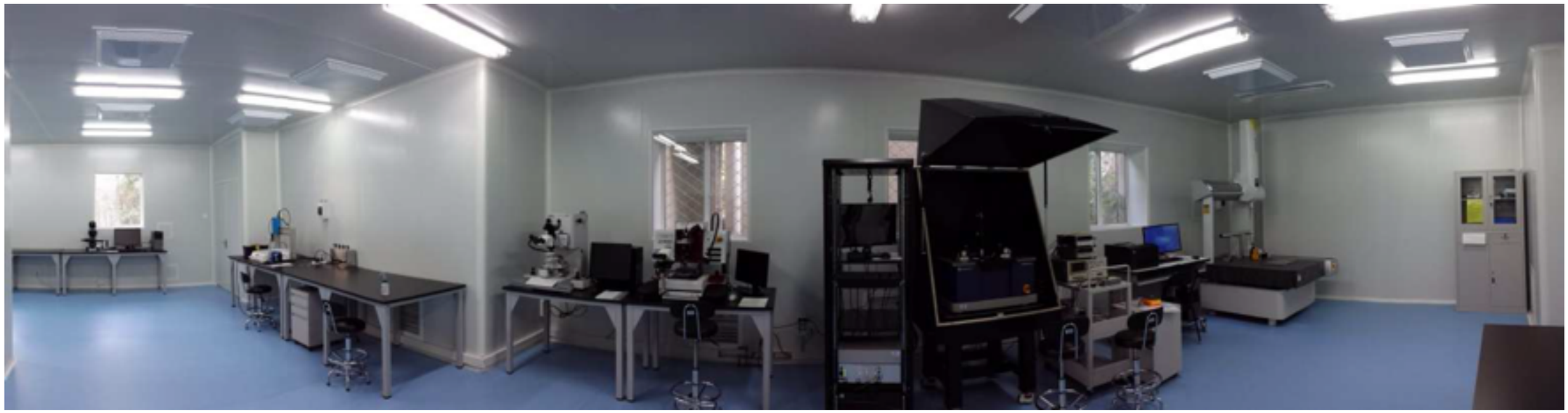
- Critical to develop an highly efficient readout architecture with extremely low power consumption; following the proposed ALPIDE readout for the ALICE ITS upgrade



- TJ quadruple-well allows the realisation of “complex” in pixel.
- Implementing the current comparator for the first submission (likely)

Tests

- Electrical characterisation and charge collection measurement of the CMOS sensor in lab (probe station, radio active source …)



- Preparing test PCB board (with sensor wire-bonded) and back-end readout system → eventually to perform beam tests (telescope under construction)

Summary and Outlook

- Have selected TowerJazz CIS 0.18 μm process for CMOS sensor design, given its several attractive features
- Have started designing the sensor diode (with conventional readout) and minimal in-pixel analog circuit

- Expect first submission around mid 2015 followed by sensor characterisation
- Critical to design readout architecture with low power consumption and reasonable readout time → but have to …
- Keep an eye on fast development in both HEP community and industry and may revisit our R&D strategy later.