Recent progress in silicon sensor development for ATLAS tracking detector upgrade

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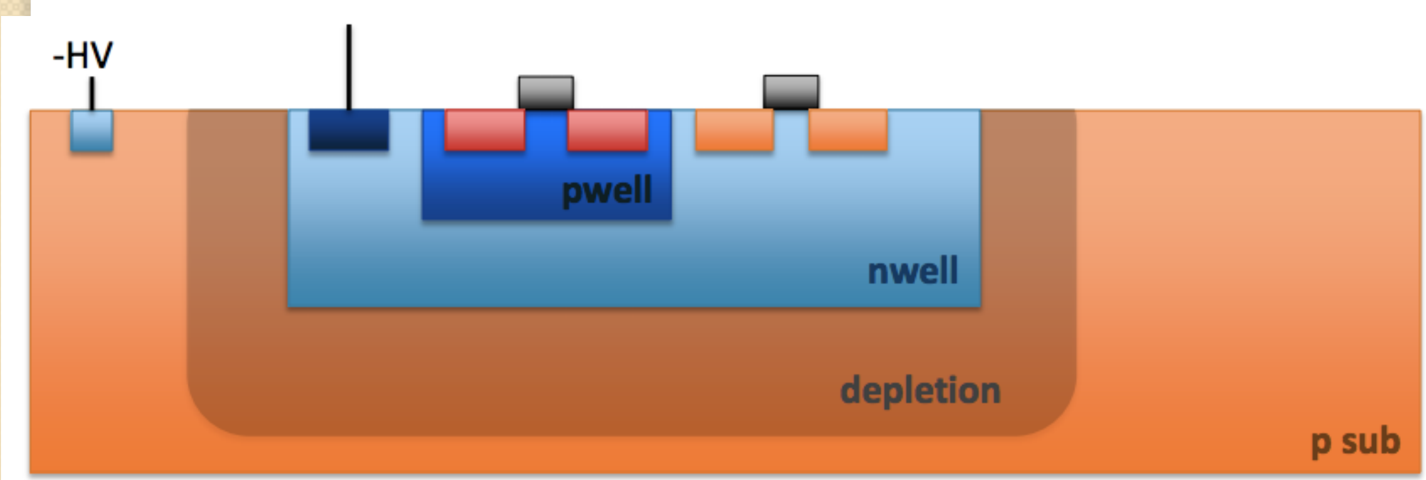
Introduction

- ATLAS ITK silicon strip detector phase 2 upgrade
- Sensor status
  - Default solution : n-on-p type planar sensors
  - Fallback solution : CMOS pixel sensors

CMOS pixel sensors developments

- Implemented in commercial CMOS (HV) technologies (350nm, 180nm)
  - Collection electrode is a large n-well/p-substrate diode
- Advantage:
  - High granularity: Typical resolution is 50nm
  - low material budget : Can be thinned down to 50um
  - Monolithic: Front-end electronics and sensor can be built in the same chip
  - Low cost
- Drawback:
  - Low MIP signal : 1700e
  - capacitive crosstalk from PMOS drain/source into collection electrode



CMOS pixel sensors developments

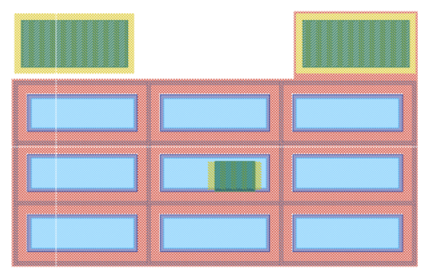
- Three years plan for CMOS technology R & D for ATLAS ITK phase 2 upgrade
  - Aim for full size sensor designed and fabricated
  - Aim for a stave designed in middle of 2017

- AMS H35 HIGH VOLTAGE TECHNOLOGY
  - http://www.europractice-ic.com/technologies_AMS.php?tech_id=hv
  - Two submissions have done (April 2014, August 2014)
  - Aug 2014 submission by UC Santa Cruz and SLAC
    - Evaluation of the capacity of the CMOS pixel

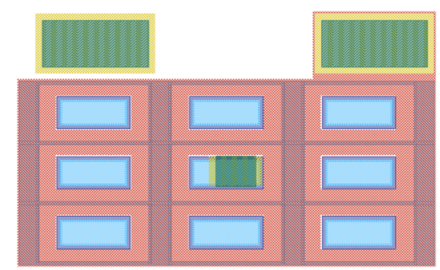
- TowerJazz 180 nm CMOS Image Sensor (CIS) technology
  - One submission has been sent (Dec 2014)

HV-CMOS pixel array design

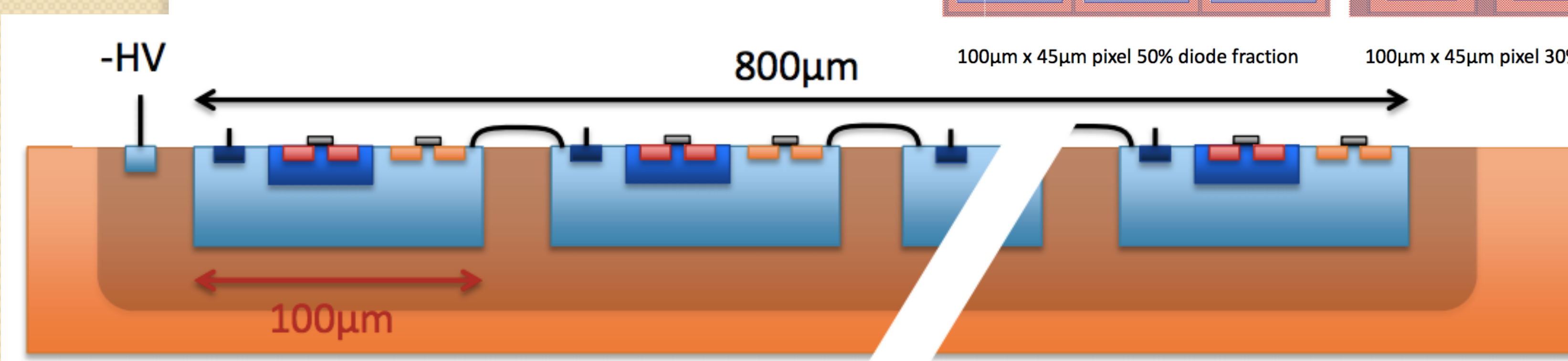
- Pixel size can be reduced to 1umX3 um or less in AMS H35 design
- For strip application, larger pixel size is considered in the last submission
  - 45µmX100µm , 45µmX200µm, 45µmX400µm 45µmX800µm
  - 30%-50% Nwell fraction
    - Expect better performance in higher Nwell fraction
  - Electronics in the strip allow for strip segmentation
  - – AMS provides options for high resistivity substrate
    - Substrate resistivity can be up to a few thousand Ω



100µm x 45µm pixel 50% diode fraction

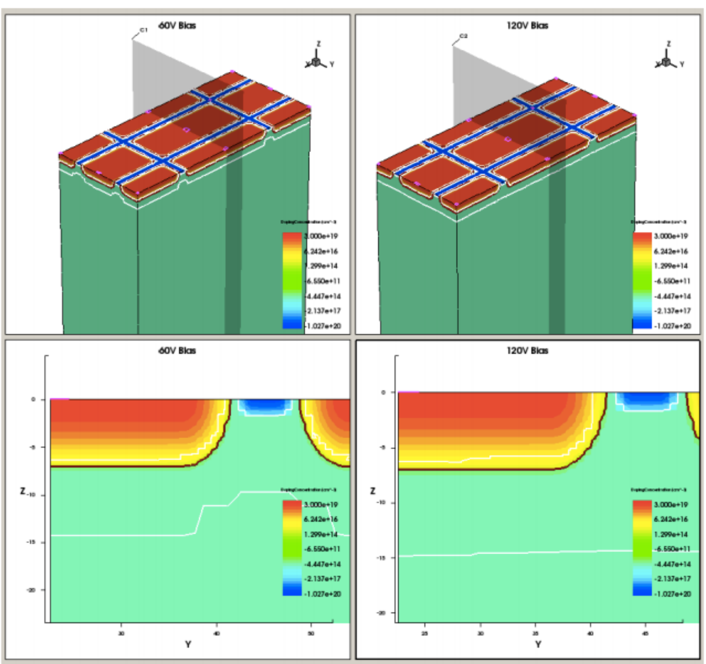


100µm x 45µm pixel 30% diode fraction

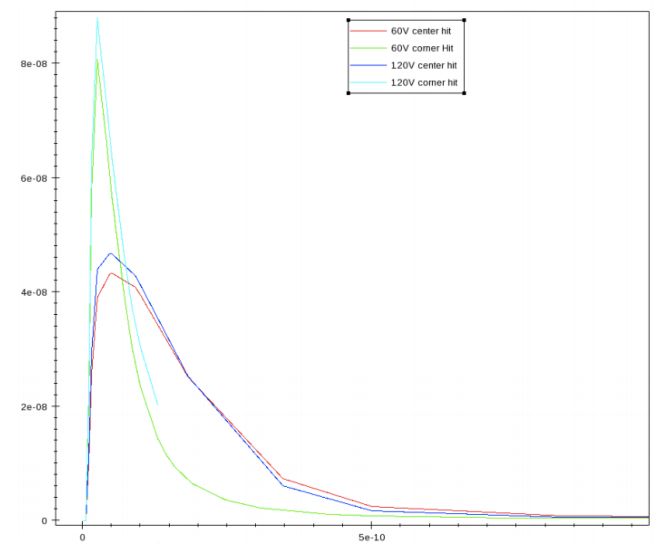


HV-CMOS pixel array design

- Other designed proprities in simulation
  - Depletion region
  - Nwell capacitance
  - Charge collected
- Drift time is designed to be 0.1-0.5ns
  - Longer drift time when the hit is in center of pixel
  - low signal amplitude
    - Can not be readout directly, need amplifier



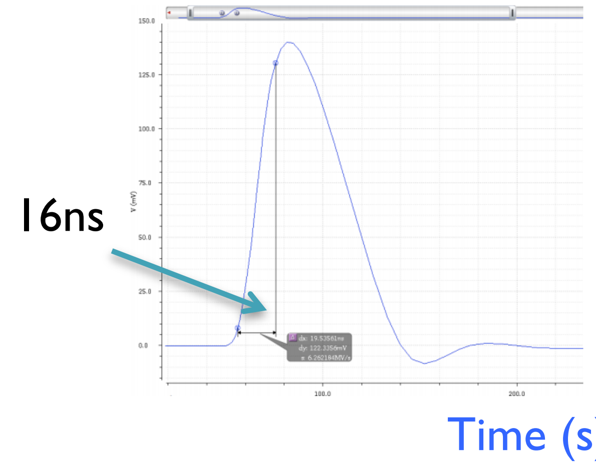
Current (A)

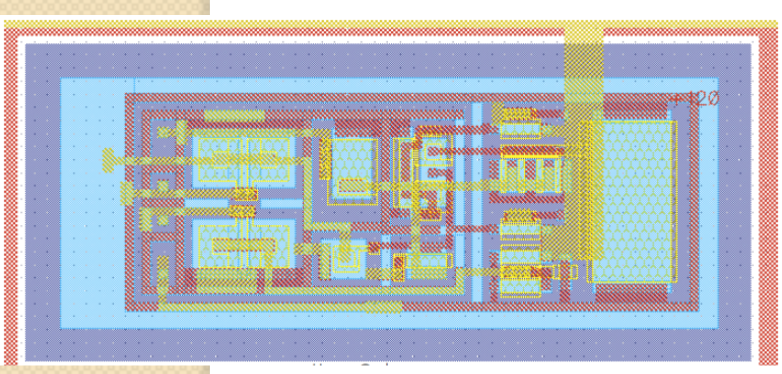


Time (s)

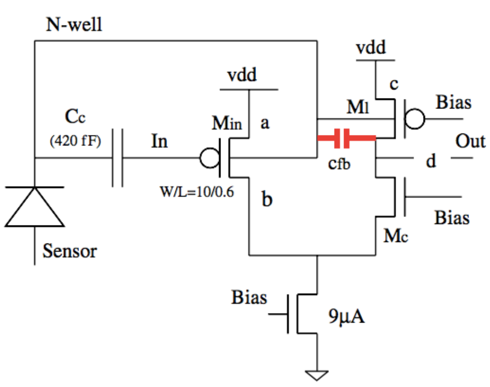
Design of amplifier

- signal to noise ratio is relatively low in HV-CMOS sensors
  - A monolithic design of a built-in low-noise amplifier is needed
    - The pixel array and amplifier are designed in the same chip
    - The noise of the monolithic amplifier Is designed to be lower than external amplifier
  - The amplifier design must be radiation hard
    - radiation tolerant layout techniques is used
  - The raise time should be fast as well for LHC application
    - 16ns raise time for active pixel signal after amplification





radiation tolerant layout

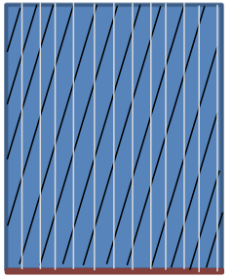


Specifications	Simulated values
Rise time	16 ns (10 - 90 %)
Noise	200 e⁻
Gain	500 mV/fC
Power consumption	210µW/ amplifier
Pulse duration	50ns

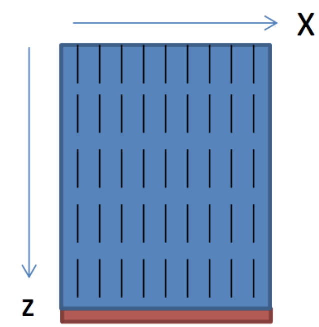
Architectures design

- Two designs are considered
- Built-in Stereo:
  - Readout binary in two set of connections on pixel matrix
  - similar to conventional planar sensor
  - not able to use the advantage of CMOS technology

Built-in Stereo- Two set of connections on pixel matrix



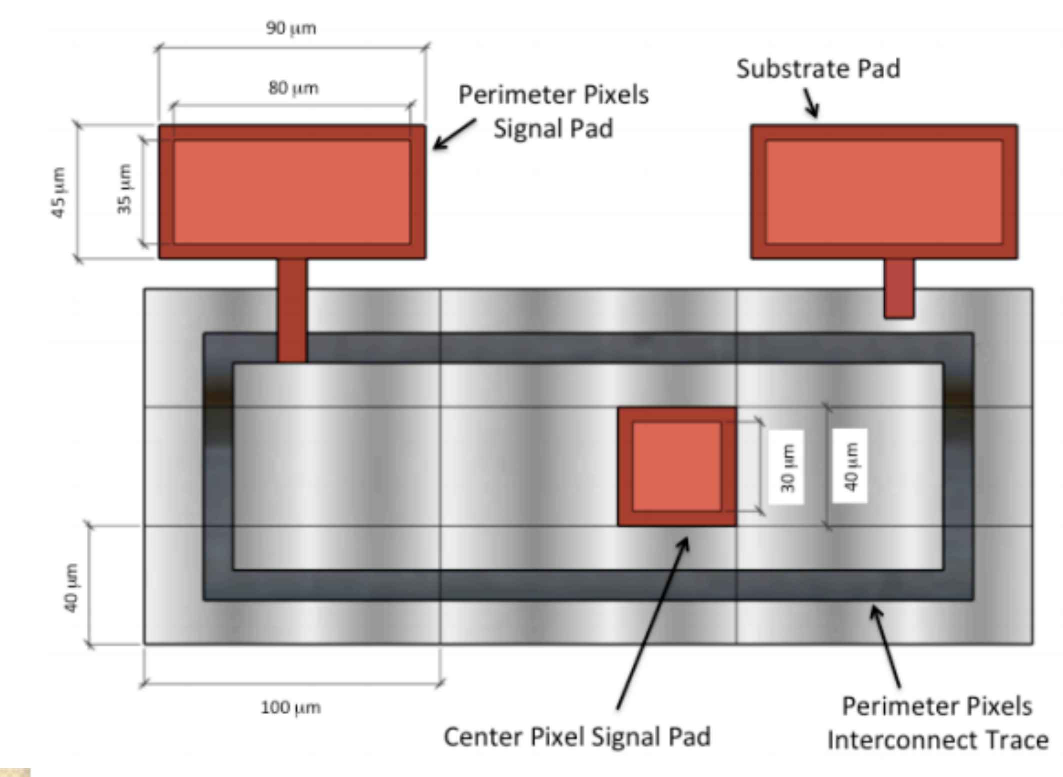
- Digital Z encode: (to be test in March 2015 submission)
  - Z encoding is found to be the best design
  - Not a binary readout, readout the address of the hits
  - In the example segment : 40X800um
    - readout 9 bits of 'x; position
    - readout 5 bits of 'z' position
    - Only needed 14 wire bond in this example
      - Reduce the number of wire bonding by order of magnitude
    - Save a lot of module building time



- Amplification and digitization will be done in HV-CMOS chip
- The Frontend readout chip (ABCN130 chip) needed to be redesigned to
    - Remove the amplifier and digitization part
    - Add receiver to receive digital info z-position
    - Mainly use for data buffering

Testing setup and major Challenge

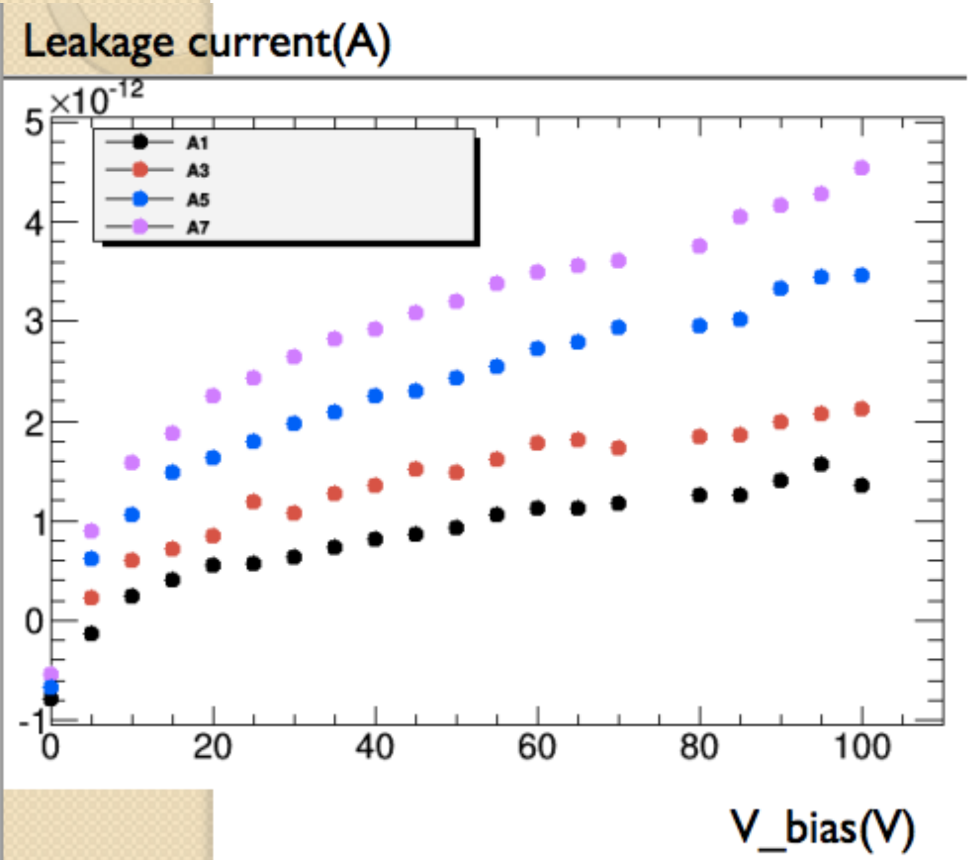
- Compared to conventional planar sensors for strip detector
  - Leakage current is about lower by at least 1000 times
  - Capacitance is lower by at least 1000 times
  - Need setup for low noise measurement



Substrate: grounded
Perimeter pixels: +HV
Central pixel: +HV

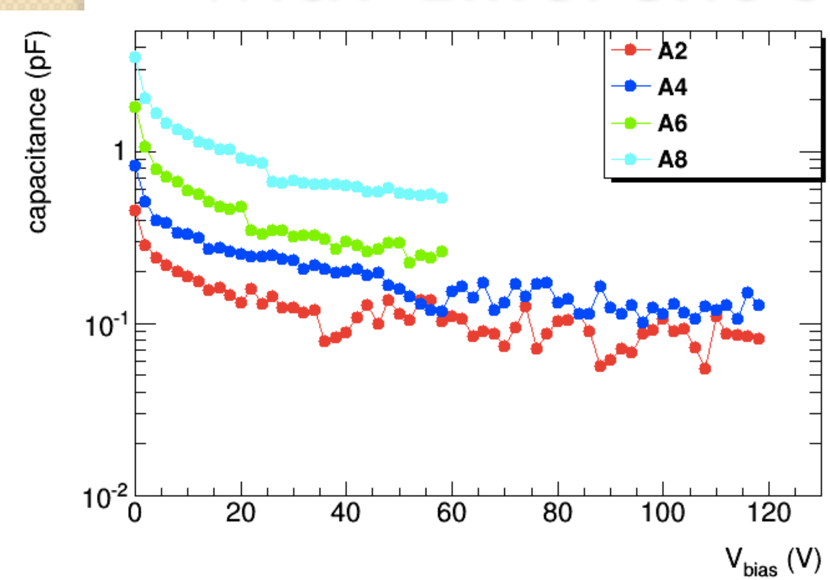
Central pixel IV

- I-V measurement
  - Can Biased up to 120V without breakdown
  - Low leakage current (pA level)
  - Leakage current proportional to pixel size.



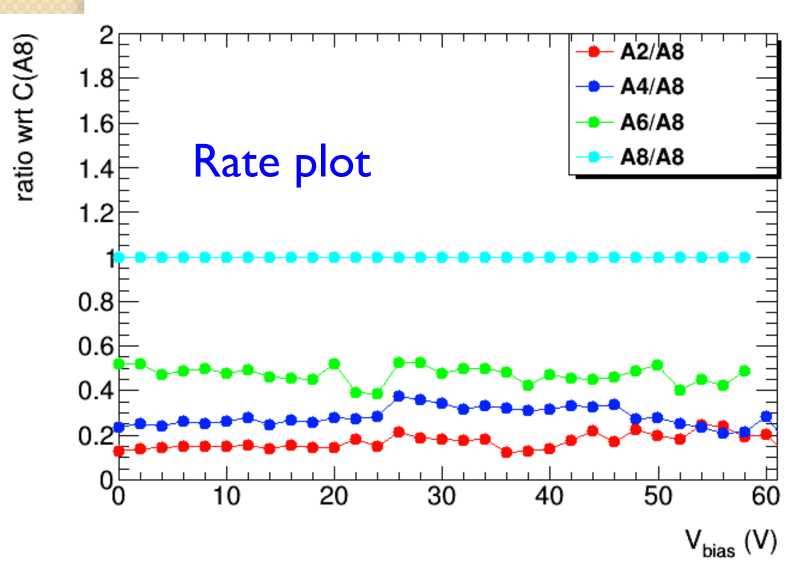
PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA01	45µm	100µm	30%	13.0%
PPA03	45µm	200µm	30%	22.7%
PPA05	45µm	400µm	30%	27.4%
PPA07	45µm	800µm	30%	29.8%

Capacitance of central pixel array with different size



The central pixel capacitance at low bias voltage is roughly proportional to pixel size.

- At low bias voltage
- C(A4) is about 1/2 of C(A8)
- C(A6) is about 1/4of C(A8)
- C(A8) is about 1/8 of C(A8)

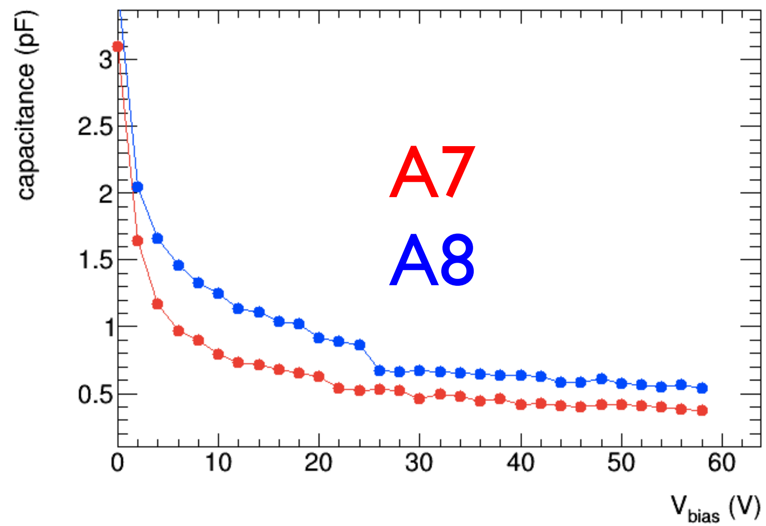


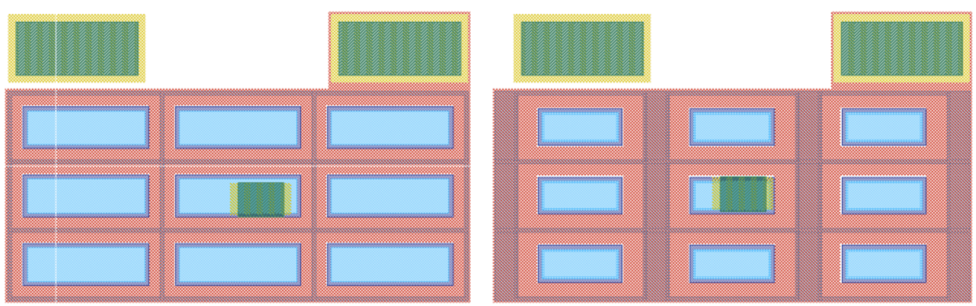
PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA02	45μm	100μm	50.4%	34.5%
PPA04	45μm	200μm	50.4%	44.0%
PPA06	45μm	400μm	50.4%	48.7%
PPA08	45μm	800μm	50.4%	51.0%

Capacitance of pixel array with different diode area fraction

PPA #	Pixel width	Pixel length	Diode Area Fraction	Metal opening ratio
PPA07	45μm	800μm	30%	29.8%
PPA08	45μm	800μm	50.4%	51.0%

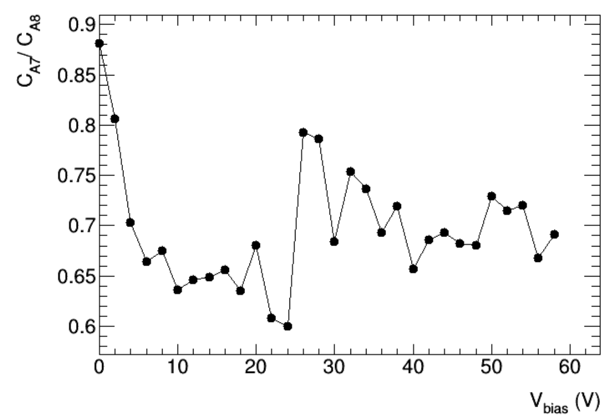
Observe lower capacitance for pixel with lower diode fraction





100μm x 45μm pixel 50% diode fraction

100μm x 45μm pixel 30% diode fraction



- C(A7) is about 70% of C(A8)

Charge collection measurements

- Use big pixel array for charge collections tests
  - ~1000 pixels connected together to give large signal in big array
  - Signal to noise ratio is about 10 using external amplifier
  - About 1700 e- are collected
  - Next step is to test the small pixel array (1000 times smaller)
    - Signal is expected to much smaller
    - Using built-in amplifier to reduce the noise

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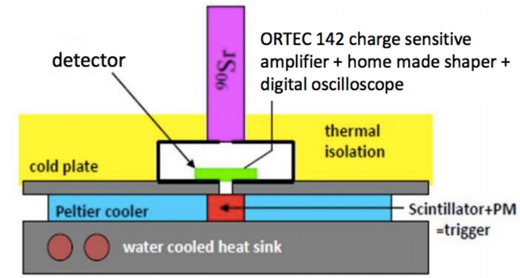
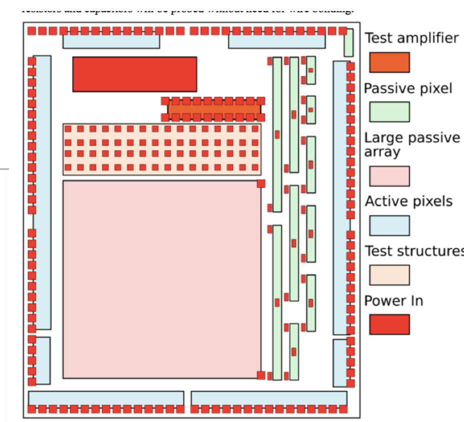
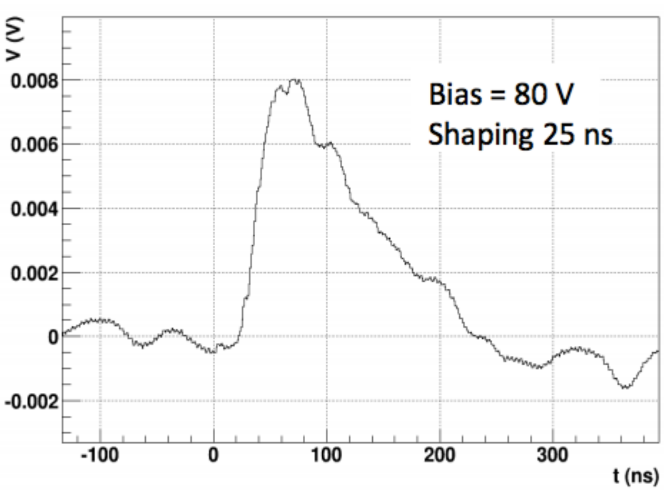
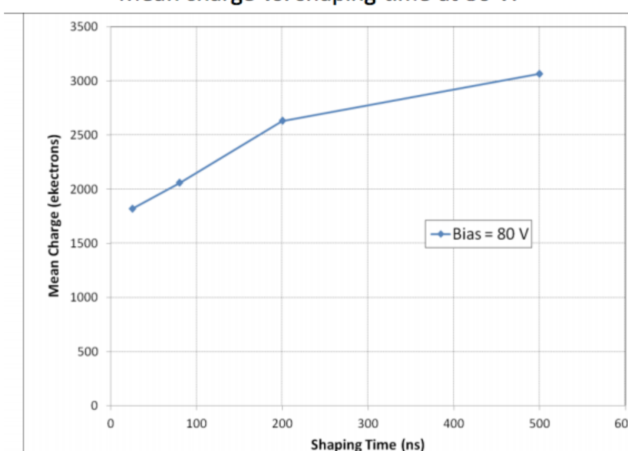






Mean charge vs. shaping time at 80 V:



Charge increases with shaping time → diffusion

Short summary of CMOS sensor testing

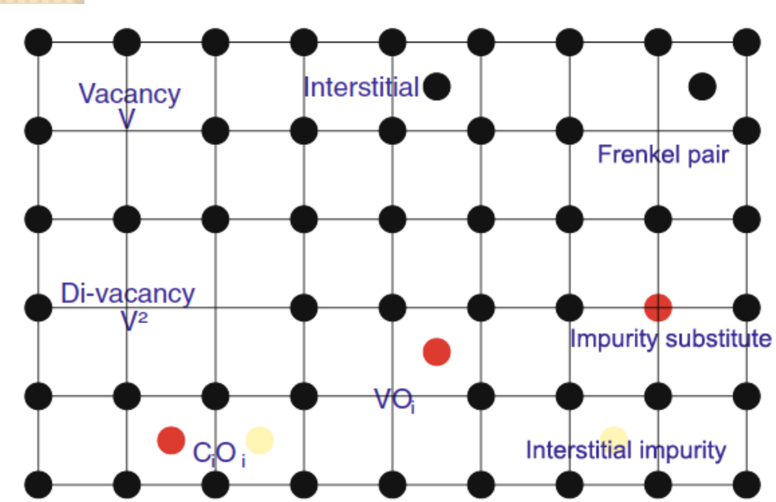
- Preliminary I-V and capacitance results for HV-CMOS CHESS1 chips
  - I-V measurement
    - Can Biased up to 120V without breakdown
    - Low leakage current (pA level)
  - C-V measurement
    - The central pixel capacitance at low bias voltage is roughly proportional to pixel size.
    - Observe lower capacitance for pixel with lower diode fraction
  - Charge collections efficiency
    - About 1700 e- are collected
    - Signal to noise ratio is about 10

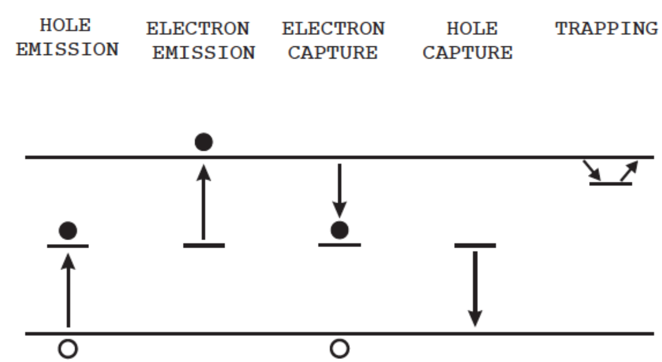
Part 2: radiation damage study in planar sensors

- planar sensor is default solution for ATLAS phase 2 upgrade
- The study of planar sensors are quite advanced
  - Lots of study have been done for radiation hardness
  - Full size sensor has been studied

Reminder of radiation damage

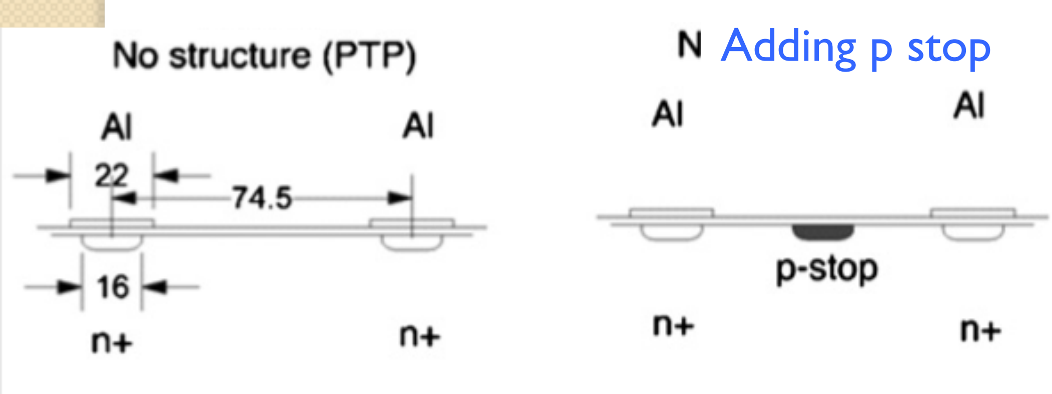
- What happen to Silicon sensor after bulk radiation damage:
  - displacements in the silicon lattice
  - Creating intermediate state
    - Lead to higher leakage current
  - Defeat state will capture the charge carriers
    - lead to lower charge collection efficiency
  - Lead to cross talk in signal readout
    - Lower isolation between two close-by strips or pixels
    - Higher inter-strip or inter-pixel capitance

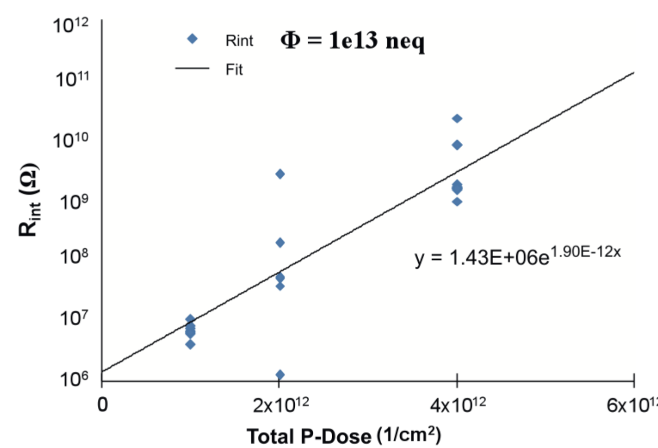




Special design for radiation hard planar sensor

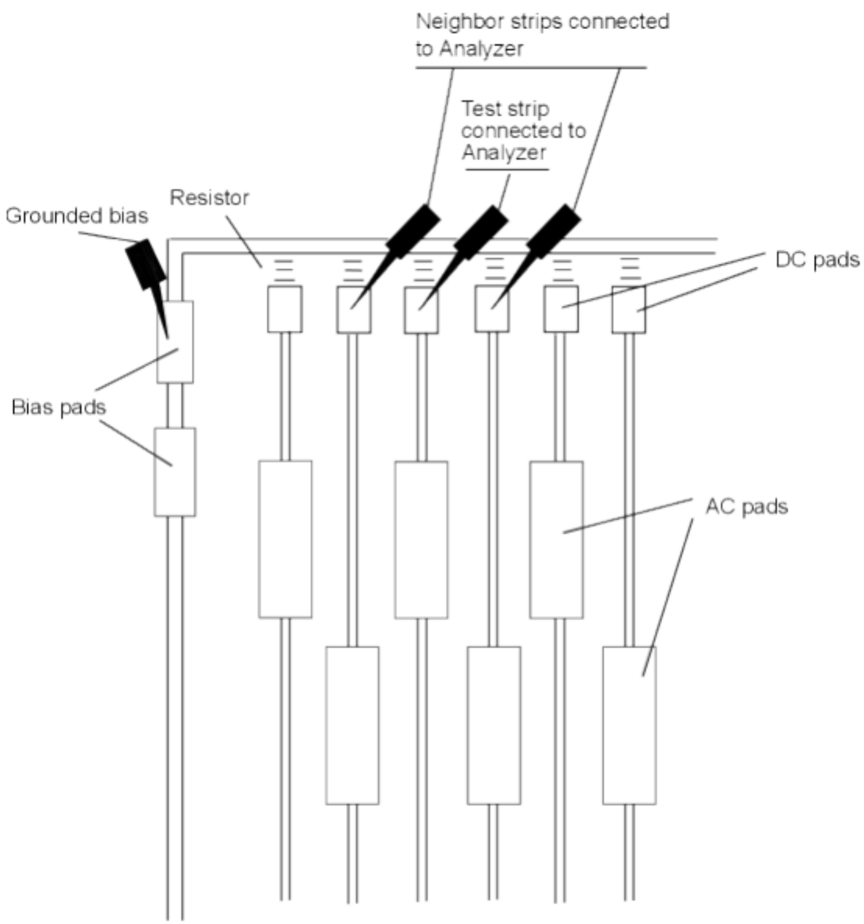
- N-on-p sensor is used as default planar strip sensor
  - Radiation hardness is not better than n-on-n
  - But it is much cheaper
- Inter-Strip Isolation is not good after radiation
  - Charge carrier can travel through surface of the silicon
    - Two strips are short together after radiation
    - degradation of the position resolution
  - Add p-stop between two close-by strips
    - Improve the isolations between strips
    - Total p stop dose is optimized to 1e12 ($1/cm^2$) level





Inter-strip resistance measurement

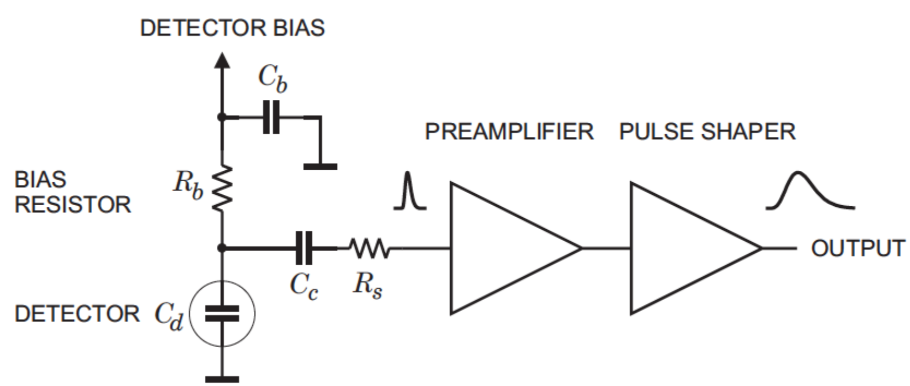
- The inter-strip resistance setup as follow
  - BZ3C , BZ3C slim, BZ3F sensors
  - Measured at -20 °C, -5 °C



Measure nA current for G Ω level resistance
Relative low S/N
Do a careful job in grouding to reduce the noise

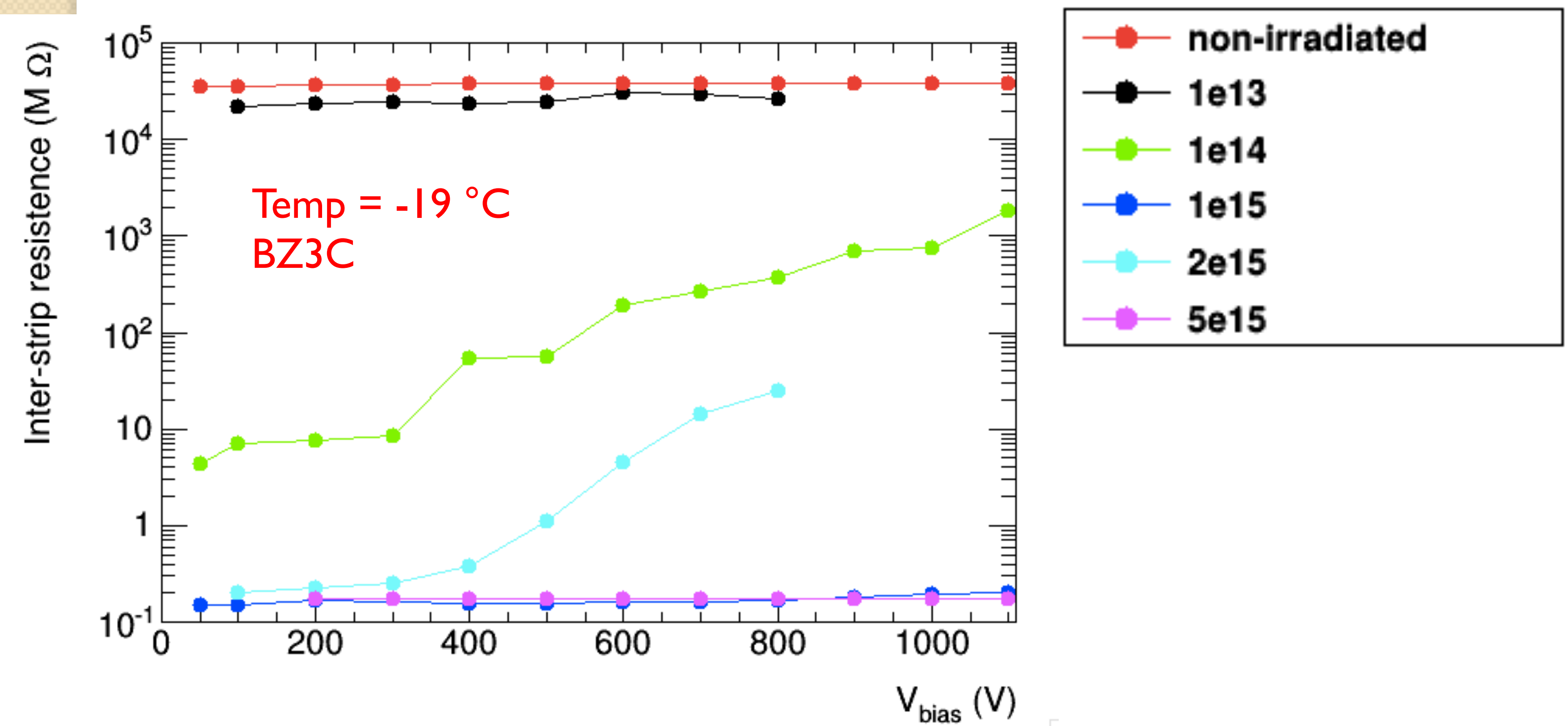
The impact of Radiation damage to inter-strip capacitance

- Radiation damage may also have large impact to inter-strip capacitance
  - lead to cross talk between channels
  - The ratio of R_int to R_bias reflect the cross talk
    - R_bias / R_int is designed to be >10
- The impact to readout pre-amplifier
  - The ratio of Rs to R_INT
  - Part of Signal to pre-amplifier will be lost when R_INT is too low



R_INT in different bias voltage

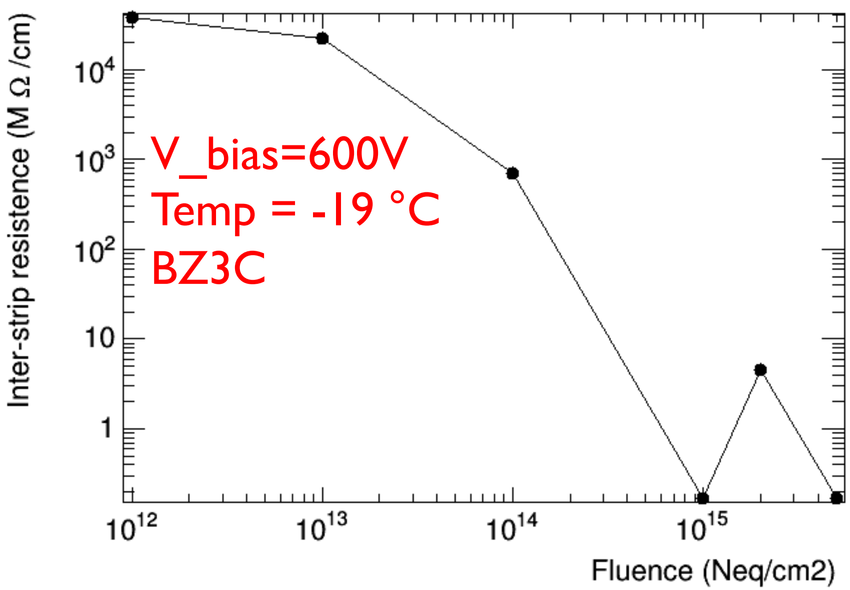
- Higher resistance with higher bias voltage.



R_INT VS fluence

- Inter-strip resistance drops from 38GΩ/cm level to 0.17MΩ/cm
- Cross talk effect
  - R_INT/ R_bias >>10 before radiation -> no cross talk
  - R_INT/R_bias = 3 at 2e15 Neq/cm^2 cross talk expected , still acceptable
- impact to readout pre-amplifier
  - R_INT/ Rs >>10
  - No major impact

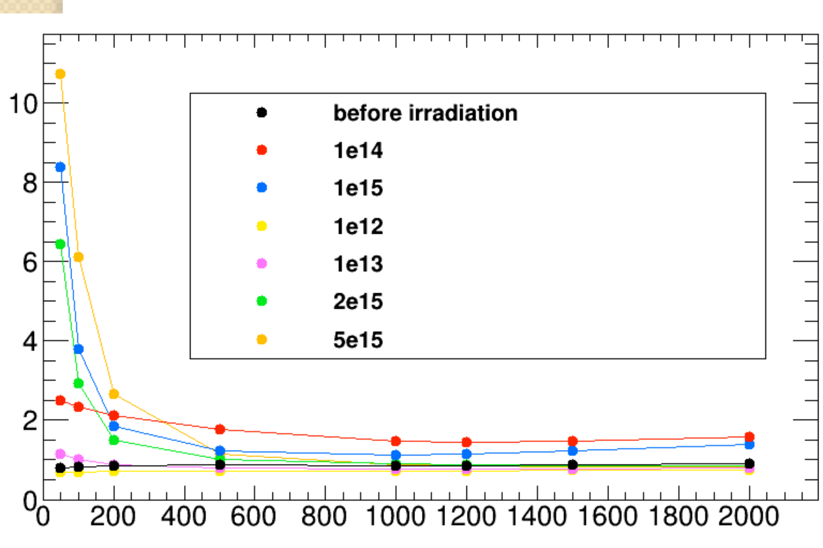
V_bias=600V

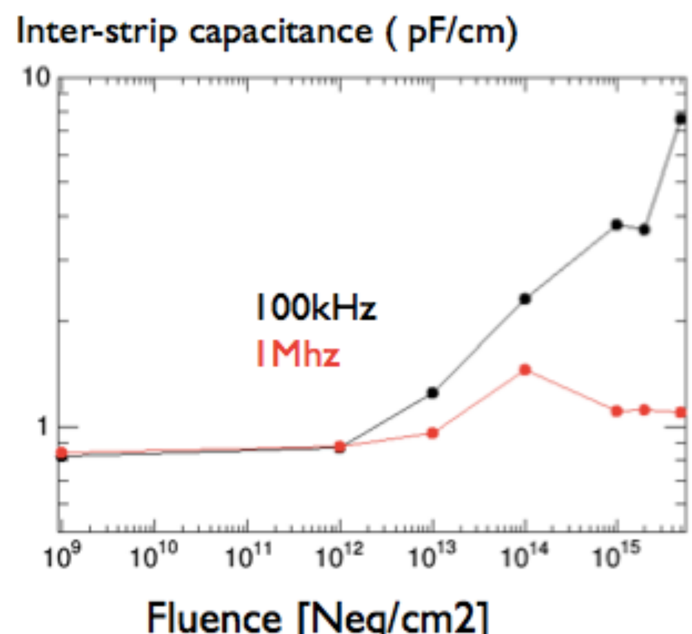


Fluence	Non-irradiated	1e13	1e14	1e15	2e15	5e15
R_INT (-19°C)	38GΩ/cm	22.2GΩ/cm	0.69GΩ/cm	0.17 MΩ/cm	4.5 MΩ/cm	0.17MΩ/cm

Inter-strip capacitance Vs flence

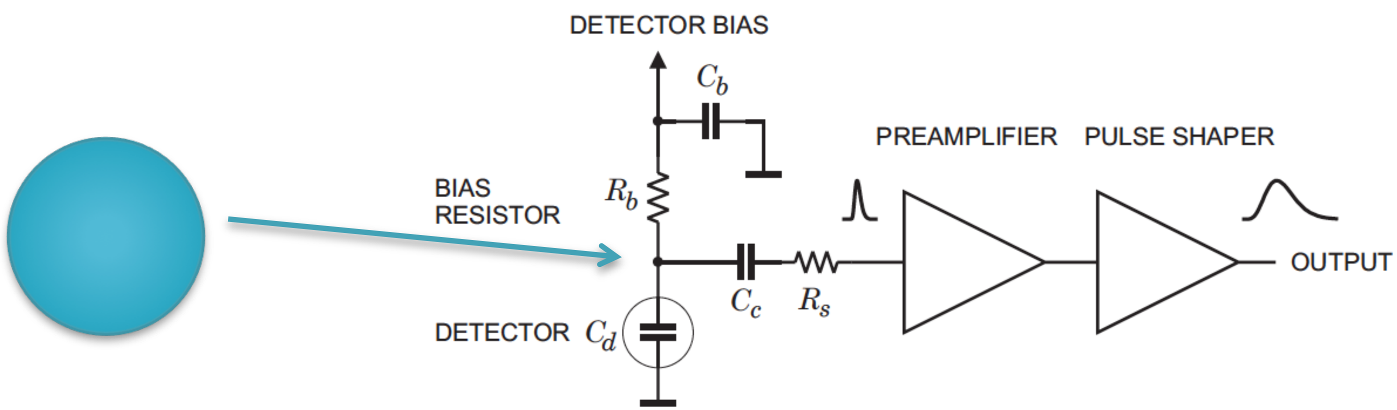
- C_int increase after radiation for slow signal (100Hz)
- Have less impact for fast signal (MHz)



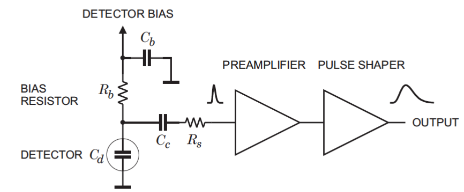


Punch through protection design in planar sensor

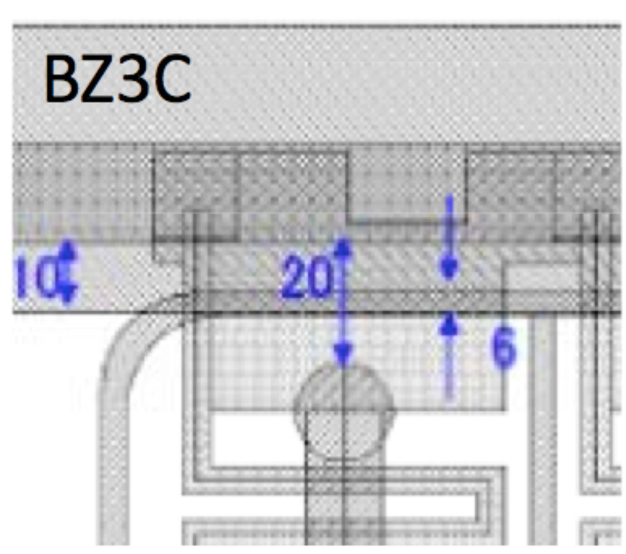
- When the proton beam is not stable or during beam dump
  - Lots of charge particle go through the sensors
- Large amount of charge accumulated before coupling capacitance
  - This accumulated is AC signal , can go through coupling capacitance
  - Large amount of siganl will damage pre-amplifier

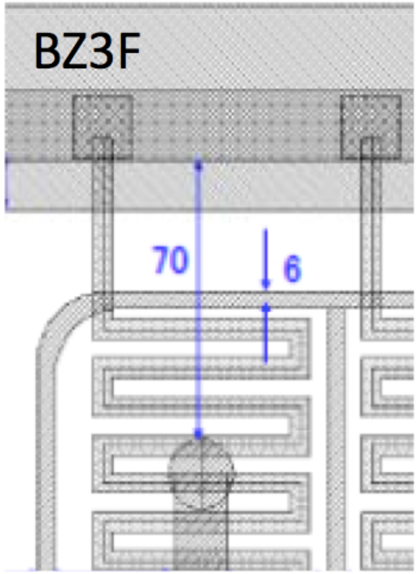


Punch through protection design in planar sensor



- Design punch through protection
  - P-n-p transistor structure
  - Two design:
    - Varying the distance between p stop and bias ring.
- The R_b is short when accumulated charge is large



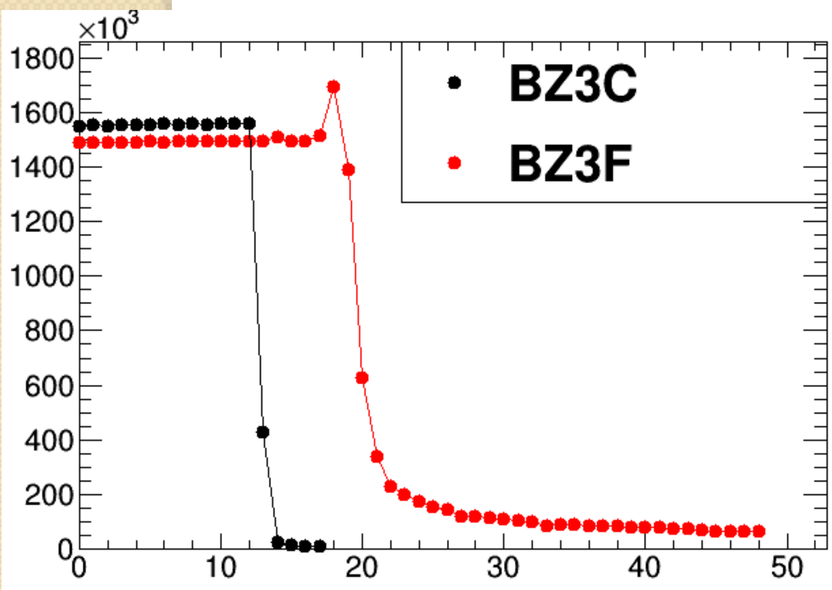


BZ3C VS BZ3F

- BZ3C has a smaller punch-through voltage before radiation.
- After radiation, both sensors have similar punch-through voltage
- PTP structure is still working well in BZ3C

before radiation

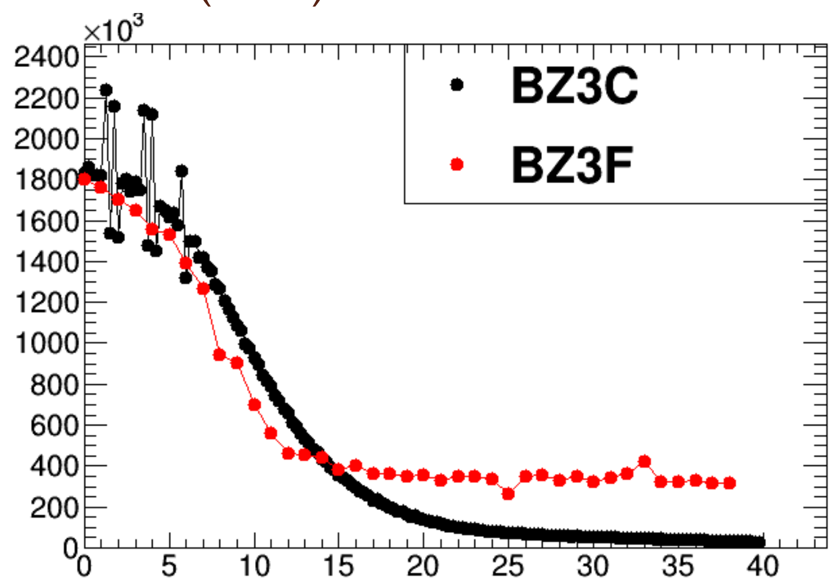
Resistance(Ohm)



Voltage (V)

After radiation

Resistance(Ohm)



Voltage (V)

Summary

- Radiation hardness planar sensor have been studied
  - sensor performance is OK after radiation
  - The design of p stop and the punch through protection structure is working as expected.